終極王牌特訓班-高速串列測試之最後進擊

接收器完整性信號分析的測試原理與應用

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BERTScope™

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Why Receiver Testing is Different

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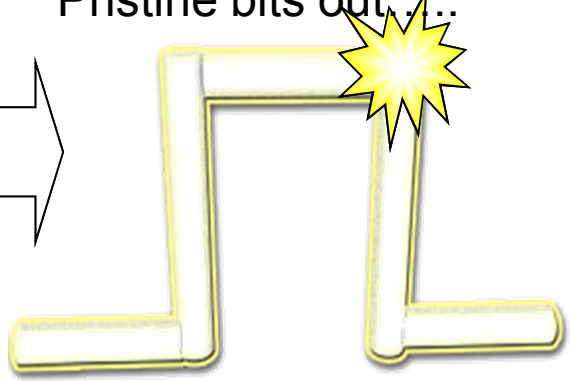
Receivers

Poor quality bits in….

"Receiver", "Re-Timer"
"Decision Circuit", "SERDES"

Receiver

Pristine bits out….



- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance….
  ….the eye shape only tells how nice the output stage is.

Bright… *Shiny…*
New…

Wrong?

Receivers are Tested with BER

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Simplified Receiver Block Diagram

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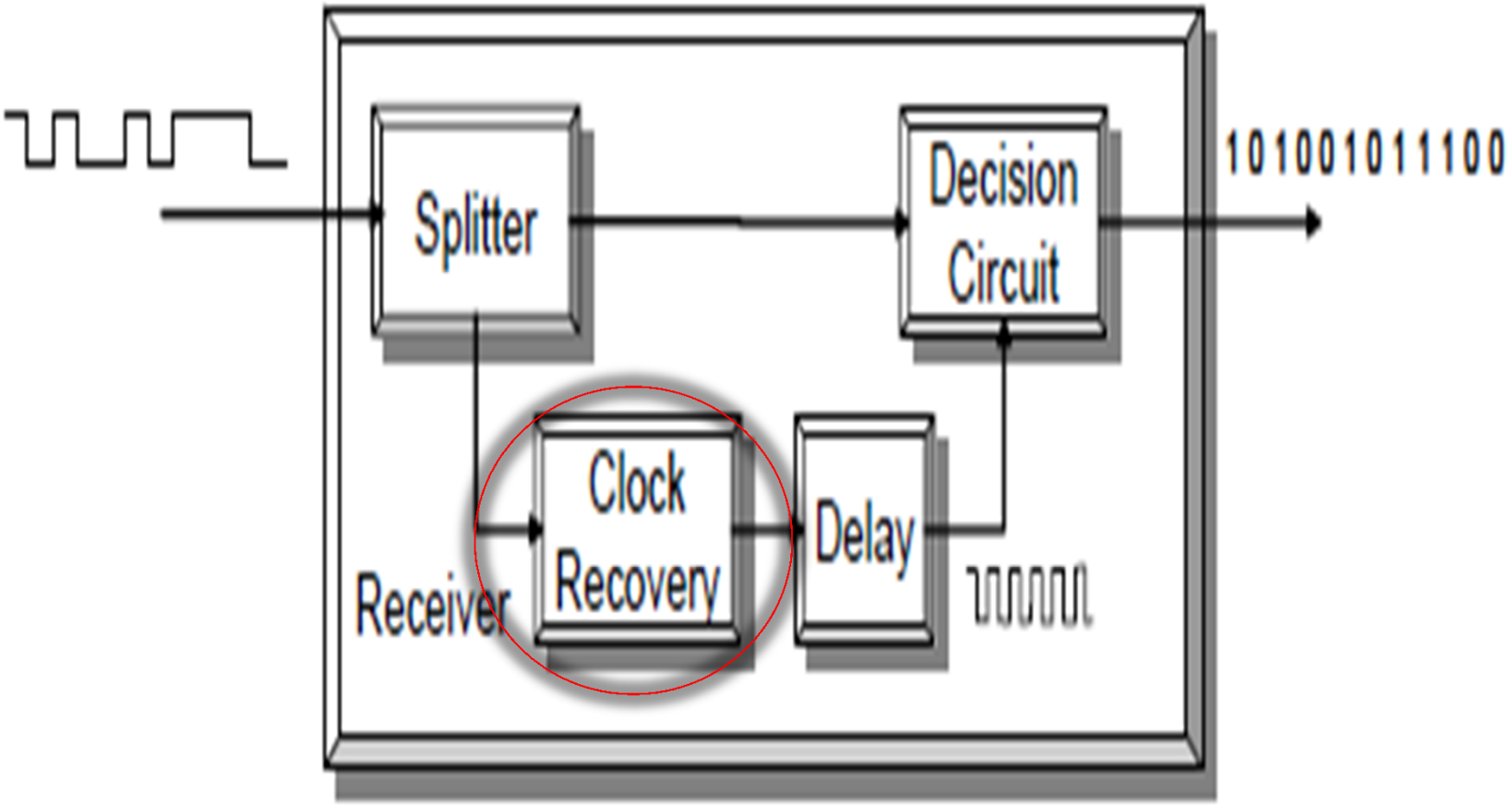

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Agenda

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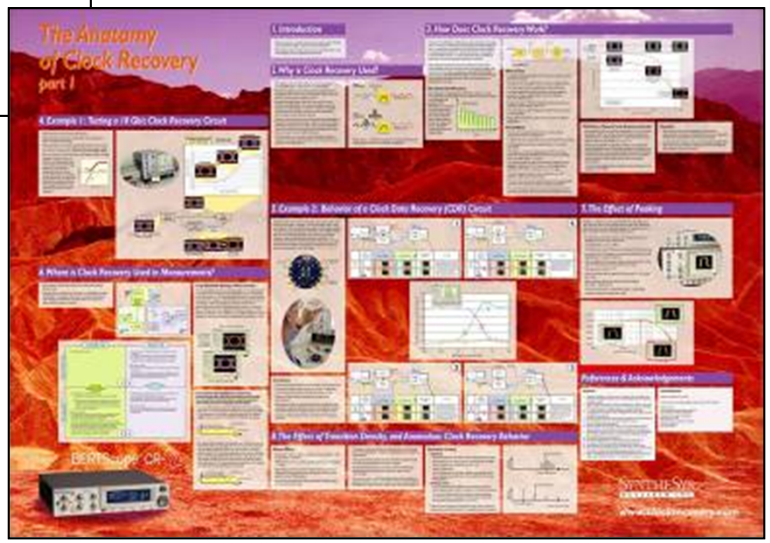
1. Why is Clock Recovery Needed?
2. Clock Recovery for Measurements
3. The Effect of Clock Recovery on Jitter
4. Calibration Considerations
5. Measurements with CR Instruments
6. Summary
7. Further Information



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1. Need to Recover the Clock

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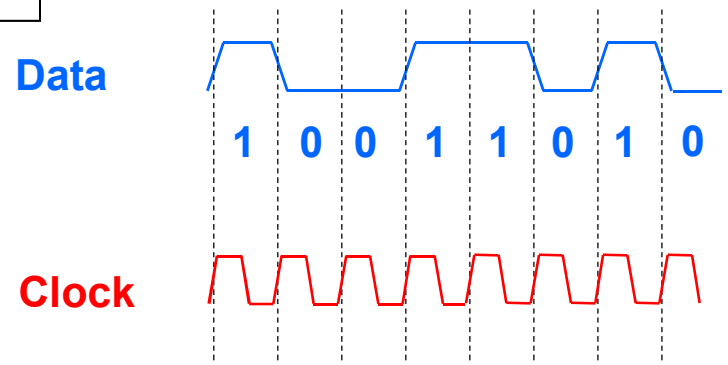
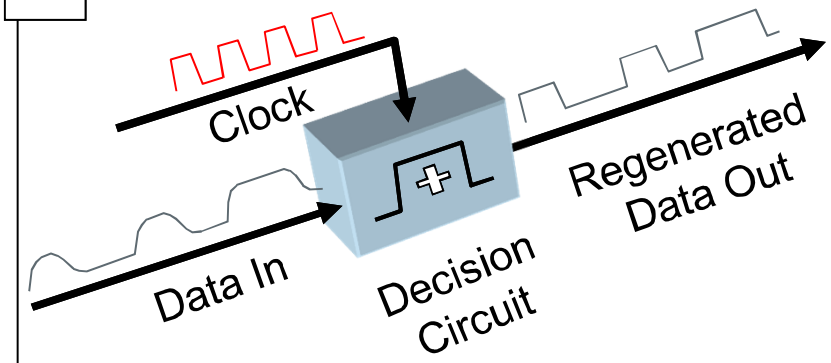
1.



- Many serial data systems use Non-Return to Zero (**NRZ**) line coding, with embedded clock.
- As the name implies, NRZ data has no state transitions between successive bits of the same state – zeros or ones.

2.



- The **clock recovery** circuit generates an **edge for every bit** – including those without transitions.
- The clock is used by the **receiver** or **instrument** to determine **when** to sample the data state.

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2. Clock Recovery for Measurements

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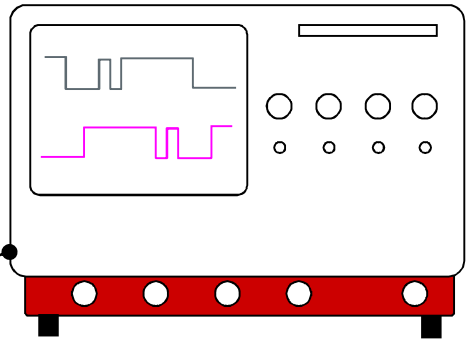
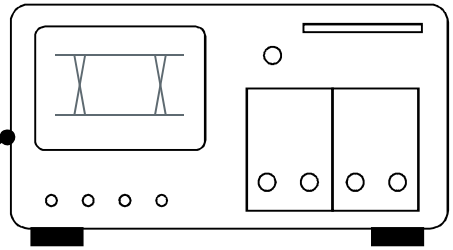
1. Clock recovery is also required for many test instruments which characterize serial data systems.
   - **Recovering clock** may be **desirable** even when Tx clock is available.
2. Instruments which sample the data contiguously, such are **'real time' oscilloscopes**, implement software based clock recovery.
   - Generally limited to lower data rates / limited measurement depth.
3. Sampled data instruments require a hardware clock, derived from hardware clock recovery.
   - **Sampling oscilloscopes** – for measuring higher data rates.
   - **Analyzing BERTs** – for greater measurement depth or higher data rates.
4. "Instrumentation Grade" clock recovery is required.
   - Calibrated, repeatable, and adjustable.





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2. How Does a Clock Recovery Work?

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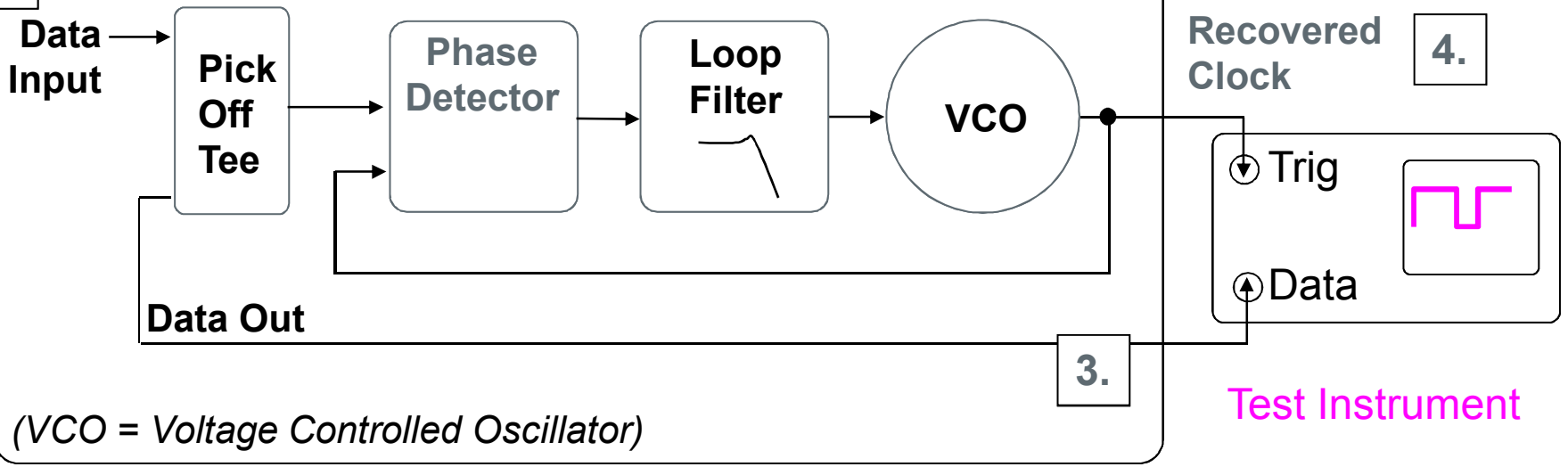
1. Modern hardware clock recovery systems are based on a specialized phase locked loop (**PLL**).
   - For Clock Recovery, a **modified phase detector** is used.
   - The phase detector **looks for edges** only, and ignores missing edges.

2.



(VCO = Voltage Controlled Oscillator)

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3. Clock Recovery Tracking of Jitter – Cleaning the Regenerated Data

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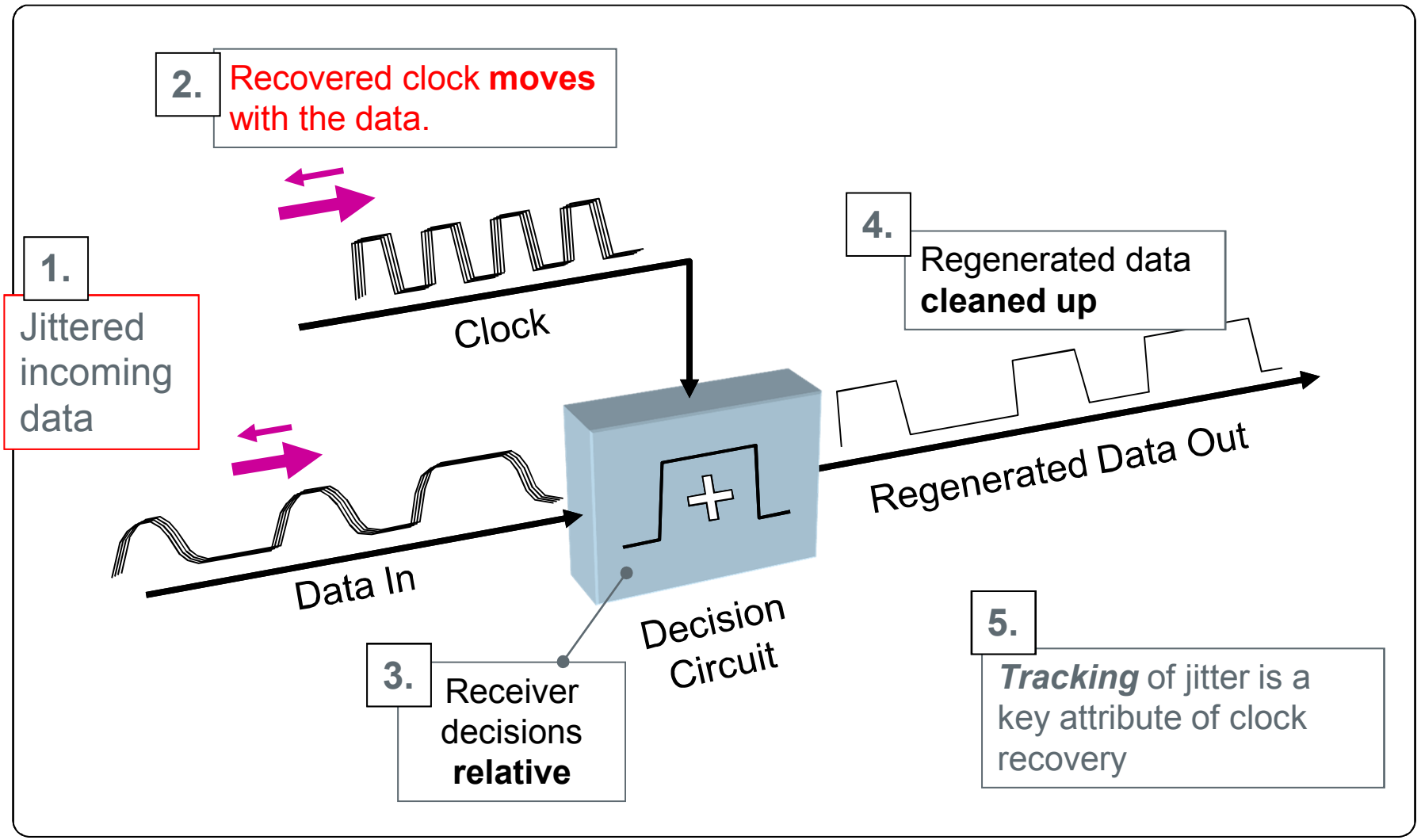

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3. PLL Loop Response

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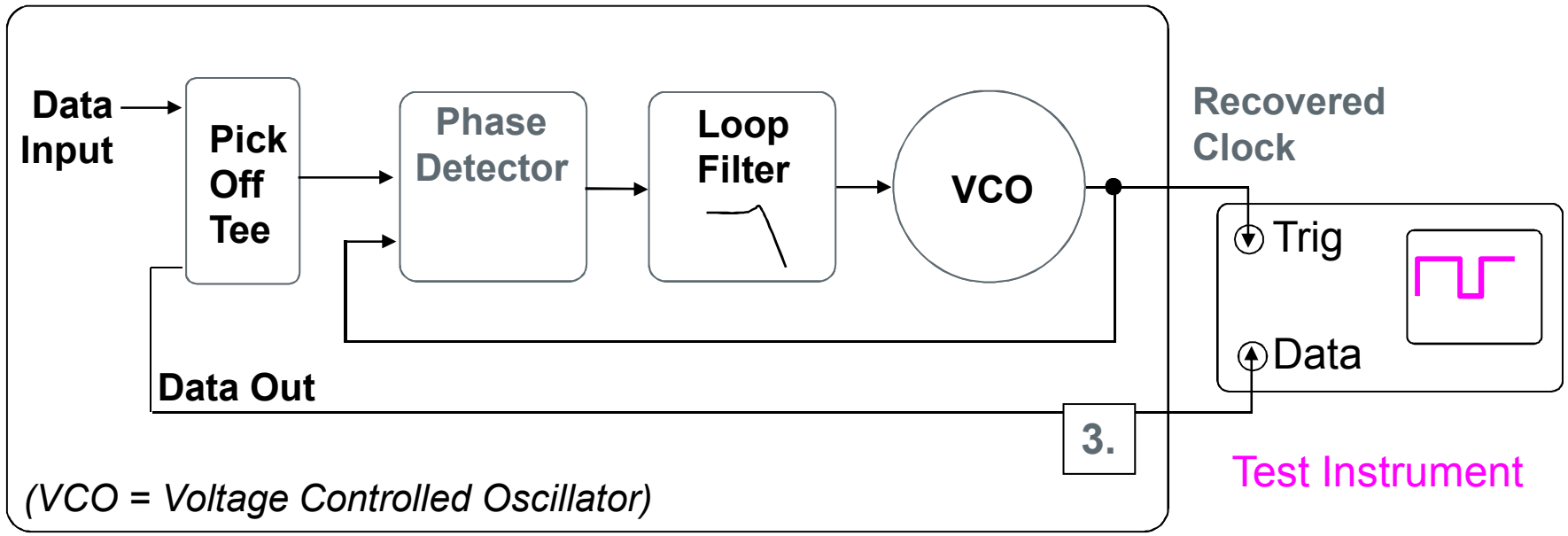

1. Variations in input frequency (edge rate) below the PLL roll off will be **tracked** by the VCO and **appear in the recovered clock output**.

2. Variations in input frequency (edge rate) higher than the PLL roll off will **not** be tracked by the VCO and **be removed from the recovered clock output**.

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3. The Loop Response - Illustrated

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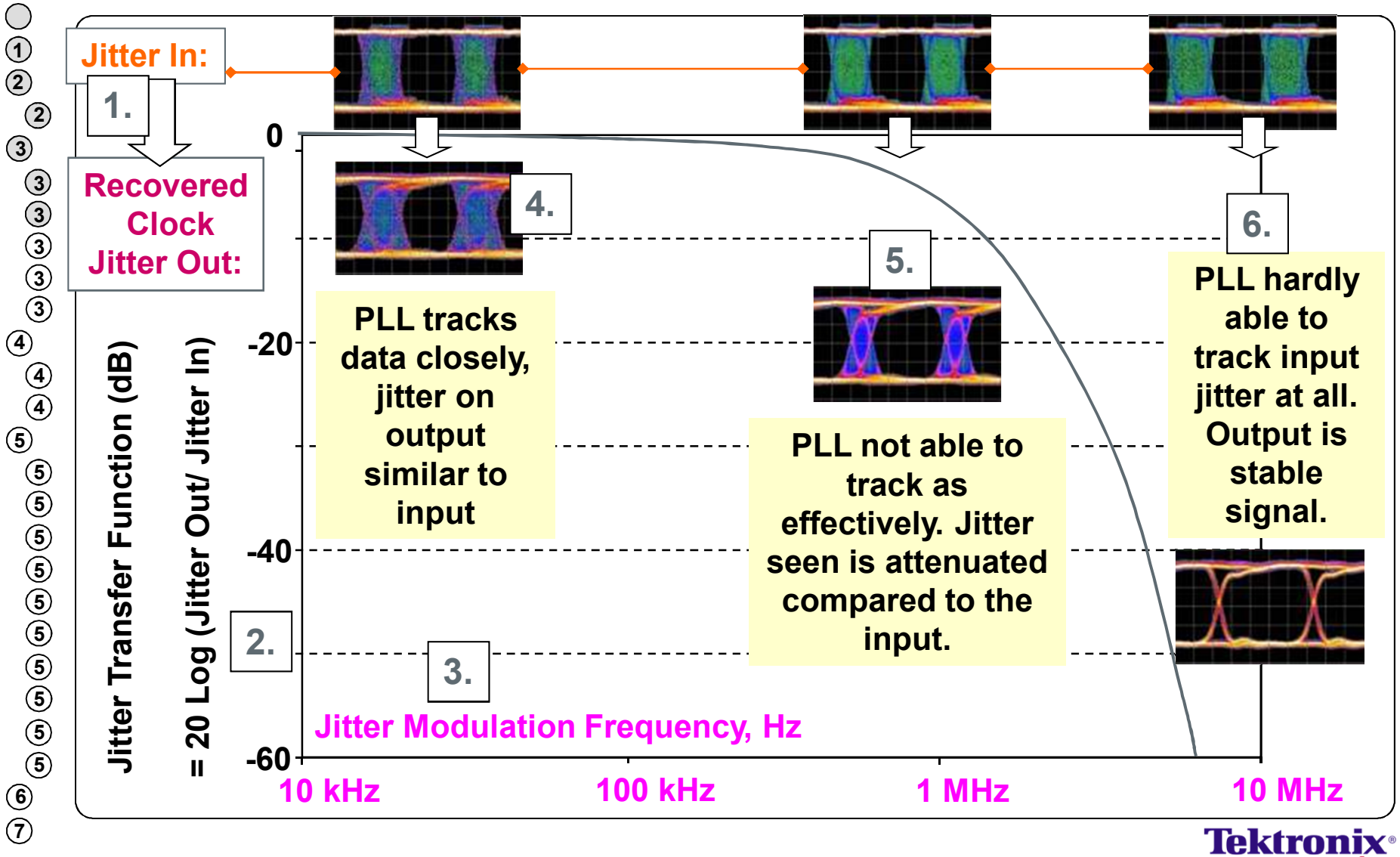

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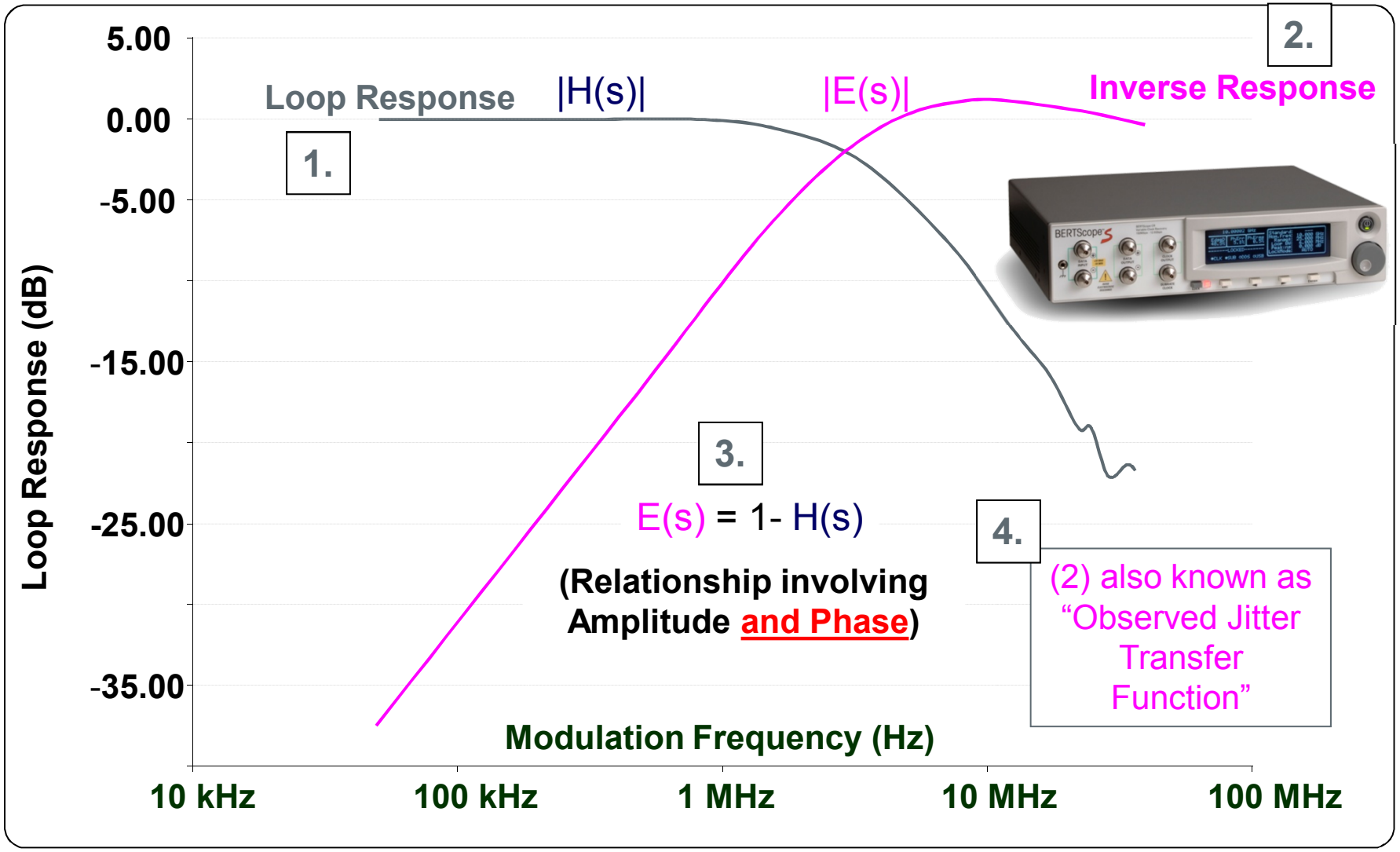
3. Phase included in Jitter Transfer Function

BERTScope™



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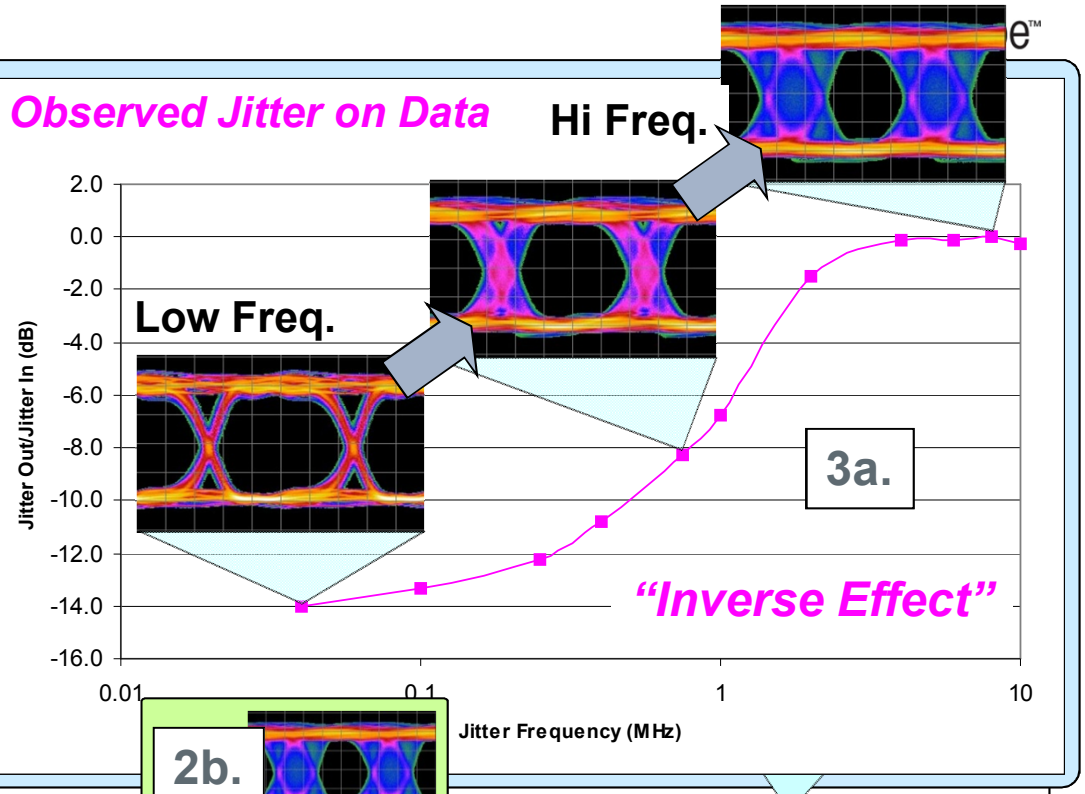
1. Change jitter freq. of data input (const. ampl.)
2. Look at recovered clock
3. Look at how jittered data behaves when regenerated



2b.

Jittered Data

1a.

Low Freq ⇨ Hi Freq
Constant amplitude

Input

Data

CR
(PLL)

Recovered Clock

Detector

Regenerated Data

Low Freq.

2a.

Hi Freq.

Tracks Jittered Data

Fails to track Jittered Data

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4. Calibration Considerations: The Effect of Peaking

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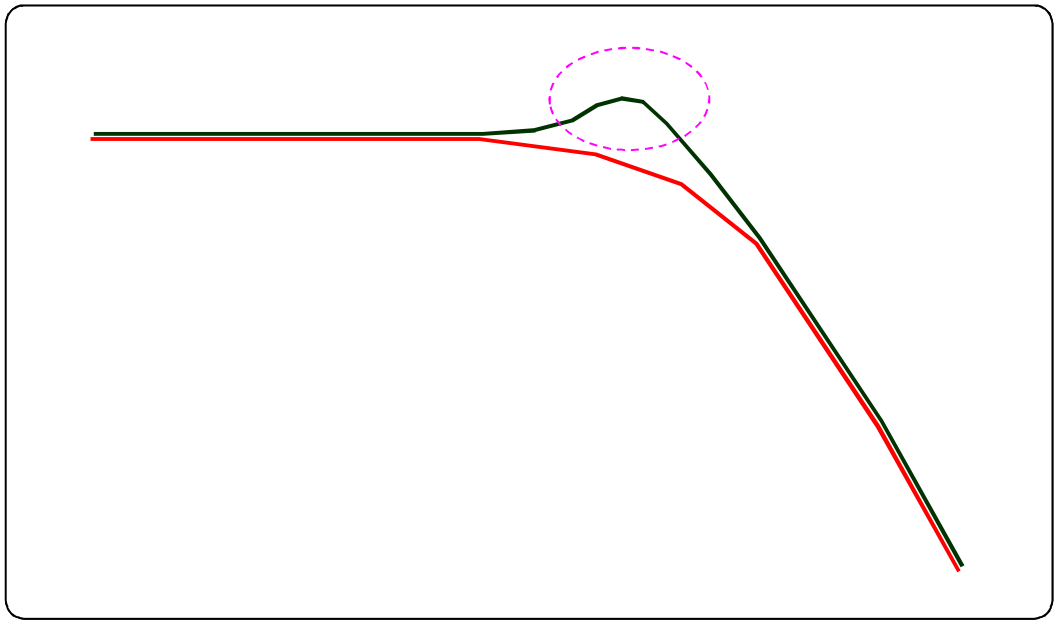
1. Loop responses can have **peaking**.



2. Peaking can cause ***Jitter Amplification*** of jitter frequency components in the region affected.
3. Peaking can **also occur** in the **Observed Jitter Transfer Function**.

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4. Experiment:
The Effect of Peaking Illustrated

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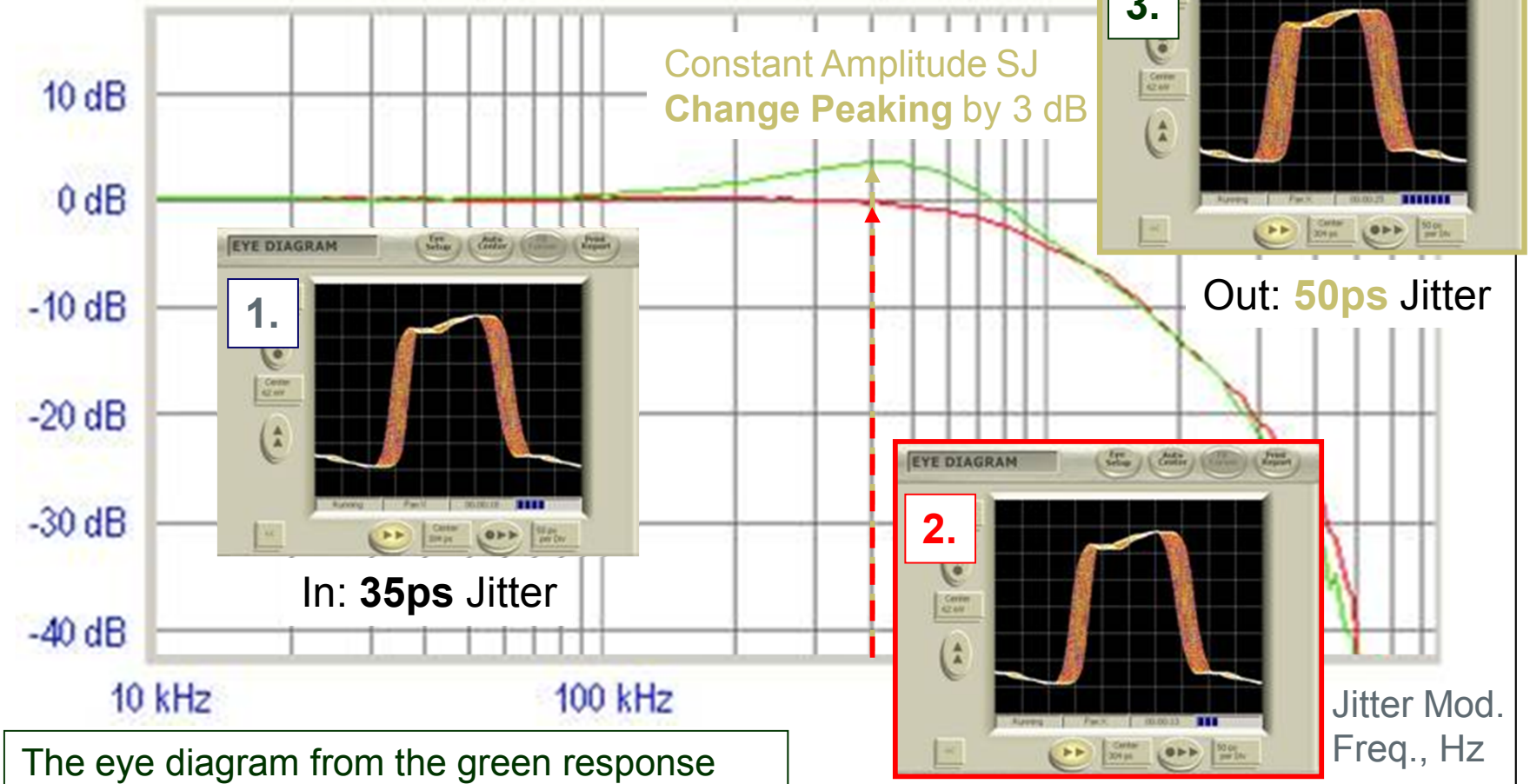
1 MHz loop bandwidth, 400 kHz SJ modulation



The eye diagram from the green response shows ***jitter gain*** – more jitter out of the device than was present on the input.

4.

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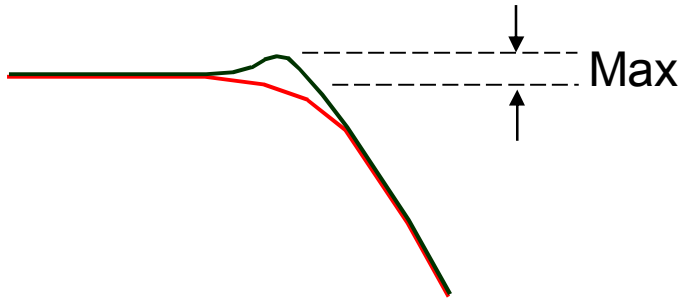
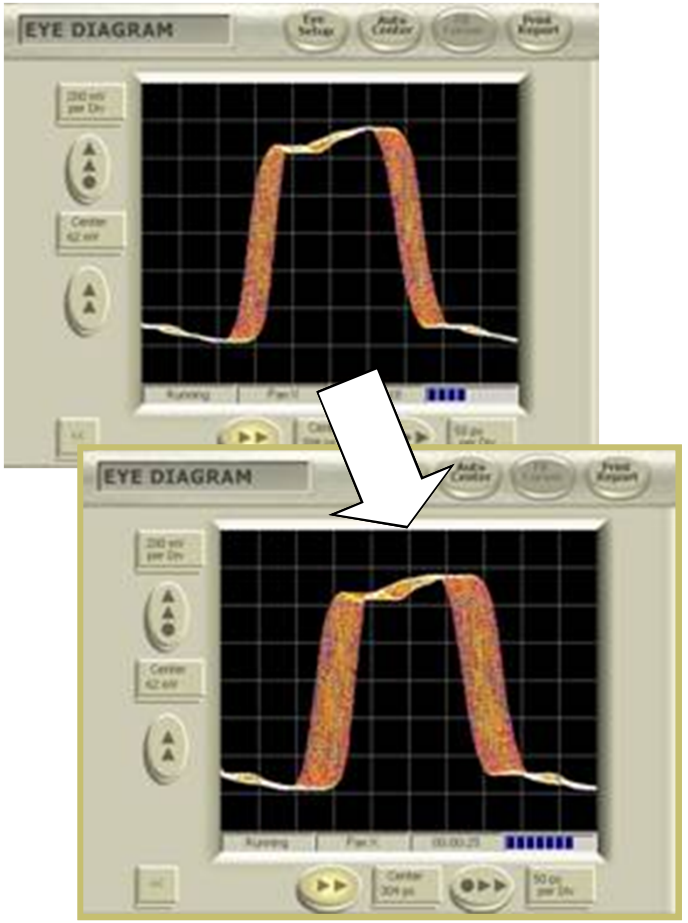
4. The Effect of Peaking Conclusions

1. **Jitter gain**, particularly in a repeatered system, is highly **undesirable**.

2. Many **standards restrict** the amount of peaking allowed.



3. **Peaking** increases the **noise/random jitter**.



5. Measurements: “Instrumentation Grade” Clock Recovery Units

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1. Clock Recovery loop response affects the **amount of jitter** “seen” by serial data analysis instruments.
   - Loop bandwidth
   - Roll off slope
   - Peaking

2. The parameters must be **tightly controlled** for **accurate and repeatable** jitter measurements.

3. The ability to **adjust** these parameters is often required.
   - CR characteristics are often dictated by many Compliance Test Standards.
   - Setting the parameters to match those in receiver allows the instrument to “see” the data as receiver does in the real system.

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5. Edge Density

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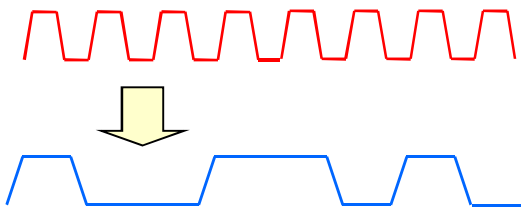
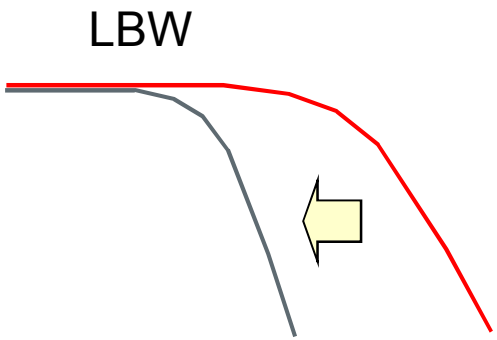
1. Different data patterns have different “edge density” or “transition density”.
   - A 1010 clock pattern has a 100 % edge density.
   - A true PRBS pattern has a 50 % edge density.



2. The pattern’s **edge density effects** the energy entering the PLL phase detector, which affects the loop response, **loop bandwidth**.

3. The calibration of loop response requires knowledge of the edge density.



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5. CR Performance Considerations

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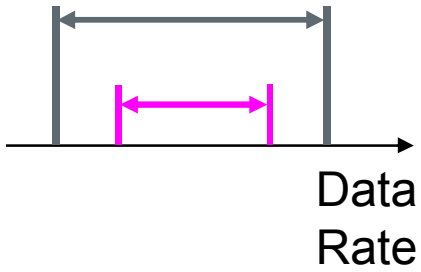
1. Performance specifications include Capture Range and Lock or Tracking range.
   - **Capture Range** - maximum deviation from nominal clock frequency the PLL will lock on.
   - **Tracking Range** – the maximum deviation from nominal clock frequency which the PLL will remain locked.



2. High Capture and Tracking Range are needed for use with systems employing Spread Spectrum Clocking (SSC).

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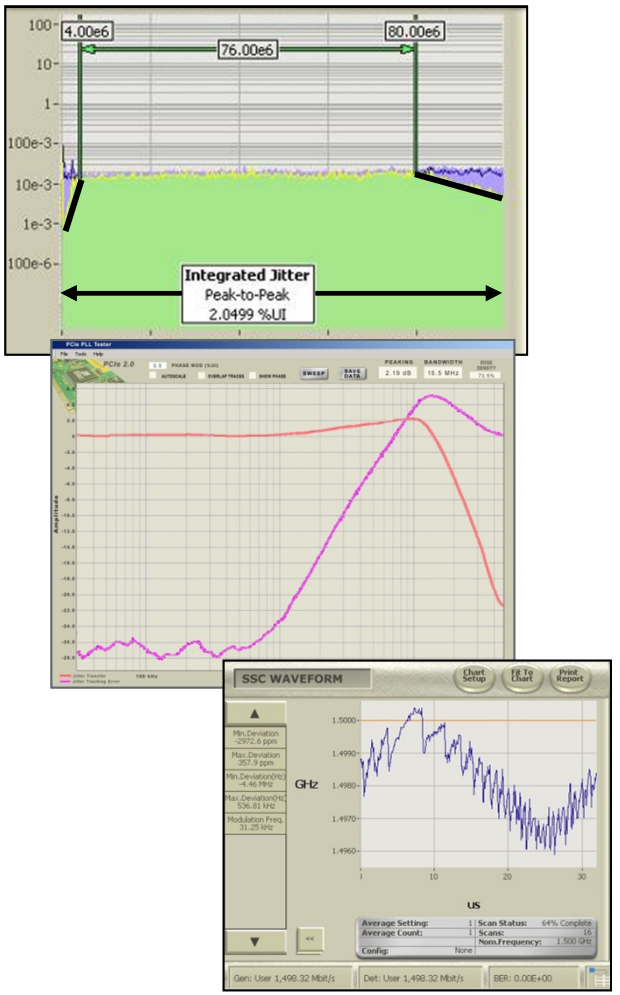
5. Measurements with a Clock Recovery Instrument?

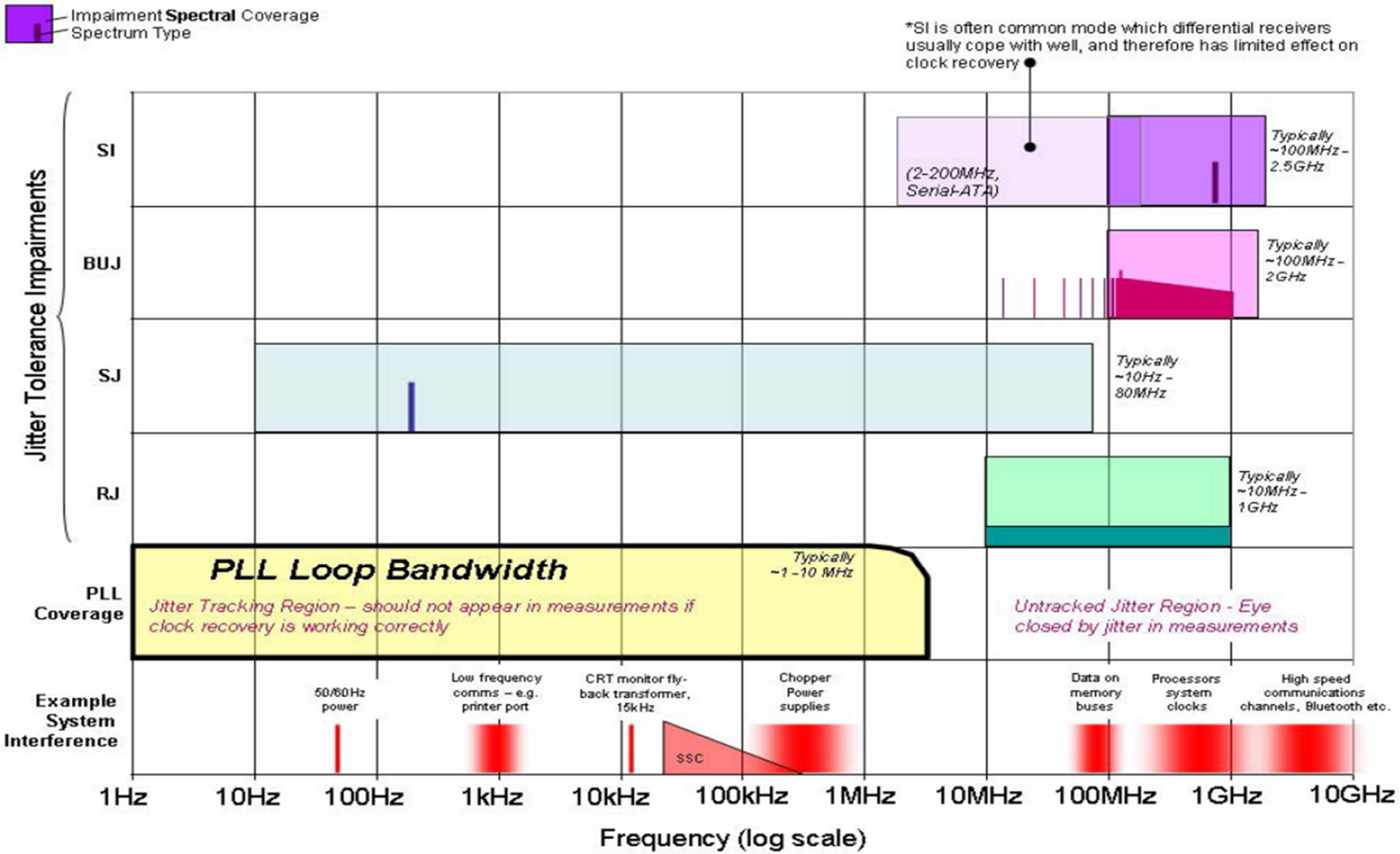
- With additional internal components, a Clock Recovery Instrument can perform **measurements** as well.

1. **Jitter Spectrum**, including SONET jitter generation measurements
2. Phase Lock **Loop Response**, such as is required by PCI Express
3. Examination of **SSC waveform** for troubleshooting

We'll look at each in more detail.



Relating Stress Types to Typical Loop Bandwidths, and Some Common Causes of System Interferences



What causes “poor bits”?

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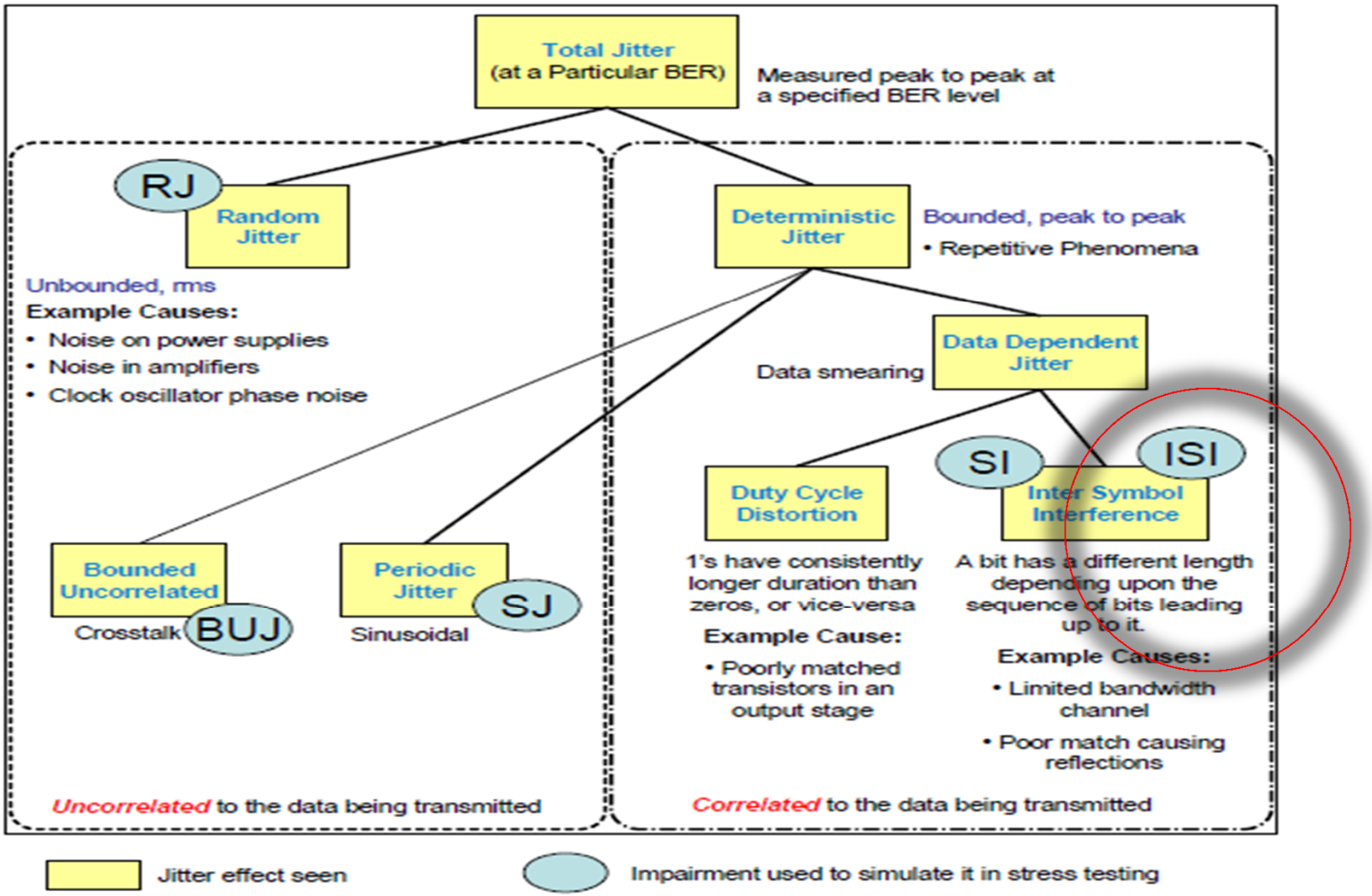

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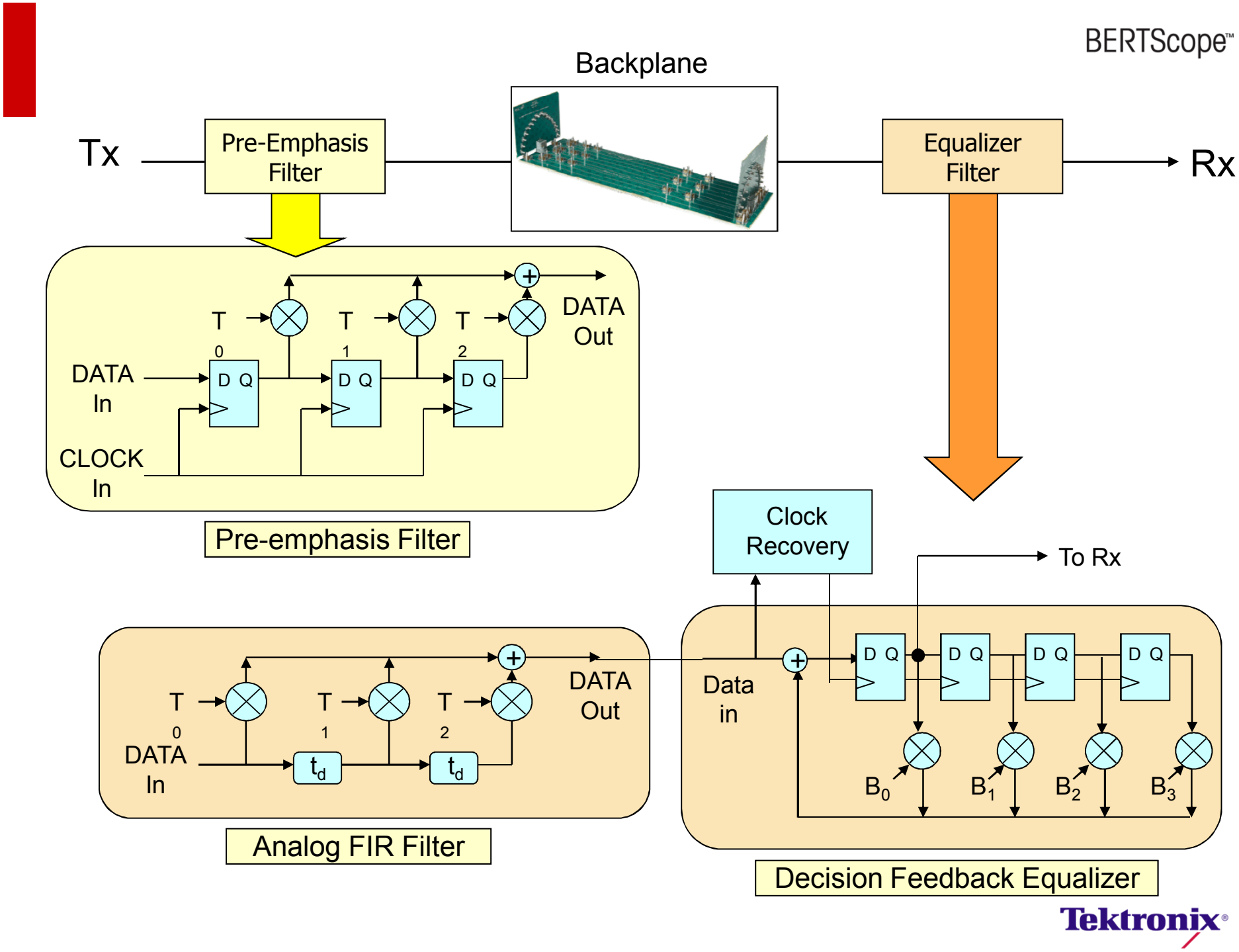
BERTScope™



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Agenda

- So What's the Problem?
- What Can Happen to Data?
- Measuring Insertion Loss
- Methods of Compensation
- Impulse Responses & FIRs
- PCIe Pre-Emphasis Example
- Designs of Equalization
- Summary

Pre-Emphasis & Equalization… What's the Big Deal?

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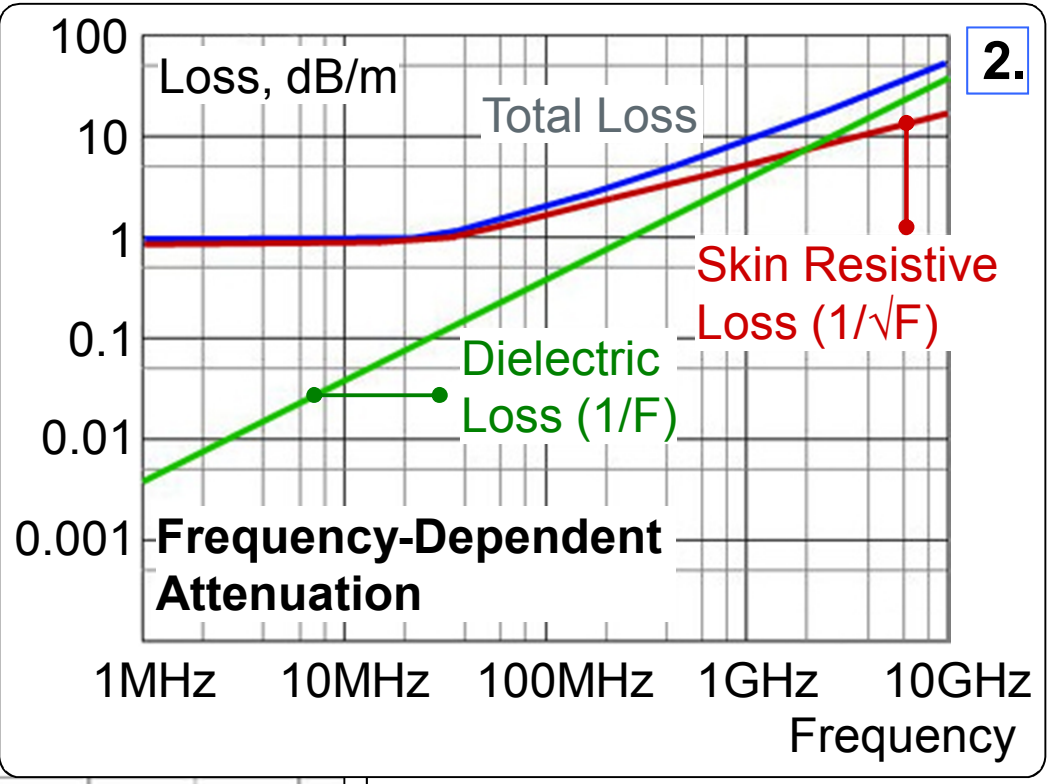
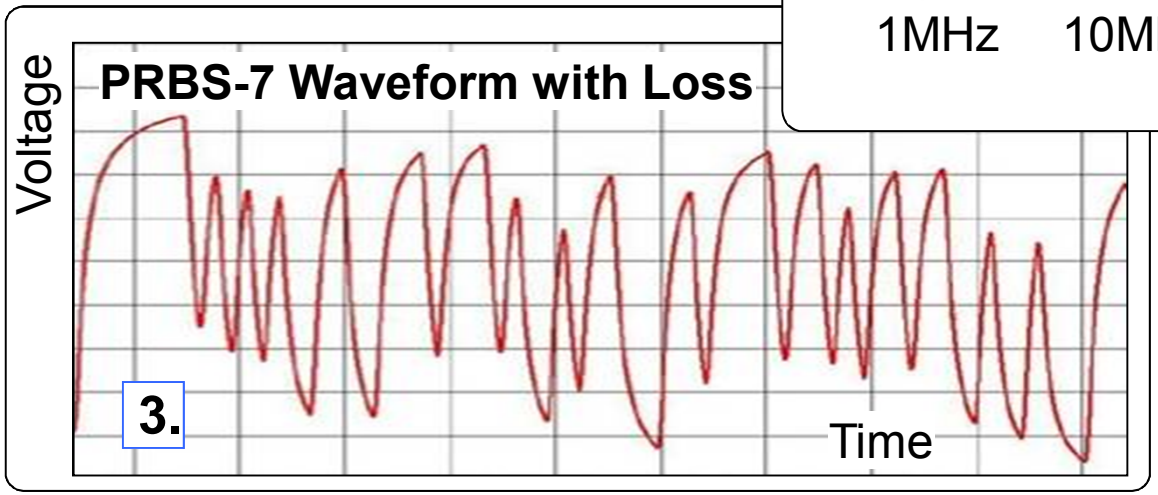
- Higher data rates, longer distances, cheaper materials are a recipe for trouble **1.**
- Bandwidth limitations are caused by frequency - dependent losses in all types of media
  - E.g. 40" of FR-4 Material





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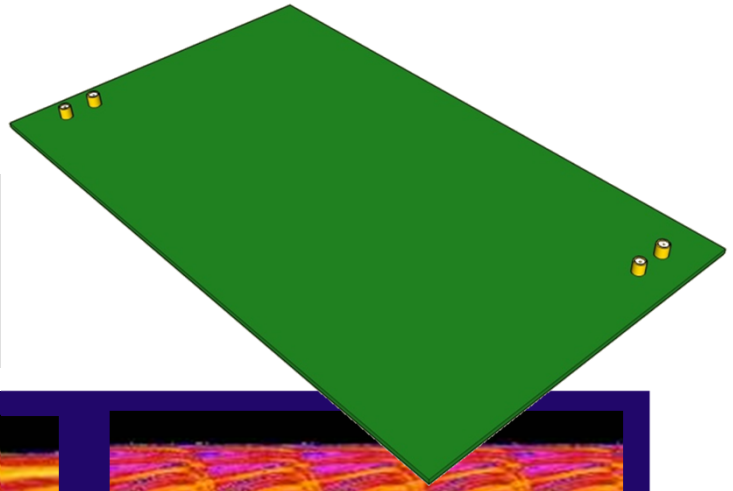
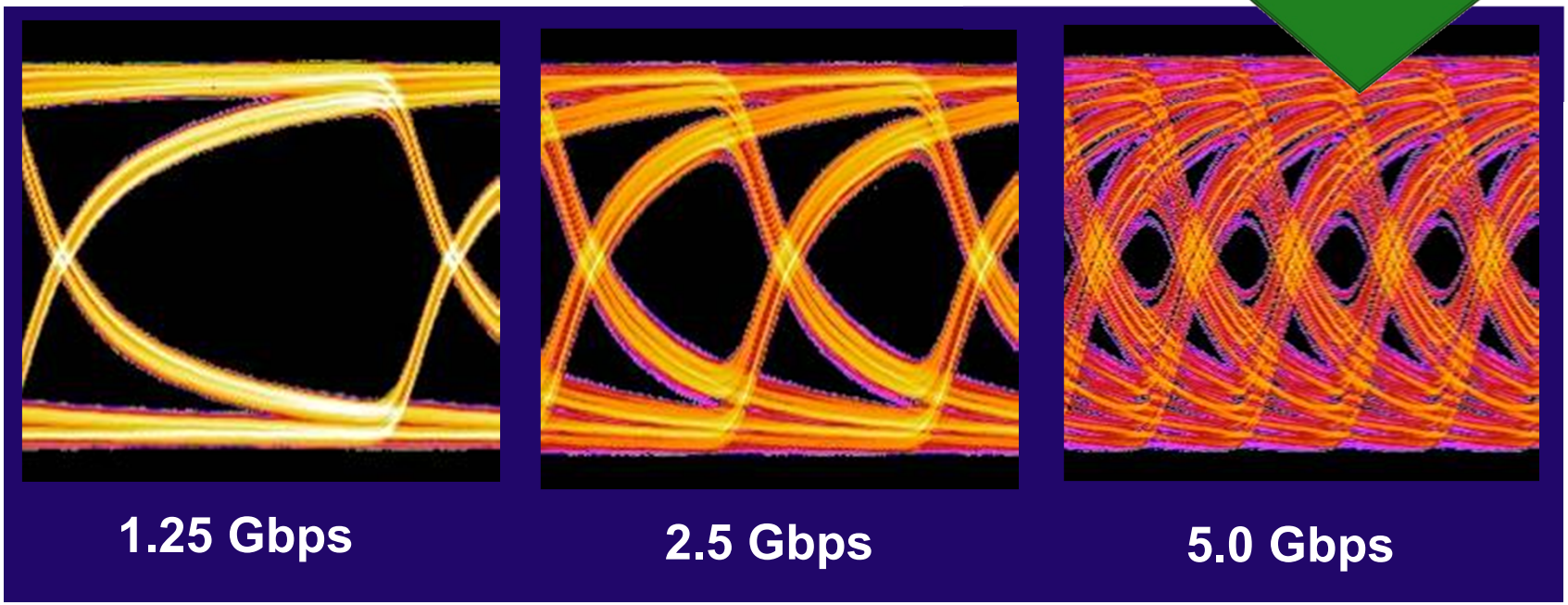
Impact of Bandwidth Limitations



- Bandwidth limitations create inter-symbol interference which eventually limit the ability to distinguish one bit from another



Noise/jitter closes-down the available headroom in the eye opening

Measured eye diagrams from a 40” PCI-Compliance ISI Trace, PRBS-7 Pattern

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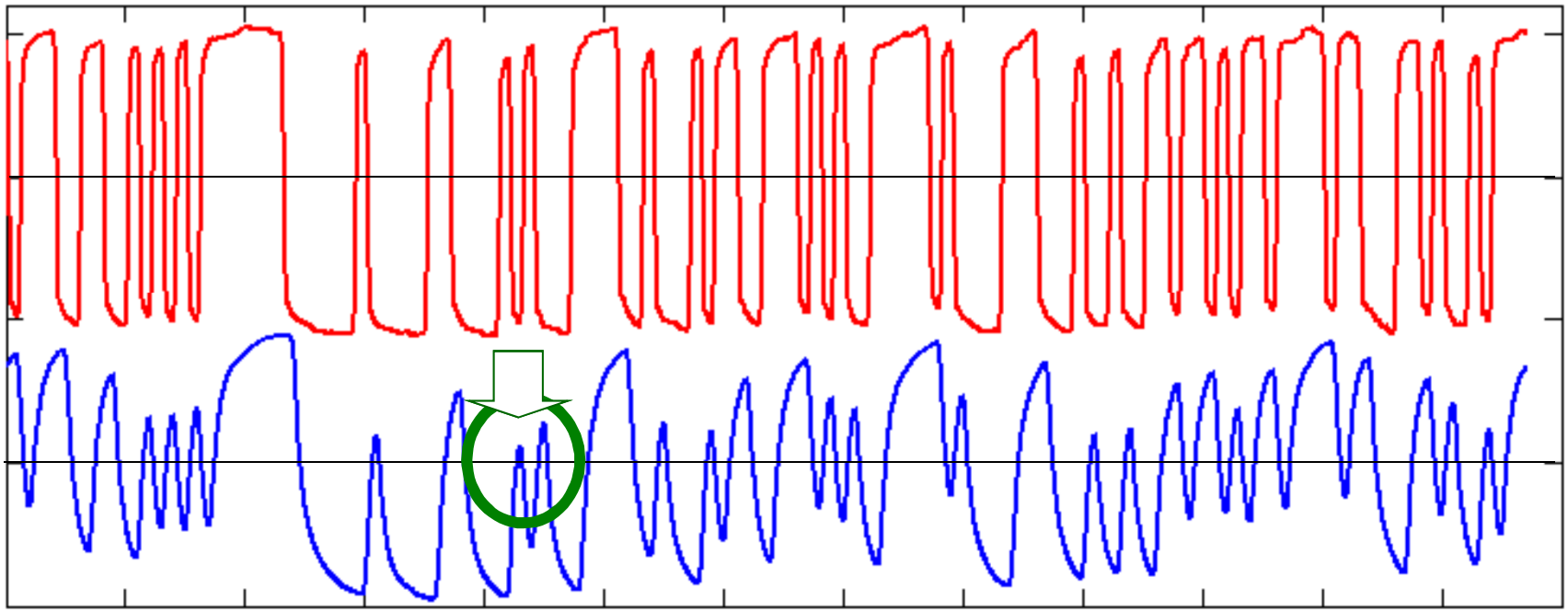
What Happens to Data?

- Using a 40” PCI-Compliance ISI channel at 5Gbps, PRBS data is significantly distorted



- Baseline wander follows consecutive bits in the bit pattern
- Certain bit patterns cause the worst opening
  - These will have high bit error rates

Channel Loss Causes Bit Errors
Pattern Dependent

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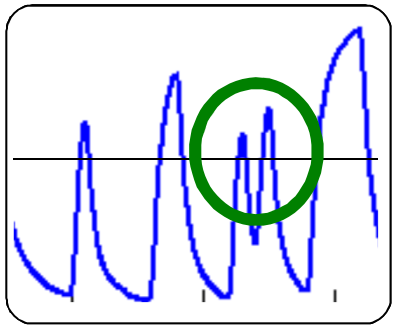
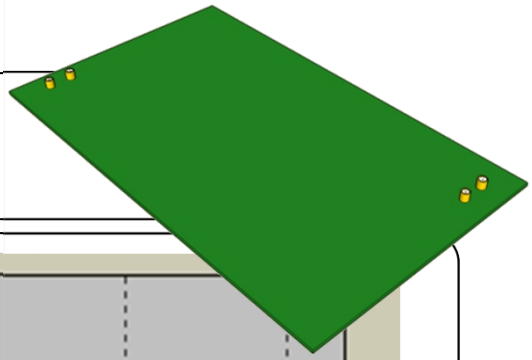
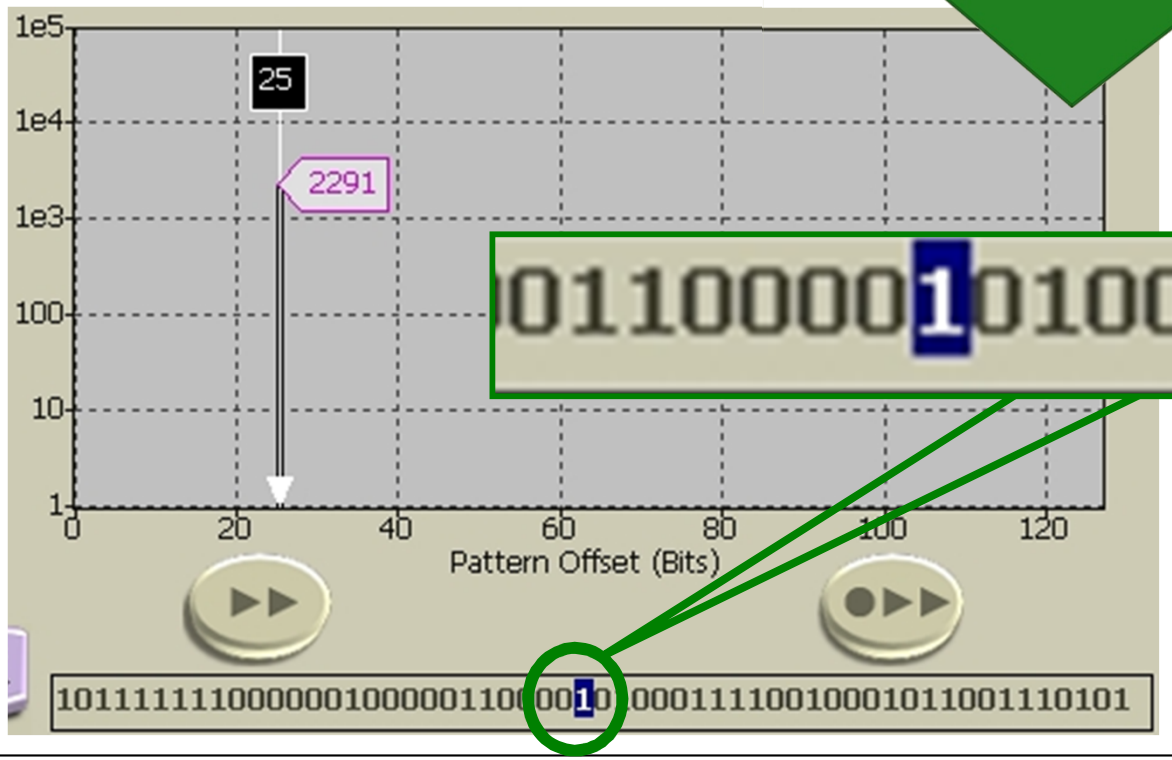
- In these types of channels, we can study bit error locations in the received pattern…







Measurement of Pattern Sensitivity (to PRBS-7 Pattern)

- Here we have found 2,291 bit errors that all happened at this most-distorted bit in the PRBS pattern

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Loss Impact on Jitter Margin

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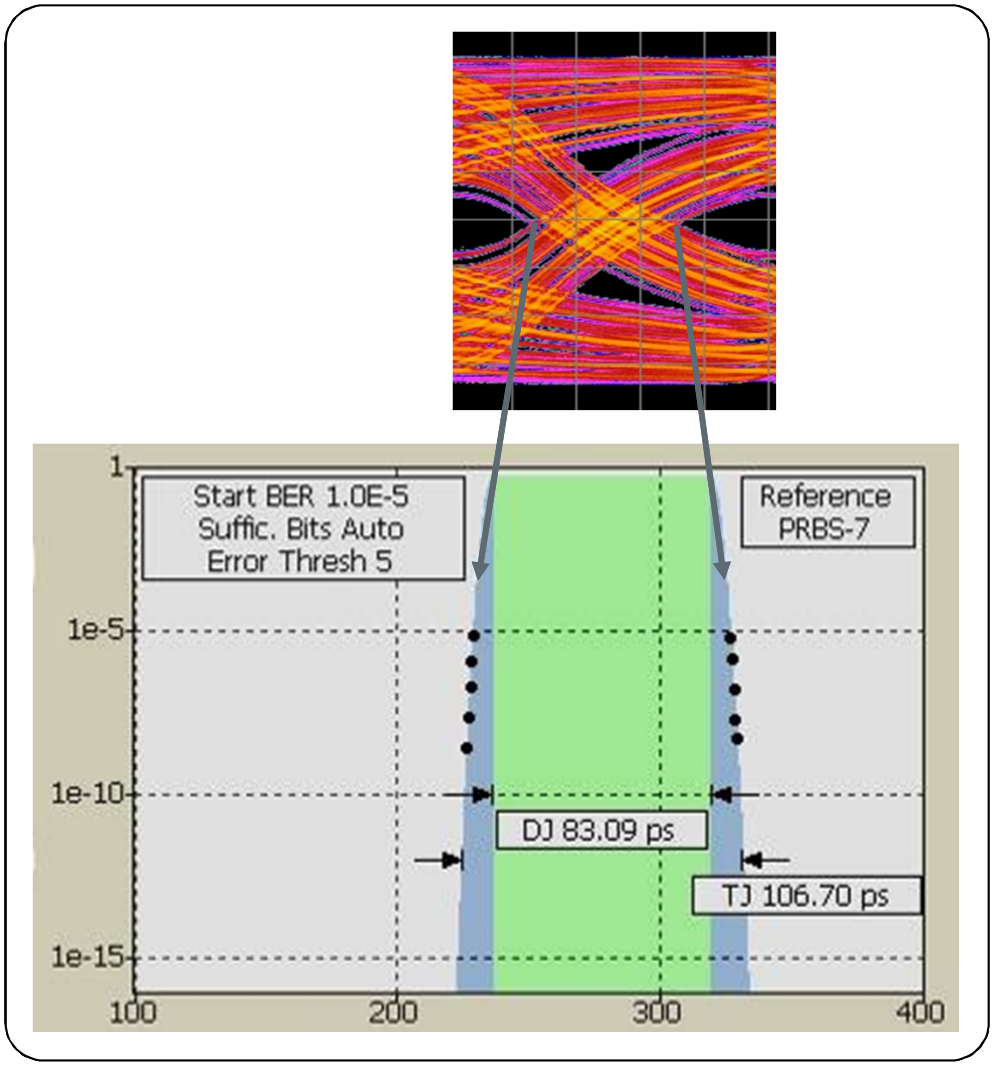
- ISI adds to Deterministic Jitter
- RJ remains close to the same
- This closes-down the eye…
  …and makes less margin
- At 5Gbps, 53% of eye is lost to jitter

We want to avoid this…



Measurement of Jitter Peak (BER Bathtub)

40” ISI Compliance Channel
5 Gbps, PRBS-7 pattern

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Insertion Loss of Channel

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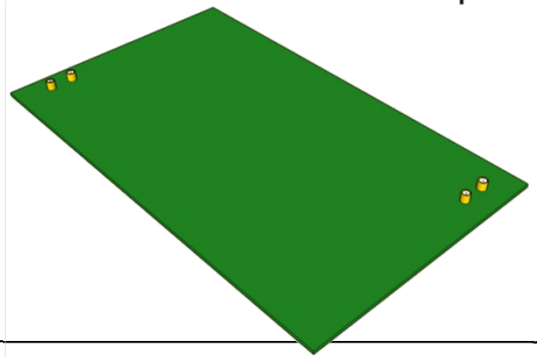
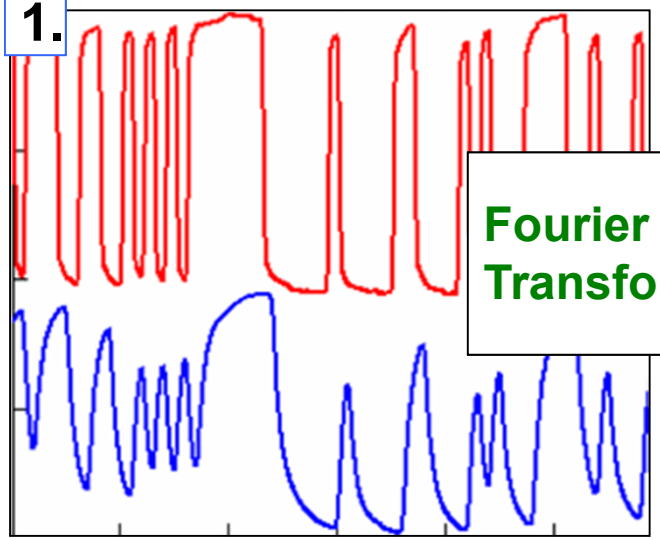


- Its easy to measure channel insertion loss (S21) with PRBS data…

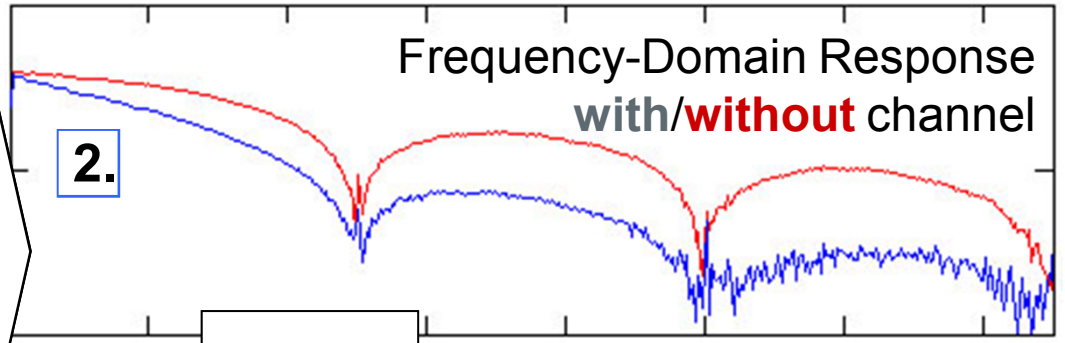
1.



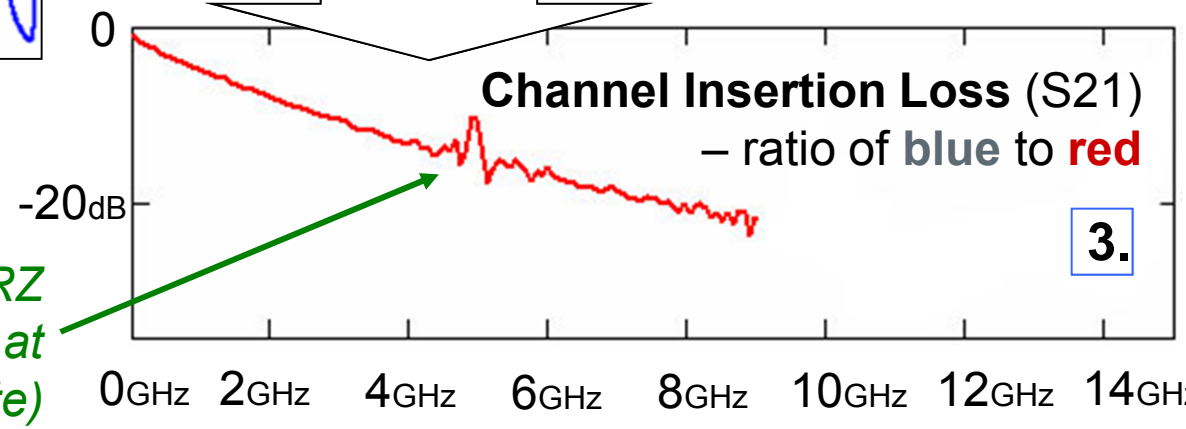
Time-Domain Response
with/without channel

Fourier Transform

2.



Ratio



(Singularity because NRZ data has frequency nulls at octaves of half-bit rate)

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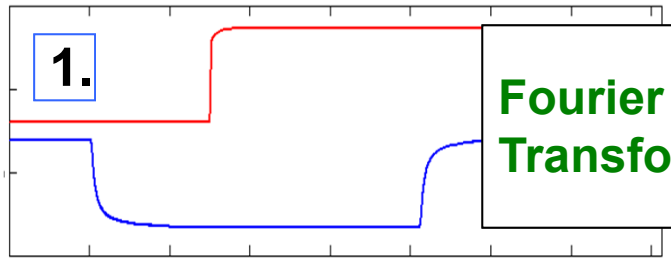
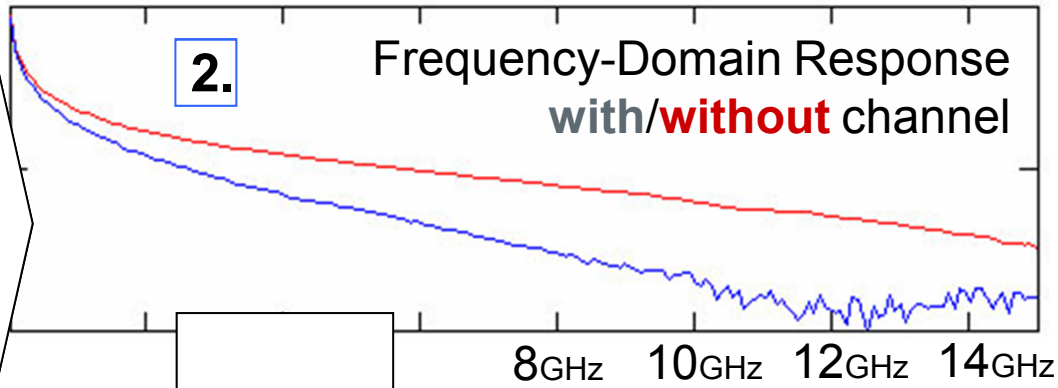
Insertion Loss of Channel (continued)

- Same can be done with a single step response…

Time-Domain Response
with/**without** channel

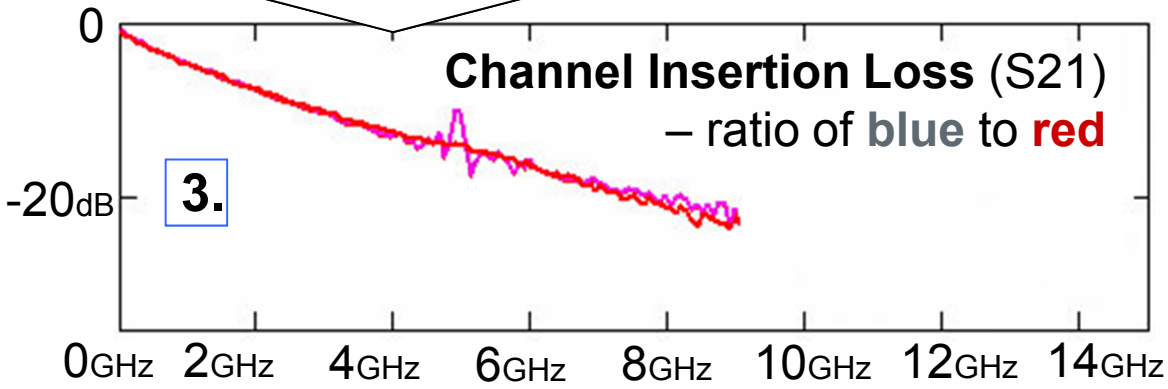


Fourier Transform



Ratio

Measurement of Averaged Single-Valued Waveform 32-samples per bit

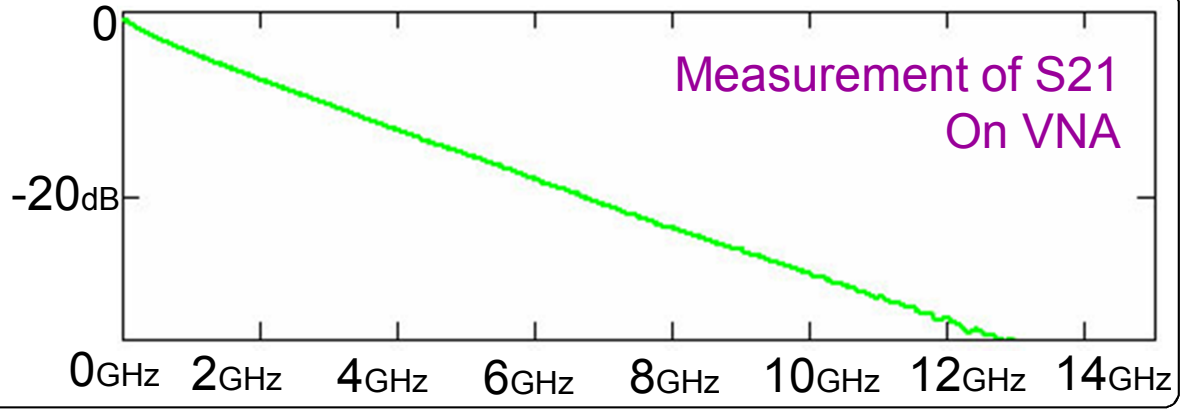


4. Both **PRBS** and **Step** data yields same loss

Insertion Loss Measurement Comparison

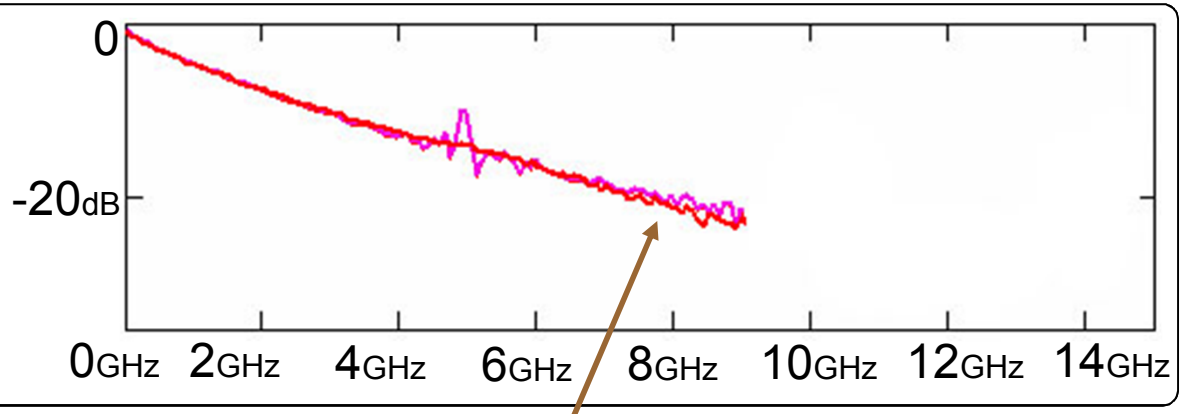
- A common but expensive way to measure insertion loss is with a Vector Network Analyzer (VNA)

1.



2.

Time-Domain
(BERTScope,
Sampling Oscilloscope)



(For all these PCIe experiments, a 7.5GHz BW filter was used for the time-domain captures, removing this filter increases S21 measurement range to >20GHz)

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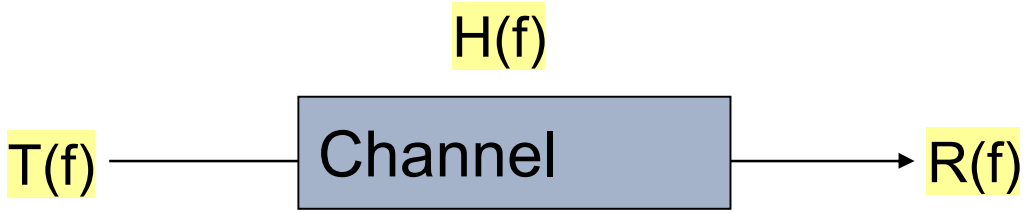
How Could You Correct For This?
Linear Signal Processing

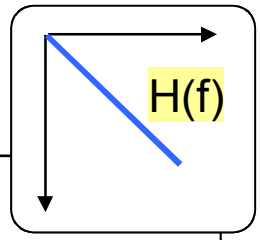
Eq

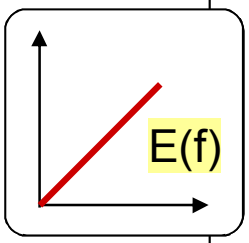
BERTScope™

1.



2.





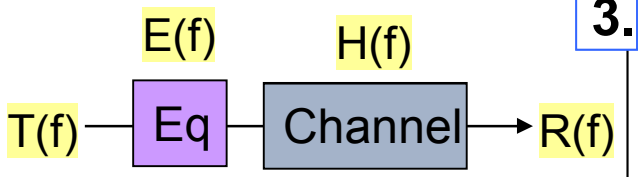
T(f) * H(f) = R(f)

Adding another filter, E(f) (equalizer) to the chain, we have

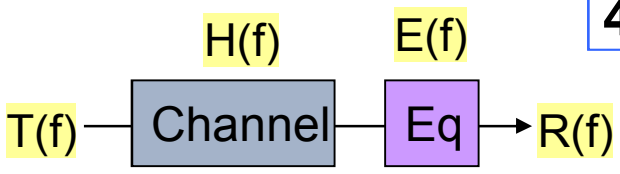
T(f) * H(f) * E(f) = R(f)

So, if E(f) = 1/H(f), then R(f) = T(f) – the ideal condition

3.

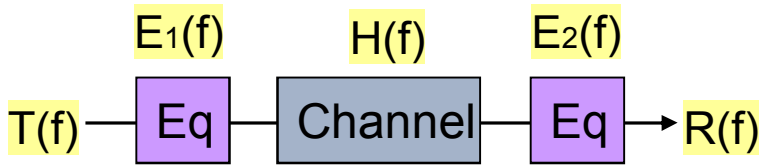


4.



Or even,

5.



Where $E(f) = E_1(f) * E_2(f)$

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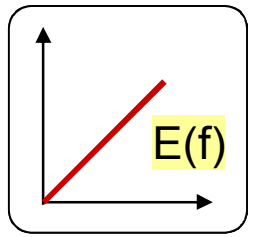
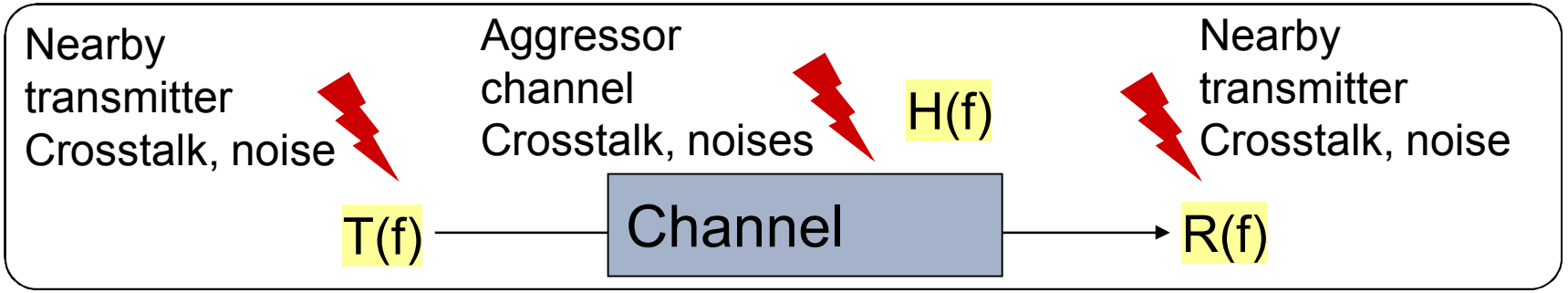
Why Choose One Architecture Over Another?

BERTScope™

- Channels have **high frequency loss**
  - so equalizers must have **high frequency gain**
- Equalizers therefore amplify high frequencies
- This **amplifies noise** as well as signal



- **Noise is added** by cross-talk, processing physics or noise interference at transmitters, receivers or channels
- Pre-emphasizing a transmitter **avoids noises** induced to the channel or receiver from being amplified
- In **dynamic** systems, a receiver is required to **estimate** how much equalization is required which can motivate **receiver-based equalization**
- **Different architectures imply different IC space/power requirements**



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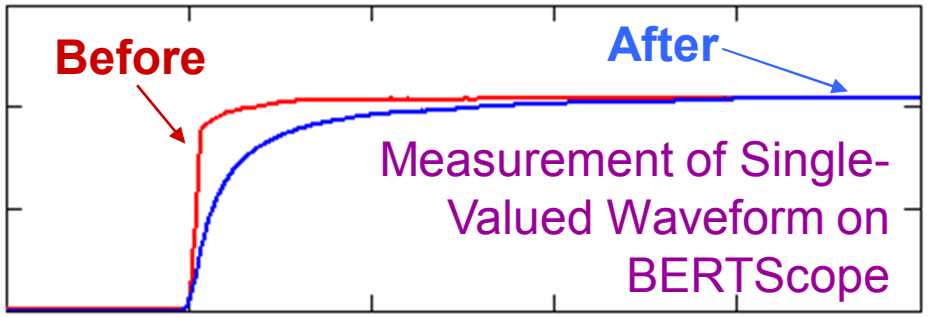
Synthesizing the Equalization Filter

Time-domain or Frequency domain

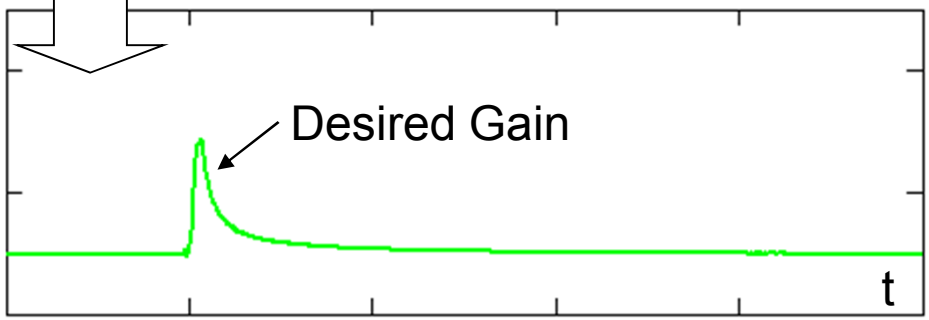
BERTScope™

Time-Domain

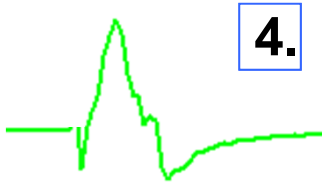
1. High-frequencies found in step transitions must be exaggerated



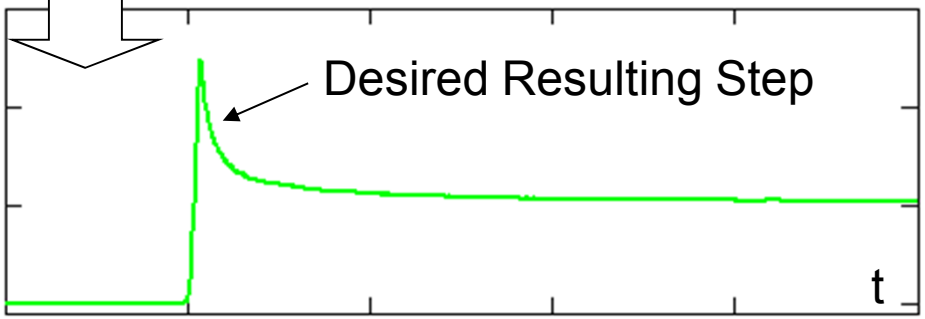
2. This amount of Gain needs to be applied to a step…



4. dGain/dt is the impulse response of the required filter



3. The resulting step response is required to pass through the channel unharmed



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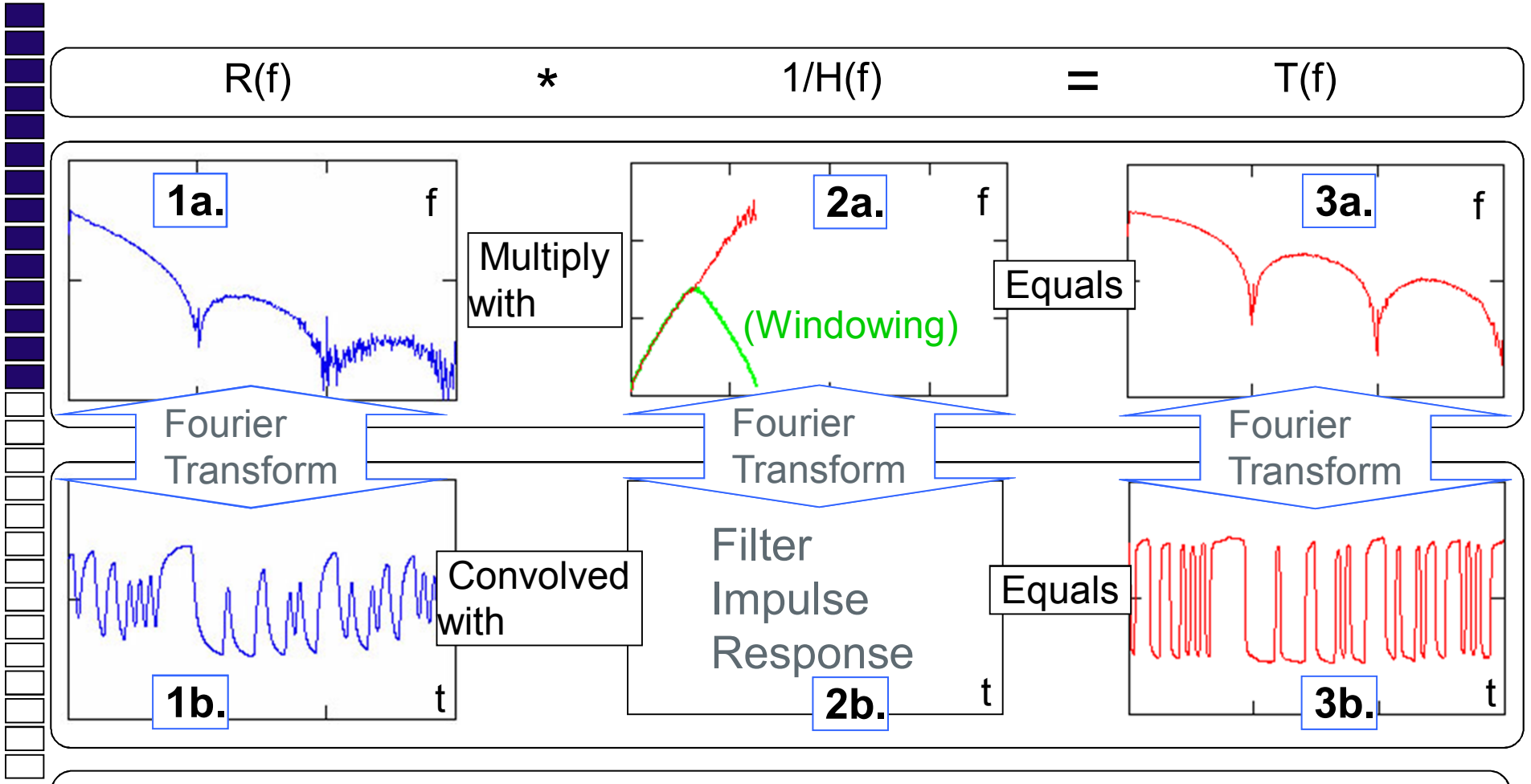
Synthesizing the Equalization

Time-domain or Frequency domain (continued)

BERTScope™



Filter response can be found by either transforming the inverse channel or by Deconvolving the time responses

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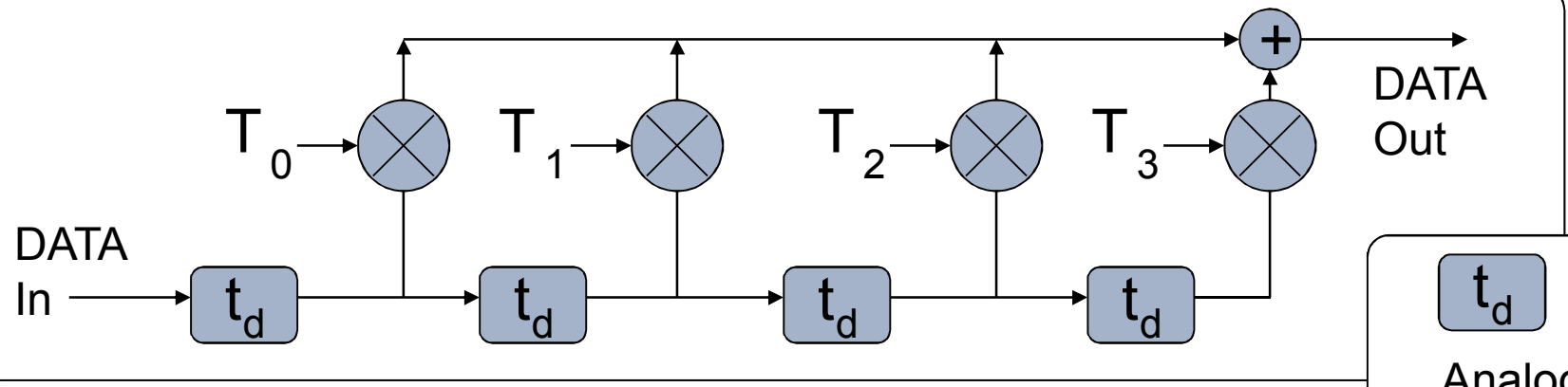
Finite Impulse Response (FIR) Filters

BERTScope™

- **Linear** Implementation that offers flat phase response



…Analog delay in real-time

- This circuit performs a **convolution** of **Data-In** with **Taps-heights**
- An impulse in, yields tap-heights spaced by t_d out
  - **Tap-heights**, therefore, are **set to be the impulse response**
- **A step in**, yields an **integration of the Tap-heights out**
- Any number of taps can be used to generate any length of impulse response
  - But **creating analog delays** can be **troublesome**

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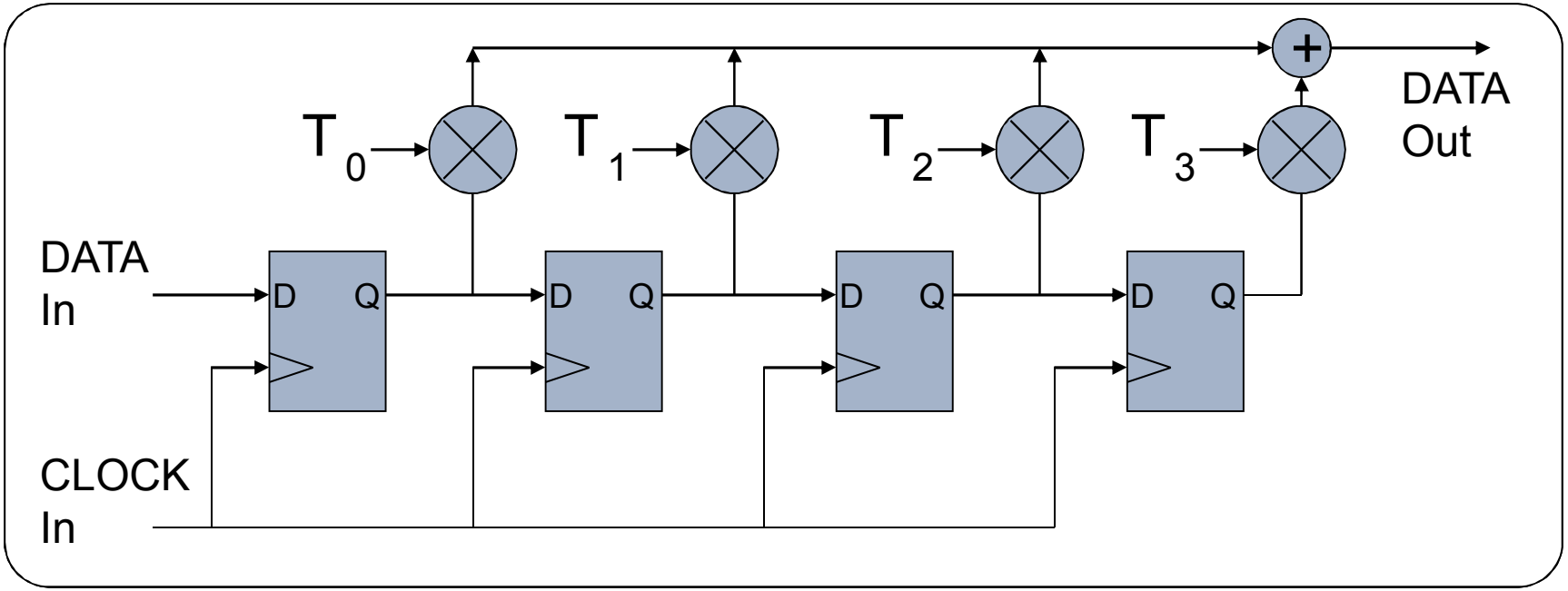
Digital Finite Impulse Response (FIR) Filters

BERTScope™

- A clock is required and only digital 1's and 0's are processed



- Again, flat phase response
- Again, **Tap-heights** are set to the **impulse response desired**
- **Delays** elements implemented with clocking input
  - This **tracks data rate**

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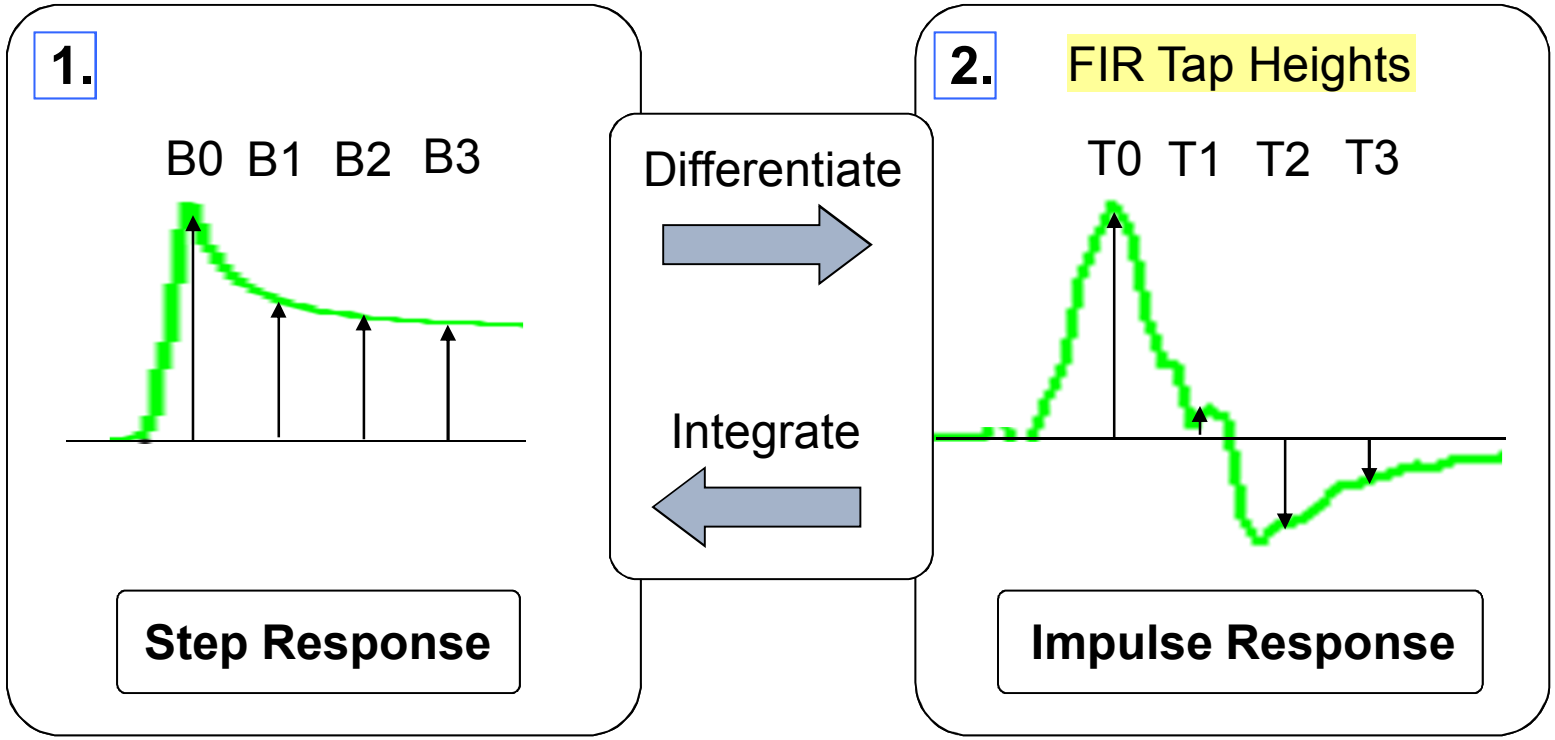
Desired Synthesized Response to an FIR
Need to Calculate Tap Heights

BERTScope™

- After we've synthesized the desired step response, to use an FIR filter, we need to compute the tap heights



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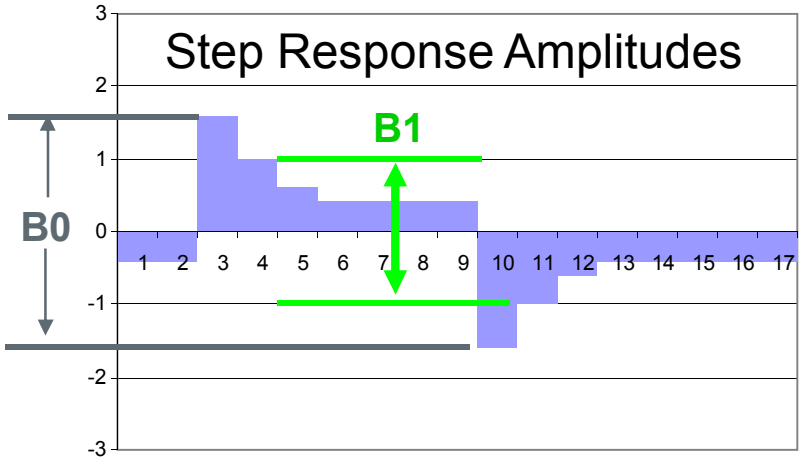
Relating Tap-Heights to Step Responses

Digital FIR's only need simple addition/subtraction

BERTScope™

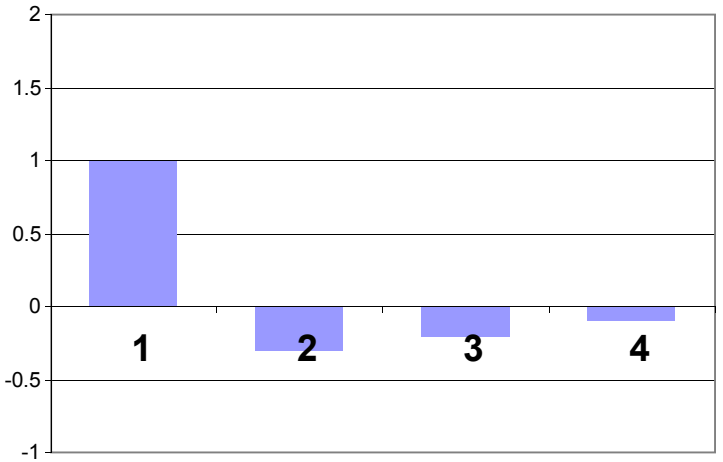
1. Calculate Tap Heights from Step Amplitudes

T0	1		=(B0+B3)/4
T1	-0.3		=(B1-B0)/4
T2	-0.2		=(B2-B1)/4
T3	-0.1		=(B3-B2)/4



2. Calculate Bit Amplitudes from Tap Heights

B0 Ampl	3.2	units	=2*(T0-T1-T2-T3)
B1 Ampl	2	units	=2*(T0+T1-T2-T3)
B2 Ampl	1.2	units	=2*(T0+T1+T2-T3)
B3 Ampl	0.8	units	=2*(T0+T1+T2+T3)



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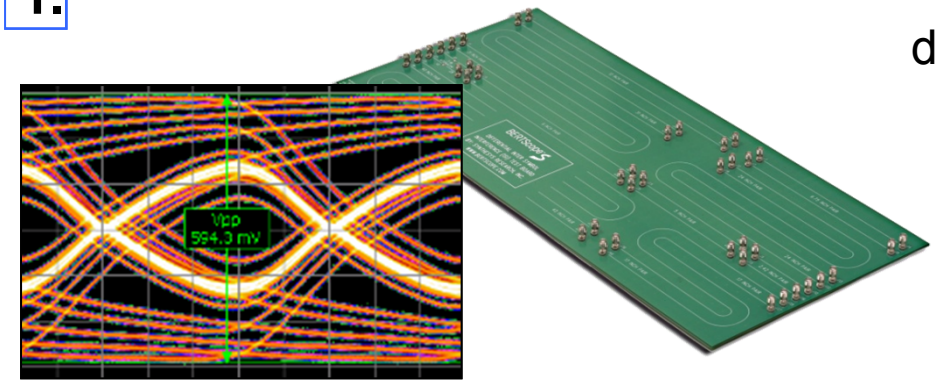
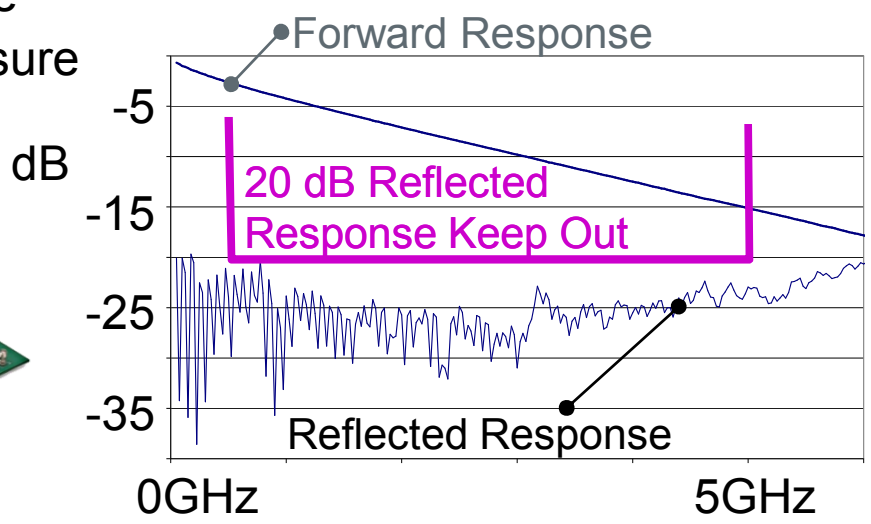
Relating to Gen2 PCIe Example
5 Gbps over variable trace lengths

BERTScope™

- The Compliance ISI channel is a 40” trace
  - Used to create 5:1 ratio of eye closure

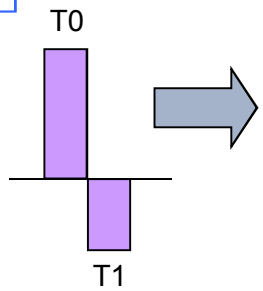
1.

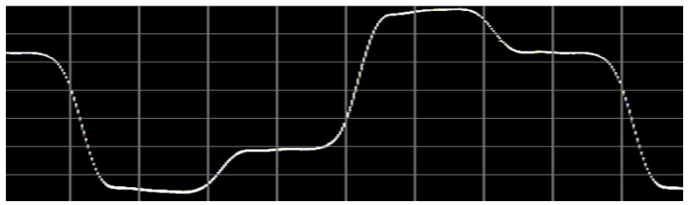


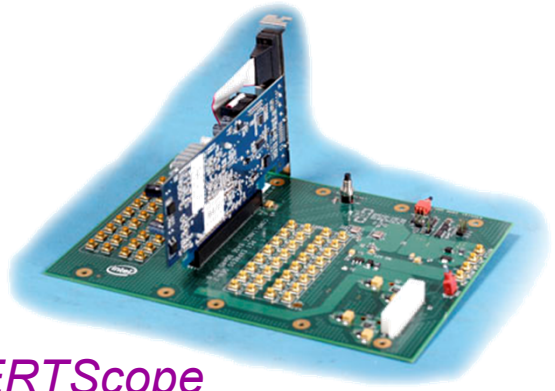


- 2-tap Pre-emphasis is used to compensate for losses

2. -3.5dB or –6dB [20*LOG(B0/B1)]







Measured Single Valued Waveform on BERTScope

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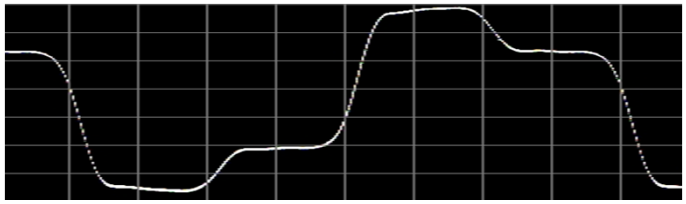
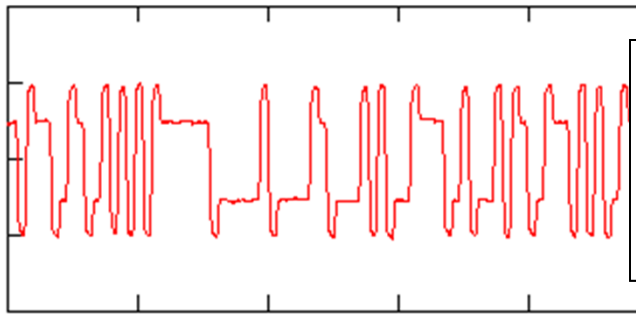
PCIe Eye Diagram

2-Tap –6dB Pre-emphasis



1.

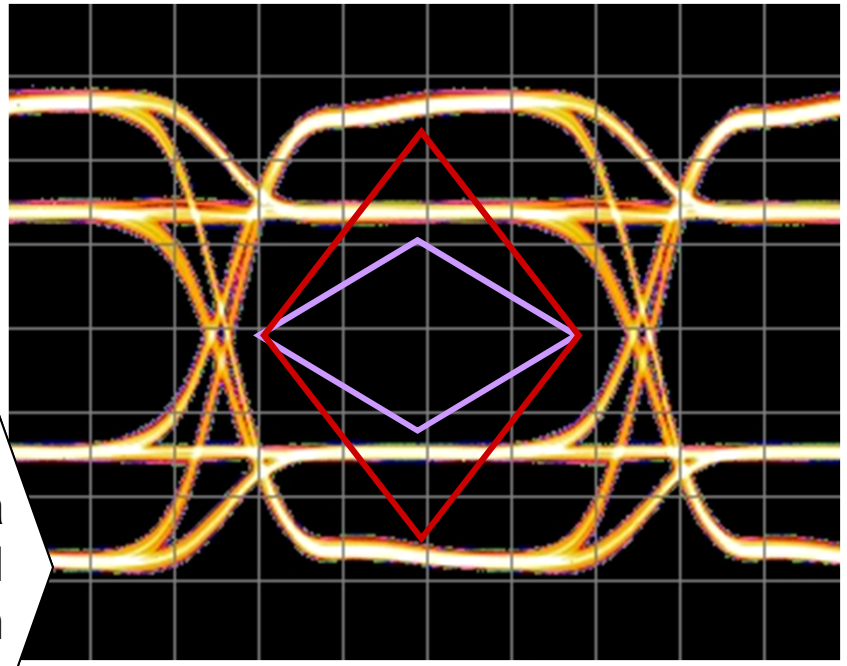
Applied to PRBS Data



2.

Causes a Multi-level Eye Diagram

3. Measurement of Eye Mask Testing On BERTScope



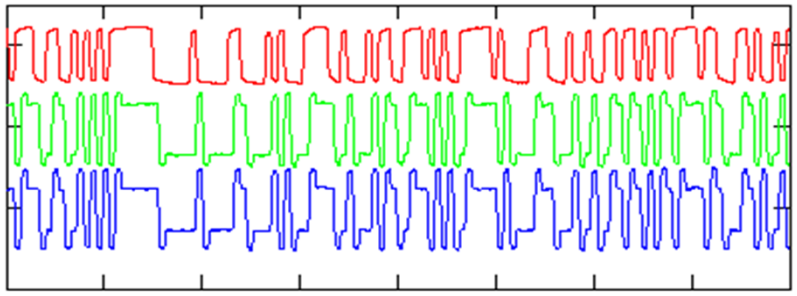
This complicates Tx mask testing - 2 masks are needed

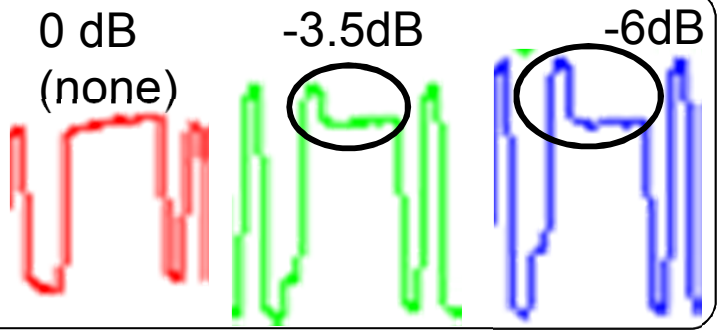
Impact of 2-tap Pre-Emphasis on PCIe Compliance Channel – Frequency Domain

BERTScope™

PRBS Time-Domain Response

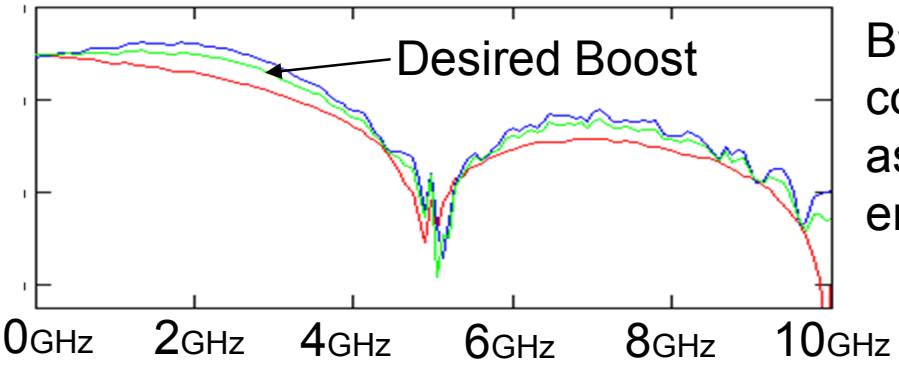
1.





Freq. Content

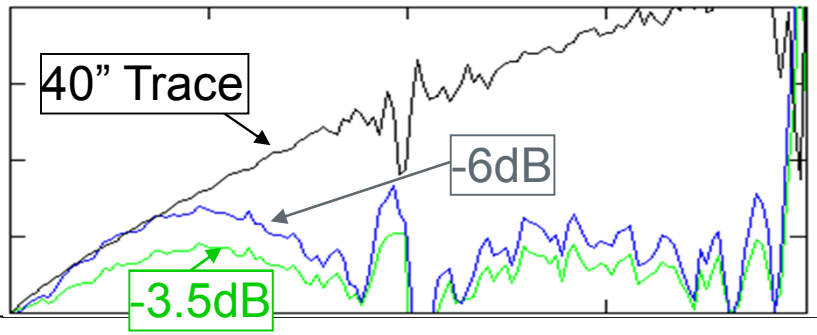
2.



By taking ratios of frequency content of pre-emphasized data as compared to non-pre-emphasized data…

Pre-Emphasis Gain

3.



…we can see what frequency boost is accomplished and compare that to the inverse of the measured trace loss.
-6dB is required for this 40” trace

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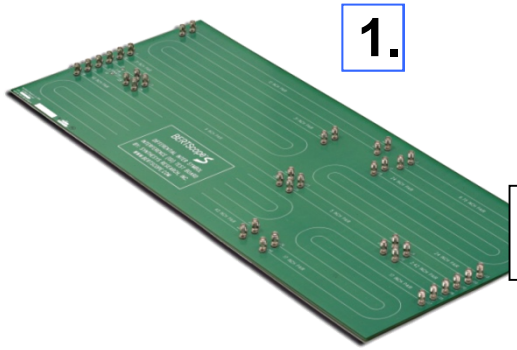
Impact on Pulses – Time Domain

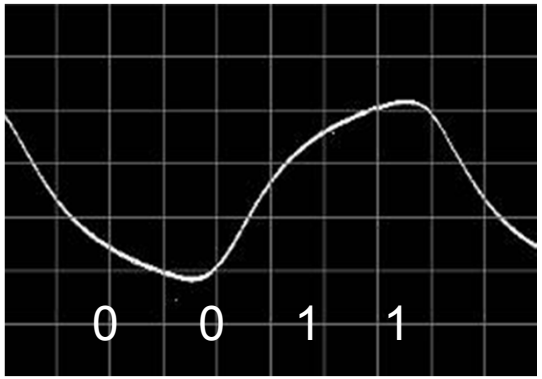
2.

By applying 6dB of Pre-Emphasis, the Channel Output at a Receiver has sharper edges and looks more like the intended pulse

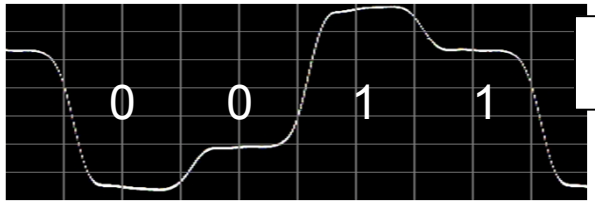
1.



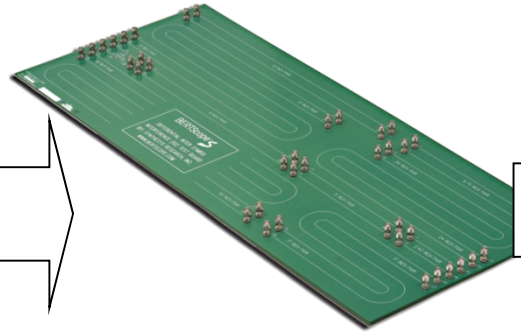
No Pre-Emphasis



3.

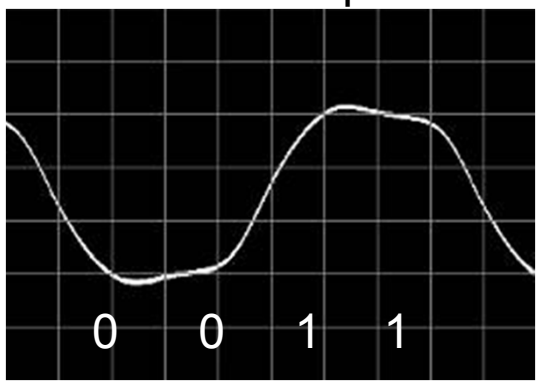


6dB Applied Pre-Emphasis



40” PCI Compliance ISI Board, 5Gbps 1100 Data

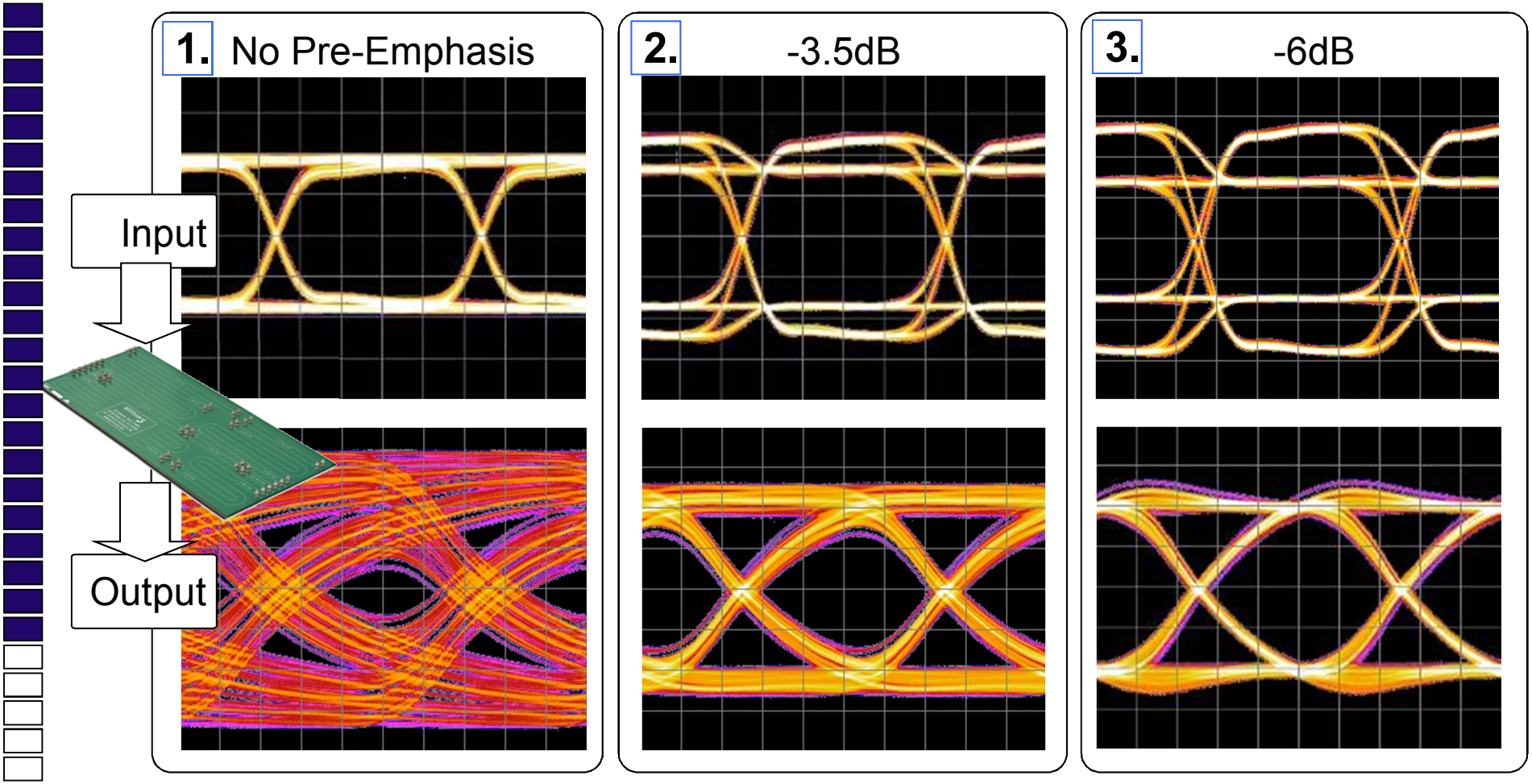
–6dB Pre-Emphasis



Measurement of Single-Valued Waveforms On BERTScope

Pre-Emphasis
Impact on Eye Diagrams

BERTScope™



Measurement of Eye Diagrams on BERTScope

40” PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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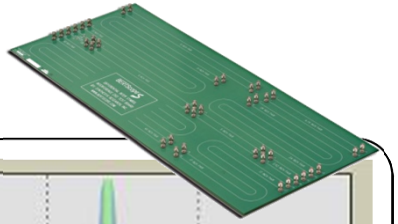
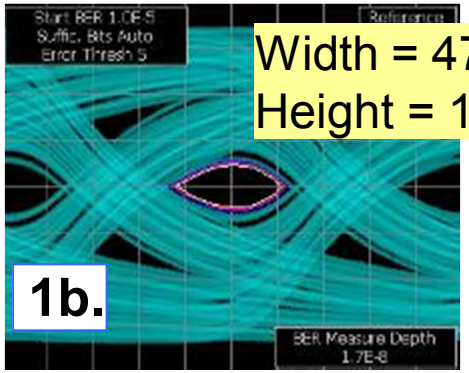
Pre-Emphasis
Impact on BER and Eye Margin

BERTScope™



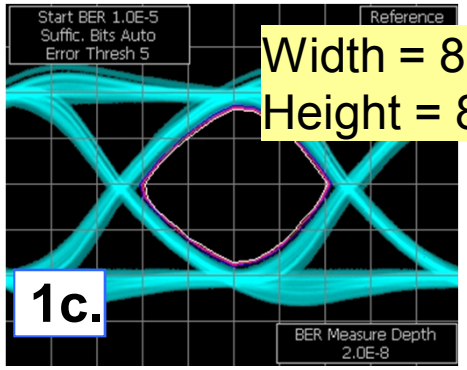
Eye Opening **1.**
(BER Contour Measurement)

Measurements on BERTScope



Width = 47%UI
Height = 18%UA

1b.

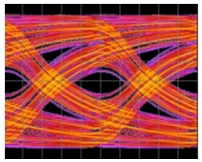


Width = 81%UI
Height = 82%UA

1c.

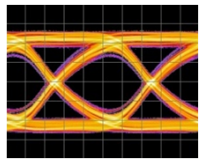
No Channel **a.**

40” Trace, no Pre-Emphasis



b.

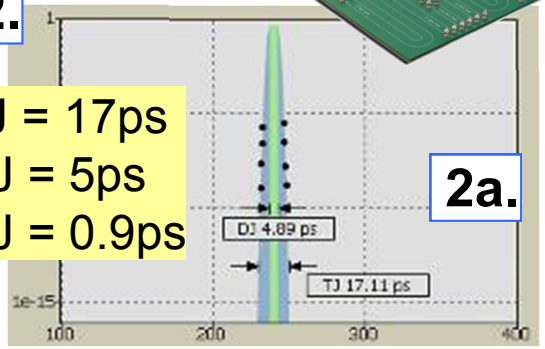
40” Trace, 6dB Pre-Emphasis



c.

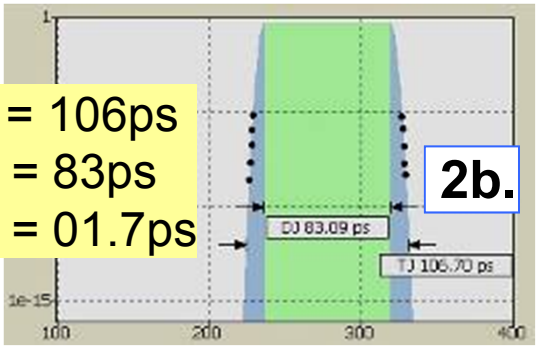
Jitter Peak **2.**
(Bathtub)

TJ = 17ps
DJ = 5ps
RJ = 0.9ps



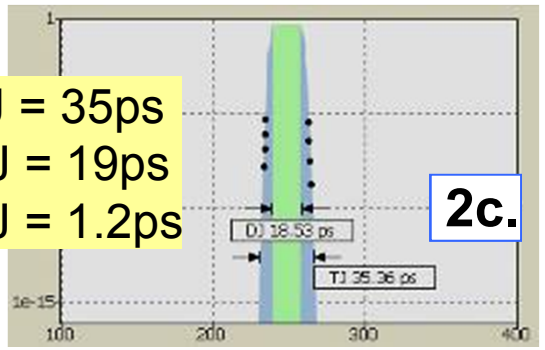
2a.

TJ = 106ps
DJ = 83ps
RJ = 01.7ps



2b.

TJ = 35ps
DJ = 19ps
RJ = 1.2ps



2c.

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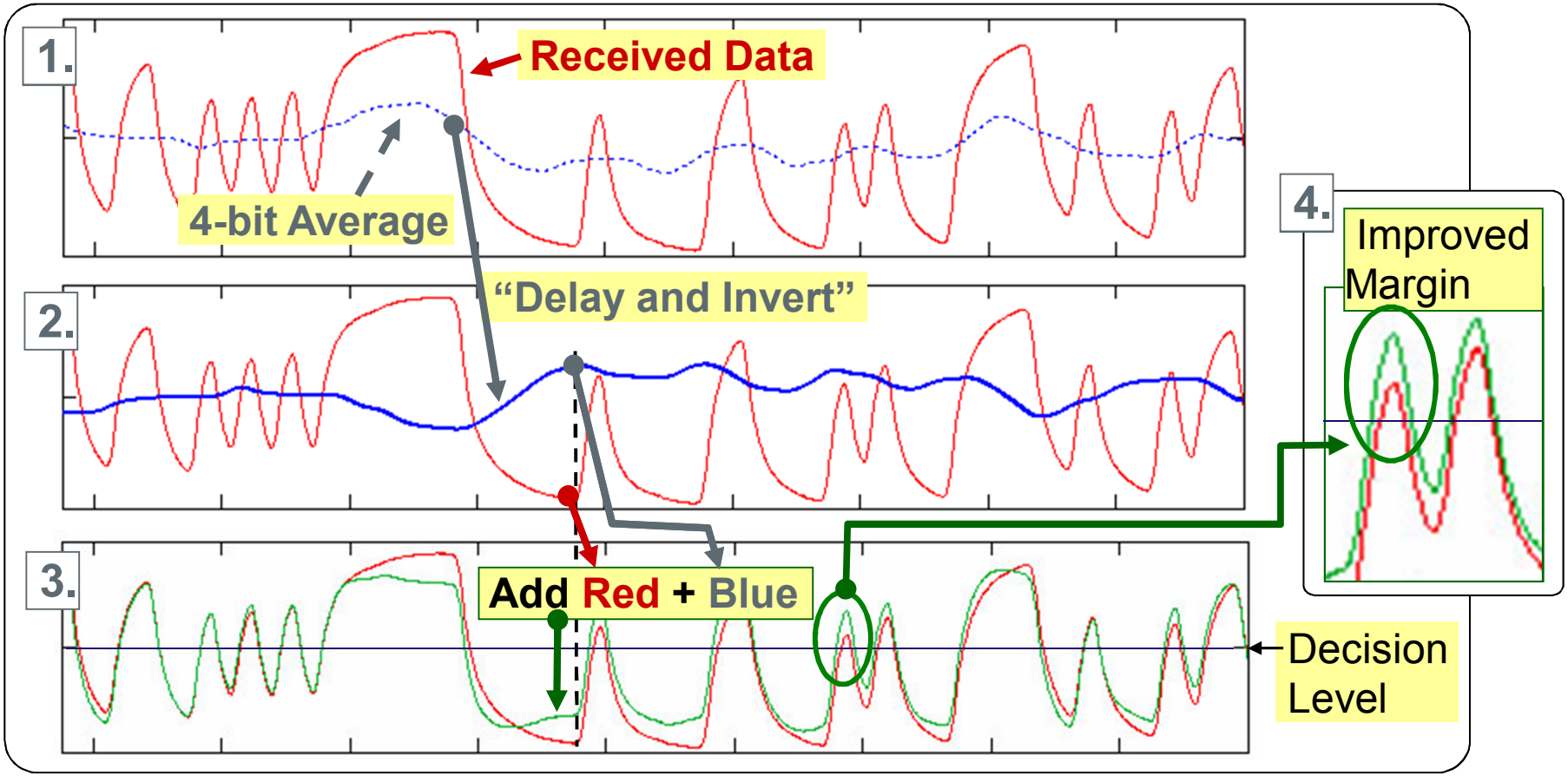
Decision Feedback Equalization
Effectively further open the eye

BERTScope™

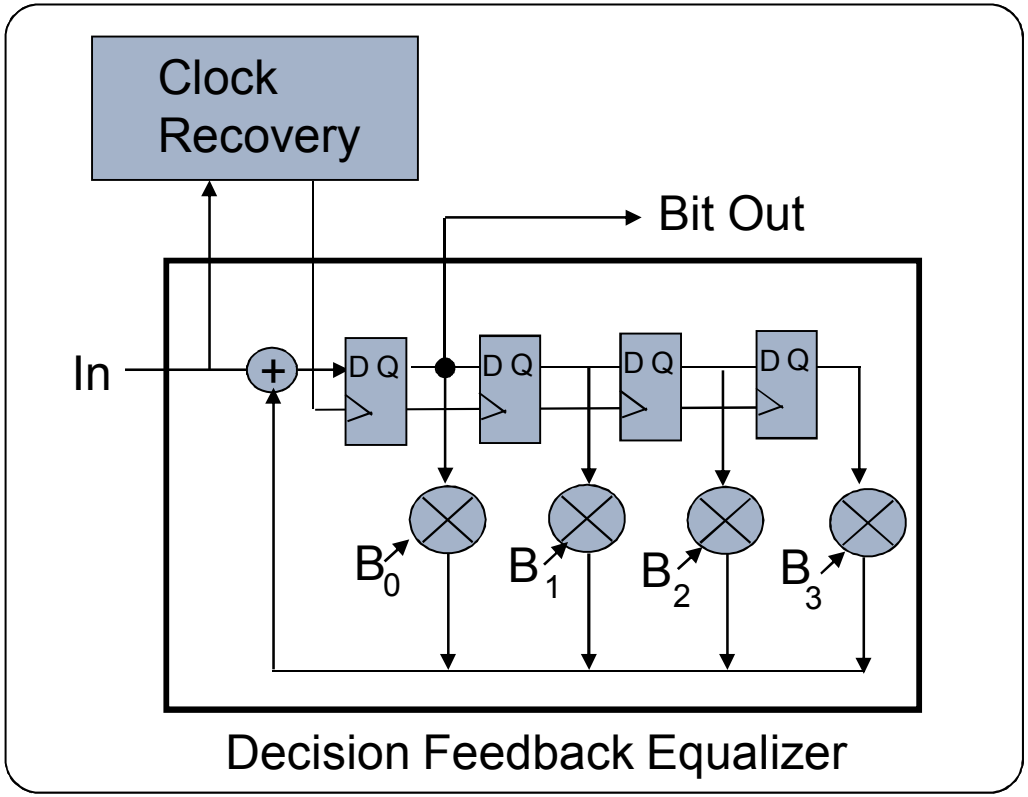
Correct baseline wander of received data stream by subtracting-off a portion of recent history



40" PCI Compliance ISI Board, 5Gbps PRBS-7 Data

Tektronix®

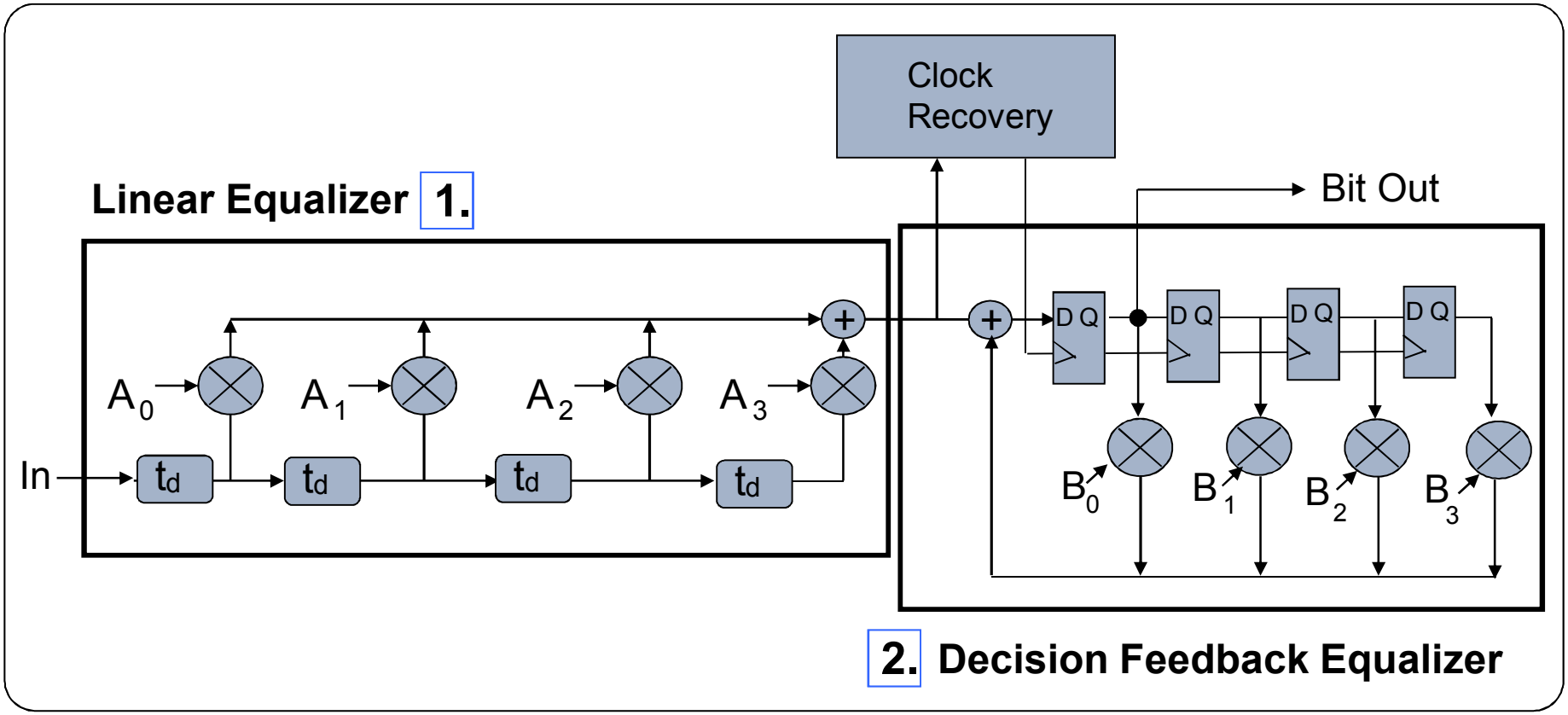
Decision Feedback Equalization
Block Diagram



- Clock recovery is required for the DFE to operate
- More or Less flip-flops can be used
  - This varies the amount of equalization

High-End Receiver-Side Equalization
Block Diagram

BERTScope™



- Implements a 4 tap linear equalizer with a 4 tap DFE

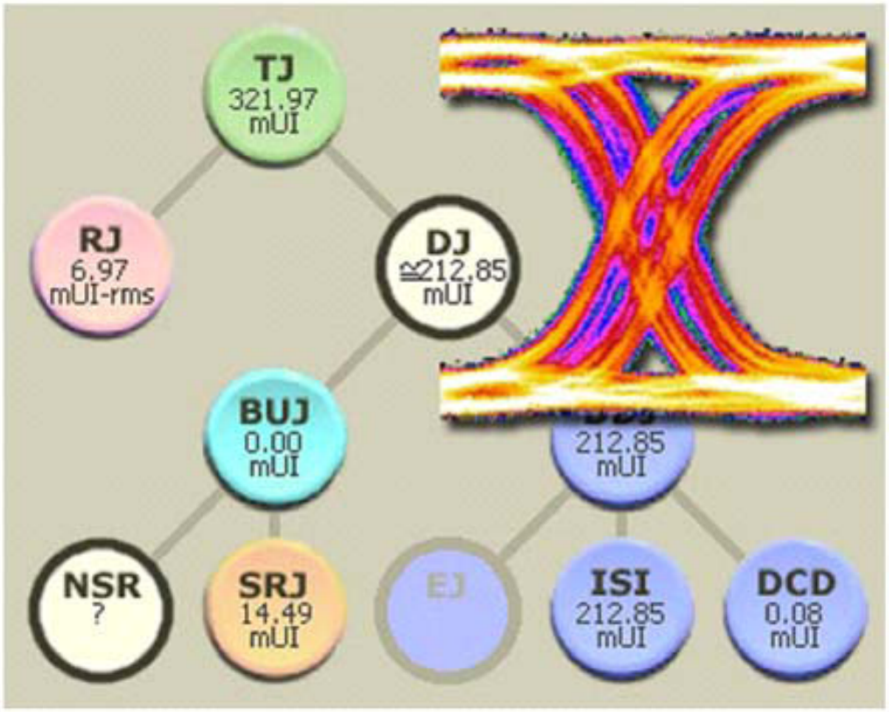
Tektronix®

Case Study:
Using BERT to Troubleshoot a Curious ISI Issue

BERTScope™

Abstract

An interesting signal integrity problem in a Gb/s circuit was successfully identified with BERTScope Jitter Map. Here we look at the issue, its cause, and explain what was going on.



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Introduction

In this customer example, the circuit of Figure 1 (a) is designed to pass data to greater than 12 Gb/s. As can be seen in (b), the eye diagram shows that as the data rate increases towards 12 Gb/s, jitter is more and more evident, rendering the circuit unfit for its intended purpose.

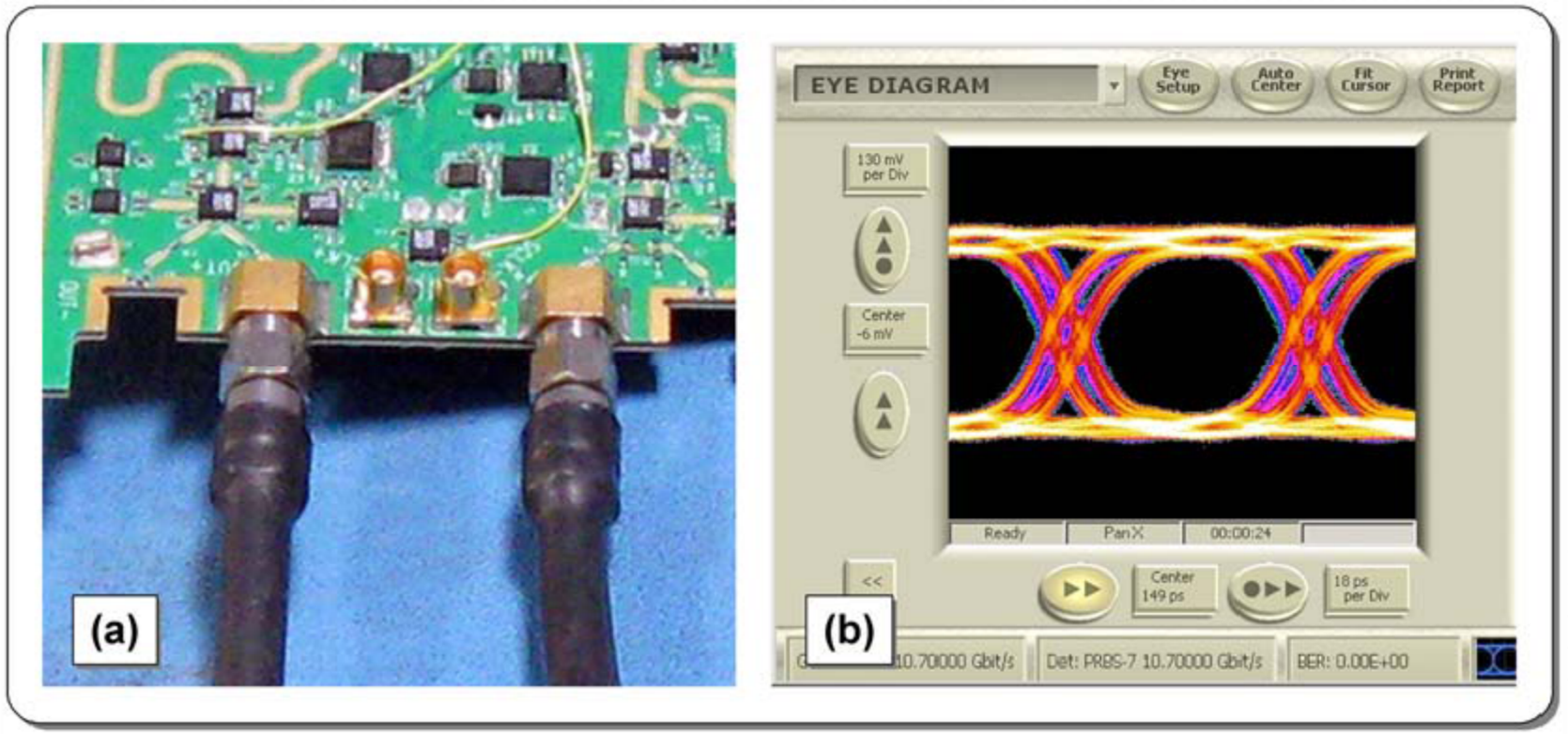

Figure 1: (a) shows the Gb/s circuit with input and output connectors. (b) is the eye diagram when 10.7 Gb/s PRBS-7 data is passed.

It is worth taking a moment to look more closely at Figure 1 (b) because it is slightly unusual. In purely qualitative terms, it is reproduced in Figure 2 (a) and compared with (b) F/2 jitter and (c) inter-symbol interference (ISI) or dispersion induced by a long circuit board channel. F/2 jitter occurs where a circuit such as a 2:1 MUX has a timing imbalance between the inputs, producing alternate bits of different lengths, irrespective of whether they are zeroes or ones. From a purely eye diagram view, the issue looks most like F/2 subrate jitter, which, given that the circuit chain contains 2:1 MUX chips, makes sense. As we will see, this is also the wrong assumption to make.

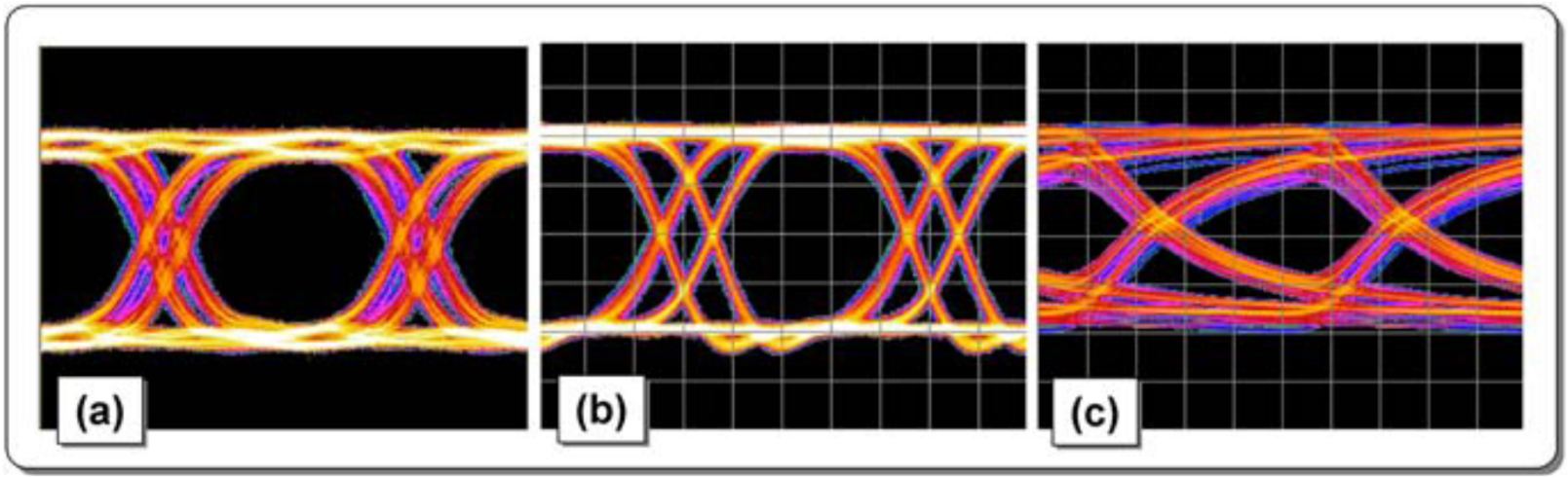

Figure 2: The eye from our DUT (a) compared with a generic eye showing F/2 jitter (b), and circuit board ISI (inter-symbol interference) (c).

Using BERT Jitter Map Function

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The picture becomes clearer as we look deeper. The eye does not look particularly noisy, and this is borne out by the BER Contour, which has closely grouped lines (Figure 3 (a)).

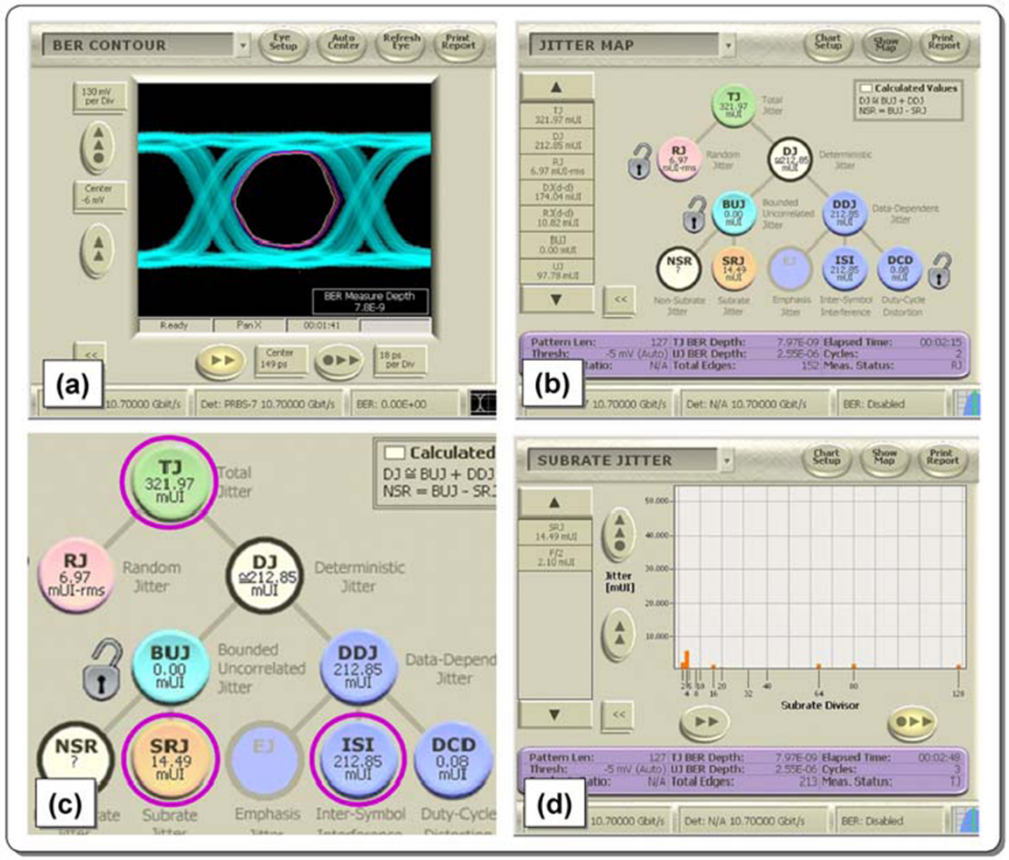

Figure 3: Looking at our device more deeply with (a) BER Contour, (b) & (c) Jitter Map main view, and the Jitter Map subrate view (d).

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Figure 3 (b) and (c) show the top level Jitter Map. Indeed, the RJ component is not a large part of the total; neither is the SRJ, or sub-rate jitter (c) & (d), so we are not facing an F/2 problem. As can be seen from (c), the biggest component of our jitter is ISI, and yet it looks different to regular circuit board ISI, having two very distinct and separate rising and falling edge paths, as shown when we look further at the ISI view (Figure 4). The graph in Figure 4 (b) distinctly shows early edges following an isolated one or zero, and late edges following several identical bits.

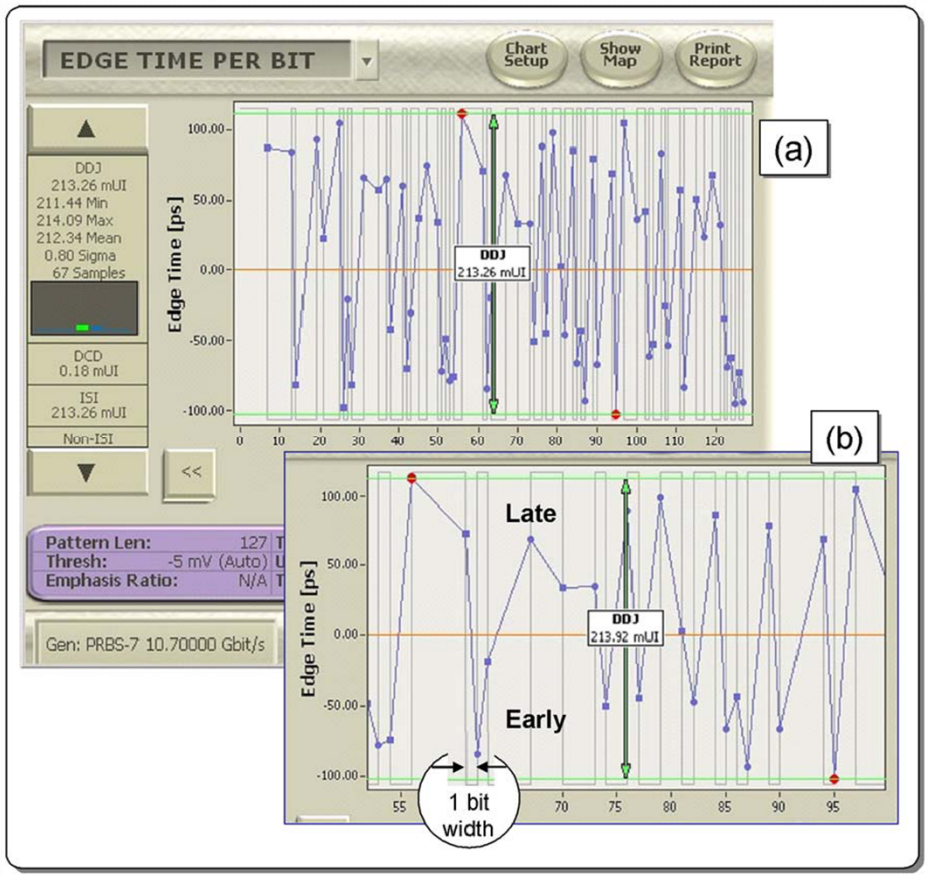


Figure 4:
ISI view showing edge timing per bit for the whole pattern (a), and zoomed in (b). The early bits all follow an isolated one or zero, whereas the late bits all follow several identical bits.

So What's Going On?

The circuit is partly composed of a series of stages such as is loosely depicted in Figure 5. The resistive splitter and the internal wire bonding of the low cost plastic package both have slight inductive issues, resulting in a mild low pass filtering effect. The effect of them together, over multiple stages, exacerbates the situation, resulting in a relatively severe overall filter response – "death by a thousand cuts."

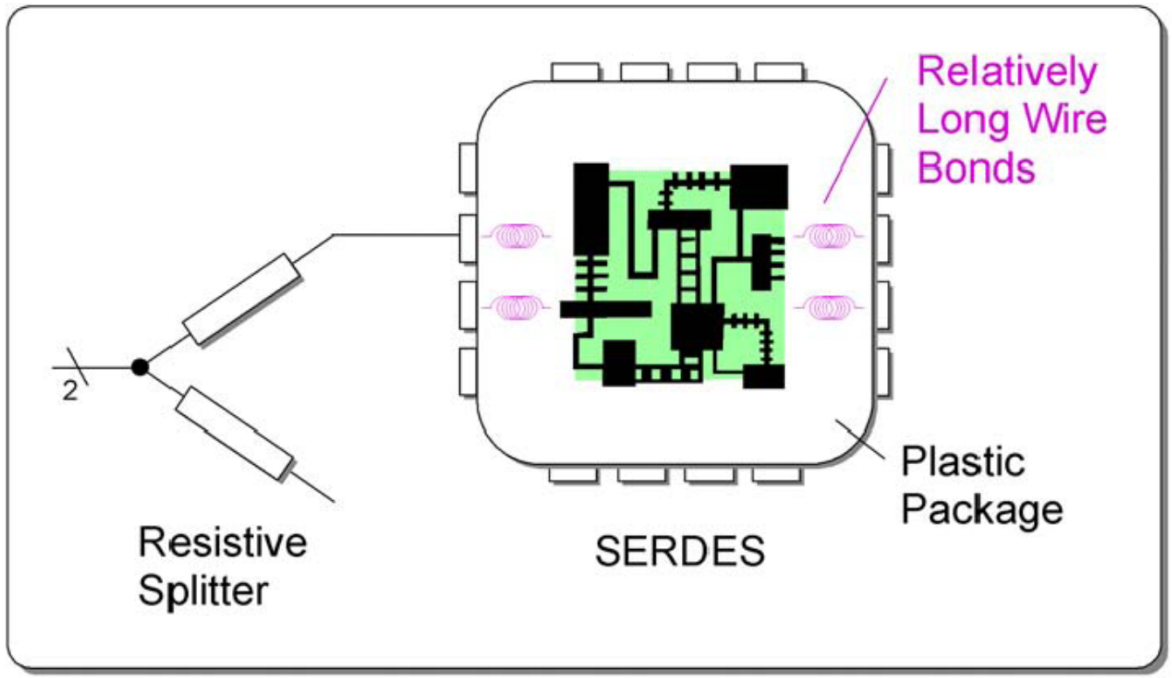


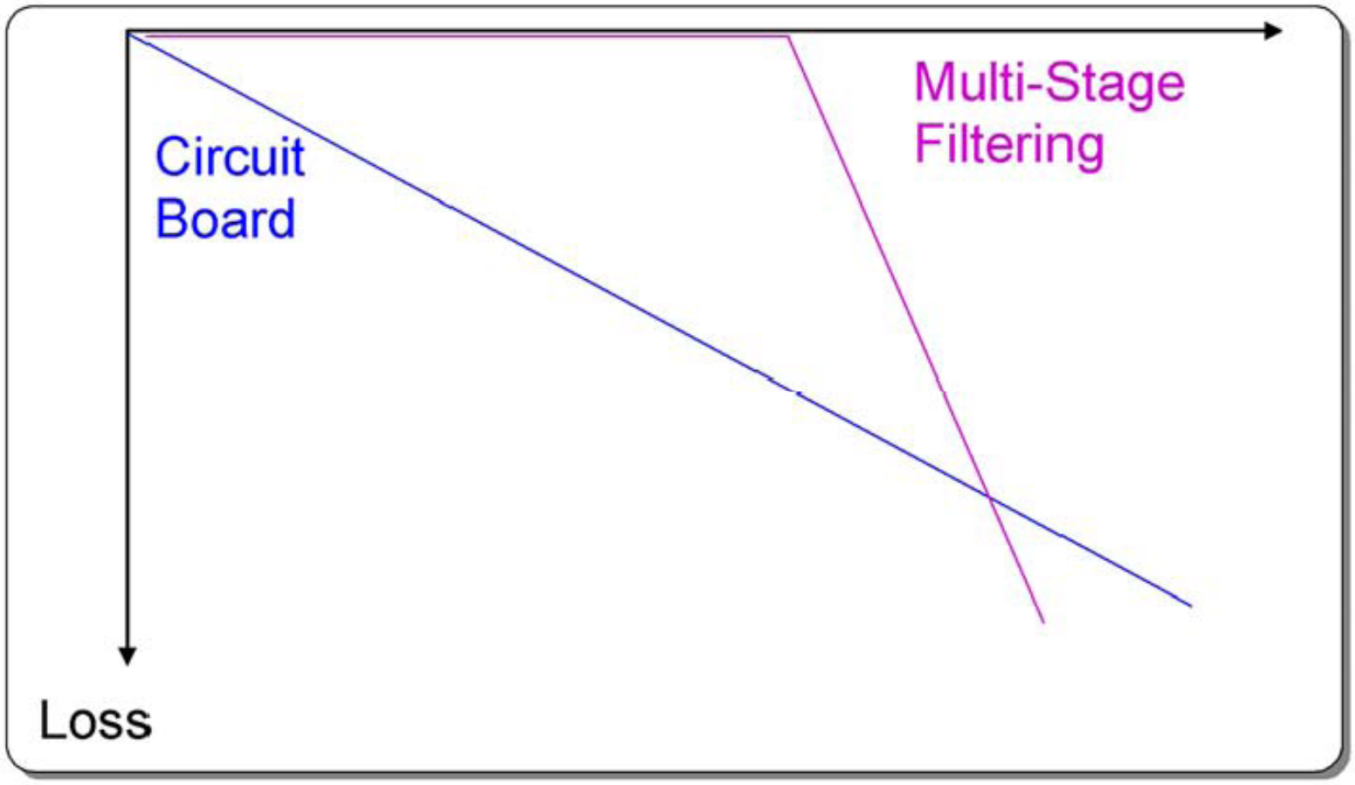
Figure 5:
One stage of the test circuit has a (differential) resistive splitter followed by a 2:1MUX.

The MUX is in a low cost plastic package that uses relatively long wire bonds internally to connect the substrate to the package pins.

ISI results from frequency response issues, frequently from bandwidth limitations of a signal path.

A common type of ISI comes from high frequency loss in circuit board material. This usually has a fairly linear slope, which essentially starts at DC, as represented in Figure 6 by the blue line.

In the case of our device under test, the loss in the individual stages sum together, forming a higher order low pass filter which starts attenuating at a higher frequency and has a steep slope, more like the purple line in the figure.



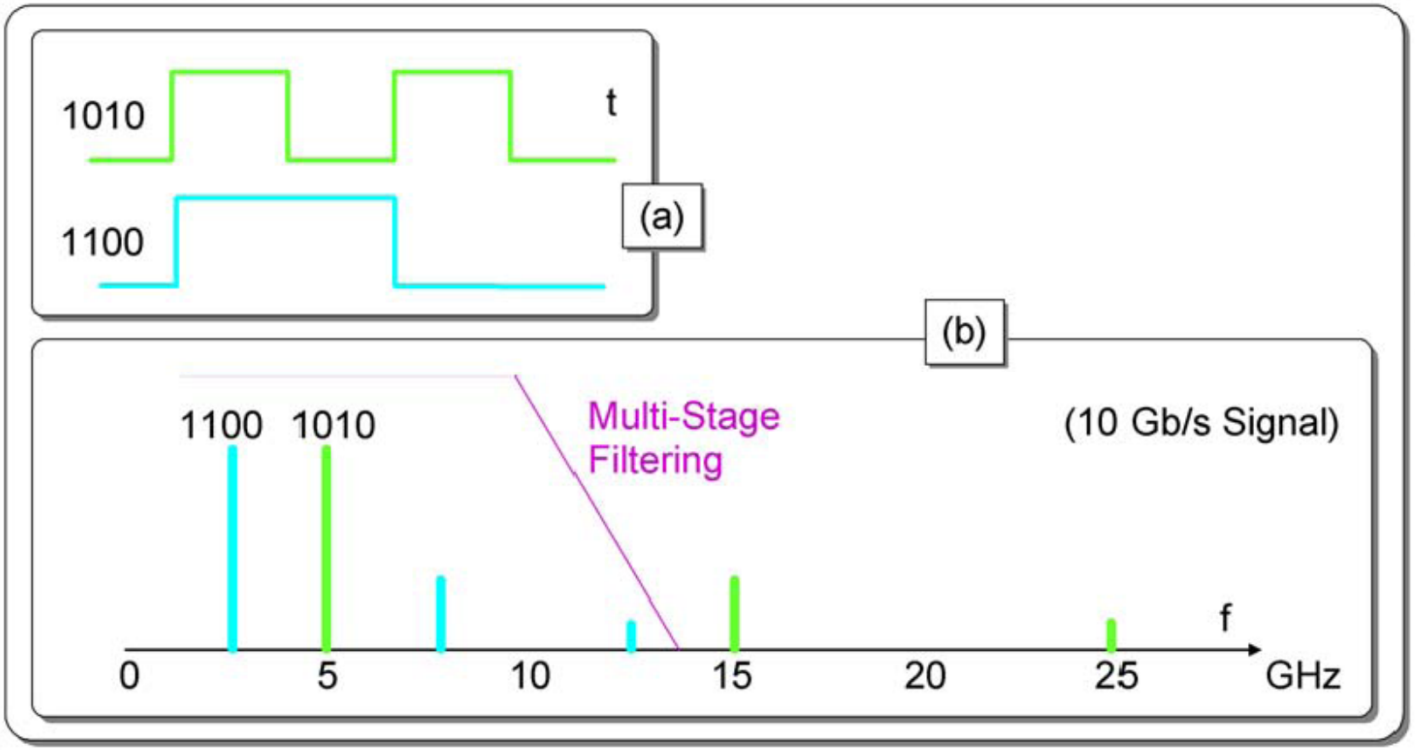


Figure 7:
Two example square wave bit sequences (a) displayed in the time domain (b) showing how the filtering might affect the harmonics of the higher frequency pattern and not any lower frequency ones.

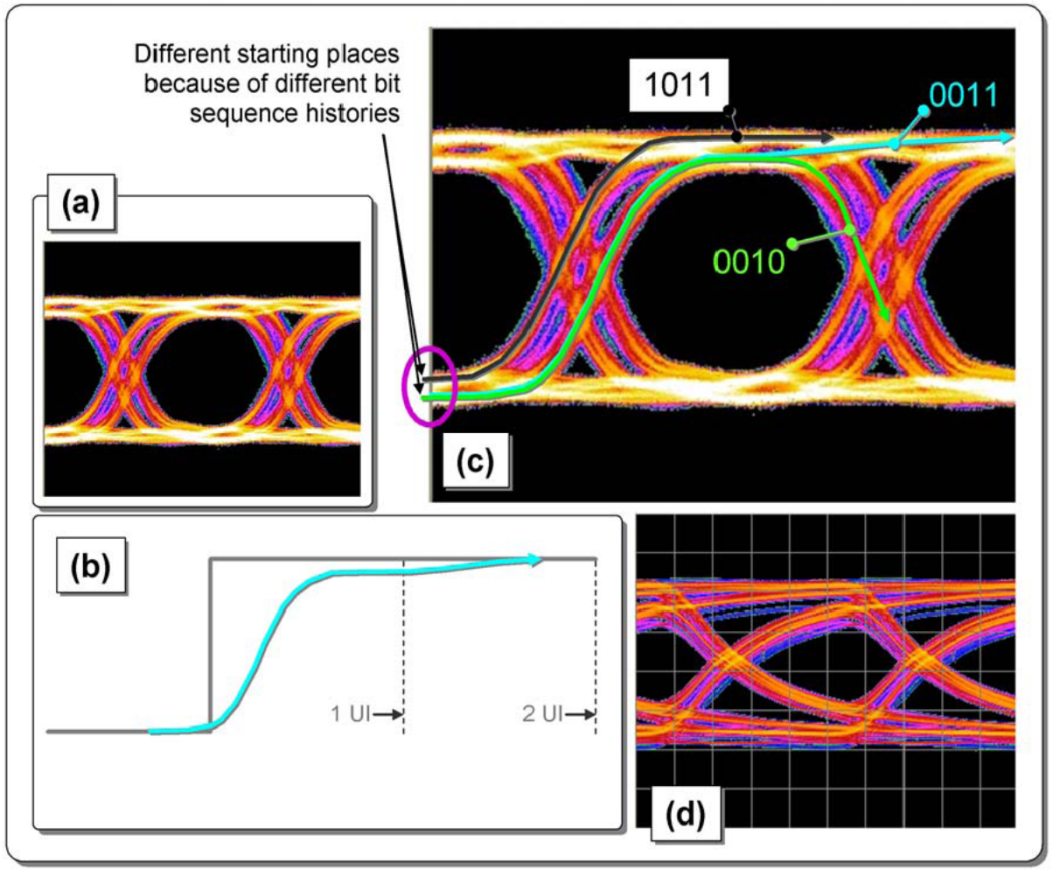


Figure 8:
For our eye in (a), a step response would look something like the blue line in (b), where the pulse doesn't reach full height until somewhere between the period for 1 and 2 UI.

This is a little like the 0011 case of (c), where the trace reaches full height by the right hand side of the eye diagram. However, if the same trace were part of a bit sequence such as 0010, then it would be diving downwards before it had reached full height.

Thus we have a situation where some sequences start downward transitions from a lower point than the others, resulting in two different edge placement times. For the circuit board ISI case, it takes many more bits before full height is reached, resulting in many starting levels for transitions.

A Quick Experimental Validation

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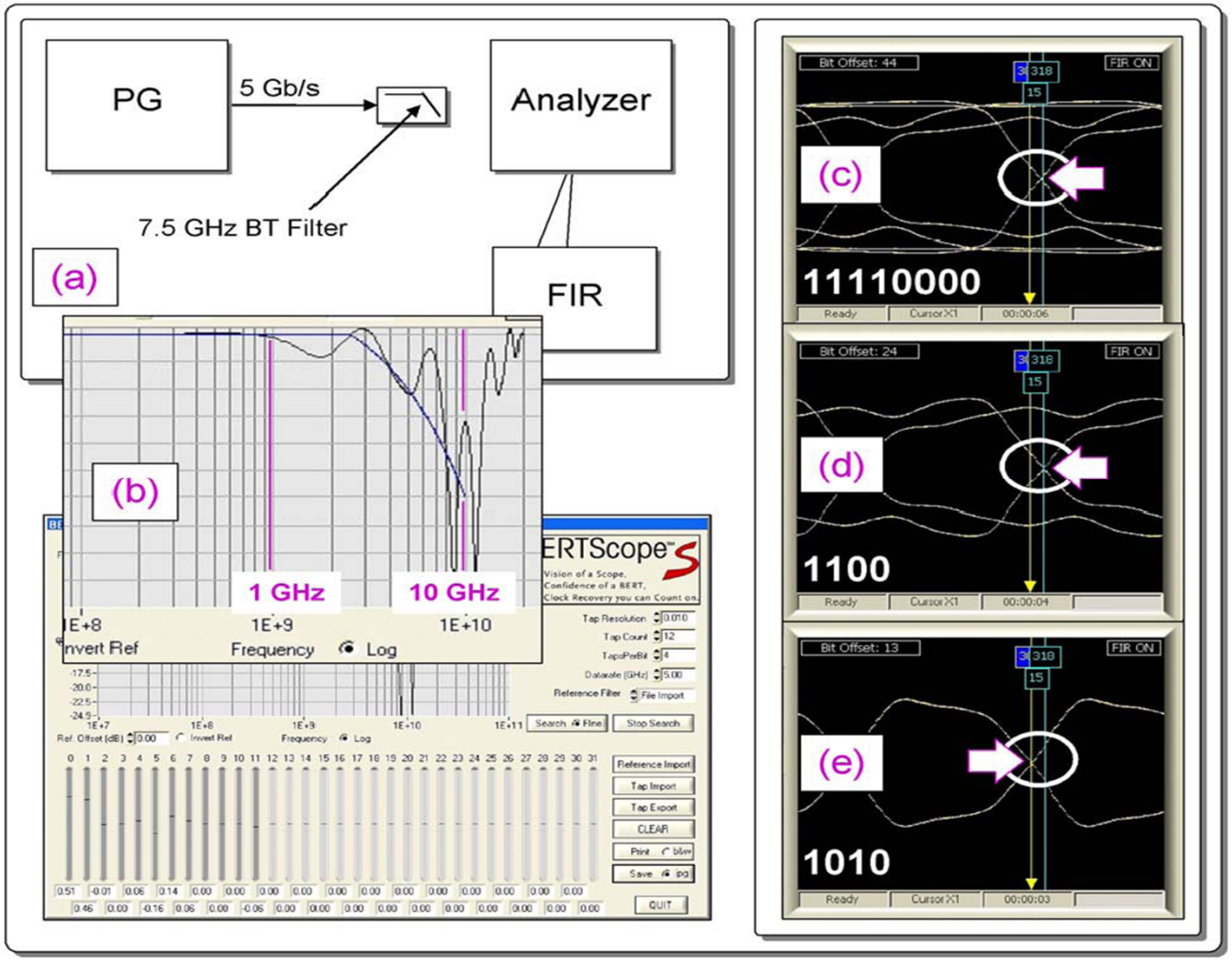

Figure 9:
A quick experiment simulating the result we saw for the device under test.
A generator (a) supplies several 5 Gb/s signals to an analyzer; the analyzer implements the response (b) black line. Three patterns are used (c), (d), (e), and two distinct edge positions are visible.

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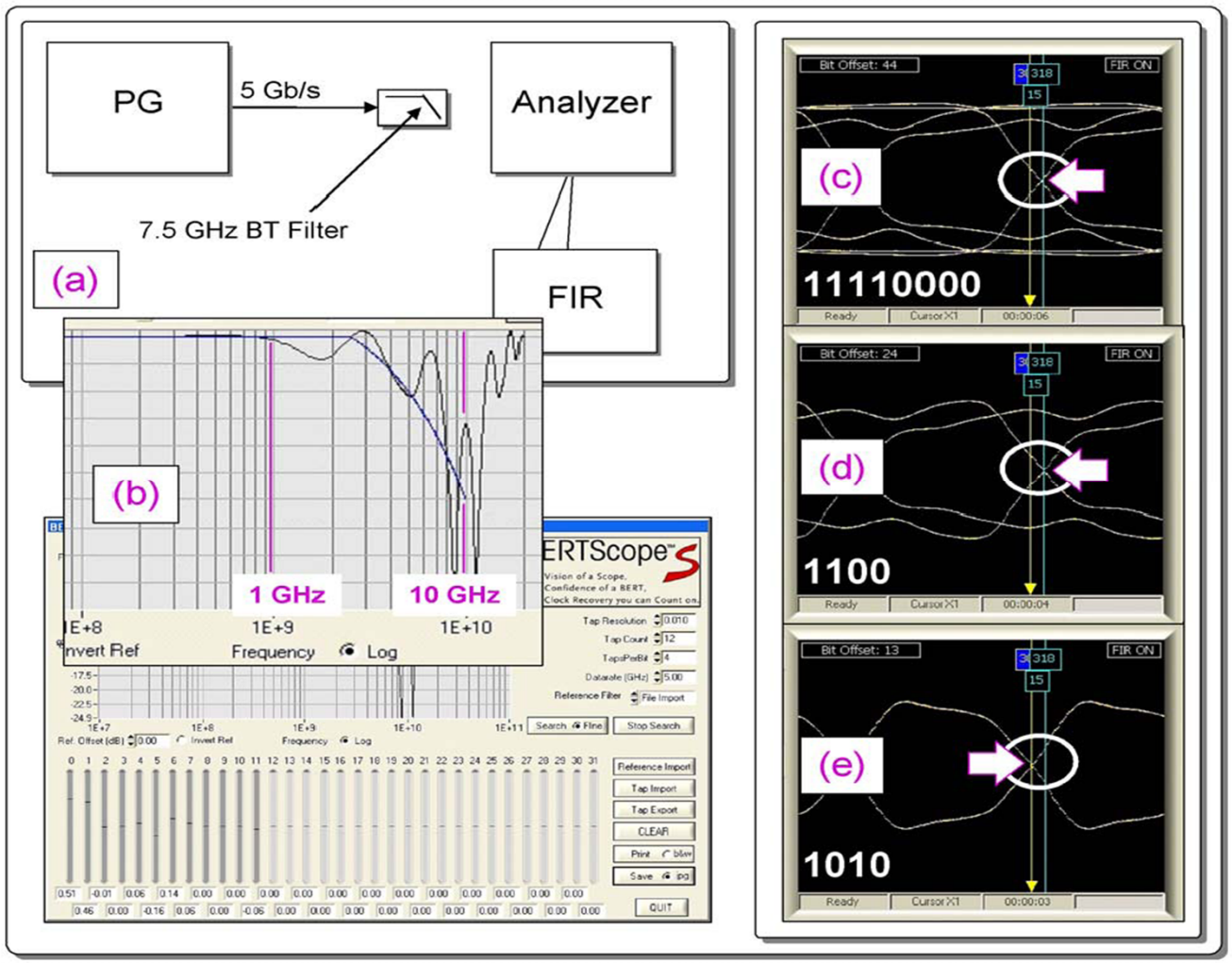


In Figure 9 (c) and (d) the edge locations are identical, and it can reasonably be expected that lower frequency patterns would do the same.

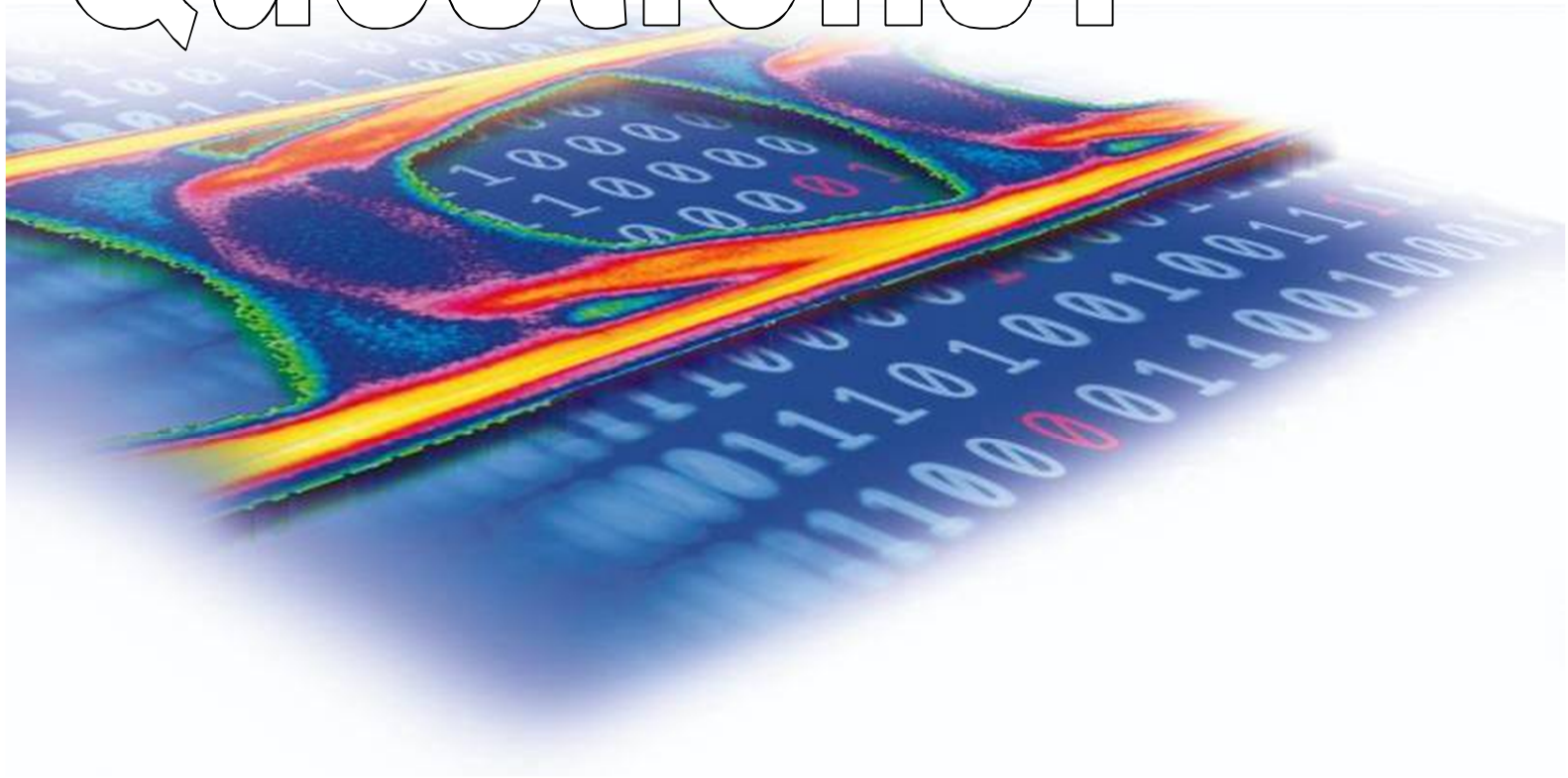
The highest frequency pattern, 1010, has an entirely different and shifted edge position, and this bears out the hypothesis that the original device under test has an ISI issue resulting from a frequency response that is flat for lower frequency components, and rolls off sharply for higher frequencies.

Summary

As we saw from the clues in Jitter Map measurements of our target device, the design suffered from ISI originating from two sources; one being the plastic packaging of the IC, which made the circuit unusable.

Jitter Map was useful in showing definitively that this was not an F/2 problem but ISI applying to the highest frequency content transitions differently than to the rest; we also used an experiment to successfully prove the type of frequency response we were facing.
Subsequent testing of the same device in a ceramic package with significantly shorter wire bonding allowed it to reach adequate performance without significant ISI being visible in the eye.

Questions?



Thank You

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