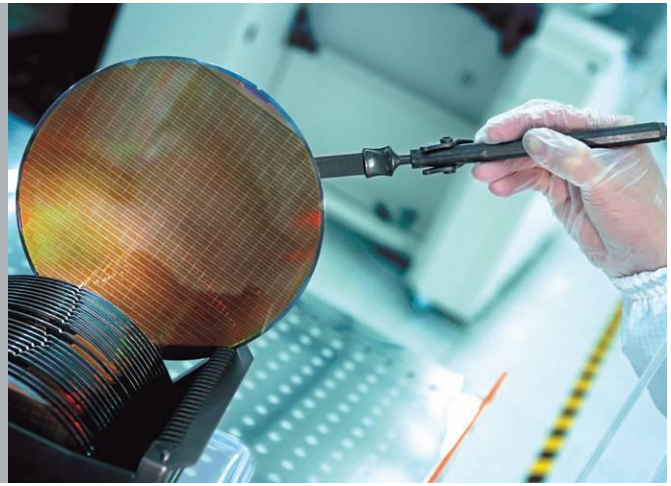
MIPI Physical Layer Test Solutions

D-PHY and M-PHY



MIPI® Solutions Team
Updated June, 2012

www.Tek.com/MIPI

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Agenda

- MIPI® Technologies & Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes:, 8b-10b, DigRF, LLI , &UniPro
  - Rx
- Summary, Q&A

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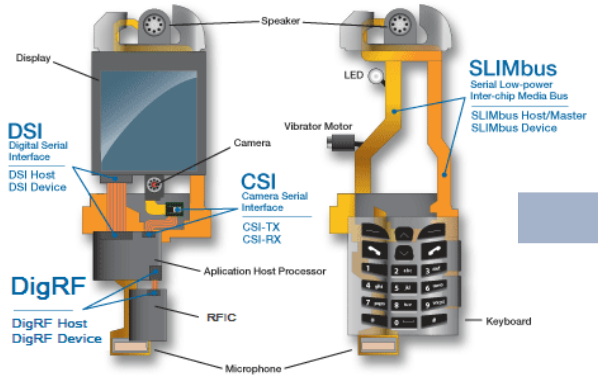
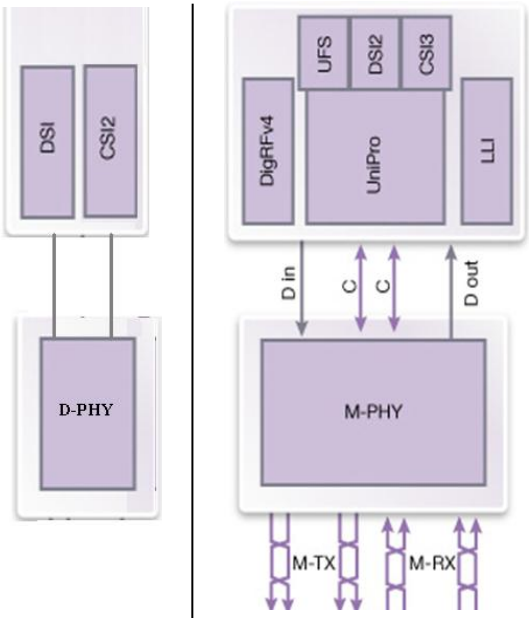
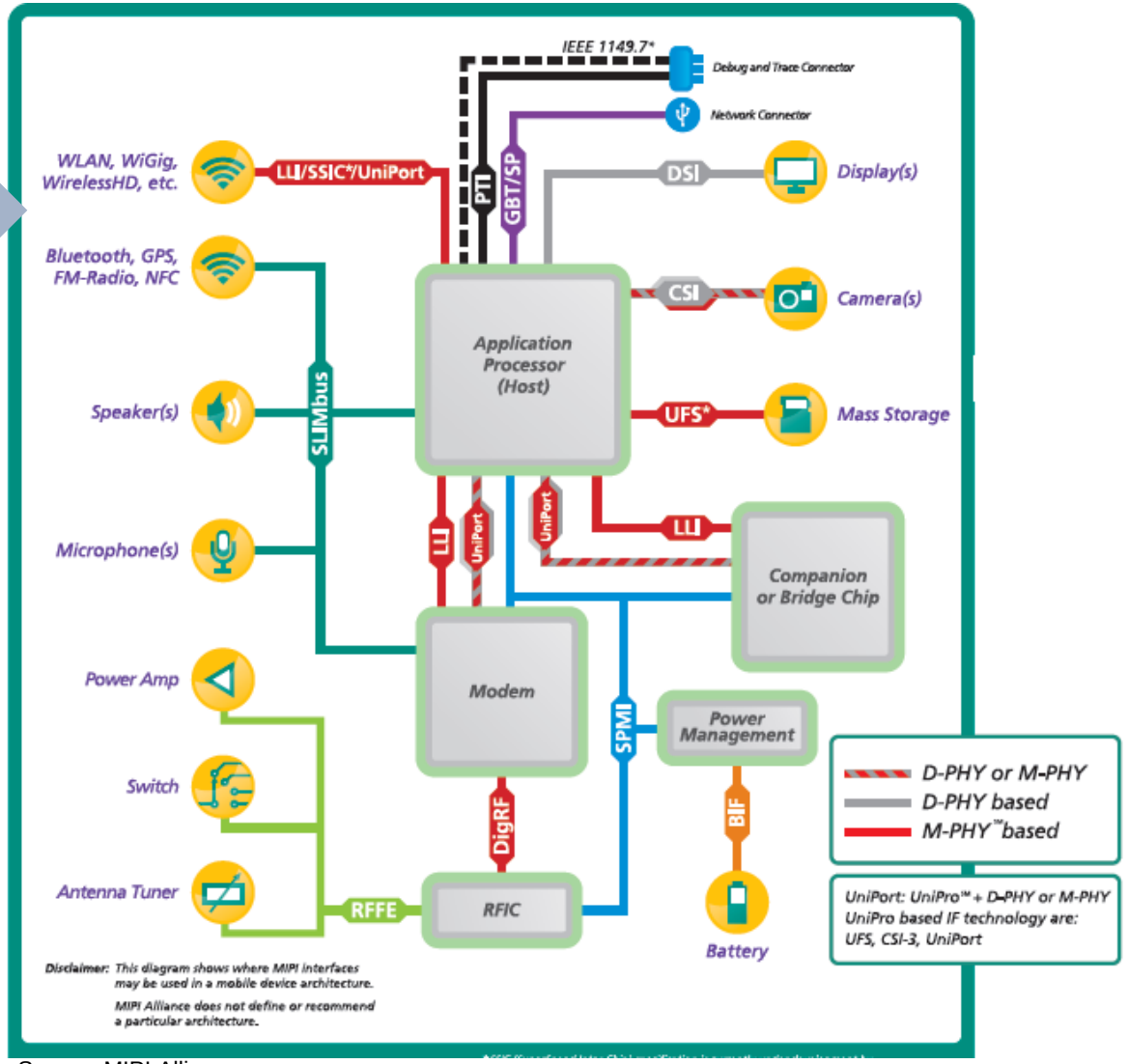
MIPI Technologies Overview
Example of a Mobile Platform







Source: MIPI Alliance

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Tek Strategic Involvement

With MIPI Alliance &UNH-IOL

- Tektronix is a ***Contributor Member*** of the MIPI Alliance
- M-PHY Tx/Rx CTS Test Document ***"Co-Authored"*** by Tektronix
- Tektronix has a close working relationship with UNH-IOL.
- ***Joint Press-Announcements*** of Tek with MIPI Alliance and UNH.
  - http://www2.tek.com/cmswpt/prdetails.lotr?ct=PR&cs=News+Release&ci=19076&lc=EN
  - "As an active MIPI contributor, Tektronix products speed the assessment of D-PHY and M-PHY performance and signal integrity. Tektronix is helping to simplify physical-layer test and validation."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2011*
  - http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6
  - "…Tektronix spurring the adoption of D-PHY and M-PHY specifications.."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2010*
  - "Tektronix has been supportive of UNH-IOL's collaborative efforts of physical layer measurement methodologies"
    - *Andy Baldman, MIPI Interop - R&D Technical Staff, UNH-IOL, Sept'2010*

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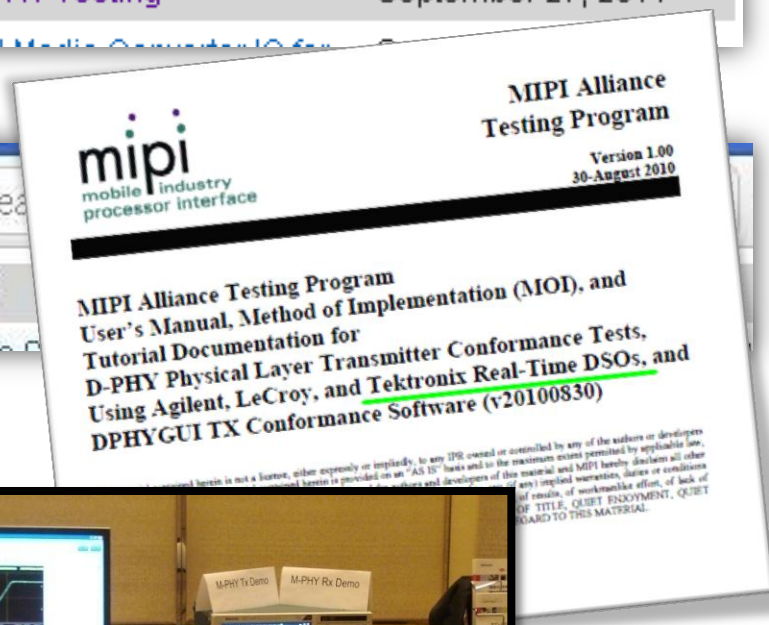
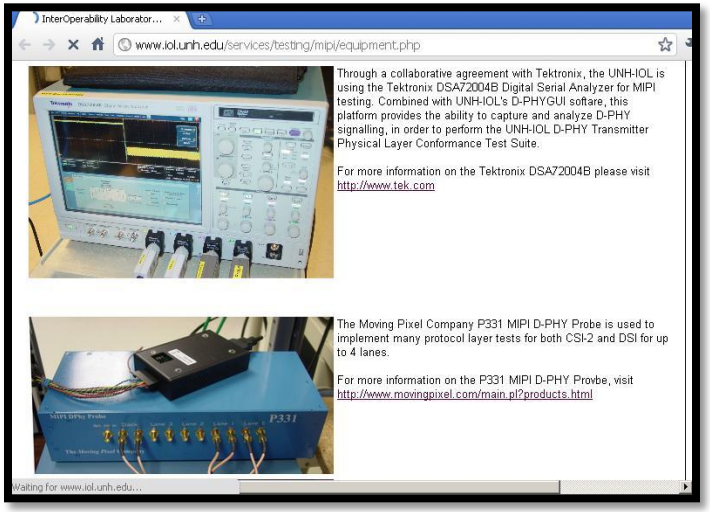
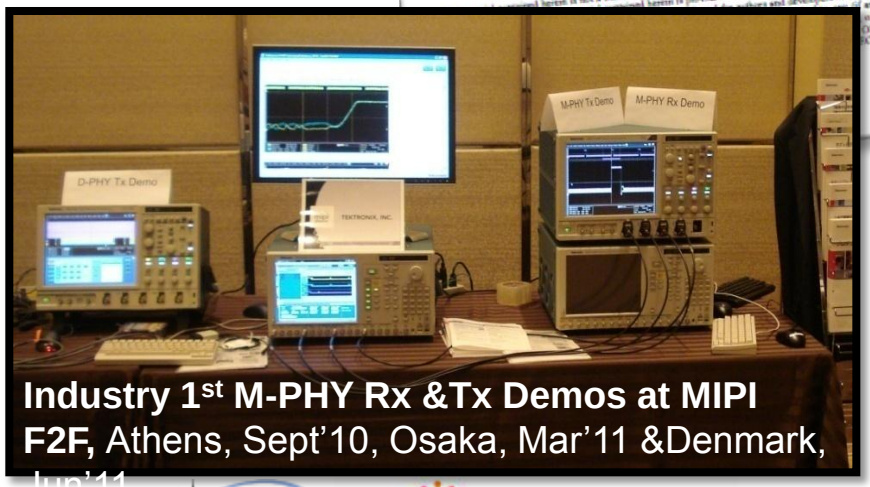
Tek Strategic Involvement

Tek Tools listed on MIPI Official Webpage, UNH Webpage &CTS Spec







Industry 1st M-PHY Rx &Tx Demos at MIPI F2F, Athens, Sept'10, Osaka, Mar'11 &Denmark, Jun'11

UNH (University of New Hampshire) is a 3rd party test house Using Tektronix setup

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Tek Strategic Involvement

Key-Customer Testimonials

- ***Joint Announcements* of Tek with ST-Ericsson, Synopsis &Mixel**
  - http://www.marketwatch.com/story/tektronix-further-strengthens-support-for-automated-mipir-m-phy-testing-2012-06-12
  - "We have been using Tektronix M-PHY test bench for over a year for M-PHY electrical characterization and analysis and to significantly speed up compliance testing. Advanced test solutions such as those available from Tektronix are critical to the emergence of a new standard like M-PHY. "
    - *Steve Kwiatkowski, HSS Test Engineer, ST-Ericsson, Grenoble, June 2012*
    - *Ahmed Bouaiss, HSS Test Project Lead, ST-Ericsson, Grenoble, June 2012*
  - http://www2.tek.com/cmswpt/prdetails.lotr?ct=PR&cs=News+Release&ci=19076&lc=EN
  - “Synopsys used the Tektronix DPO70804 and DSA8200 oscilloscopes to ensure that the silicon-proven DesignWare MIPI M-PHY met the necessary electrical characteristics and performance requirements”
    - *Hezi Saar, Product marketing manager, Synopsis, Inc. August’ 2011*
  - “MIPI testing requirements involve a large set of PHY layer checkpoints. Automating PHY testing is essential for high efficiency and predictability. We were glad to support Tektronix….”
    - *Ashraf Takla, CEO, Mixel Inc, July’ 2010*

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  - Scopes-Decode: CSI, &DSI
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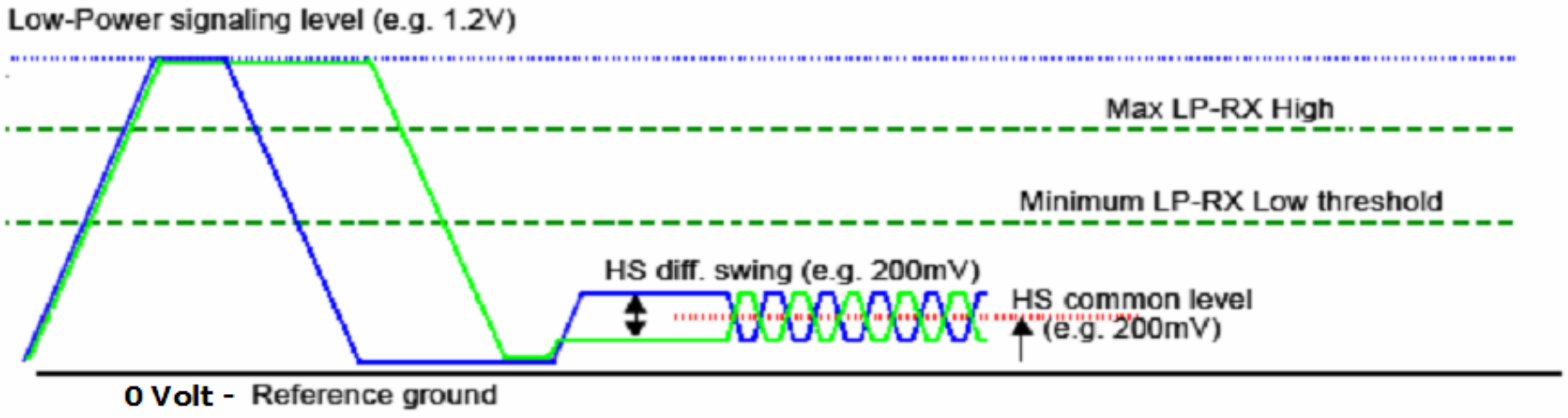
What is D-PHY ?

- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP



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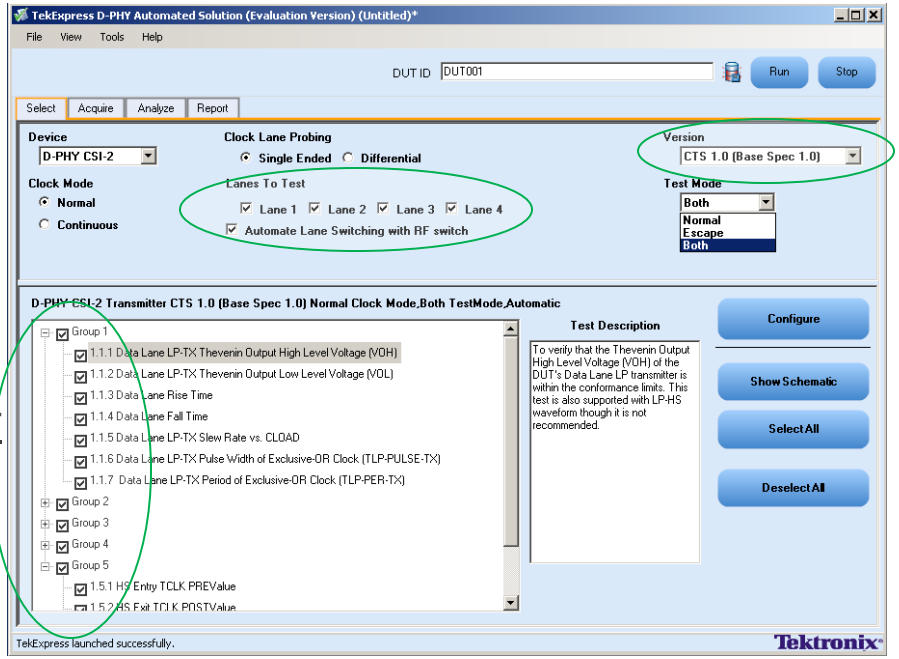
D-PHY Testing Challenges

- Logo testing is not required, but Optional.
  - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, similar to a DDR bus.
  - Mobile Phones do not need compliance logo, unlike USB/SATA devices
- No two MIPI devices are the same
  - Variable Data Rates
  - Up to 4 lanes of Data traffic,
  - Multiple different data formats
  - Specification enables custom limits.
- Characterization is significantly important
  - Mobile OEMs select the suppliers based on characterization reports.
- Several measurements (Total 49) to be performed.
  - Clock Lane
  - Data Lane
  - Clock-Data Timing

D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Runs on 7K/C and 70K/B/C/D scopes
  - Opt.TEKEXP is Pre-Requisite



- Differentiation
  - **Un-parallel** Automation (Auto-Cursors)
  - **100%** Widest Test Coverage
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.0)
- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & ”Zoom-in” Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready

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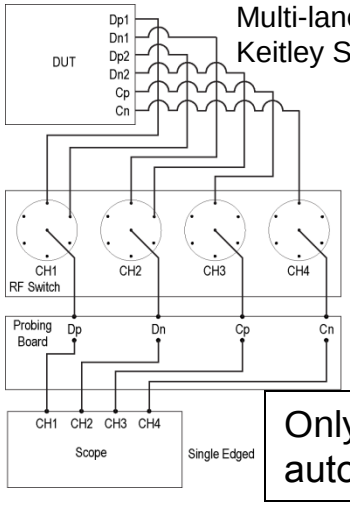
D-PHY Tx : Opt.D-PHYTX Features

Feature	Benefit
Unparallel-Automated Testing	• Performs Single-button Fully-Automated testing. • "Automatically" Identifies the testing region for each test using auto-cursors, and does not require operator intervention. • Minimizes your testing time and resources.
Widest Tests Coverage	• 100% Coverage • 49 out of 49 total CTS tests
Fully-Automated Multilane Testing	• Enables Single-button execution for "multi-lane" DUTs, using any external RF switch (Recommended Keithley S46-6666A switch: www.keithley.com/products/switch/rfmicrowave/?mn=S46) • Provide single-printable report for all tests and all lanes together, tabulated lane-by-lane.
Fully-Automated TemperatureChamber	• Validate All High Speed tests using differential probes, Socket XL cables, High-Temperature Tips and Standard Filter Files.
Characterization/ Margin Testing	• Unit Intervals automatically calculated based on the DUT datarates • Allows to perform ULPS &Normal Mode tests • Allows custom-limits or limits-editing to perform Margin testing. • Allows selective tests run in Clock Continuous mode
Test-Reports	• Provides "Zoon-In" screenshots of cursors for each test

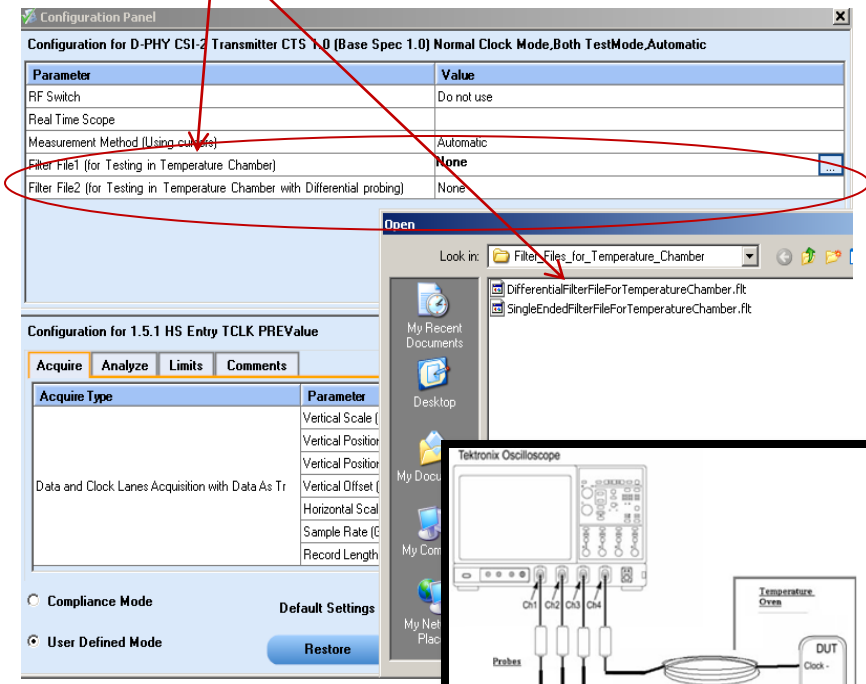
D-PHY Tx : Opt.D-PHYTX Features

Provision to Load Filter-files for Temperature Chamber or Channel De-embedding

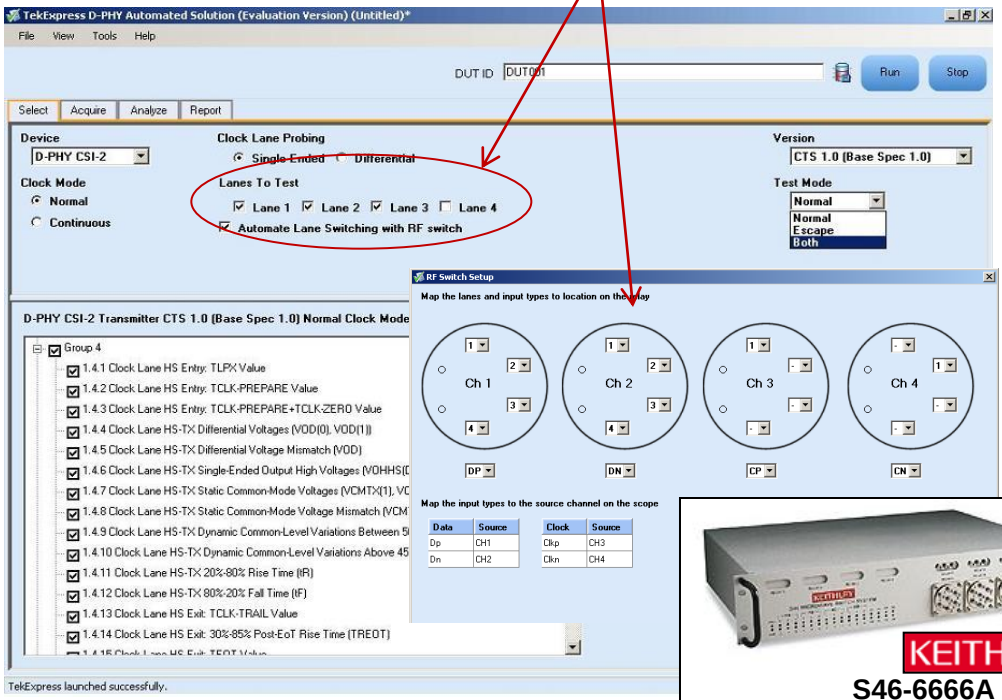


Multi-lane Automation Setup using Keitley S46-6666A/ any RF Switch

Only solution for Single-button automation of “multi-lane” DUTs.

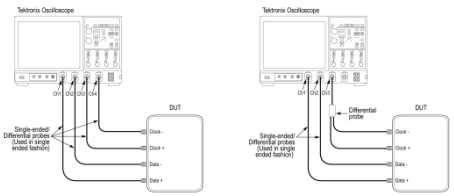


Socket Cable XL (020-2900-00 with High Temperature Tips (020-2958-00) or other on P73xx



S46-6666A Switch

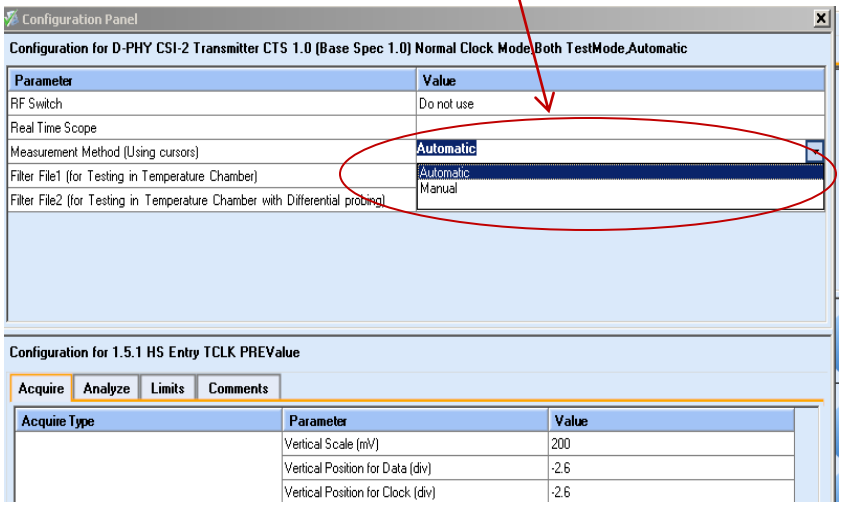
D-PHY Tx : Opt.D-PHYTX Features



Single-Lane Automation Setup using SE/Diff probes

Test Reports with “ZOOM-IN” screenshots of the cursors placement for each test.

Switch between Automatic and Manual cursor palcement. In Automatic mode, software can find the LP/HS regions automatically. Switch to Manual for debug or if your signal is too noisy.



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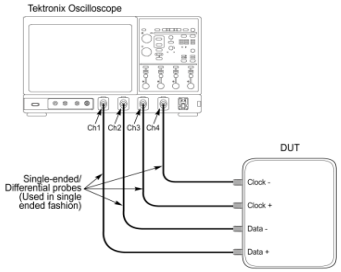
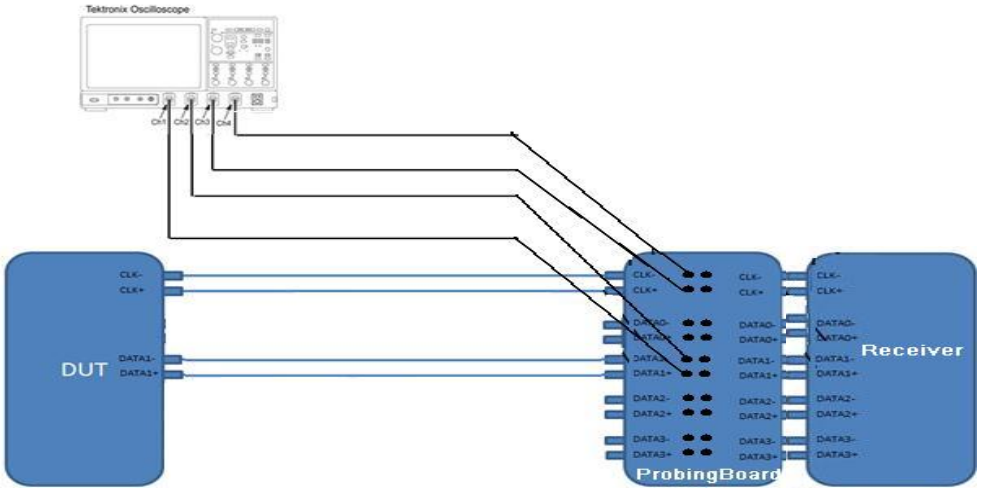
D-PHY Tx : D-PHY DUT Scenarios
Use Cases/ Test Setup Examples – 1 (Live-Setups)

- Use-Case: Single-lane **Live-Setup** (i.e Tx-Rx ends connected), and **DUT has no SMA i/f**.
- Test Setup: “No Termination Board” Required. No Probing board Required. Use Solder-In/ Square-Pins directly to connect at the PINs of the DUT.



- Use-Case: Single-lane **Live-Setup** (ie.Tx-Rx ends connected), and **DUT has Only SMA i/f.**
- Test Setup: “No Termination Board” Required, But a Probing-Board Required for SMA i/f.



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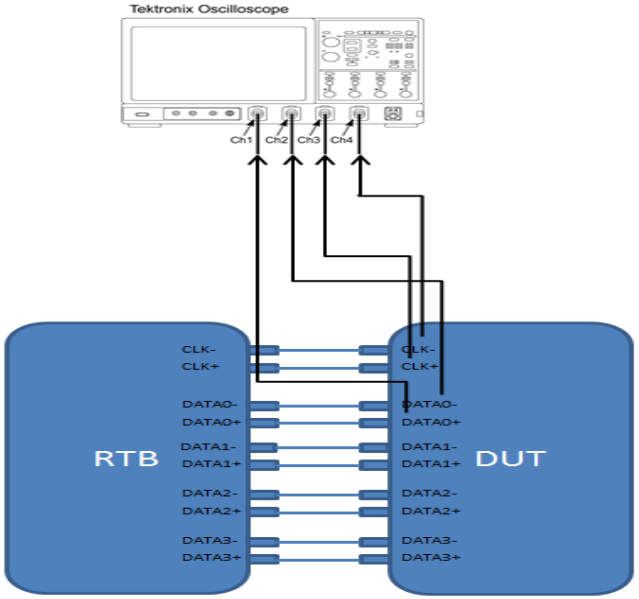
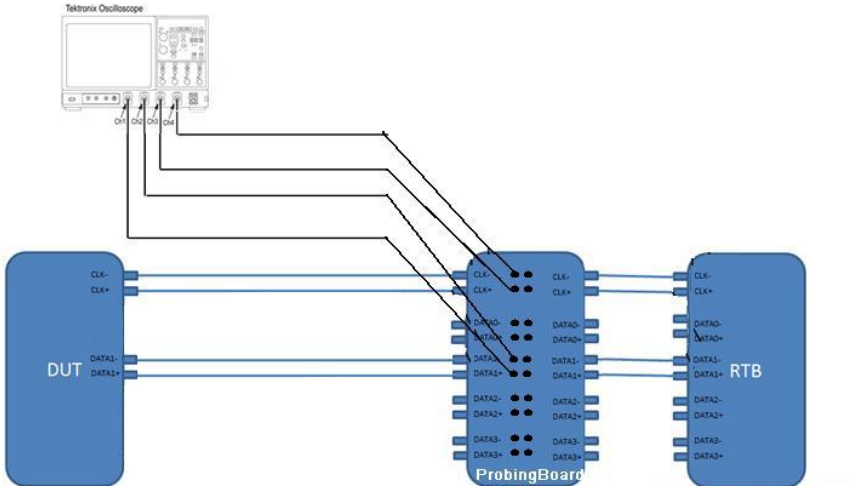
D-PHY Tx : D-PHY DUT Scenarios
Use Cases/ Test Setup Examples – 2 (Non-live Setups)

- Use-Case: Single-lane **Non-Live-Setup** with Stand-alone DUTs, and **DUT has no SMA i/f.**
- Test Setup: “Termination Board” Required. Use Solder-In/ Square-Pins directly to connect Test Setup: “No Termination Board” Required. Use Solder-In/ Square-Pins directly to connect. Cables between RTB and DUT must be shortest matched pair as possible.



- Use-Case: Single-lane **Non-Live-Setup** with Stand-alone DUTs, and **DUT has Only SMA i/f.**
- Test Setup: “Termination Board” Required. And, a Probing-Board Required for SMA i/f..



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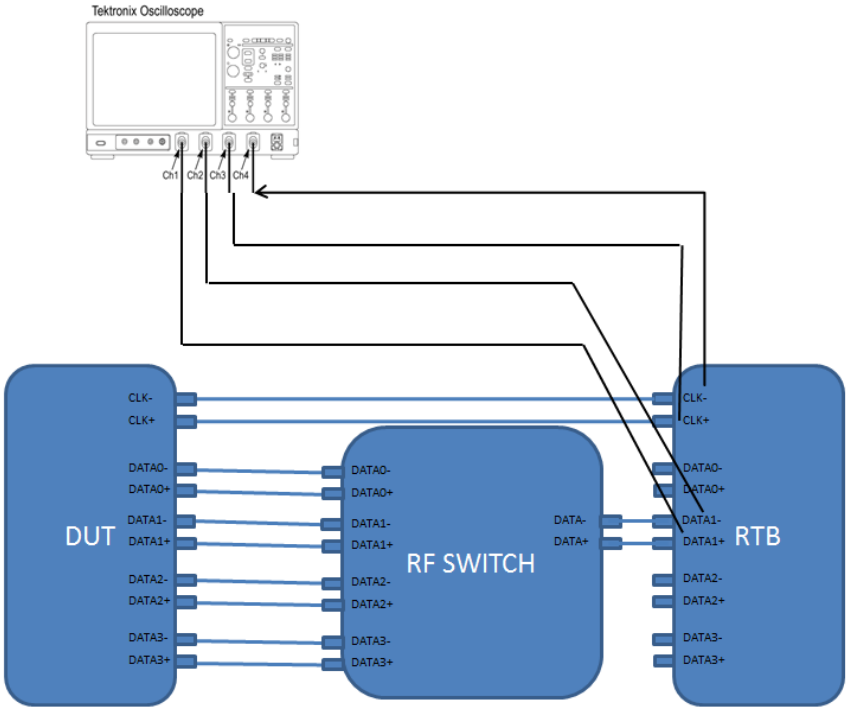
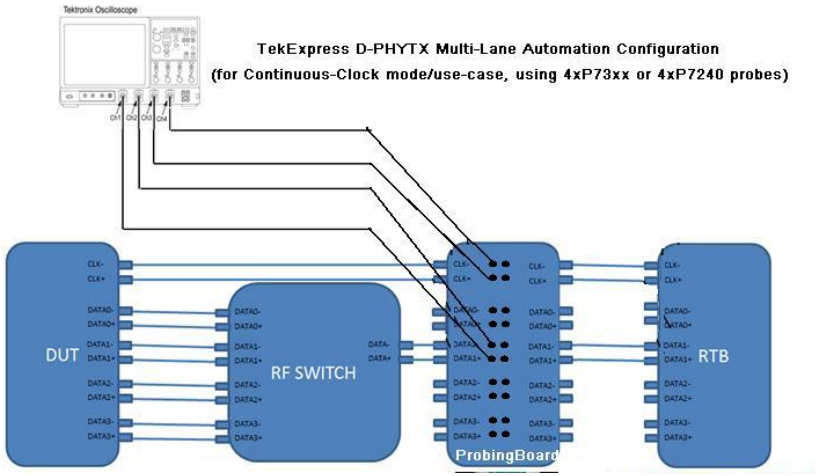
D-PHY Tx : D-PHY DUT Scenarios
Use Cases/ Test Setup Examples – 3 (Multi-Lane DUT)

- Use-Case: **Multi-lane Non-Live-Setup** with Stand-alone DUTs, and **DUT has no SMA i/f.**
  Test Setup: "Termination Board" Required. Use Solder-In/ Square-Pins directly to connect. Optional: **Keithley RF Switch** for multi-lane Automation



- Use-Case: **Multi-lane Non-Live-Setup** with Stand-alone DUTs, and **DUT has Only SMA i/f.**
  Test Setup: "Termination Board" Required. And, a Probing-Board Required for SMA i/f. Optional: **Keithley RF Switch** for multi-lane Automation



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D-PHY Tx: Results Correlations

Tek D-PHYTX, and UNH-IOL tool DPHYGUI

Test ID	Measurement name	Tek Result Dp	Tek Result Dn	Unit	UNH Result Dp	UNH Result Dn	Deviation in % Dp	Deviation in % Dn
1.1.1	Data Lane LP-TX Thevenin Output High Level Voltage (VOH)	1.212	1.209	V	1.212	1.209	0.00	0.00
1.1.2	Data Lane LP-TX Thevenin Output Low Level Voltage (VOL)	0.024	0.021	V	0.204	0.213	-88.24	-90.14
1.1.3	Data Lane Rise Time	24.35	23.89	nS	28.06	24.99	-13.22	-0.83
1.1.4	Data Lane Fall Time	14	13.52	nS	13.97	13.64	0.21	0.90
1.2.1	Clock Lane LP-TX Thevenin Output High Level Voltage (VOH)	1.191	1.209	V	1.191	1.209	0.00	0.00
1.2.2	Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL)	0.009	0.045	V	0.219	0.415	-95.89	-88.89
1.2.3	Clock Lane Rise Time	22.92	22.2	nS	22.83	22.11	0.39	-0.49
1.2.4	Clock Lane Fall Time	14.2	10.68	nS	14.42	10.71	-1.53	2.59
1.3.1	Data Lane HS Entry: Data Lane TLPX Value		70.08	nS		70.11	-0.03	-0.03
1.3.2	Data Lane HS Entry: THS-PREPARE Value		72.32	nS		72.40	-0.11	-0.11
1.3.3	Data Lane HS Entry: THS-PREPARE + THS-ZERO Value		178.88	nS		178.87	0.01	0.01
1.3.4	Data Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)	-211.6	217.2	mV	-214.8	218.3	-1.49	-0.50
1.3.5	Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})		5.6	mV		3.5	37.50	37.50
1.3.6	Data Lane HS-TX Single Ended Output High Voltages ($V_{OHHS(P)}$,$V_{OHHS(N)}$)	456	453	mV	417.5	417	8.44	7.95
1.3.7	Data Lane HS-TX Common-Mode Voltages ($V_{CMTX(P)}$,$V_{CMTX(N)}$)	305.96	306.78	mV	305.2	306.7	0.25	0.03
1.3.8	Data Lane HS-TX Common-Mode Voltage Mismatch ($\Delta V_{CMTX(0,1)}$)		0.408	mV		0.7	-41.71	-41.71
1.3.9	Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz		13.59	mVpk		14.3	-4.97	-4.97
1.3.10	Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz (ΔV_{CM}		7	mVrms		7	0.00	0.00
1.3.11	Data Lane HS-TX 20%-80% Rise time (t_R)		223.6	pS		223.5	0.04	0.04
1.3.12	Data Lane HS-TX 80%-20% Fall time (t_F)		228.6	pS		229.6	-0.44	-0.44
1.3.13	Data Lane HS Exit: $T_{HS-TRAIL}$ Value		62.45	nS		62.4	0.18	0.18
1.3.14	Data Lane HS Exit: 30%-80% Post-EoT Rise Time(T_{REOT}) Value		17.04	nS		16.3	2.47	2.47
1.3.15	Data Lane HS Exit: TEOT Value		79.49	nS		78.7		-0.66
1.3.16	Data Lane HS Exit: THS-EXIT Value		10.98	nS	Not Available			
1.4.1	Clock Lane HS Entry: T_{LPX} Value		71.28	nS		71.5	0.04	0.04
1.4.2	Clock Lane HS Entry: $T_{CLKPREPARE}$ Value		51.9	nS		50.6	3.26	3.26
1.4.3	Clock Lane HS Entry: $T_{CLKPREPARE}$ +T_{ZERO} Value		294.6	nS		298.1	-1.24	-1.24
1.4.4	Clock Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)	-188.31	136.99	mV	-184.7	132.7	1.95	1.95
1.4.5	Clock Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})		51.33	mV		58.2	-11.80	-11.80
1.4.6	Clock Lane HS-TX Single Ended Output High Voltages ($V_{OHHS(P)}$,$V_{OHHS(N)}$)	447	471	mV	378.6	404.1	15.30	14.20
1.4.7	Clock Lane HS-TX Common-Mode Voltages ($V_{CMTX(P)}$,VCMTX$_{(N)}$)	314.06	310.84	mV	314.1	310.9	-0.01	-0.02
1.4.8	Clock Lane HS-TX Common-Mode Voltage Mismatch ($\Delta V_{CMTX(0,1)}$)		1.61	mV		1.6	0.63	0.63
1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz		17.3	mVpk		12.2	29.48	29.48
1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz (ΔV_C		7.46	mVrms		7.4	0.81	0.81
1.4.11	Clock Lane HS-TX 20%-80% Rise time (t_R)		277.3	pS		263.4	5.36	5.36
1.4.12	Clock Lane HS-TX 80%-20% Fall time (t_F)		275.39	pS		258.3	6.62	6.62
1.4.13	Clock Lane HS Exit: $T_{CLK-TRAIL}$ Value		93.32	nS		92.7	1.23	1.23
1.4.14	Clock Lane HS Exit: 30%-80% Post-EoT Rise Time(T_{REOT}) Value		17	nS		17.5	-2.91	-2.91
1.4.15	Clock Lane HS Exit: TEOT Value		70.31	nS		70.8		-0.19
1.4.16	Clock Lane HS Exit: THS-EXIT Value		178.24	nS	Not Available			
1.4.17	Clock Lane HS Clock Instantaneous (UI_{INST})	Min 1.134 / Mean	Max 1.38	pS	Min NA / Mean	Max 1.36	Min NA / Mean	Max 1.77 / 1.20
1.5.1	HS Entry T_{CLKREQ} Value		87.28	nS		89.3	-2.26	-2.26
1.5.2	HS Exit $T_{CLKPOST}$ Value		10361.52	nS		10297.7	0.62	0.62
1.5.3	HS Clock Rising Edge Alignment to First Payload Bit							
1.5.4	Data-to-Clock Skew (TSKEW[TX])							
	Clock UI		1.25	nS		1.25		0.00
	Maximum Data to clock skew		-275	mUI		-263		-4.73
	Minimum Data to clock skew		-452	mUI		-444		5.09
	Mean Data to clock skew		-346	mUI		-358		3.41

Setup: MSO 20GHz scope, 4x P6248 probes, Termination board and probing board from UNH.

* As LP HS waveform is used in this use-case, Tek algorithm finds the LP-00 region and computes VOL in that region, whereas the UNH algorithm considers t computing VOL. If LP signal is used, the same measurement has 100% correlation.

Deviation in %	
Dp	Dn
0.00	0.00
-88.24	-90.14
-13.22	-0.83
0.21	0.90
0.00	0.00
-95.89	-88.89
0.39	-0.49
-1.53	2.59
-0.03	-0.03
-0.11	-0.11
0.01	0.01
-1.49	-0.50
37.50	37.50
8.44	7.95
0.25	0.03
-41.71	-41.71
-4.97	-4.97
0.00	0.00
0.04	0.04
-0.44	-0.44
0.18	0.18
2.47	2.47
	-0.66
0.04	0.04
3.26	3.26
-1.24	-1.24
1.95	1.95
-11.80	-11.80
15.30	14.20
-0.01	-0.02
0.63	0.63
29.48	29.48
0.81	0.81
5.36	5.36
6.62	6.62
1.23	1.23
-2.91	-2.91
	-0.19
Min	Max
NA	1.77
Mean	1.20
-2.26	-2.26
0.62	0.62
	0.00
	-4.73
	5.09
	3.41

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D-PHY Tx : Opt.D-PHY Debug and Analysis Solution

- Opt.D-PHY : D-PHY Essentials
  - DPOJET option for Setup Library &MOI
  - Provides Debug Analysis and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.DJA is Pre-Requisite
- Differentiation
  - Fully-Flexible for Debug Analysis &Characterization
  - Breadth of Tests Coverage
  - Based on State-of-the-art DPOJET tool

- Value proposition
  - Tek 3.5GHz scope is the Minimal Configuration for accurate testing
  - Single tool (DPOJET) for both MIPI Phy standards - Opt.M-PHYTX &Opt.D-PHY
  - Comprehensive DPOJET Reports.
  - D-PHY extension spec (1.5G) ready

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D-PHY Tx : 1.5G Data Rate Extension Spec v1.1

Spec Announced January, 2012

- Both Opt.D-PHYTX and Opt.D-PHY are **Fully-Supported for 1.5G**.
  - All Measurement Algorithms remain same
  - **Only "Limits" vary** for following Five parameters for 1.5G datarate.
    1. HS rise/fall time (tr, tf),
    2. VOD mismatch (dVOD),
    3. TX data to clock skew (TSKEW[TX]),
    4. RX setup and hold times (TSETUP[RX], THOLD[RX]),
    5. TX/RX return loss (SddTX, SddRX).
  - Both Opt.D-PHYTX and Opt.D–PHY support Limits Editing today.

Agenda

- MIPI Technologies &Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI, &UniPro
  - Rx
- Summary, Q&A

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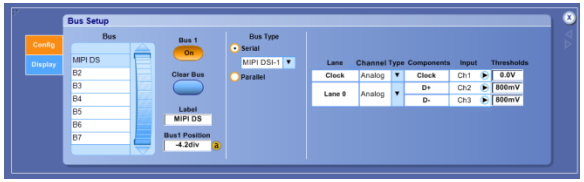
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

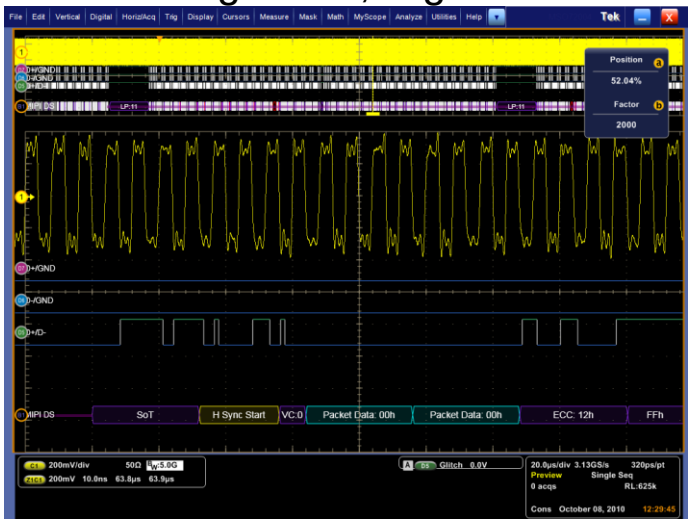
Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI &CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial-- > Select MIPI DSI or CSI from the drop down list.



Probe using Mixed Channels

Analog Clock, Digital Data



Digital Clock, Analog Data

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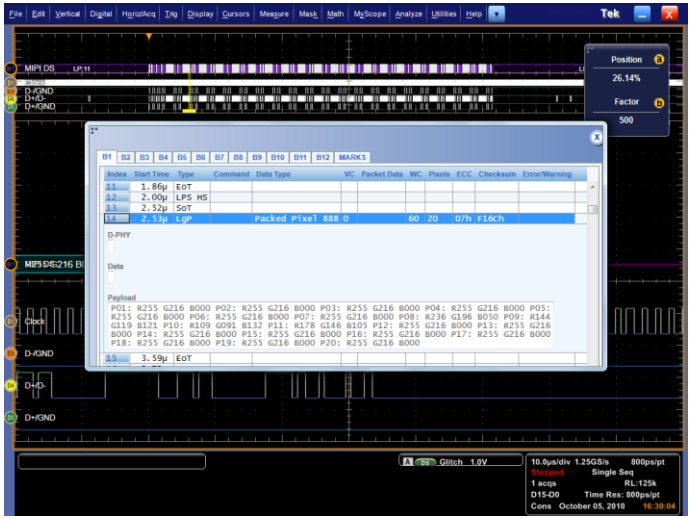
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

Timestamps

- Decodes LP &HS states, BTA, DCS, ECC, Checksum, Escape Mode, etc
- Decodes SoT, EoT, Data Type, Virtual Channel, Word Count, Short / Long packet, Number of pixels, Each pixel values shown in R-B-G format.
- Timestamps for each Event &Event Table
- Zoom on a row of pixels



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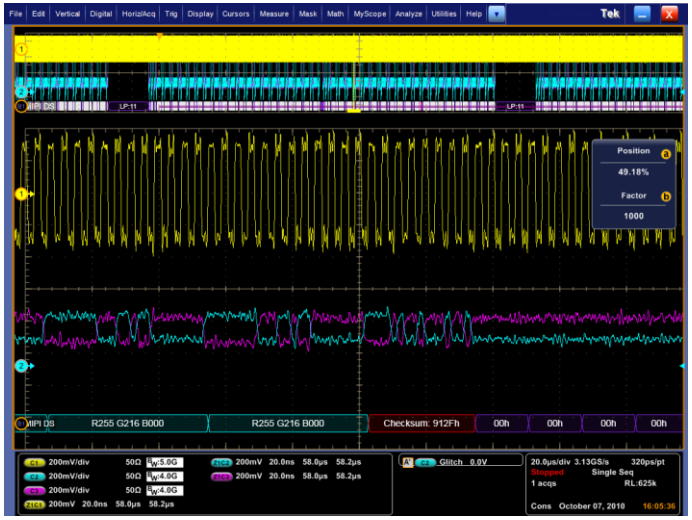
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

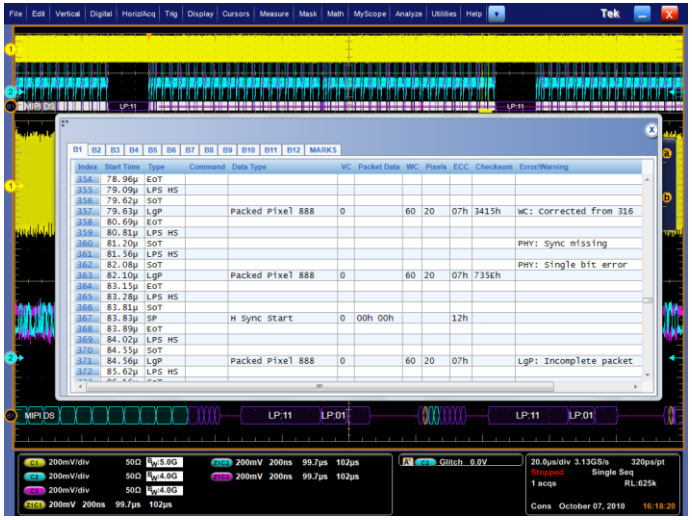
Errors/ Warnings indicated in Decode waveform &Event Table

Missing Sync

Checksum Error



ECC error



Errors and Warnings indicated in event table

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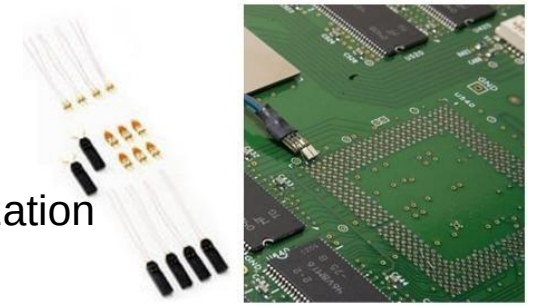
D-PHY Tx &Decode: Recommended Test Setup

www.Tek.com/MIPI

- Scope
  - DPO7354/C or DPO/DSA/MSO70404/B/C/D or higher for rise time accuracies
- Probes
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500/P73xx (clock is non-continuous), or 3x TDP3500/P73xx (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- Scope Software
  - Opt.D-PHYTX on TEKEXP for Conformance Test
  - Opt.D-PHY on DPOJET for Debug, Analysis &Characterization
  - Opt.SR-DPHY for Decoding CSI-2 and DSI traffic
- Fixtures
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups: We recommend following UNH-IOL Termination board
    - http://www.iol.unh.edu/services/testing/mipi/fixtures.php
    - www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc



P7380 probe used with a probe-tip

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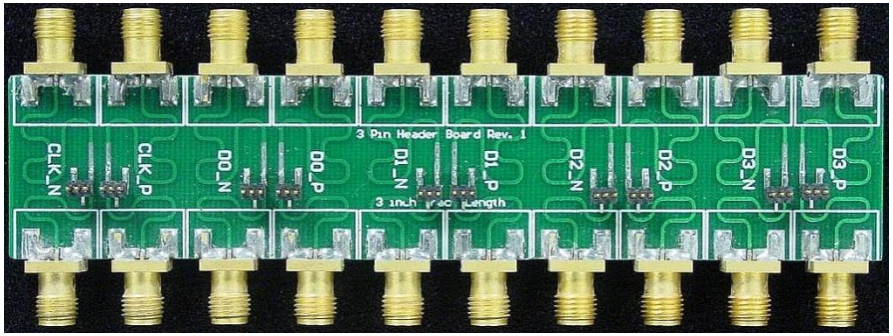
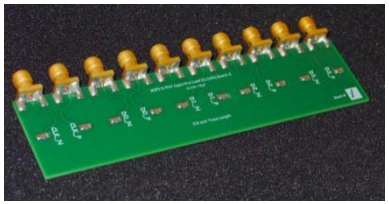
D-PHY Tx: Optional Accessories

Optional Based on DUT Scenarios (i.e. SMA/ Non-live setup/ Multi-lane)

- UNH-IOL RTB Reference Termination Board (list price: $2,895.), UNH-IOL Probing Board (list price: $450.), and Capacitive Load Board for Clock and Data Lane LP-TX Signaling tests (list price: $295.).
  - http://www.iol.unh.edu/services/testing/mipi/fixtures.php
  - www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc





- RF Switch,
  - Keithley S46-6666A, for multi-lane automation:
  - http://www.keithley.com/products/switch/rfmicrowave/?mn=S46

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Agenda

- MIPI Technologies &Tek Strategic Involvement
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  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI, &UniPro
  - Rx
- Summary, Q&A

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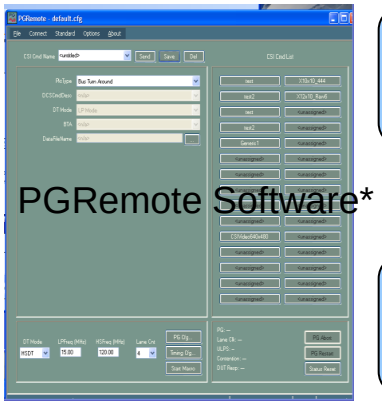
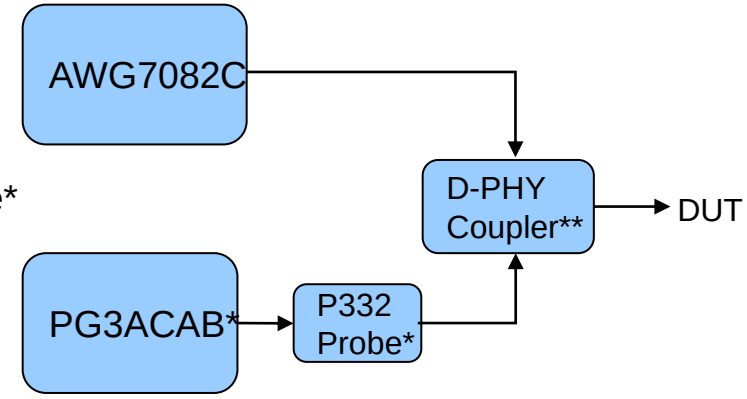
D-PHY Rx : Test Solution Overview

Manual Setup based on PG with PGRemote Software

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals

Recommended Manual Setup





*These Moving Pixel products are available as Tektronix part number
**Tektronix part number not available yet. Expected Soon.

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D-PHY Rx : Test Solution Overview

100% Test Coverage to CTS v0.98

Group 1 LP - RX voltage and timing requirements			
Test	**Title**	**Page**	**Equipment**
2.1.1	LP - RX Logic 1 Input Voltage (V_{IH})	108	PG
2.1.2	LP - RX Logic 0 Input Voltage, non-ULP State (V_{IL})	110	PG
2.1.3	LP - RX Logic 0 Input Voltage, ULP State ($V_{IL-ULPS}$)	112	PG
2.1.4	LP - RX Minimum Pulse Width Response (T_{MIN-RX})	113	PG
2.1.5	LP - RX Input Hysteresis (T_{HYST})	114	PG
2.1.6	LP - RX Input Pulse Rejection (e_{SPIKE})	116	PG + AWG + DC Power Supply
2.1.7	LP - RX Interference Tolerance (V_{INT} and f_{INT})	120	PG + AWG
2.1.8	LP - CD Logic Contention Thresholds (V_{ILCD} ans V_{IHCD})	122	PG + AWG

Group 2 LP - RX Behavioral Requirements			
Test	**Title**	**Page**	**Equip**
2.2.1	LP - RX Initialization Period (T_{INIT})	125	PG
2.2.2	ULPS Exit: LP - RX $T_{CLKULPS}$ Timer Value	126	PG
2.2.3	Clock Lane LP - RX Invalid/Aborted ULPS Entry	127	PG
2.2.4	Data Lane LP - RX Invalid/Aborted Escape Mode Entry	128	PG
2.2.5	Data Lane LP - RX Invalid/Aborted Escape Mode Command	130	PG
2.2.6	Data Lane LP - RX Escape Mode Invalid Exit (Informative)	132	PG
2.2.7	Data Lane LP - RX Escape Mode, Ignoring Post Trigger-Command Extra Bits	134	PG
2.2.8	Data Lane LP - RX Escape Mode Unsupported/Unassigned Commands	136	PG

Group 3: HS - RX Voltage and Setup/Hold Requirements			
Test	**Title**	**Page**	**Equipment**
2.3.1	HS - RX Common Mode Voltage Tolerance ($V_{CMRX(DC)}$)	139	PG
2.3.2	HS-DX Differential Input High Threshold (V_{DTH})	141	PG
2.3.3	HS-DX Differential Input Low Threshold (V_{DTL})	143	PG
2.3.4	HS - RX Single-Ended Input High Voltage (V_{SHA})	144	PG
2.3.5	HS - RX Single-Ended Input Low Voltage (V_{SLA})	146	PG
2.3.6	HS - RX Common Mode Interference 50MHz - 450MHz (delta VCMRX(LF))	148	PG + AWG
2.3.7	HS - RX Common Mode Interference Beyond 450MHz (delta VCMRX(HF))	150	PG + AWG
2.3.8	HS - RX Setup/Hold and Jitter Tolerance	151	PG + AWG

Group 4: HS - RX Timer Requirements			
Test No.	**Title**	**Page**	**Equipment**
2.4.1	Data Lane HS - RX $T_{D-TERM-EN}$ Value	156	PG
2.4.2	Data Lane HS - RX $T_{HS-SETTLE}$ + $T_{HS-SKIP}$ Tolerance	158	PG
2.4.3	Data Lane HS - RX $T_{HS-SETTLE}$ Value	160	PG
2.4.4	Data Lane HS - RX $T_{HS-SETTLE}$ Tolerance	162	PG
2.4.5	Data Lane HS - RX $T_{HS-TERM}$ Value	164	PG
2.4.6	Clock Lane HS - RX $T_{CLK-TERM-EN}$ Value	166	PG
2.4.7	Clock Lane HS - RX $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ Tolerance	167	PG
2.4.8	Clock Lane HS - RX $T_{CLK-SETTLE}$ Value	169	PG
2.4.9	Clock Lane HS - RX $T_{CLK-SETTLE}$ Tolerance	171	PG
2.4.10	Clock Lane HS - RX $T_{CLK-TERM}$ Value	173	PG
2.4.11	Clock Lane HS - RX $T_{CLK-PRE}$ + $T_{CLK-POST}$ Tolerance	175	PG

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Agenda

- MIPI Technologies &Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI , &UniPro
  - Rx
- Summary, Q&A

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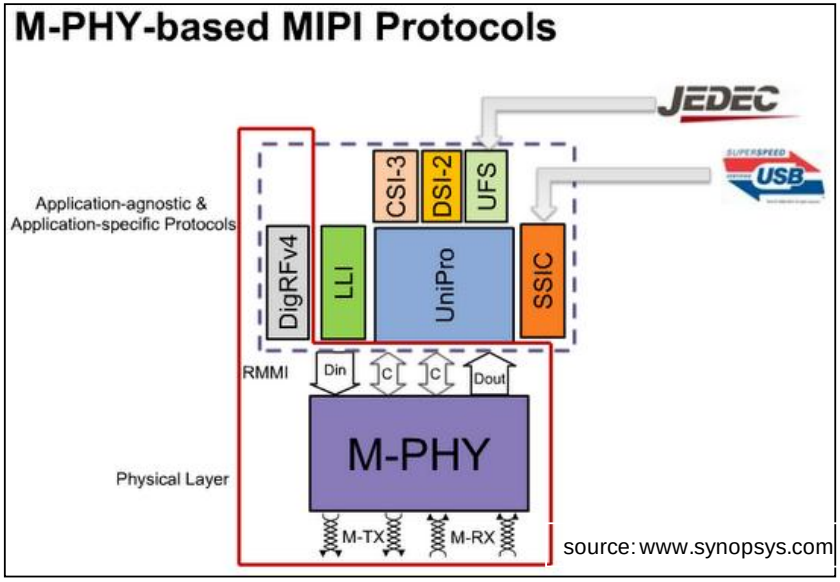
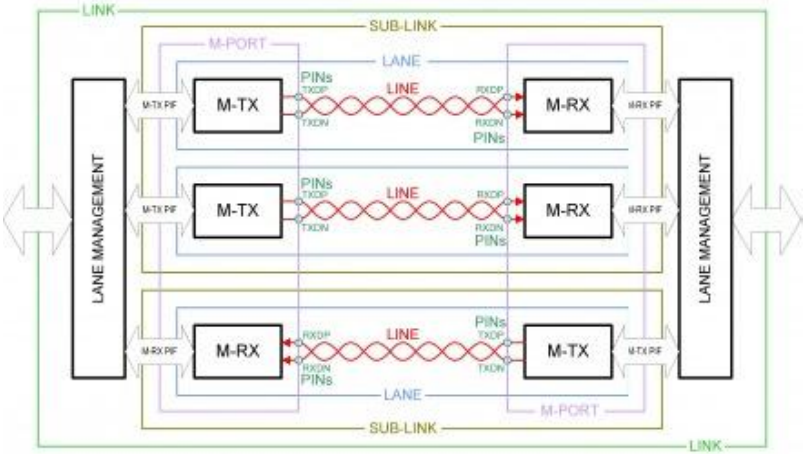
What is M-PHY ?

- M-PHY is a high-speed serial interface to the DigRFv4, UniPro, LLI, CSI-3 and DSI-2 interconnect standards of the MIPI Alliance, and the UFS and SSIC protocol standards of JEDEC and USB-IF respectively.
- M-PHY is a flexible architecture that allows the implementer to support high data rates at minimal power, cost & I/O redesign, for applications such as High Definition Video
- A Fast, Scalable, Serial Communications Architecture
  - Link – Connects M-PHY Transmitter to an M-PHY Receiver
  - Sub-link – Manage one or more lanes
  - Lane – Operation defined in the protocol (DSI, CSI, UniPro, DigRF)





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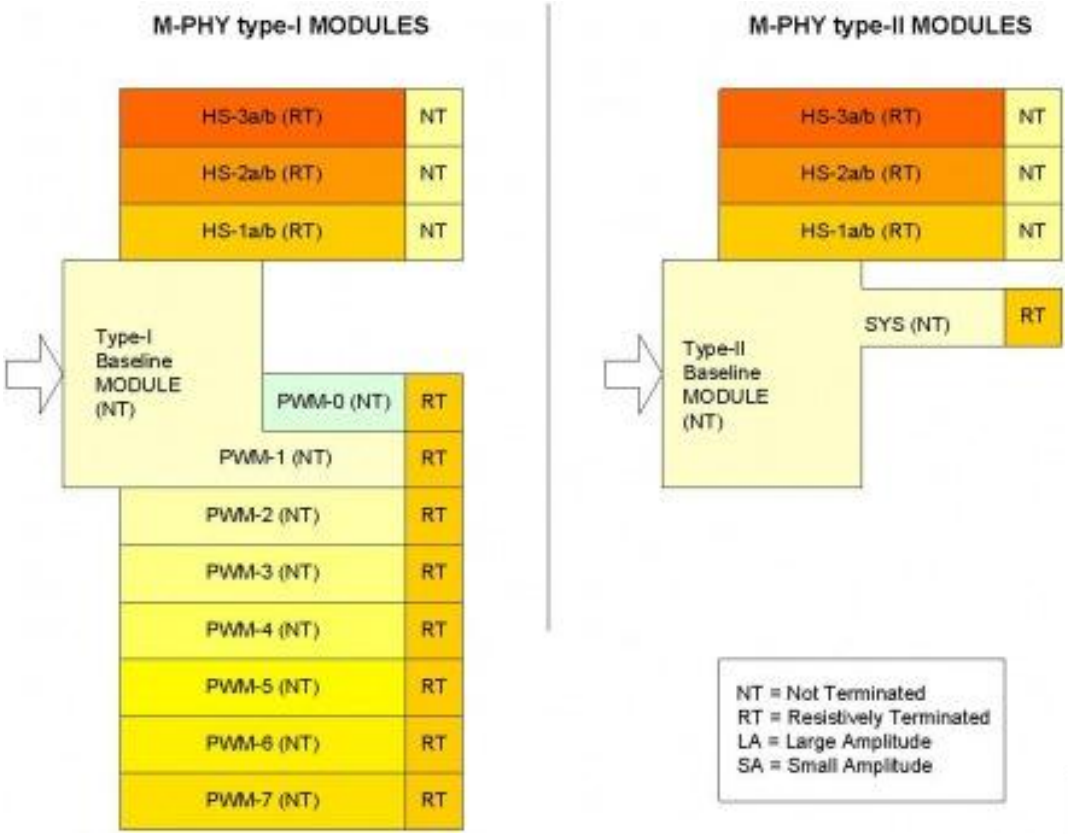
What are M-PHY Type-I and Type-II ?



Application	Type	HS-GEAR
DigRF v4	II	1
CSI-3	I	2
DSI-2	I	2
JC-64.1 UFS	I	2
LLI	I	3

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M-PHY Transmitter Testing Challenges

M-PHY Signal Characteristics							
Signaling mode	**Datarates**			**Amplitudes**		**Impedance**	
	Gears	A (Gbps)	B (Gbps)	Large	Small	Resistive Terminated	Non Terminated
High Speed (HS)	G1	1.25	1.45	Terminated: 160-240mV, Non-Terminated: 320-480mV	Terminated: 100-130mV, Non-Terminated: 200-260mV	50 ohms	-
	G2	2.5	2.91				
	G3	5	5.83				
PWM (ie. TYPE-I)	Gears	Min (Mb/s)	Max (Mb/s)			50 ohms	10k ohms
	G0	0.01	3				
	G1	3	9				
	G2	6	18				
	G3	12	36				
	G4	24	72				
	G5	48	144				
	G6	96	288				
	G7	192	576				
SYS (ie. TYPE-II)			576 (Mb/s)			50 ohms	10k ohms

- Higher data rate will increase importance of Signal Integrity of links
  - More emphasis on timing/jitter and noise (signal integrity)
  - Receiver testing will be needed to stress-test resulting BER
- 1000+ tests per lane, covering multiple Gears, Terminations, Amplitudes.
- Termination – Restive or not Terminated.
  - LS mode can operate either of them
  - HS mode it is always terminated, so swings are halved.
- Type-I and Type-II are Low speed modes, and are NOT interoperable
  - Type-I operates on independent local clocks. Type-II requires a shared Ref-clock.
  - DUTs may support both

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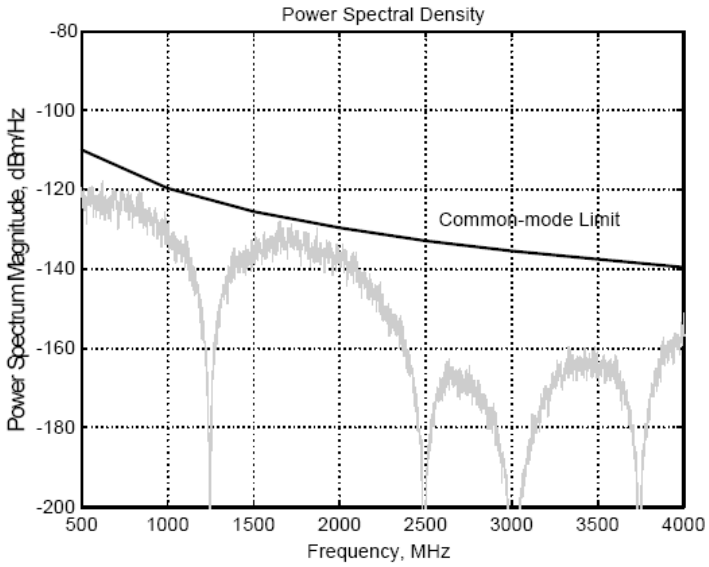
M-PHY Transmitter Testing Challenges
Multiple instruments for Different tests (Electrical and PSD)

- M-PHY DiRF is an interface between base band and RF chip
  - Common mode (CM) signal component dominates EMI – interferes with LNA
- Conformance Test Requirement:
  - Power Spectral Density (PSD) of CM signal shall be within the mask
  - *CM Mask = -180 - (14.3*ln (f_MHz) - 159) dBm/Hz over 500-3000 MHz*
  - PSD is frequency domain test, and usually done using Spectrum Analyzer separately, in addition to an Oscilloscope for remaining tests.



Common-Mode Limit

F, MHz	Limit, dBm/Hz
500	-109.9
1000	-119.8
1500	-125.6
2000	-129.7
2500	-132.9
3000	-135.5
3500	-137.7
≥4000	-139.6

Figure 34 Common-mode Power Spectral Magnitude Limit

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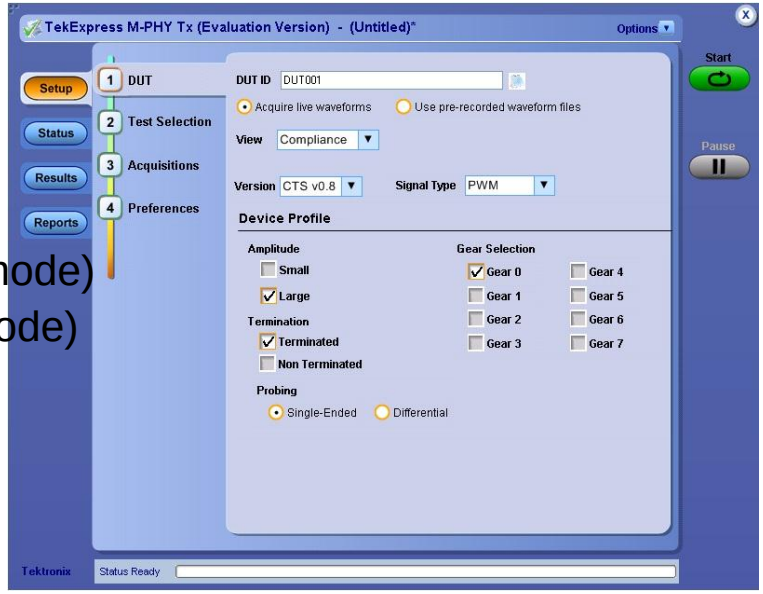
M-PHY Tx : Opt.M-PHYTX Automated Solution

- Opt.M-PHYTX
  - TekExpress (2.0) option for Single-button Automated transmitter testing
  - Provides Conformance &Debug Testing to M-PHY Base Spec v1.0 &UNH's CTS.
  - Runs on DPO/DSA70KB/C/D or MSO70K/C scopes (6GHz and above)
  - TekExpress framework &license is included.
  - Opt.DJA is pre-requisite. Opt.M-PHY not required.
- Differentiation
  - All HS and PWM Gears
  - Most Complete Test coverage
    - (95% HS, 74% PWM).
  - Seamless Debug on failures (User-Defined mode)
  - Multi-lane one-time Setup (Diff Acquisition mode)
  - Scope-based Power-Spectral Density tests
- US list price
  - Opt.M-PHYTX: $5570



- Value proposition
  - For Gear2 M-PHY Tx testing, Tek 8GHz oscilloscope is sufficient. Where as, competition recommends a 12GHz or 13GHz oscilloscope.
  - For Gear3 M-PHY Tx testing, Tek 20G oscilloscope is sufficient. Where as, competition recommends a 25GHz oscilloscope.

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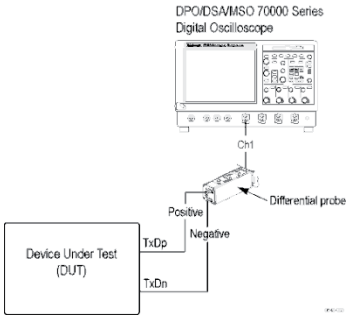
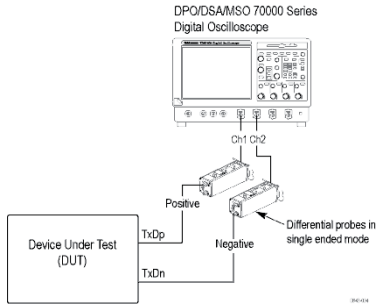
M-PHY Tx : Opt.M-PHYTX Automation Features

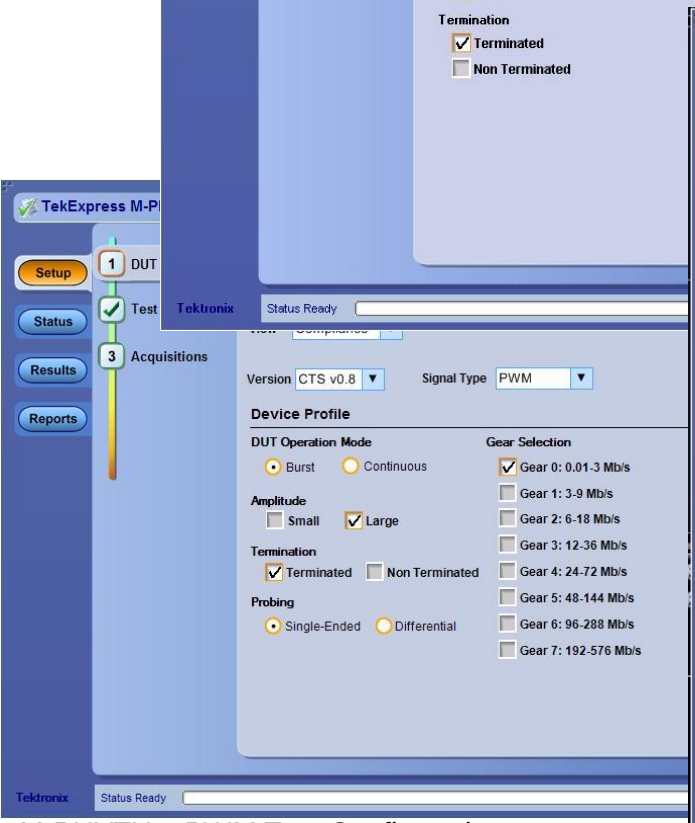
Key Feature	Benefit
Automated Testing	• Significantly reduces testing time, and enables you to test devices faster • Automates apprx 1000 tests in regression, in different combinations of Gears, Sub-Gears, Terminations, Amplitudes, etc
Most Complete Tests coverage	• All HS Gears including Gear3, and all PWM Gears • HS Automates 95% of High Speed, and 75% of PWM tests
Highly Optimized Setup	• Performs Power Spectral Density (PSD) Tests using Oscilloscope-integrated Algorithms Uniquely, • Does not require an External Spectral Analyzer or Extra Hardware to Perform PSD Measurements
Seamless Debug	• User-Defined mode allows Pause on a Test while in Automation, and Switch to DPOJET Analysis Tool for Detailed Debug of failures
Multi-lane one-time Setup	• Connect upto 4-lanes of DUT to 4-channels on an oscilloscope, using differential mode of acquisition.
Setup Configuration	• Allows Selecting Different Gears and Sub-gears of HS and PWM Signals, Large/Small Amplitudes, Impedance Termination/Un-termination, etc
Test reports	• Provides Single Printable Report, across Different Combinations • Provides Pass/Fail Summary Table, along with Margin Details, Optional Waveform Captures, and Eye Diagrams

M-PHY Tx : Opt.M-PHYTX Automation Features

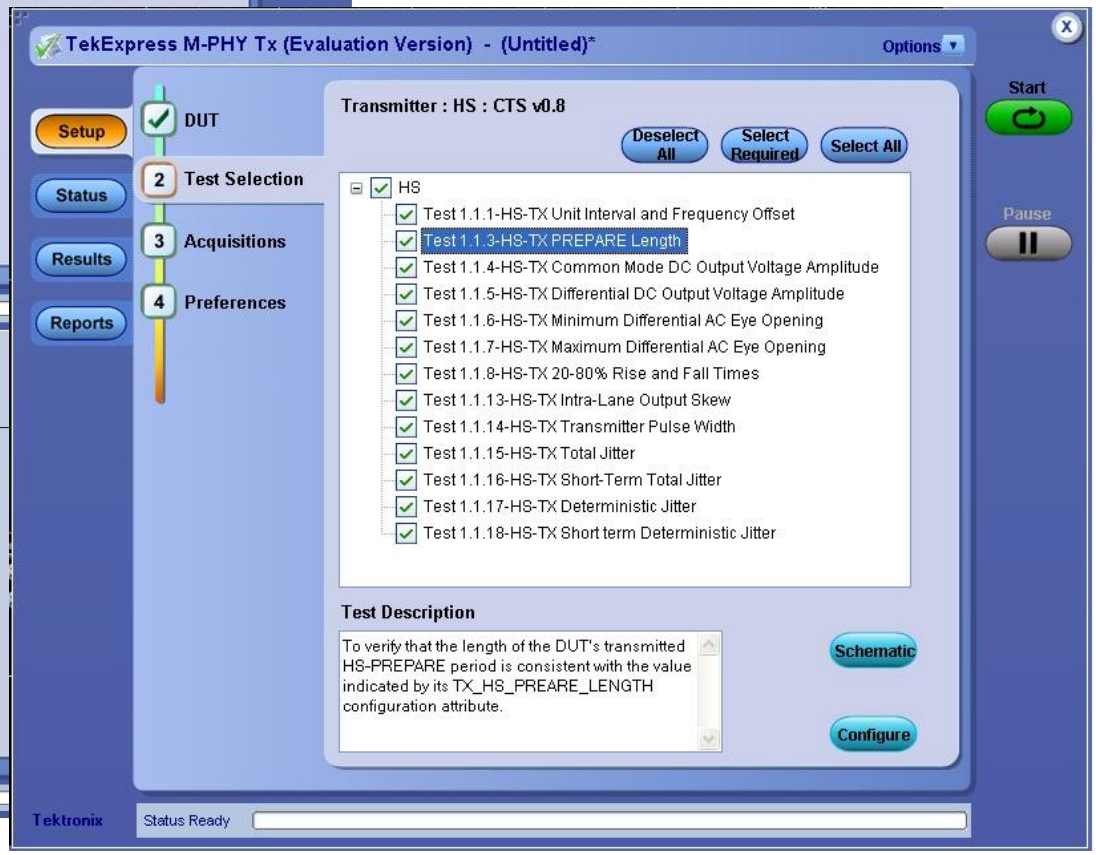
M-PHYTX – HS Test Configurations







M-PHYTX – PWM Test Configurations



M-PHYTX – HS Tests Coverage

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M-PHY Tx : Opt.M-PHYTX Automation Features

User-Defined Mode – Few Configurable Parameters (HS &PWM)

Table 18: HS test parameters (User Defined mode) (cont.)

Parameter group	Parameter name	Range	Default	Units
HS: Ref Levels	Absolute/Percentage	Absolute, Percentage	Absolute	N/A
	Autoset basetop method	AUTO, MINMAX, FULLHISTOGRAM, EYEHISTOGRAM	AUTO	N/A
	High level [3]	51 to 90 (in %) -10 to 10 (in Absolute)	90 (in %) 0 (in	% or V
	Mid level [3]	20 to 80 (in %) -10 to 10 (in Absolute)	50 (i 0 (in	
	Low level [3]	10 to 49 (in %) -10 to 10 (in Absolute)	10 (i 0 (in	
	Hysteresis [3]	2 to 20 (in %) -2 to 2(in Absolute)	5 (in 0.05	
HS: Filters	Low pass filter (F1) spec	NONE, FIRST, SECOND, THIRD	NON	
	High pass filter	1–100 (1–10 for test 1.1.1 only)	1	
	Low pass filter (F2) spec	NONE, FIRST, SECOND, THIRD	SEC	
	Low pass filter	620–630 (1–10 for test 1.1.1 only)	2	
	Filter ramp time	0–10	0.25	
	Filter blanking time	0–10	0.25	
HS: Prepare Length	Gear1A-HS Prepare Length	0–15	10	
	Gear1B-HS Prepare Length	0–15	10	
	Gear2A-HS Prepare Length	0–15	10	
	Gear2B-HS Prepare Length	0–15	10	
	Gear3A-HS Prepare Length	0–15	10	
	Gear3B-HS Prepare Length	0–15	10	

Table 18: HS test parameters (User Defined mode) (cont.)

Parameter group	Parameter name	Range	Default	Units
HS: Clock Recovery	Clock Recovery Method	Constant Clock-Mean, PLL Custom BW	Constant Clock-Mean	N/A
	PLL Model Type	1/2		N/A
	Damping	500–2000		
	Loop Bandwidth	0.1–10		
	Nominal data rate	Enabled, Disa		
	Known data pattern	Enabled, Disa		
	Pattern file path	N/A		
HS: Mask file path	Gear Type	Gear1A, Gear Gear2A, Gear Gear3A, Gear		
	NT LA Mask File path	Path to mask f		
	NT SA Mask File path	Path to mask f		
	RT LA Mask File path	Path to mask f		
	RT SA Mask File path	Path to mask f		
HS: Skew	From Edge	RISE, FALL, E		
	To Edge	SAMEAS, OPPOSITEAS		

Table 20: PWM test parameters (User Defined mode)

Parameter group	Parameter name	Range	Default	Units
PWM: Acquire	Horizontal scale	1000–10000	1	µs/div
	Resolution	2000–10000	10	ps/pt
	Sampling Rate [1]	0.10, 0.25, 0.50	0.25	GS/s
	Trigger Level [1, 2]	0–100	0	V
	Slope [1]	RISE, FALL, EITHER	RISE	N/A
	Coupling [1]	DC, AC, HF REJECT, LF REJECT, NOISE REJ	DC	N/A
	Pulse width when [1]	WITHIN, OUTSIDE	WITHIN	N/A
	Polarity	Positive, Negative	Positive	N/A
	Lower limit [1]	1–10	1	UI
	Gear 0 Upper limit [1]	1–20	15	UI
	Gear 1 Upper limit [1]	1–20	15	UI
	Gear 2 Upper limit [1]	1–20	15	UI
	Gear 3 Upper limit [1]	1–20	15	UI
	Gear 4 Upper limit [1]	1–20	15	UI
	Gear 5 Upper limit [1]	1–20	15	UI
	Gear 6 Upper limit [1]	1–20	15	UI
	Gear 7 Upper limit [1]	1–20	15	UI
PWM: Prepare Length	G0 - LS Prepare Length	0–15	10	N/A
	G1 - LS Prepare Length	0–15	9	N/A
	G2 - LS Prepare Length	0–15	8	N/A
	G3 - LS Prepare Length	0–15	7	N/A
	G4 - LS Prepare Length	0–15	6	N/A
	G5 - LS Prepare Length	0–15	5	N/A
	G6 - LS Prepare Length	0–15	4	N/A
	G7 - LS Prepare Length	0–15	3	N/A

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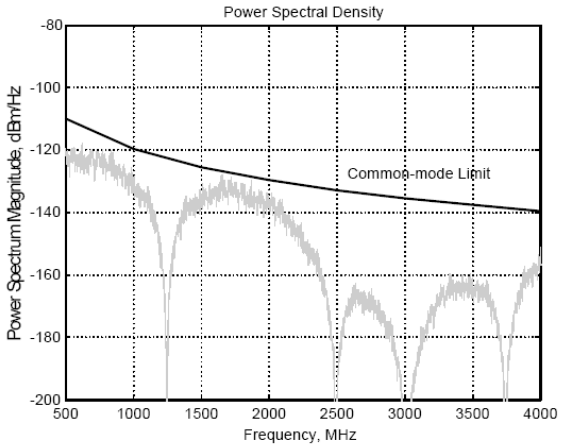
M-PHY Tx: Opt.M-PHYTX Automation Features

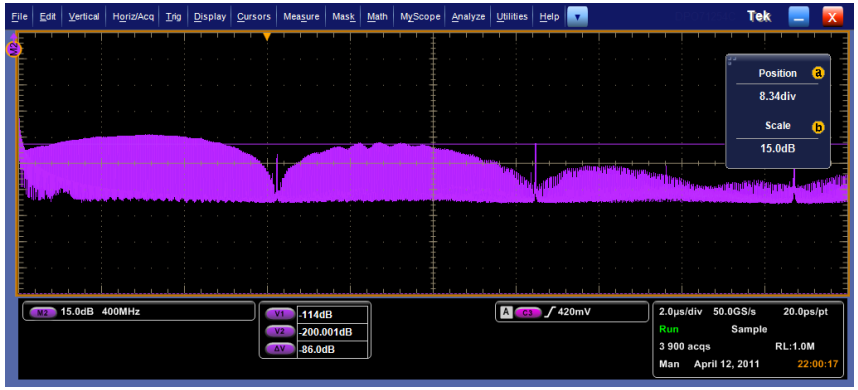
Power Spectral Density(PSD), Eye Diagram Examples

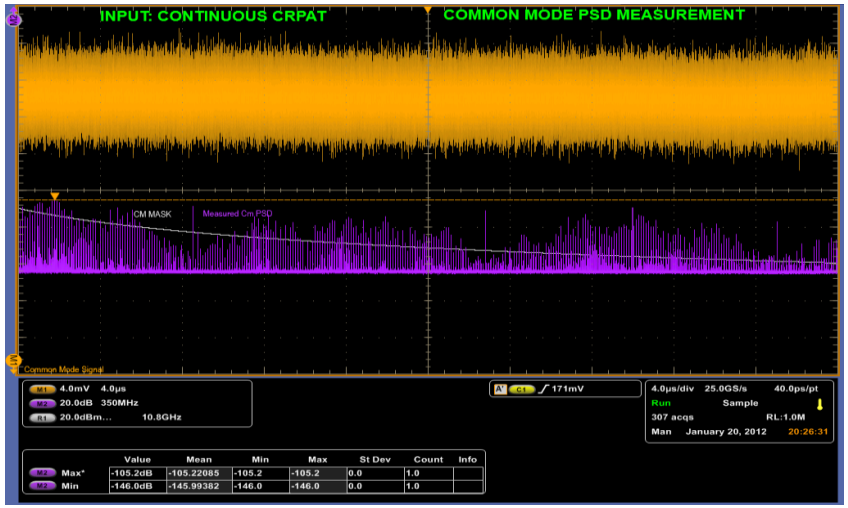


Common-Mode Limit

F, MHz	Limit, dBm/Hz
500	-109.9
1000	-119.8
1500	-125.6
2000	-129.7
2500	-132.9
3000	-135.5
3500	-137.7
≥4000	-139.6

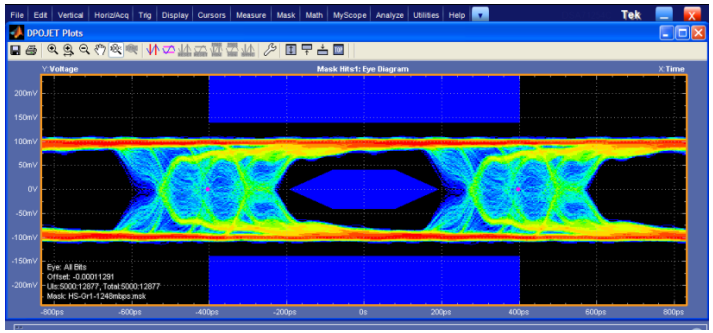
Figure 34 Common-mode Power Spectral Magnitude Limit





PSD Spectrum using Scope Math

Eye Diagram



M-PYTX performs both Time & Frequency Domain Tx Tests.

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M-PHY Tx : Opt.M-PHYTX Automation Features

Comprehensive Test Reports

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TekExpress HS-TX
Report

DUT ID:	DUT001	Device Type:	Transmitter
Date/Time:	Feb. 13, 2012 / 05:00:50	Execution Time:	47 Min
CTS Version:	CTS v0.8		
Overall Compliance Mode:	TRUE		
Overall Test Result:	FAIL		
Scope Model:	DPO70804	Scope F/W Version:	5.3.4 BUILD 25
Scope Serial Number:	Q434	SPC, Factory Calibration:	PASS;PASS
Probe Model (CH1):	N/A	TekExpress Version (FW, App):	2.0.0.198, 0.0.0.44
Probe Serial Number (CH1):	N/A	DPOJET Version:	"3.5.0 Build 17"
Probe Model (CH2):	N/A		
Probe Serial Number (CH2):	N/A		
Probe Model (CH3):	"TCA292D"		
Probe Serial Number (CH3):	"N/A"		
Probe Model (CH4):	"TCA292D"		
Probe Serial Number (CH4):	"N/A"		

Test Name	Lane	Term-ination	Gear	Ampl-itude	Measurement Details	Measured value	Units	Test Result	Margin
Test 1.1.1-HS-TX Unit Interval and Frequency Offset	Lane0	RT	Gear1A	LA	SSCFREQDEV(Fig-1)	8.308	ppm	Pass	1991.692
					SSCPROFILE(Fig-2)	801.282	pS	Informative	-N.A-
			Gear2A	LA	SSCFREQDEV(Fig-3)	4.608	ppm	Pass	1995.392
					SSCPROFILE(Fig-4)	400.641	pS	Informative	-N.A-
Test 1.1.4-HS-TX Common Mode DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_CommonModeVoltage (Fig-5)	202.489	mV	Pass	42.489, 57.511
			Gear2A	LA	Test_HS_CommonModeVoltage (Fig-6)	202.959	mV	Pass	42.959, 57.041
Test 1.1.5-HS-TX Differential DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_DiffDCDifPVoltage (Fig-7)	230.898	mV	Pass	70.898, 9.102
					Test_HS_DiffDCDifNVoltage (Fig-8)	-234.252	mV	Pass	5.748, 74.252
			Gear2A	LA	Test_HS_DiffDCDifPVoltage (Fig-9)	216.96	mV	Pass	56.96 , 23.04
					Test_HS_DiffDCDifNVoltage (Fig-10)	-226.903	mV	Pass	13.097, 66.903
Test 1.1.6-HS-TX Minimum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	MASKHITS(Fig-11)	0	#hits	Pass	0
			Gear2A	LA	MASKHITS(Fi				
Test 1.1.7-HS-TX Maximum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	EYEHIGH(Fi				
					EYELOW(Fig				
					MASKHITS(Fi				
			Gear2A	LA	EYEHIGH(Fi				
					EYELOW(Fig				
					MASKHITS(Fi				
Test 1.1.8-HS-TX 20-80% Rise and Fall Times	Lane0	RT	Gear1A	LA	Test_HS_RiseTim				
					Test_HS_FallTime				
			Gear2A	LA	Test_HS_RiseTim				
					Test_HS_FallTime				

Single-printable report covering results from Multiple lane, Multiple Gears, Amplitudes, etc

Results from multiple test-configuration, of a single-test

Test Name	Lane	Termination	Gear	Amplitude	Measurement Details	Measured value	Units	Test Result	Margin	Low Limit	High Limit	Compliance Mode
Test 1.2.1-PWM-TX Transmit Bit Duration	Lane0	RT	Gear0	SA	Transmit Bit Duration	1	Mbps	Pass	0.99 , 2	>= 0.01	<= 3	Yes
				LA	Transmit Bit Duration	1	Mbps	Pass	0.99 , 2	>= 0.01	<= 3	
			Gear1	SA	Transmit Bit Duration	5	Mbps	Pass	2 , 4	>= 3	<= 9	
				LA	Transmit Bit Duration	5	Mbps	Pass	2 , 4	>= 3	<= 9	
			Gear2	SA	Transmit Bit Duration	10	Mbps	Pass	4 , 8	>= 6	<= 18	
				LA	Transmit Bit Duration	10	Mbps	Pass	4 , 8	>= 6	<= 18	
			Gear3	SA	Transmit Bit Duration	36	Mbps	Pass	24 , 0	>= 12	<= 36	
				LA	Transmit Bit Duration	36	Mbps	Pass	24 , 0	>= 12	<= 36	
			Gear4	SA	Transmit Bit Duration	36	Mbps	Pass	12 , 36	>= 24	<= 72	
				LA	Transmit Bit Duration	36	Mbps	Pass	12 , 36	>= 24	<= 72	
			Gear5	SA	Transmit Bit Duration	60	Mbps	Pass	12 , 84	>= 48	<= 144	
				LA	Transmit Bit Duration	60	Mbps	Pass	12 , 84	>= 48	<= 144	
			Gear6	SA	Transmit Bit Duration	100	Mbps	Pass	4 , 188	>= 96	<= 288	
				LA	Transmit Bit Duration	100	Mbps	Pass	4 , 188	>= 96	<= 288	
			Gear7	SA	Transmit Bit Duration	200	Mbps	Pass	8 , 376	>= 192	<= 576	
				LA	Transmit Bit Duration	200	Mbps	Pass	8 , 376	>= 192	<= 576	

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M-PHY Tx : Opt.M-PHY Essentials Testing Solution

- Opt.M-PHY: M-PHY Essentials
  - DPOJET option for Setup Library &MOI
  - Provides Debug Analysis and Characterization Testing
  - Based on Latest M-PHY Base Spec v1.0 and Conformance Test Suite v0.65.
  - Runs on 70K/B/C scopes (6 GHz and above)
  - Opt.DJA is Pre-Requisite
- Differentiation
  - Industry **1st** Testing Tool, since Sept'2010
  - **Wider** High-Speed Tests Coverage
  - Fully-Flexible for Debug Analysis &Characterization
  - Based on State-of-the-art DPOJET tool

- Value proposition
  - Single tool (DPOJET) for both MIPI Phy standards - Opt.M-PHY &Opt.D-PHY
  - Comprehensive DPOJET Reports.

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Agenda

- MIPI Technologies &Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI , &UniPro
  - Rx
- Summary, Q&A

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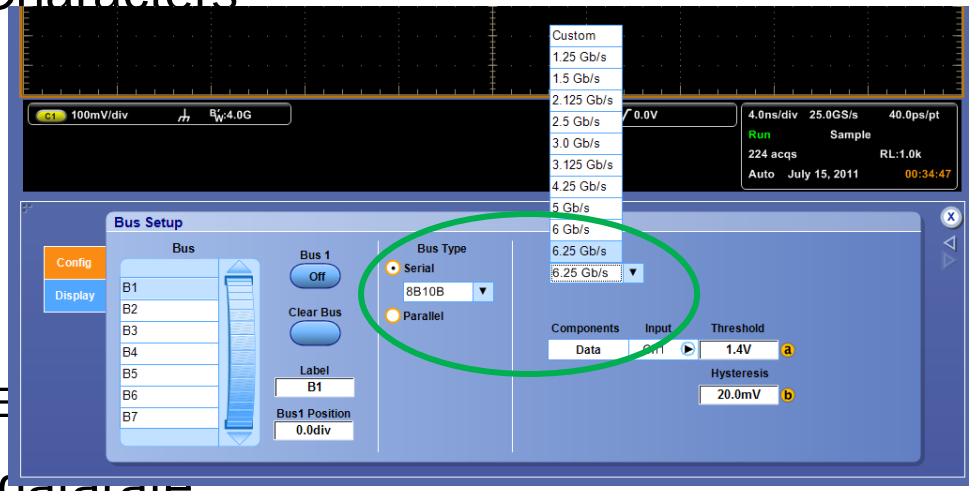
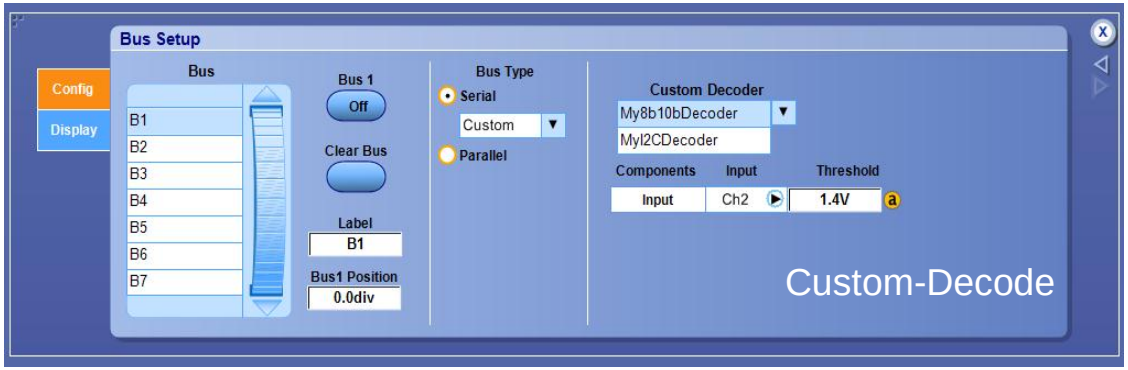
M-PHY Decode: Opt.SR-810B for 8b-10b Decode

- Decode into Symbols or 10-bit Characters
- Decode upto 6.25Gb/s Datarate
- Trigger & Search on
  - Any Control Character
  - Character/ Symbol
  - Pattern
  - Error (Character Error & Disparity E
- Custom-Decode upto 6.25Gb/s datarate
- Supported on all 70KC and MSO70K scopes.
- Software installed as part of TekScope firmware





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M-PHY Decode: Opt.MPHYVIEW for DigRFv4 Decode

- Automated Decoding:
  - Automatically recognizes data speeds, disassembles, and displays the decoded data in different readable-data formats
- 4 Lanes Decoding:
  - Acquires up to 4 lanes of data traffic at a time.
- On-line, Offline and Remote Analysis:
  - Uses TekVisa to connect to a scope.
  - Remote execution through LAN network.
- Filter Tab, Search and Options Tab:
  - Fillter the records in the listing based on user criteria.
  - Searching &highlight records that satisfy given criteria
  - Set display, disassembly, and configuration options.

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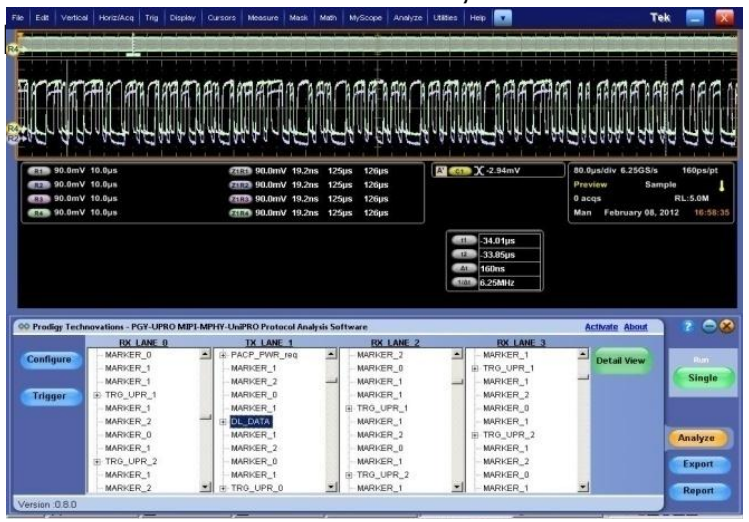
M-PHY Decodes: PGY-UPRO and PGY-LLI

UniPro and LLI Scope-Decodes

- PGY-UPRO and PGY-LLI are Decode Software re-sell from Prodigy Technovations.
  - Provides M-PHY UniPro and M-PHY LLI Protocol Decode and Analysis.
  - Runs on DPO/DSA/MSO70000/B/C/D models (6GHz and above), with P73xx or P75xx differential probing
  - License mechanism is same as scope options TEK-PGY-HDMI-PA-SW, or PDI-R.
  - Opt. ST6G Serial trigger is optionally required.



- Differentiation
  - SW Leverages ST6G serial trigger features
  - SW is First-to-Market

- Value proposition
  - SW Seamless Integration with all 70K scopes.
  - SW enables system level protocol debugging.
  - 4-Lane Automated Decoding, and Verifies CRC errors

- Datasheet &Trial Copy:
  - http://www.prodigytechno.com/PGY-MIPI-UPRO-LLI.htm **(Click Downloads)**

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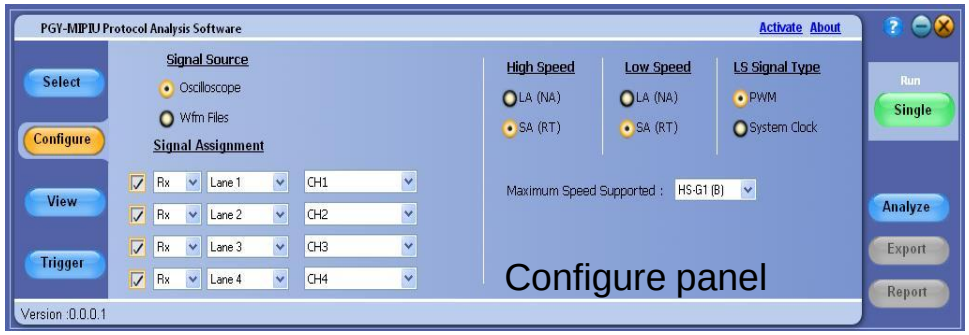
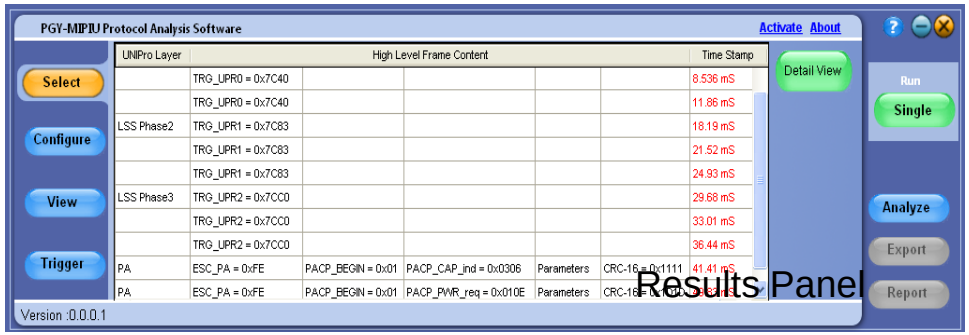
M-PHY Decodes: PGY-UPRO and PGY-LLI

- Decode Table with Messages &Time stamp
- Overlay of decoded messages on waveform
- Packet content details, with description
- Error packets
- State diagram shows Sequence of messages
  - → ACK frame/NACK frame with time stamp.
- Trigger on UniPRO message contents (Optional)
  - Trigger PA layer message
  - Trigger on Data link layer packet message





Agenda

- MIPI Technologies &Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI, &UniPro
  - Rx
- Summary, Q&A

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M-PHY Receiver Testing Challenges

- Different Signal Generation
  - PWM
  - NRZ
  - Reference clock
  - 8b/10b encoding
  - Differential & Common Mode DC
- Signal Impairments needs of Conformance Testing
  - Periodic Jitter
  - Random Jitter
  - ISI
  - S-parameter.

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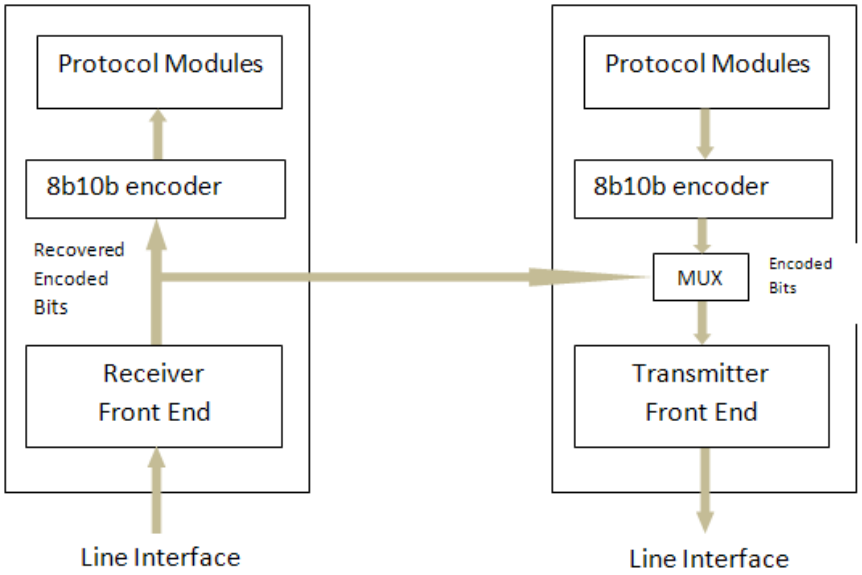
M-PHY Receiver Testing Challenges
Loopback mode BER testing

- Loopback mode is used for BER testing.
- In loopback, the receiver routes/ re-transmits the recovered MPHY signal via the transmitter. Receiver will not do decoding of 8b10b symbols.
- Loopback mode requires both transmitter and receiver to be configured to same TEST MODE and GEAR.



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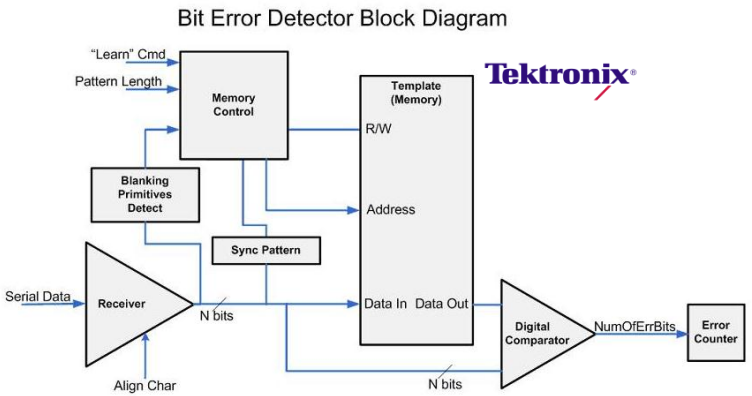
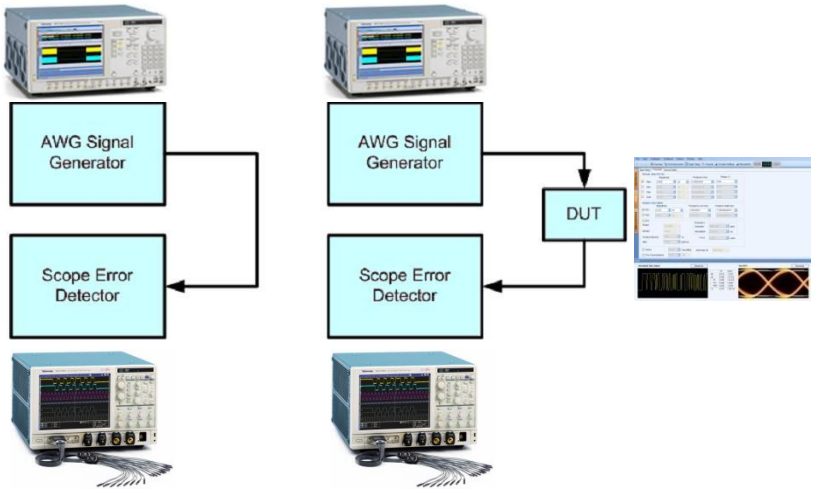
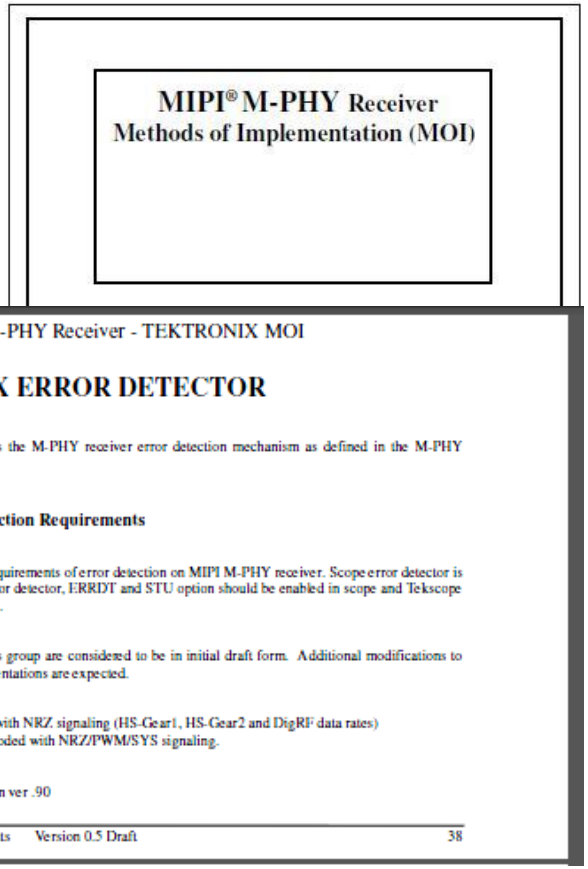
M-PHY Rx : Based on Scope built-in Error Detector

Scope-Integrated M-PHY BER using Opt.ERRDT Shipping Today



- 8B/10B Data:
  - Hardware Serial trigger: 1.25 Gb/s to 6.25 Gb/s
  - BER covers PRBS 312Mbs and above data rates.




MIPI® M-PHY Receiver
Methods of Implementation (MOI)

MIPI M-PHY Receiver - TEKTRONIX MOI

RX ERROR DETECTOR

Overview:
This section of tests verifies the M-PHY receiver error detection mechanism as defined in the M-PHY Specification.

GROUP 1: M-RX Error Detection Requirements

Overview:
This group of tests verifies various requirements of error detection on MIPI M-PHY receiver. Scope error detector is used for this purpose. For M-PHY error detector, ERRDT and STU option should be enabled in scope and Tekscope firmware v6.1.1.32 or later is required.

Status:
The test descriptions contained in this group are considered to be in initial draft form. Additional modifications to both the test descriptions and implementations are expected.

Pay Load:
Continuous PRBS 7/PRBS 9 Pattern with NRZ signaling (HS-Gear1, HS-Gear2 and DigRF data rates)
Custom burst pattern with 8b/10b encoded with NRZ/PWM/SYS signaling.

Note:
Please refer to the MPHY specification ver .90

MIPI M-PHY Rx MOI Measurements Version 0.5 Draft 38

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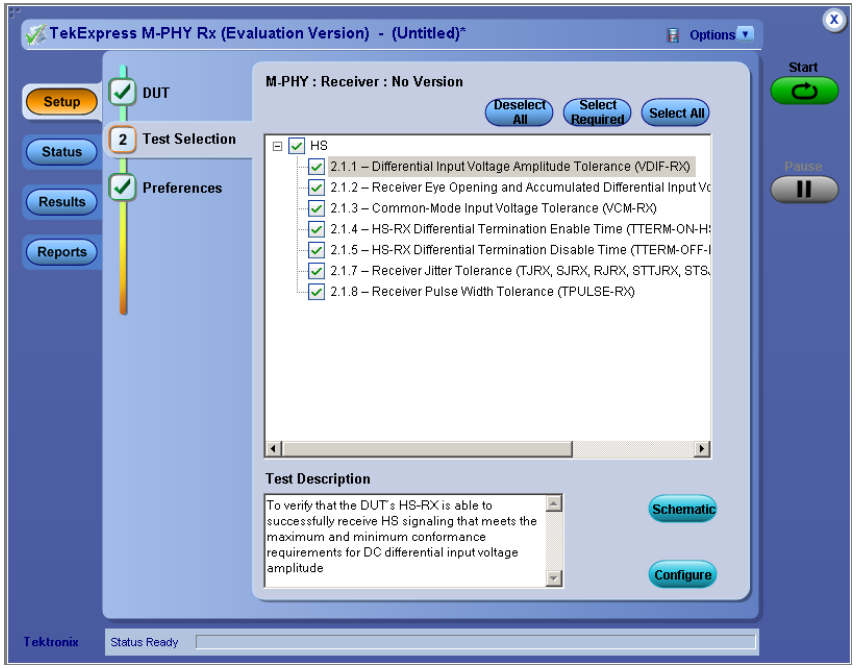
M-PHY Rx : Opt.M-PHYRX Automated Solution

- Opt.M-PHYRX
  - TekExpress (2.0) option for Fully-Automated receiver testing
  - Provides Conformance Testing
  - Based on Latest M-PHY Base Spec v1.0 &UNH's Conformance Test Suite
  - Runs on DPO/DSA70KB/C or MSO70K/C scopes
  - TekExpress framework is included.
- Differentiation
  - Simply 2-box setup.
  - Built upon Scope ErrorDetecror ERRDT.
  - Wide HS test coverage



- Value proposition
  - Test Reports with Pass/Fail summary, with Bit-Error counts

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M-PHY Rx : Opt.M-PHYRX Features

Feature	Benefit
Automated Testing	• Reduces the complexity of executing receiver tests • Reduces testing time • Enables you to test devices faster
Tests coverage	• Automated test setup has comprehensive coverage of high speed Rx tests, with Pre-created patterns.
Simple setup	• Simple Scope+AWG setup for a complete Receiver as well as Transmitter testing of M-PHY. • No other instrument is needed.
Integrated BER	• Leverages Bit-Error-Rate or Error-Count testing using Scope-Integrated ERRDT software in the background. • Scope Integrated ERRDT enables easy and quick setup, saves resource time and costs. • Scope ERRDT testing supports PRBS 312Mbps &above for all Gears. • No external/ extra hardware is required to perform BER testing
Signal Validation	• Check the acquired signal for correct Data rate/ Unit-Interval, MARKER0 (both positive and negative disparity), or one complete CRPAT (LLI specific),
Test reports	• Provides a Pass/Fail summary for all tests. •-Provides additional information such as test setup hardware and software details, Signal type selected, Bit Error, Execution time and User-comments.

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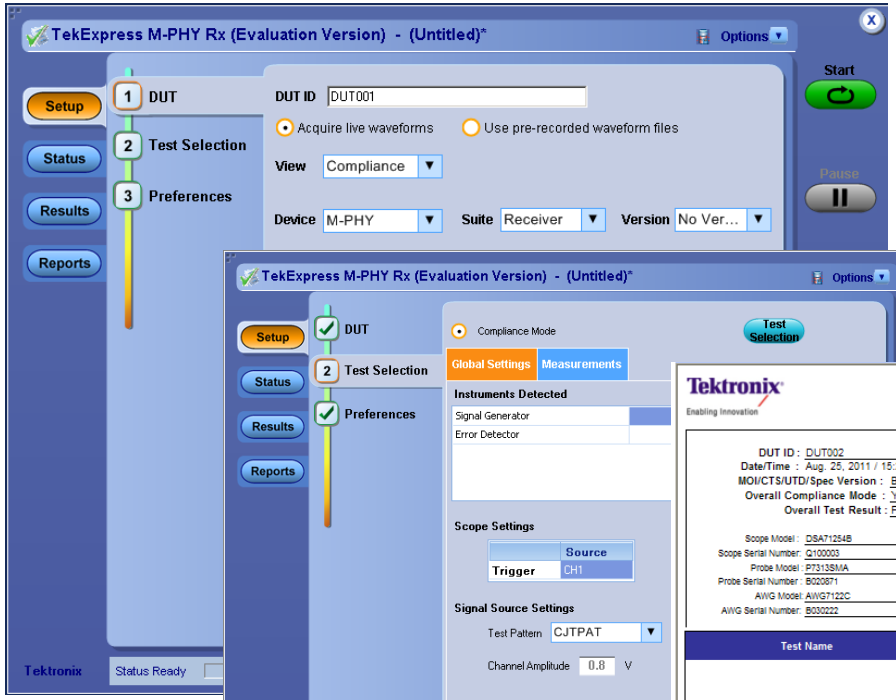
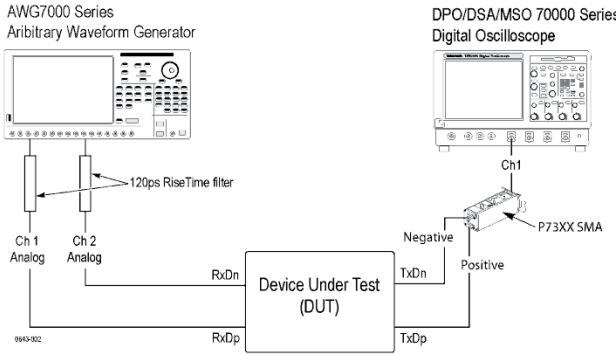
M-PHY Rx : Opt.M-PHYRX Features





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TekExpress MPHY-RX

Receiver Test Report

DUT ID : DUT002
Date/Time : Aug. 25, 2011 / 15:28:26
MOI/CTS/UTD/Spec Version : Base Spec 1.0
Overall Compliance Mode : Yes
Overall Test Result : Fail

Device Type : M-PHY
Execution Time : 31 Min

Scope Model : DSA71254B
Scope Serial Number : Q100003
Probe Model : P7313SMA
Probe Serial Number : B020871
AWG Model AWG7122C
AWG Serial Number : B030222

Scope F/W Version : 5.3.4 DEVBUILD
SPC, Factory Calibration : PASS:PASS
TekExpress Version : 1.0.0.19
DPOJET Version NA
AWG Firmware Version : 4.1.1.5

Test Name	Measurement Details	Pattern	Bit Error	Test Result	Limit	Execution Time
2.1.1 – Differential Input Voltage Amplitude Tolerance (VDIF-RX)	Gear 1 A Low Amplitude	CJTPAT	0	Pass	=0	3 Min
	Gear 1 A Average Amplitude - Informative	CJTPAT	0	N.A	=0	
	Gear 1 A High Amplitude	CJTPAT	0	Pass	=0	
2.1.2 – Receiver Eye Opening and Accumulated Differential Input Voltage (TEYE-RX. VDIF-ACC-RX)	Gear 1 A Average Amplitude	CJTPAT	0	Pass	=0	<1 Min
	Gear 1 A Low Amplitude - Differential Low	CJTPAT	0	Pass	=0	
	Gear 1 A Average Amplitude - Differential Low - Informative	CJTPAT	0	N.A	=0	
	Gear 1 A High Amplitude - Differential Low	CJTPAT	0	Pass	=0	
	Gear 1 A Low Amplitude - Differential High	CJTPAT	0	Pass	=0	
	Gear 1 A Average Amplitude - Differential High - Informative	CJTPAT	0	N.A	=0	
2.1.3 – Common-Mode Input Voltage Tolerance (VCM-RX)	Gear 1 A High Amplitude - Differential High	CJTPAT	0	Pass	=0	4 Min
	Gear 1 A Minimum Prepare	CJTPAT	0	Pass	=0	
2.1.4 – HS-RX Differential Termination Enable Time (TTERM-ON-HS-RX)	Gear 1 A Maximum Prepare	CJTPAT	0	Pass	=0	1 Min
	Gear 1 A Minimum Stall	CJTPAT	0	Pass	=0	
2.1.5 – HS-RX Differential Termination Disable Time (TTERM-OFF-HS-RX)	Gear 1 A Maximum Stall	CJTPAT	0	Pass	=0	1 Min
	Gear 1 A LTJ - Frequency 1	CJTPAT	206	Fail	=0	
2.1.7 – Receiver Jitter Tolerance (TJRX, SJRX, RJRX, STTJRX, STSJRX)	Gear 1 A LTJ - Frequency 2	CJTPAT	224507	Fail	=0	2 Min
	Gear 1 A LTJ - Frequency 3	CJTPAT	0	Pass	=0	
2.1.8 – Receiver Pulse Width Tolerance (TPULSE-RX)	Gear 1 A Minimum Pulse Width	CJTPAT	0	Pass	=0	1 Min
	Gear 1 B Low Amplitude	CJTPAT	0	Pass	=0	
2.1.1 – Differential Input Voltage Amplitude Tolerance (VDIF-RX)	Gear 1 B Average Amplitude - Informative	CJTPAT	0	N.A	=0	2 Min
	Gear 1 B High Amplitude	CJTPAT	0	Pass	=0	
2.1.2 – Receiver Eye Opening and Accumulated Differential Input Voltage (TEYE-RX. VDIF-ACC-RX)	Gear 1 B Average Amplitude	CJTPAT	0	Pass	=0	2 Min
	Gear 1 B Low Amplitude - Differential					

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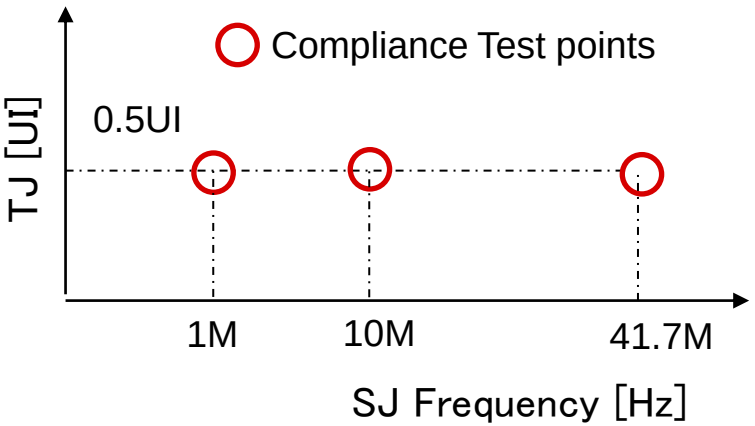
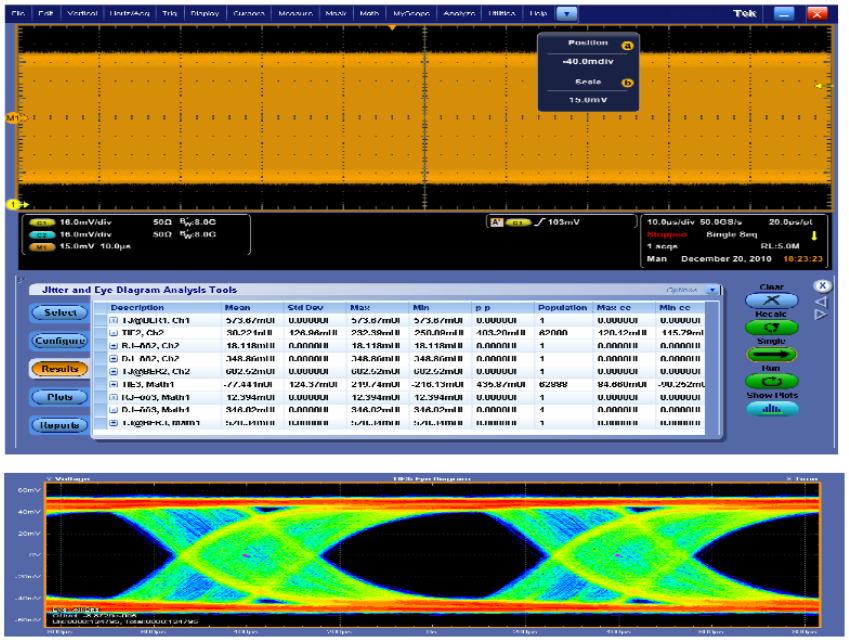
M-PHY Rx Test Setup: Test Impairments using AWG

Manual Setup/ Capabilities

- Supports Flexible signal impairments using Serial Express (optionally) for Characterization.
- Supports Jitter insertion and Pulse Width Modulation (PWM) as per the base specification v1.0.
- Supports testing the DUT in both loopback and non-loopback mode.



1. Long Term Jitter based pattern for PRBS7 continuous Pattern
   - Sinusoidal Jitter Frequency (SJ1) =1 MHz



Example Jitter generation using AWG &Cable impairments, as per the specs.

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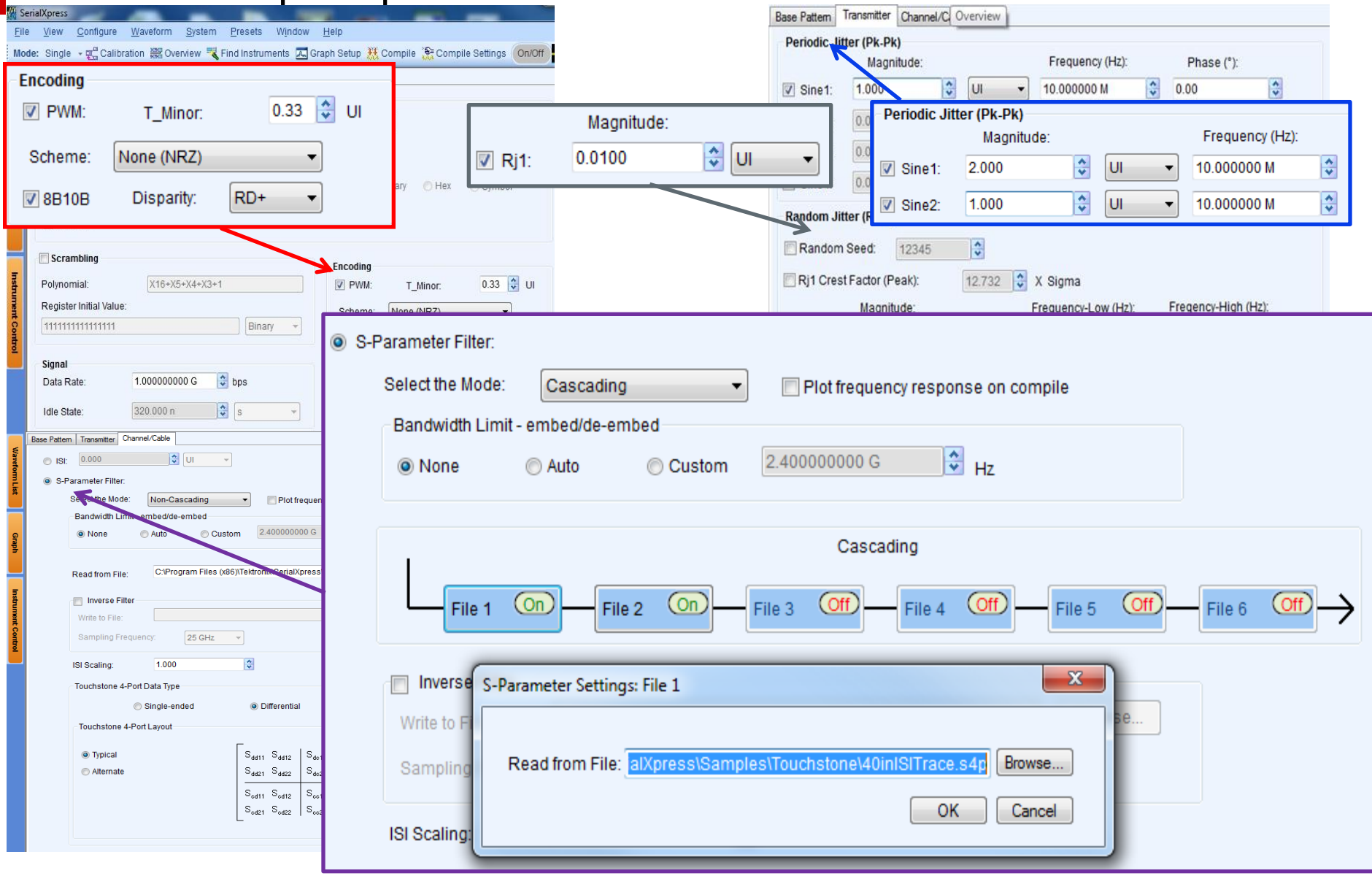
M-PHY Rx Test: Test Impairments using SerialXpress

Manual Setup/ Capabilities



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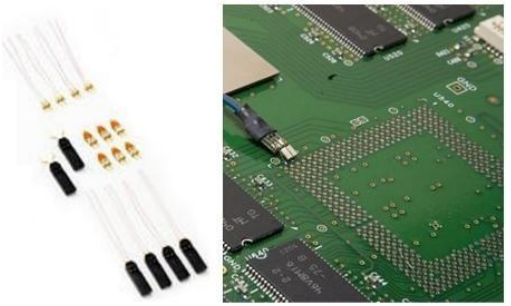
M-PHY Tx &Rx Recommended Test Setup (www.tek.com/MIPI)

- Scopes
  - DPO70604/B/C or above, for HS-Gear1 Only (Tx &Rx).
  - DPO70804/B/C or above, for HS-Gear1&2 Only (Tx &Rx)
  - DPO71254/B/C or above, for All HS-Gears (Rx Only)
  - DPO72004/B/C or above, for All HS-Gears (Tx &Rx).
- Probes
  - 2x P73xxSMA/P73xx, for Tx HS upto Gears2, or 2x P75xx with P75LRST for Tx HS upto Gear3.
  - 2x P73xxSMA/P73xx, for Tx PWM All Gears.
  - 1x P73xxSMA, for Rx.
- Signal Generators for Rx
  - AWG7082C, AWG7102 or above, for HS-Gear1 Only.
  - AWG7122C without Interleave, for HS-Gear1&2 Only.
  - AWG7122C with Interleave (option 06), for All HS-Gears.
- Software
  - New Opt.M-PHYTX Transmitter Automated Solution (Opt.DJA is pre-requisite).
  - New PGY-UPRO Protocol Decode (Opt.ST6G optionally required).
  - New PGY-LLI Protocol Decode (Opt.ST6G optionally required).
  - Opt.M-PHYRX Receiver Automation (Opt.ERRDT is pre-requisite).
  - Opt.SR-810B, for 8b-10b Decode
  - MPHYVIEW, for DigRFv4 Protocol Decode
  - Optional: Opt.M-PHY Essentials based on DPOJET
  - Optional: SerialXpress for custom-patterns using AWG



P7380 probe used with a probe-tip

- Fixtures
  - As MIPI is chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected. For live-setups: No Fixtures required. For non-live setups UNH-IOL Termination boards expected to be available soon

M-PHY Rx Recommended Test Setup – Continued

- Recommended Accessories, for opt.M-PHYRX Receiver Automation setup
  - 2x Matched pair of SMA cables
  - 1x GPIB Cable
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors

- Optional: Accessories for Rx “custom-patterns” using SerialXpress (manual setup)
  - 2x Matched pair of SMA cables, , for AWG custom patterns creation
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors
  - 2x BiasTee (part number 5542 from Pico Second), for AWG Interleave Option (for HS-Gear3)
  - 2x TCA-SMA Connectors, for AWG custom patterns creation
  - Option 01 –Memory expansion to 64 M enabled on AWG
  - Option 08 – Fast Sequence Switching enabled on AWG
  - Option 09 – Subsequence and Dynamic Jump enabled on AWG.

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M-PHY Tx Setup Recommendation (Rationale)

M-PHY Tx HS Mode Requirement				
GEAR	Data Rate(bps)	Highest frequency component(Hz)	5th Harmonic frequency(Hz)	Minimum transition time(pS)
1A	1248000000.00	624000000.00	3120000000.00	80.128
1B	1457600000.00	728800000.00	3644000000.00	68.606
2A	2496000000.00	1248000000.00	6240000000.00	40.064
2B	2915200000.00	1457600000.00	7288000000.00	34.303
3A	4992000000.00	2496000000.00	12480000000.00	20.032
3B	5830400000.00	2915200000.00	14576000000.00	17.151

M-PHY Tx PWM Mode Requirement					
	Data Rate				
Gear	Lowest Data Rate	Highest Data Rate	Highest Frequency Component	5th Harmonic of highest frequency component	RT/FT(Sec)
0	1.00E+04	3.00E+06	1.3500E+07	6.7500E+07	2.33E-08
1	3.00E+06	9.00E+06	1.6071E+07	8.0357E+07	7.78E-09
2	6.00E+06	1.80E+07	3.2143E+07	1.6071E+08	3.89E-09
3	1.20E+07	3.60E+07	6.4286E+07	3.2143E+08	1.94E-09
4	2.40E+07	7.20E+07	1.2857E+08	6.4286E+08	9.72E-10
5	4.80E+07	1.44E+08	2.5714E+08	1.2857E+09	4.86E-10
6	9.60E+07	2.88E+08	5.1429E+08	2.5714E+09	2.43E-10
7	1.92E+08	5.76E+08	1.0286E+09	5.1429E+09	1.22E-10

SCOPES Recommendation for M-PHY Tx - High-Speed Tests								
		DPO/DSA/MSO 70604, B and C	DPO/DSA/MSO 70804, B and	DPO/DSA/MSO 71254, B and	DPO/DSA/MSO 71604, B and	DPO/DSA/MSO 72004, B and	DPO/DSA 72504D	DPO/DSA 73304D
HS Gear	Requirements from Specification	BW = 6 GHz, RT = 45 pS	BW = 8 GHz, RT = 34 pS	BW = 12.5 GHz, RT = 22 pS	BW = 16 GHz, RT = 17 pS	BW = 20 GHz, RT = 14 pS	BW = 25 GHz, RT = 12 pS	BW = 33 GHz, RT = 9 pS
G1A	DR = 1248 Mbps, RT=80.128 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G1B	DR = 1457.6 Mbps, RT= 68.606 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G2A	DR = 2496 Mbps, RT= 40.064 pS	No	Yes	Yes	Yes	Yes	Yes	Yes
G2B	DR = 2915.2 Mbps, RT= 34.303 pS	No	Yes	Yes	Yes	Yes	Yes	Yes
G3A	DR = 4992 Mbps, RT= 20.032 pS	No	No	No	No	Yes	Yes	Yes
G3B	DR = 5830.4 Mbps, RT= 17.151 pS	No	No	No	No	Yes	Yes	Yes

PROBES Recommendation for M-PHY Tx - High-Speed Tests									
		P7360A	P7380A	P7313	P7506	P7508	P7513A	P7516	P7520
HS Gear	Spec Requirement	BW = 6 GHz, RT = 52.5 pS(20/80)	BW = 8 GHz, RT = 41.25 pS(20/80)	BW = 13 GHz, RT = 30 pS(20/80)	BW = 6 GHz, RT = 56.25 pS(20/80)	BW = 8 GHz, RT = 41.25 pS(20/80)	BW = 13 GHz, RT = 30 pS(20/80)	BW = 16 GHz, RT = 24 pS(20/80)	BW = 20 GHz, RT = 21.75 pS(20/80)
G1A	DR = 1248 Mbps, RT=80.128 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G1B	DR = 1457.6 Mbps, RT= 68.606 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G2A	DR = 2496 Mbps, RT= 40.064 pS	No	No	Yes	No	No	Yes	Yes	Yes
G2B	DR = 2915.2 Mbps, RT= 34.303 pS	No	No	Yes	No	No	Yes	Yes	Yes
G3A	DR = 4992 Mbps, RT= 20.032 pS	No	No	No	No	No	No	No	Yes
G3B	DR = 5830.4 Mbps, RT= 17.151 pS	No	No	No	No	No	No	No	Yes

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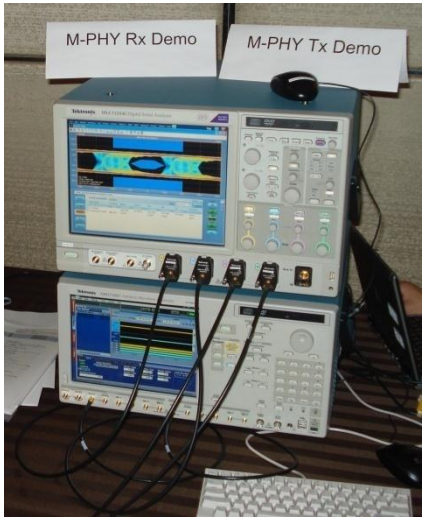
Tektronix M-PHY Testing Solution

- Industry **1st** tools
  - Tektronix announced M-PHY Measurements &Decode tools, in September 2010, during MIPI Alliance Athens F2F.
- Simply **"2-Box"** Solution : Just a Scope + AWG needed for Tx &Rx.
- PSD (Power Spectral Density) measurements on Scope are IP-Patented



Industry 1st M-PHY Tools Demonstrated
at MIPI-Alliance F2F, Athens, Sept'10 and Osaka, March'11

cf.us.biz.yahoo.com/iw/100927/0666379.html?.v=1&printer=1

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Press Release Source: Tektronix

Tektronix Introduces Industry's First Test Tools for MIPI M-PHY Debug and Validation

Monday September 27, 9:00 am ET

Support for New High-Speed M-PHY Specification Includes DPOJET toolset, and M-PHY DigRFv4 Decode for Tektronix Oscilloscopes

BEAVERTON, OR--(Marketwire - 09/27/10) - Tektronix, Inc., the world's leading manufacturer of oscilloscopes, today introduced the industry's first testing tools for the MIPI® Alliance M-PHY standard, allowing customers to immediately get started with performance verification and debug for this important new specification using Tektronix DPO/DSA/MSO70000B Series oscilloscopes.

The announcement was made in conjunction with the MIPI Alliance All-Members meeting taking place this week in Athens, Greece. The M-PHY specification is an essential part of the MIPI Alliance's vision for more efficient high-speed interfaces on mobile devices. Compared to the current D-PHY specification, M-PHY supports faster chip-to-chip

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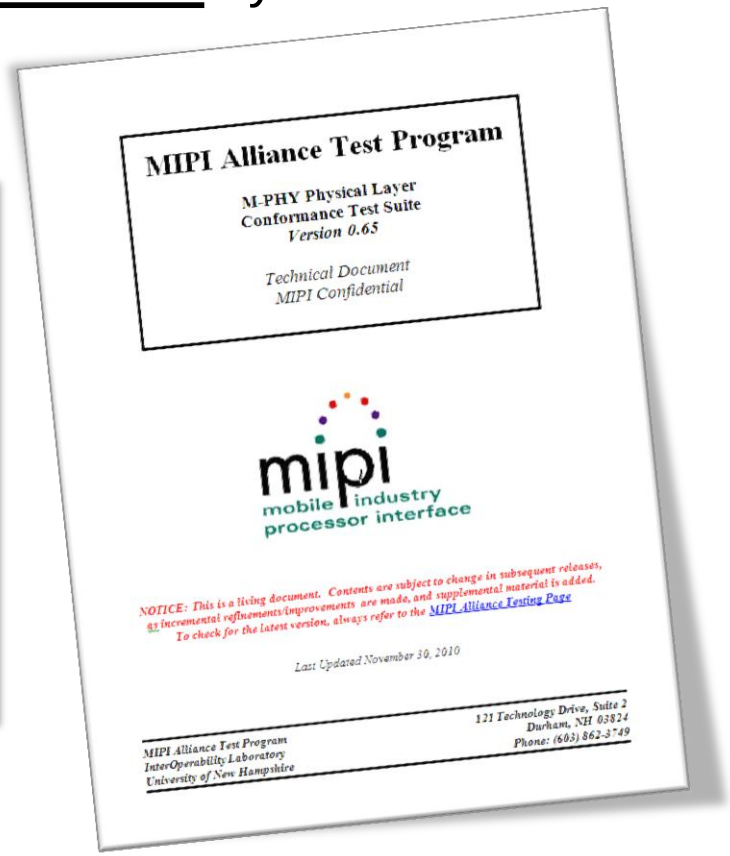
Tektronix M-PHY Testing Solution

Customer-Proven &Highly-Reliable Solution

- Example customer video using Tektronix M-PHY solution: http://www.synopsys.com/dw/ipdir.php?ds=mipi_m-phy .

- M-PHY CTS Test Spec **"Co-Authored"** by Tektronix



iol mipi alliance Tektronix

Agenda

- MIPI Technologies &Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx
  - Scopes-Decodes: 8b-10b, DigRF, LLI, &UniPro
  - Rx
- Summary, Q&A

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Summary - Tektronix MIPI PHY Solutions

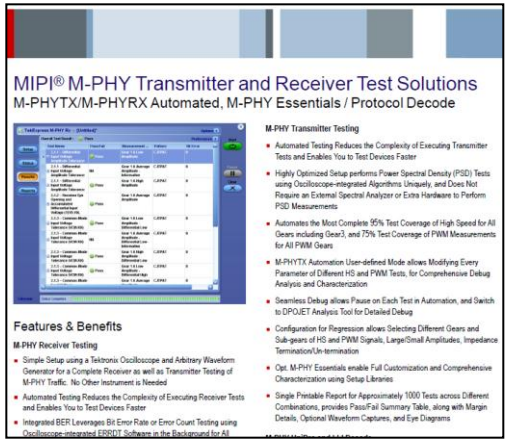
www.Tek.com/MIPI

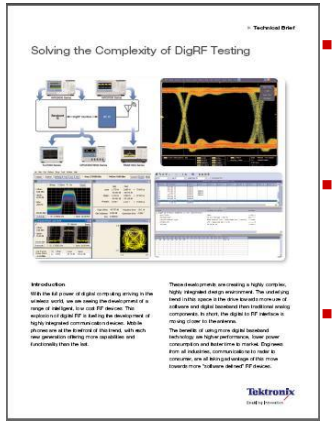
- Tektronix is 1st to Market for M-PHY testing, announced in Sept, 2010
- Tektronix is a **Contributor Member** of the MIPI Alliance
- Tektronix is actively-participating in MIPI PHY &other Working Groups
- Tektronix has a close working relationship with UNH-IOL

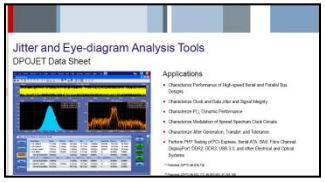
Tektronix MIPI Solutions Portfolio (www.Tek.com/MIPI)				
Standard	**Physical Layer Trasmitter**	**Physical Layer Receiver**	**Protocol Layer Analysis**	**Stimulus**
D-PHY, DSI, CSI-2	1x DPO7354 or DPO70404B Oscilloscope	1x PG3ACAB Pattern Generator	1x TLA7012 ot TLA7016 TLA Mainframe	1x PG3ACAB or PG3AMOD
	4x P7240, TAPxx, P6245 or P6249 probes, OR	1x P332 D-PHY Probe for PG	1x LA ModuleTLA7BBx	1x P331 D-PHY Probe for PG
	4x P73xx, or TDP3500 probes (3x if Clock-Continuous)	1x PGRemote SW	1x P6980 LA Probe	1x PGRemote SW
	1x TEKEXP Opt.D-PHYTX, or DPOJET Opt.D-PHY	1x AWG7082C or above	1x D-PHY to P6980 Adapter	
	1x Opt.SR-DPHY for CSI/DSI Decode	1x D-PHY Coupler	1x CSI or DSI decode SW for TLA (Free)	
	No Fixtures for Live-Setups. UNH Fixtures for Non-Live.			
M-PHY, DigRFv4, DSI-2, CSI-3	1xDPO72004 for upto HS-Gear3	1x AWG7122C with opt#6 for Gear3		
	2x P73xx, P73xxSMA, P75xx Probes per Lane	1x Opt.M-PHYRX Receiver SW		
	1x Opt.M-PHY for Tx Debug, Analysis &Validation	1x SerialXpress SW		
	1x Opt.MPHYVIEW, Opt.SR-810B, LLI or UniPro Decode			
	No Fixtures for Live-Setups. UNH Fixtures for Non-Live.			

Additional References

www.Tek.com/MIPI







www.Tek.com/MIPI :

- M-PHY Datasheet (61W-27714-2)
  - http://www.tek.com/datasheet/mipi%C2%AE-m-phy-transmitter-and-receiver-test-solutions
- D-PHY Datasheet (61W-25621-4)
  - http://www2.tek.com/cmswpt/psdetails.lotr?ct=PS&cs=psu&ci=17415&lc=EN
- D-PHY/ CSI/ DSI Application Note
  - http://www2.tek.com/cmswpt/tidetails.lotr?ct=TI&cs=apn&ci=17638&lc=EN
- DigRF Application Note
  - http://www2.tek.com/cmswpt/tidetails.lotr?ct=TI&cs=tbr&ci=11854&lc=EN
- Opt.M-PHY MOI
  - http://www.tek.com/method-implementation/mipi%C2%AE-m-phy-methods-implementation
- Opt. D-PHY MOI
  - http://www.tek.com/method-implementation/mipi-d-phy-test-method-implementation-moi
- PGY-UPRO and PGY-LLI Datasheet
  - http://www.prodigytechno.com/PGY-MIPI-UPRO-LLI.htm
- MPHYVIEW DigRFv4 Decode Datasheet &Manual
  - http://www.movingpixel.com/MIPI_MPhy.html#MIPI_MVu
- MIPI Alliance Video on Tek Solutions
  - http://www.youtube.com/watch?v=Mf9rv-X2YG4&feature=channel

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Additional References, at www.mipi.org

Tektronix Contributed Literature at MIPI Alliance Official website

- MIPI Conference Presentations page
  - Tektronix - Test Challenges and Strategies: http://www.mipi.org/learning-center/presentations ,
  - http://www.mipi.org/sites/default/files/tutorials/Tektronix%20-%20Test%20Challenges%20and%20Strategies.pdf
- MIPI Member-to-member presentations:
  - Tektronix Algorithm for identifying D-PHY signal regions: http://www.mipi.org/allmembers
- Contributed Articles page:
  - Tektronix article on Physical Layer Test Strategies for MIPI Standards: http://www.mipi.org/news-events/contributed-articles
- MIPI Test Demos page
  - Tektronix Demos: http://www.mipi.org/content/test-forum-days-company-demos
- MIPI Test Forum Days page
  - Tektronix Presentations: http://www.mipi.org/content/mipi-alliance-test-forum-days
- Member press releases:
  - Mobile Asia Expo: http://www.mipi.org/news-events/mobile-asia-expo
  - Tektronix M-PHY TxRx most-cost-effective solution: http://www.mipi.org/news-events/member-press-releases
  - Tektronix D-PHY one-button automation: http://www.mipi.org/news-events/member-press-releases?page=1
- Member Product Spotlights:
  - Tektronix MIPI solutions: http://www.mipi.org/member-directory/tektronix-inc

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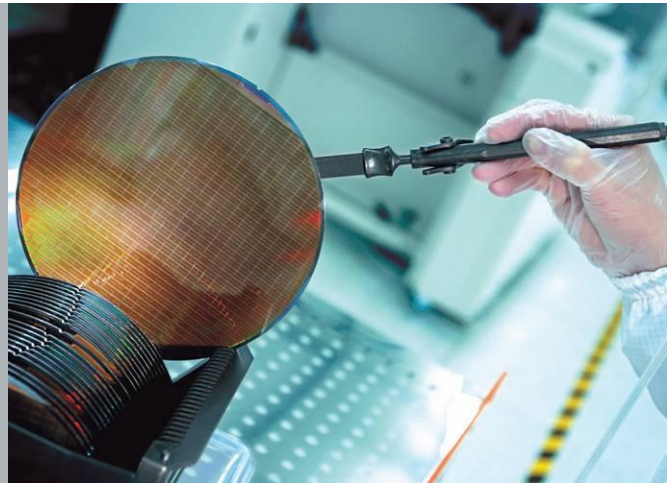
Q &A

Thank you



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Backup

D-PHY Tx Field Demo Setup

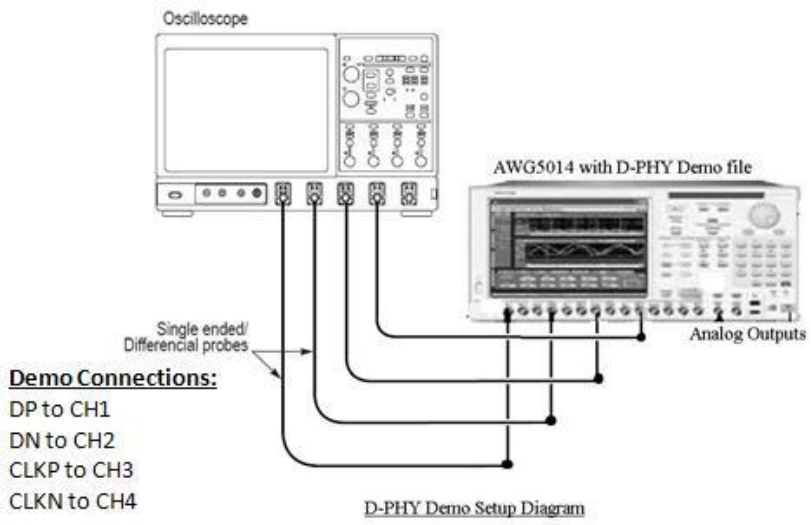
For both Opt.D-PHYTX and Opt.D-PHY

Option#1:Using AWG:

- 1x DPO7354 or Higher BW Scope
- Scope Software:
  - Opt.D-PHYTX with TEKEXP, for Automation demo
    - 10 Free Trial Runs with no time bound
    - Demo Keys: www.cse.tek.com/CSBU/opt_key/opt_key_demo_upgrade/
  - Or, Opt.D-PHY with DPOJET, for Debug
- 1x AWG5014
- 4x BNC to BNC cables for 7K &70K
- 4x TCA to BNC Adapters for 70Ks.
- Demo Kits from Salesnet
  - MIPI D-PHY Measurements Demo Guide
  - D-PHYTX TekExpress Product Demo Demo Guide
- Optional: Keithley RF switch for Multi-lane demo

Option#2: Using Reference-Waveforms:

- 1x DPO7354 or Higher BW Scope
- Scope Software:
  - Opt.D-PHYTX with TEKEXP, for Automation
  - Opt.D-PHY with DPOJET, for Debug demo.
- Demo Kits from Salesnet
  - MIPI D-PHY Measurements Demo Guide
  - D-PHYTX TekExpress Product Demo Demo Guide



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M-PHY TX and M-PHY Decodes Demo Kit

Opt.M-PHYTX, PGY-UPRO and PGY-LLI

TX Demo Setup Using AWG Only:

- 1x DPO70604B or Higher BW Scope
- 1x AWG7082C or AWG7122B/C
- 2x SMA-to-SMA cables for **Tx** Demo
- Scope Software:
  - Opt.M-PHYTX with Opt.DJA for **Tx** demo
- DemoKit - M-PHY**TX Automation Demo**
  - M-PHY_TxRx_Demo_Kit on Salesnet MIPI page includes TxRx Demo Guide, and AWG waveform files.

Decode Demo Setup Using AWG Only:

- 1x DPO70604B or Higher BW Scope
- 1x AWG7082C or AWG7122B/C
- 2x SMA-to-SMA cables for **Tx** Demo
- Scope Software:
  - PGY-UPRO or PGY-LLI for **Decode** demo
- Demo Kit – **Decodes Demo**
  - **PGY_UPRO_LLI demo kit** on Salesnet MIPI page includes AWG waveform files for use in PGY-UPRO and PGY-LLI Decode Demo.
  - PGYUPRO and PGY-LLI provides 10 free trial runs to be used within 7 days trial period. A trial copy of PGY-UPRO and PGY-LLI software is available from, **http://www.prodigytechno.com/PGY**-MIPI-UPRO-LLI.htm (Click Downloads). Permanent license keys will be provided for demo scopes. Also, the software downloader includes/installs a set of pre-recorded waveforms that can be used for offline demos.

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M-PHY **TxRx** and D-PHY-Decode Field Demo Setup

For Opt.M-PHY, Opt.M-PHYRX and Opt.SR-DPHY.

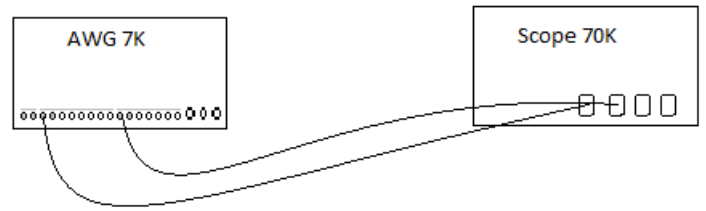
M-PHY **TxRx** Demo Using AWG Only:

- 1x DPO70604 or Higher BW Scope
- 1x AWG7082C or AWG7122B/C.
- 2x SMA-SMA cables for **Tx** Demo
- 1x P7313 SMA and matched pair SMA cable for **Rx** Demo
- Scope Software:
  - Opt.M-PHY with DPOJET, for **Tx** demo
  - Opt.M-PHYRX with ERRDT for **Rx** demo
  - MPHYVIEW, for **Decode** demo
- For Opt.M-PHYRX **Automation** demo
  - Use M-PHYRX AWG patterns from Tek.com directly with Opt.M-PHYRX.
- For **MOI Signal impairments &Characterization** demo,
  - Opt.M-PHY DPOJET Measurements, and Receiver ErrorDetector Demo Kit Demo Guide(M-PHY_TxRx_Demo_Kit.zip) file on Salesnet MIPI page is needed. It includes,
  - M-PHY_TxRx_DemoGuide.doc.
  - ERRDT scripts
  - Rx Calibration setupfiles
  - Rx Measurement setupfiles

D-PHY Decode Demo Using DPO3 Demo Board:

- Demo Kit from Salesnet
  - Opt.SR-DPHY Demo Guide Demo Guide file from Salesnet MIPI page
  - Opt. SR-DPHY_MIPIdecode_Demo Video Demo Guide file from Salesnet MIPI page

M_PHY Setup



- 2x SMA to SMA cables for Tx Demo
- 1x P7313 SMA and matched pair SMA cable for Rx Demo

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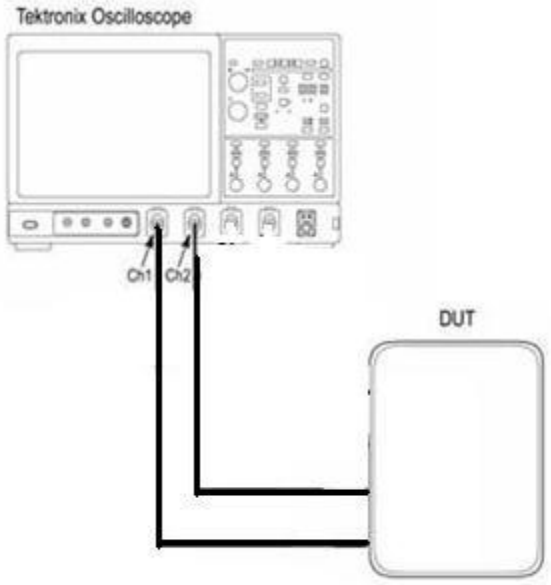
M-PHY Tx : Opt.M-PHY Additional Information

100% High-Speed Tests Coverage

Test Group	Test Name	Symbol
Spec/Limits Update	Migrate Limits for Latest Spec	All R1 &R2 tests
HS-LargeSwing	Differential Peak to Peak voltage	$V_{DIF\_PK\_L\_NT\_TX}$
		$V_{DIF\_PK\_L\_RT\_TX}$
		$V_{DIF\_PK\_S\_NT\_TX}$
		$V_{DIF\_PK\_S\_RT\_TX}$
	Common Mode Voltage	$V_{CM\_S\_TX}$
		$V_{CM\_L\_TX}$
	Slew rate in fastest slewrate state	SRDIF_TX[1]
	Transmitter Pulse width	TPULSE_TX
	Eye Opening	TEYE_TX
	deterministic jitter	DJTX
	total jitter	TJTX
	total jitter for short lane	TJTX
	short term jitter	STJTX
	Resolution of slew rate states	ΔSRDIF_TX
	Power Spectral Density/ Magintude	PSD
HS-SmallSwing	Differential Peak to Peak voltage	$V_{DIF\_PK\_L\_NT\_TX}$
		$V_{DIF\_PK\_L\_RT\_TX}$
		$V_{DIF\_PK\_S\_NT\_TX}$
		$V_{DIF\_PK\_S\_RT\_TX}$
	Common Mode Voltage	$V_{CM\_S\_TX}$
		$V_{CM\_L\_TX}$
	Slew rate in fastest slewrate state	SRDIF_TX[1]
	Transmitter Pulse width	TPULSE_TX
	Eye Opening	TEYE_TX
	deterministic jitter	DJTX
	total jitter	TJTX
	total jitter for short lane	TJTX
	short term jitter	STJTX
	Resolution of slew rate states	ΔSRDIF_TX
	Power Spectral Density/ Magintude	PSD



Single-Ended/Differential (Two per Lane)

M-PHY Tx Test Setup

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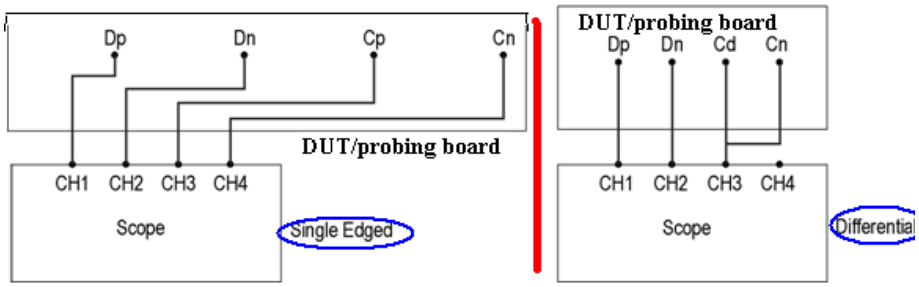
D-PHY Tx : Opt.D-PHYTX Test Solution
Additional Features &Benefits

Feature	Benefit
Setup Customization	• Modify the test setup as per the DUT configuration. • Unit Intervals are automatically calculated based on the DUT datarates.
Characterization/ Margin Testing	• Allows custom-limits or limits-editing to perform Margin testing. • Performs characterization of your design.
Detailed Test-Reports	• Provides Pass/Fail summary table • Provides margin details on each test • Provides "Zoon-In" screenshots of the cursors placement for each test. • Provides "single-printable" consolidated report for all tests.
Error Handling	• Test reports with Errors/ Exceptions information help identify Setup/ Acquisition issues quickly
Flexible probing	• Probe using Differential, Trimode, or Single-ended probes.
Offline/ Remote Analysis	• Perform measurements using either live or pre-acquired waveforms • Allows remote execution of tests.
Flexible probing	• Probe using Differential, Trimode, or Single-ended probes.

Opt.D-PHYTX and Opt.D-PHY

Testing Recommendations

- D-PHY Tx Test Setup, Using 4xSE/ 4xDiff probes or 3x Diff probes.
  - Dp and Dn each connect to1xprobe (SE/Diff).
  - If clock is Non-Continuous, **2xDiff** probe are needed for Cp &Cn.
  - If clock is Continuous, **1xDiff** probe is sufficient for Cp &Cn.



Feature	Opt.D-PHY (D-PHY Essentials)	Opt.D-PHYTX (D-PHY Automated)
Pre-Requisite tools	DPOJET	TEKEXP
Automatic tests based on test group, and selected probes.		✓
Single button execution for all measurements		✓
Configurable setup and Editing of test limits	✓	✓
Detailed or Summary Reports	Detailed Only	Detailed &Summary
Automatically Save Test Reports and Waveforms		✓
D-PHY Specific User Interface		✓
Testing Recommendation	Debug , Analysis &Characterization	Conformance, Verification, &Characterization

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M-PHY Rx - ERRDT

Unique differentiators versus a BERT

- Ability to Ignore/Reject AlignPrimitives/ SkipOrderSets
- Ability to Learn the Test Pattern from the signal (SATA Bit Error only)
- Ability to Trigger on Errors and Display the Signal Waveform
- Ability to Debug other channels when an error occurs
- Ability to provide Bit, Symbol, Illegal Character, and Disparity Error information

The following table summarizes the effectiveness and limitiations of various types of Error Detection.

Error Type	Effectiveness	Error Rate	Resolution	Limitations
Character	90-95%	Error Characters / Monitored Characters	Character	Can miss errors if a character is changed to a legal character.
Frame	100% (finds all errors)	Error Frames / Monitored Frames	Frame	Many bit errors can equal 1 frame error
Symbol	100% (finds all errors)	Error Symbols / Monitored Symbols	Symbol	Several bit errors can equal 1 symbol error
Bit	100% (finds all errors)	Error Bits / Monitored Bits	Bit	Pattern length limited by memory depth

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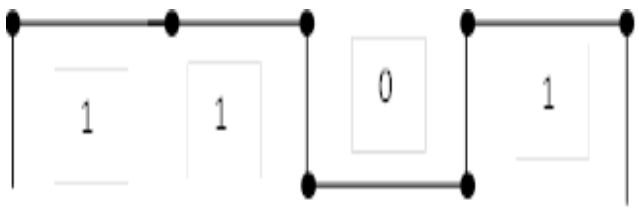
M-PHY Transmitter Test Challenges

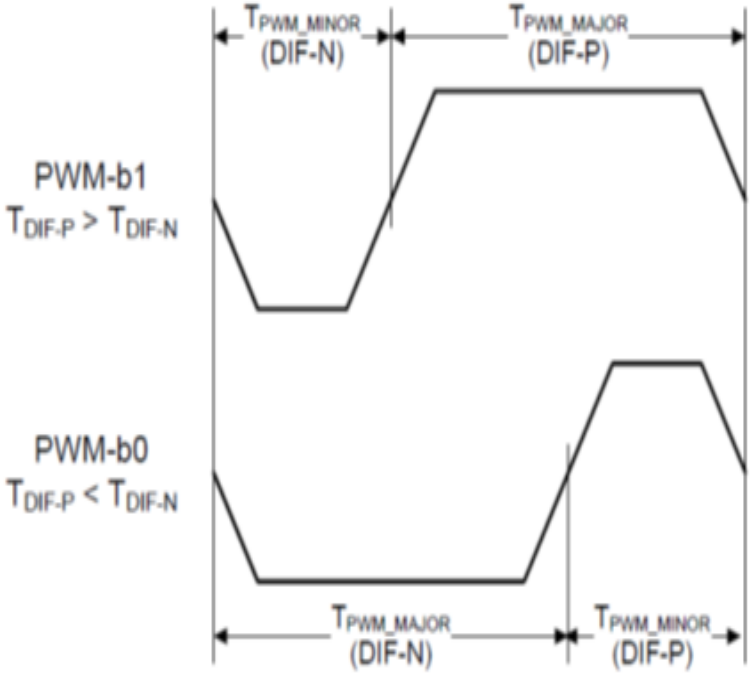
PWM Signal Analysis

- NRZ - High Speed Mode

(HS- Mode)



- PWM - Low Speed Mode (LS-Mode)



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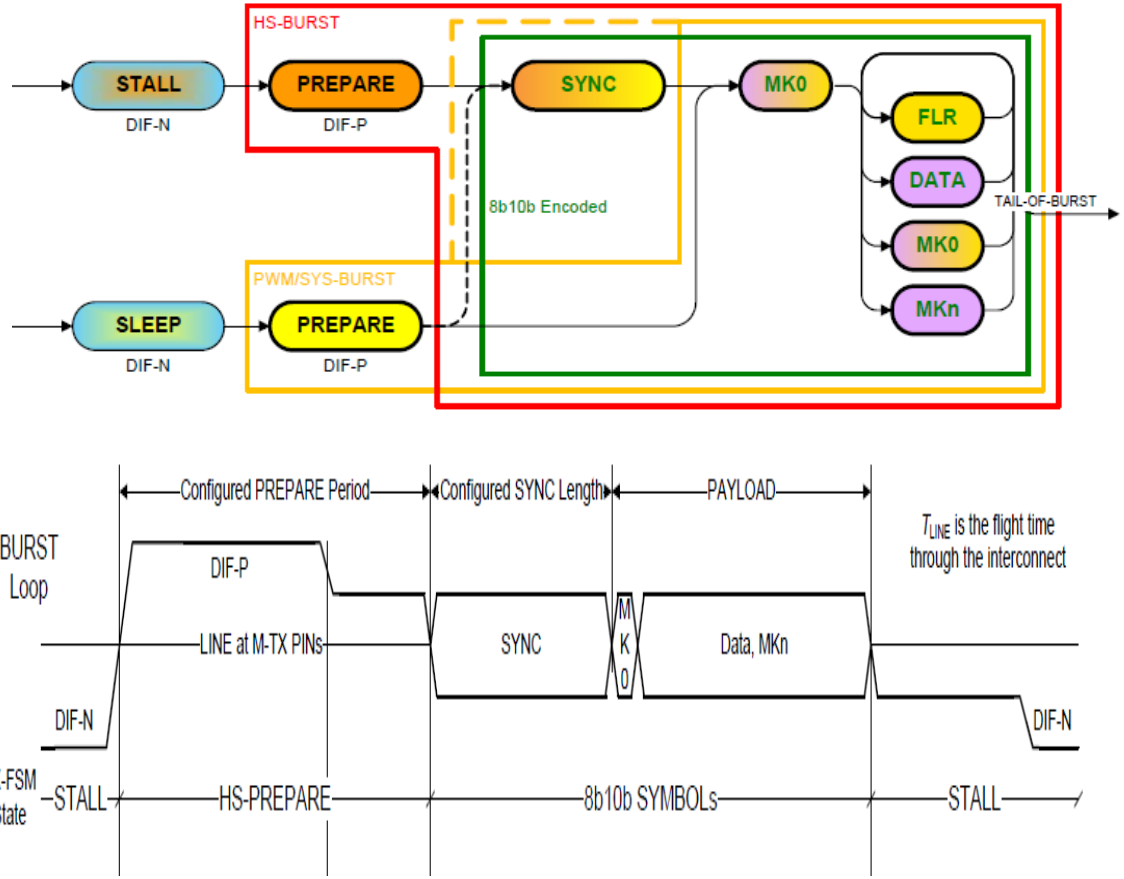
M-PHY Transmitter Test Challenges
Identifying Burst States



[Ref1]

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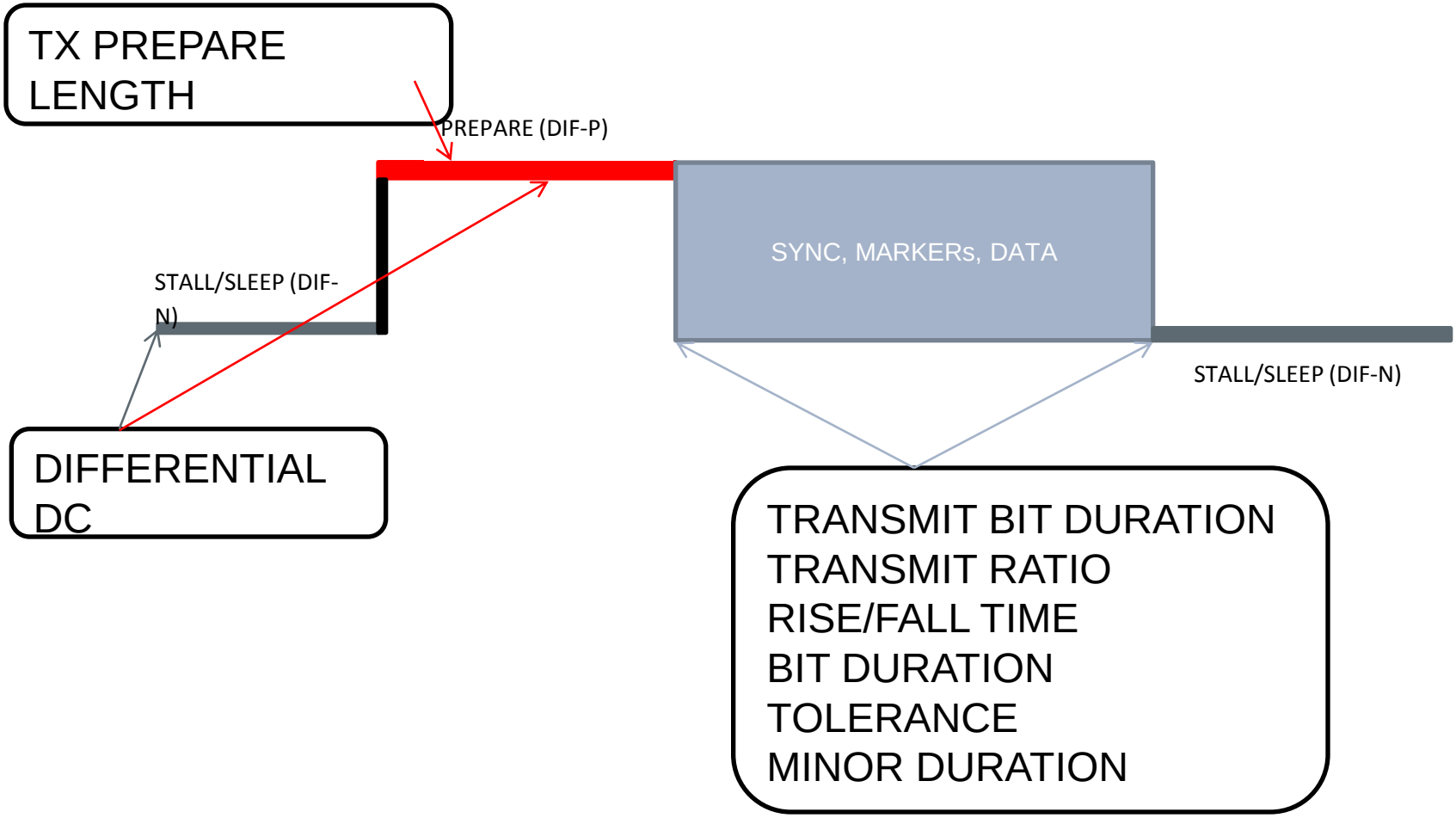
M-PHY Transmitter Test Challenges

Burst States & Conformance Tests



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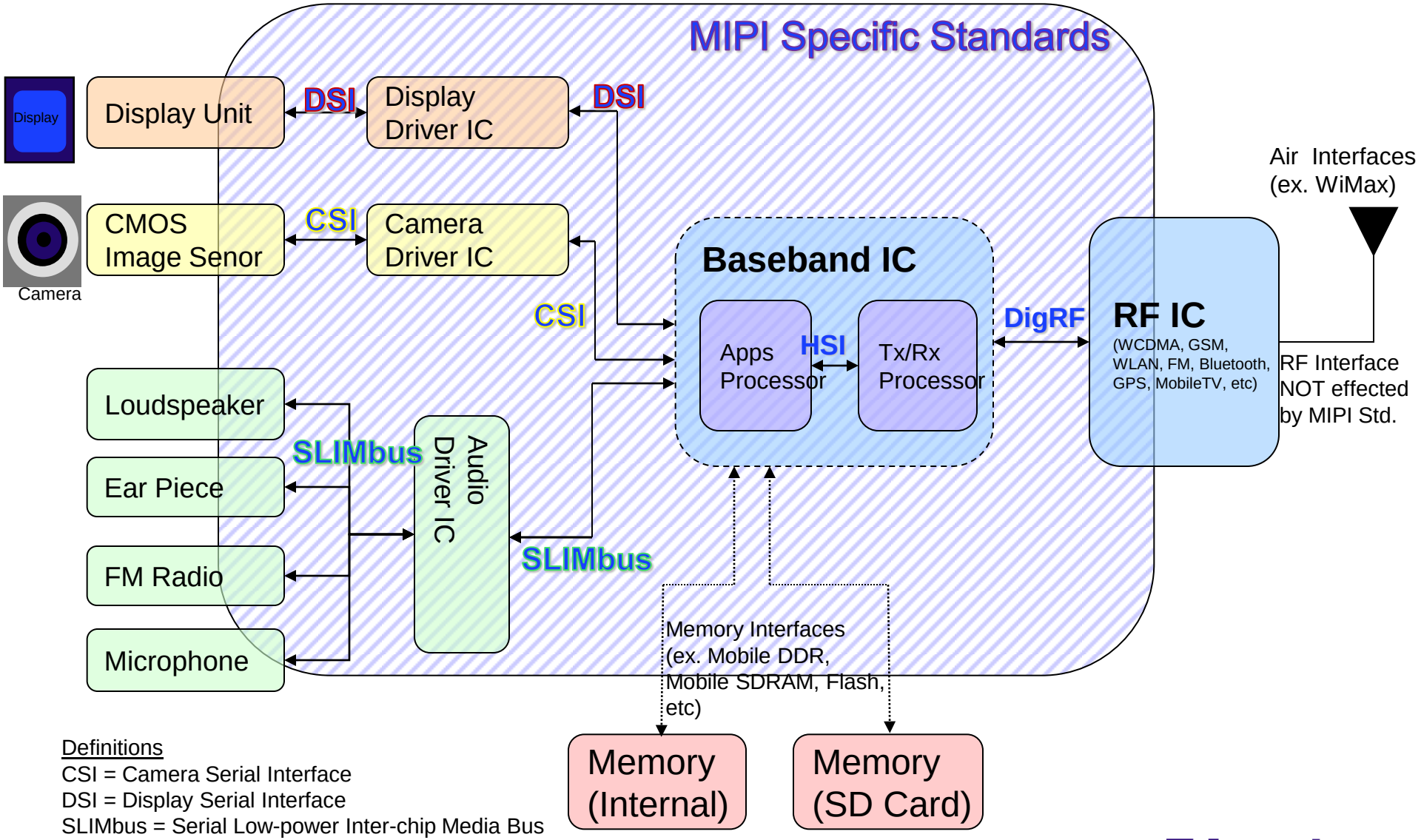
MIPI Standards Overview

Example Mobile Device Block Diagram



Definitions
CSI = Camera Serial Interface
DSI = Display Serial Interface
SLIMbus = Serial Low-power Inter-chip Media Bus

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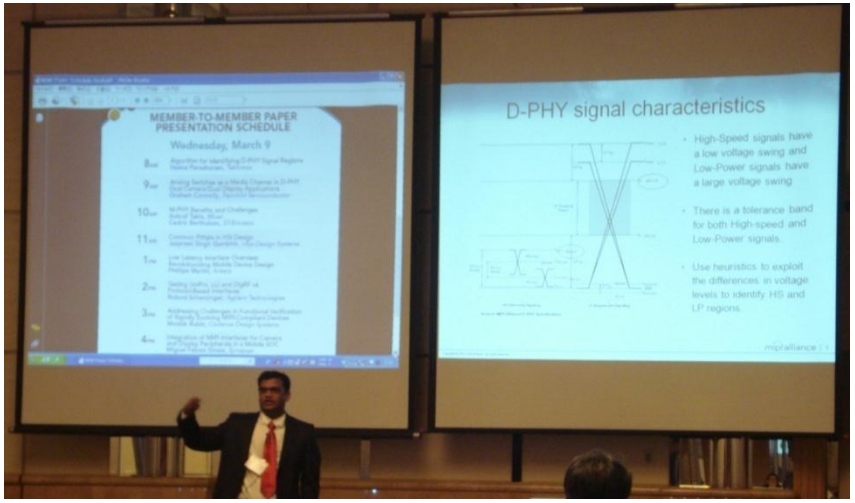
Tek Demonstrated Industry 1st Tools at MIPI F2F events

Industry 1st M-PHY Rx Jitter Tolerance, M-PHY Tx &D-PHY Demos at MIPI-Alliance F2F, Osaka, March'11, and Denmark, June'11:

Tek Technical-paper presentation at MIPI-Alliance F2F, Osaka, March'11



Industry 1st M-PHY Tx measurements Demo at MIPI-Alliance F2F, Athens, Sept'10

Tek D-PHY Tx measurements Demo at MIPI-Alliance F2F, San Diego, June'10

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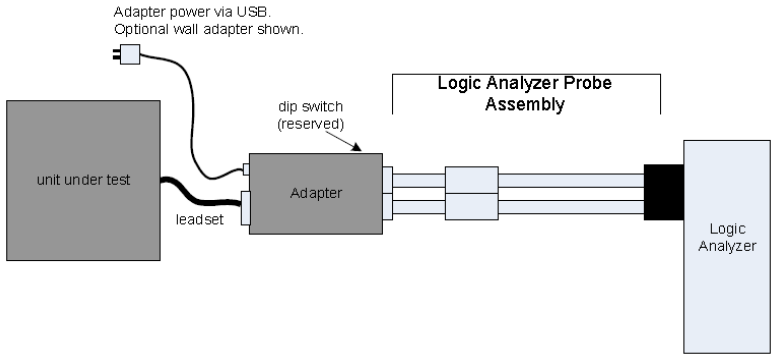
SLIMbus & H.S.I: Tektronix Solution

Test Setup &Adapters

- **Two Adapters: SLIMBus2TLA and HSI2TLA**
  - Serial to parallel Adapter to be used with Logic Analyzer
  - The Adapter is protocol Aware and converts the data to parallel form.
  - Parallel data allows the user to more easily setup a trigger and interpret the data.
  - The adapter is USB powered (ships with a USB cable)



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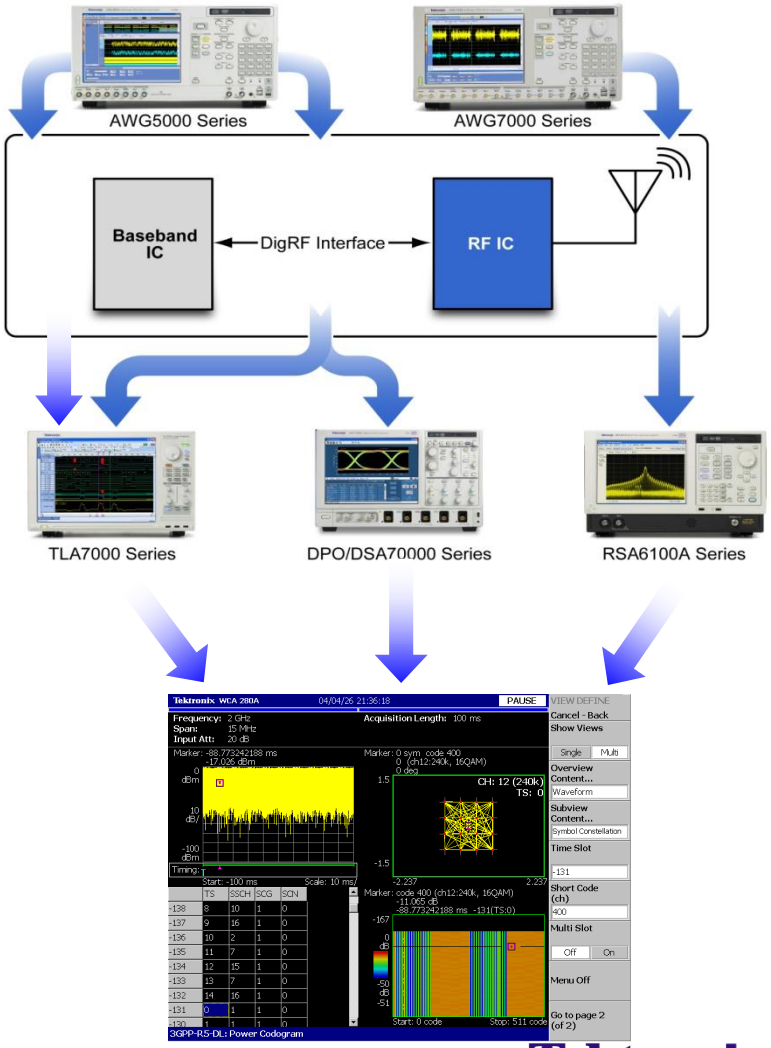
DigRF : Tektronix Solution (Manual Setups, no MOI/ Automation available)

Complete solution from Baseband to RF

- Complete solution using industry leading test equipment
  - AWG5000 for Signal Generation
  - TLA7012 for DigRF & Digital Analysis
  - DPO7000 for Signal Integrity issues
  - RTSA for RF and Modulation Analysis
- DigRF Physical Layer & Protocol analysis on logic analyzer without using specialized external hardware
  - Standard probes acquire the signal
  - DigRF Application software processes the data
- Flexibility to generate and analysis ideal, non-ideal and propriety versions of DigRF
  - DigRF Application is customizable by the user



Tektronix MIPI Solutions

Single Scalable-setup for MIPI D-PHY/M-PHY to USB3 &HDMI -Example

MIPI &HSS
Optimal Configuration:

Model	Description	Qty	D-PHY		M-PHY		USB3.0		HDMI &HEAC	
			Tx	Rx	Tx	Rx	Tx	Rx	Tx	Rx
DSA71254C	**12.5 GHz Digital Serial Analyzer; 4 analog channels**	1								
DSA71254C	**Frame and Bit Error Rate Detector (requires ST6G option)**									
DSA71254C STG6	Serial Pattern triggering up to 6.25Gb/s									
AWG7122C	**Signal Generator**	1								2 qty
AWG7122C 06	**Interleaved high bandwidth output**	1								
AWG7122C 01	Waveform length expansion (32M to 64M points)	1								
AWG7122C 08	Fast sequence switching (requires export control license)	1								
TEKEXP	TekExpress Automated Compliance Software	1								
MIPI Specific										
P7313	DIFFERENTIAL PROBE, 12.5 GHZ	3	3qty		2qty					
DSA71254C D-PHY	D-PHY Transmitter Debug &Characterization (requires DJA)	1								
TEKEXP D-PHYTX	D-PHY Automated Solution	1								
DSA71254C M-	M-PHY Transmitter Debug &Characterization (requires DJA)	1								
PG3ACAB	Moving Pixel Digital Pattern Generator Cabinet	1								
P331/ P332	Moving Pixel - 1Gbs Serial Probe for PG3A	1								
PGRemote-CSI/DSI	Moving Pixel - PG3A generation of CSI or DSI signals	1								
D-PHY Coupler Set	AWG / PG3A Coupler Set (Not on Tek price list yet)	1								
SR-DPHY	D-PHY - CSI2/DSI Decode software	1								
MPHYVIEW	M-Phy - DigRFv4 Decode software	1								
HDMI Specific										
P7313SMA	DIFFERENTIAL SMA PROBE, 12.5 GHZ	2							2qty	2qty
AF3102		1								
DSA71254C HT3		1								
DSA71254C HT3 DS		1								
TEKEXP HEAC		1								
Opt. 2XL		1								
020-3018-00	HDMI Direct Synthesis Accessory Kit	1								
USB Specific										
TEKEXP USB-RMT	USB 3.0 Receiver Automation Software	1								
TEKEXP USB-TX	Tekexpress Automated USB 3.0 Tx Solution	1								
TF-USB3-AB-KIT	USB 3.0 A/B Fixture/Cable Kit	1								
Optional Software										
SDX100	JITTER GENERATION SOFTWARE for AWG7000	1								
SDX100 ISI	S-Parameter and ISI creation option (requires SDX100)	1								