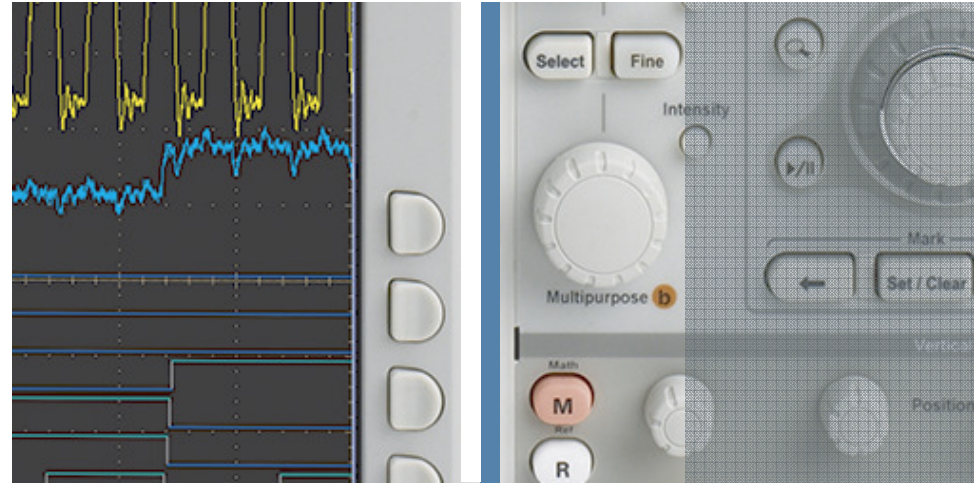


Introduction to Jitter and Serial Data Link Analysis



Kalev Sepp
Sr. Applications Design Engineer





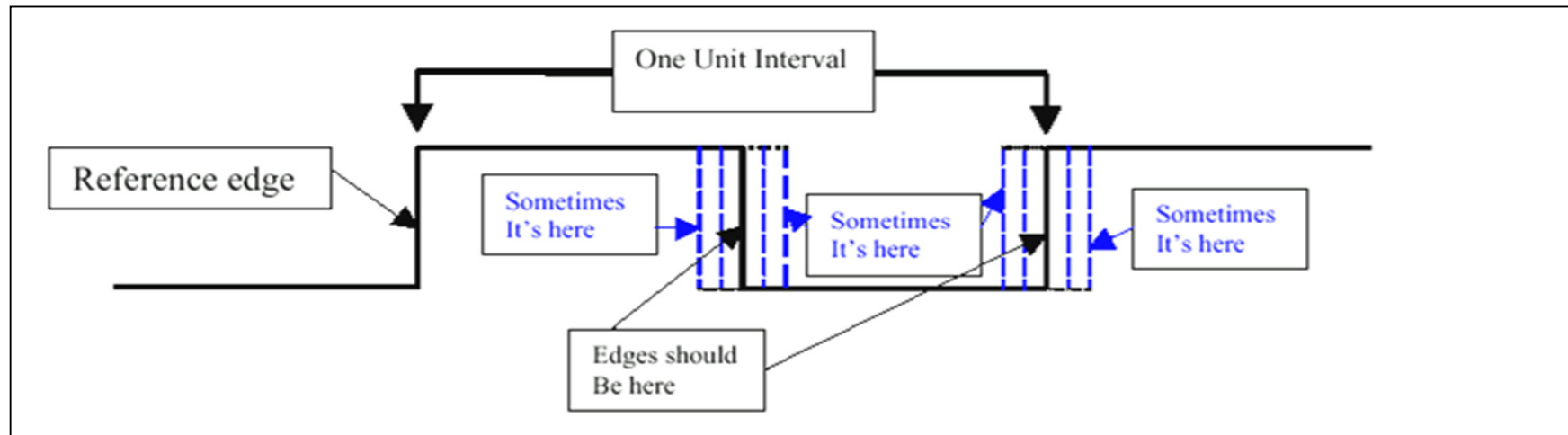
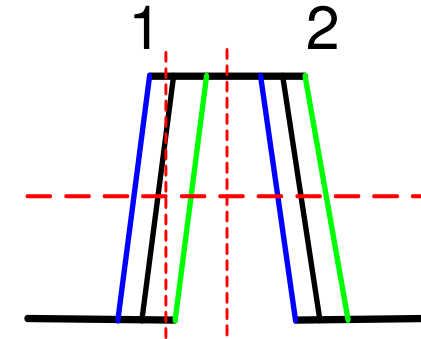
Agenda

- What is jitter?
- Jitter Measurements and Decomposition
- Clock Recovery and Reference Levels
- Channel Effects on the Signal and Measurements
- De-embedding and Equalization
- PCI Express 3.0 Example
- Tips for Effective Channel Modeling and Measurements
- Conclusions

What is Jitter?

■ Definitions

- “The deviation of an edge from where it should be”
- ITU Definition of Jitter: “Short-term variations of the significant instants of a digital signal from their ideal positions in time”

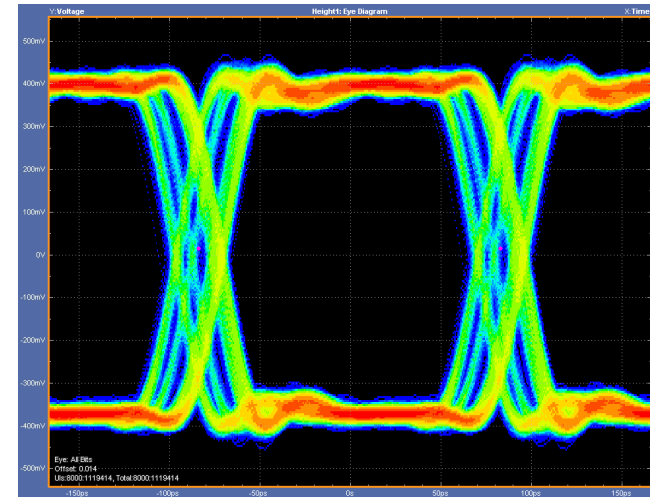


Jitter is caused by many things...

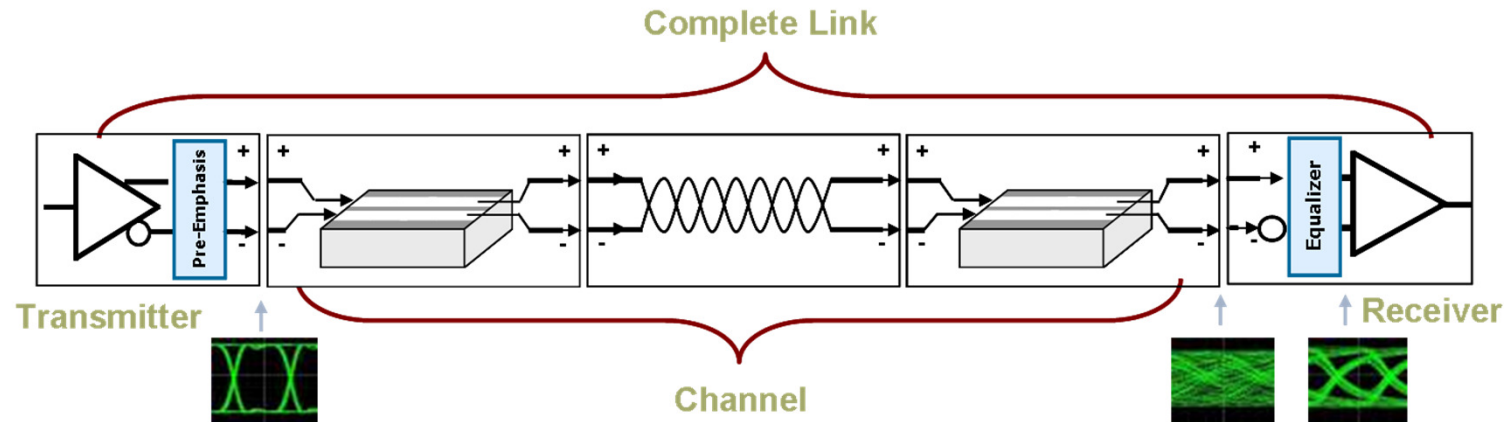
- Causes of Random Jitter
 - Thermal noise - Generally Gaussian
 - External radiation sources
 - Everything else that doesn't qualify into any other category

- Causes of Periodic Jitter
 - Injected noise (EMI/RFI) & Circuit instabilities
 - Power supply and oscillators
 - Will often have harmonic content
 - Transients on adjacent traces
 - Cabling or wiring (crosstalk)
 - PLL's problems
 - Internal noise (incl. quantization, effects of discrete implementation like DLL)
 - Loop bandwidth (tracking & overshoot)
 - Deadband (oscillation / hunting)
 - Intentional like SSC (spread spectrum clocking)

- Causes of Data Dependent Jitter
 - Transmission Losses
 - There is no such thing as a perfect conductor
 - Circuit Bandwidth
 - Skin Effect Losses
 - Dielectric Absorption
 - Dispersion – *esp. Optical Fiber*
 - Reflections, Impedance mismatch
 - path discontinuities (connectors)



Jitter Propagation, Measurements and Budgets



- Jitter varies at different locations (test points) of a serial data link
 - Amplitude variations convert to jitter (ISI – intersymbol interference)
 - Additional sources (crosstalk, EMI)
- Jitter is one of the **primary performance** indicator in a Serial Data Link
- Traditionally measured as TIE – time interval error
 - Statistically presented by peak-to-peak (p-p) or root mean square (rms)
 - Equivalent to Eye Width, Eye Closure
- Budgeted between Transmitter, Channel and Receiver



Motivation for Jitter Decomposition

- **Problem:** TIE or Eye width do not estimate circuit and link performance very well with respect to specified bit-error-rate (BER)
 - Different jitter components propagate differently
 - Some jitter components can be compensated, others not
- **Speed:** Directly measuring error performance at $1e-12$ requires directly observing MANY bits ($1e14$ or more). This is **time consuming!** Extrapolation from a smaller population can be done in seconds instead of hours.
- **Knowledge:** Jitter decomposition gives **great insight** into the root causes of eye closure and bit errors, and is therefore invaluable for analysis and debug.
- **Flexibility:** Already have a scope on your bench? You can do Jitter@BER measurements without acquiring more, perhaps somewhat specialized equipment.

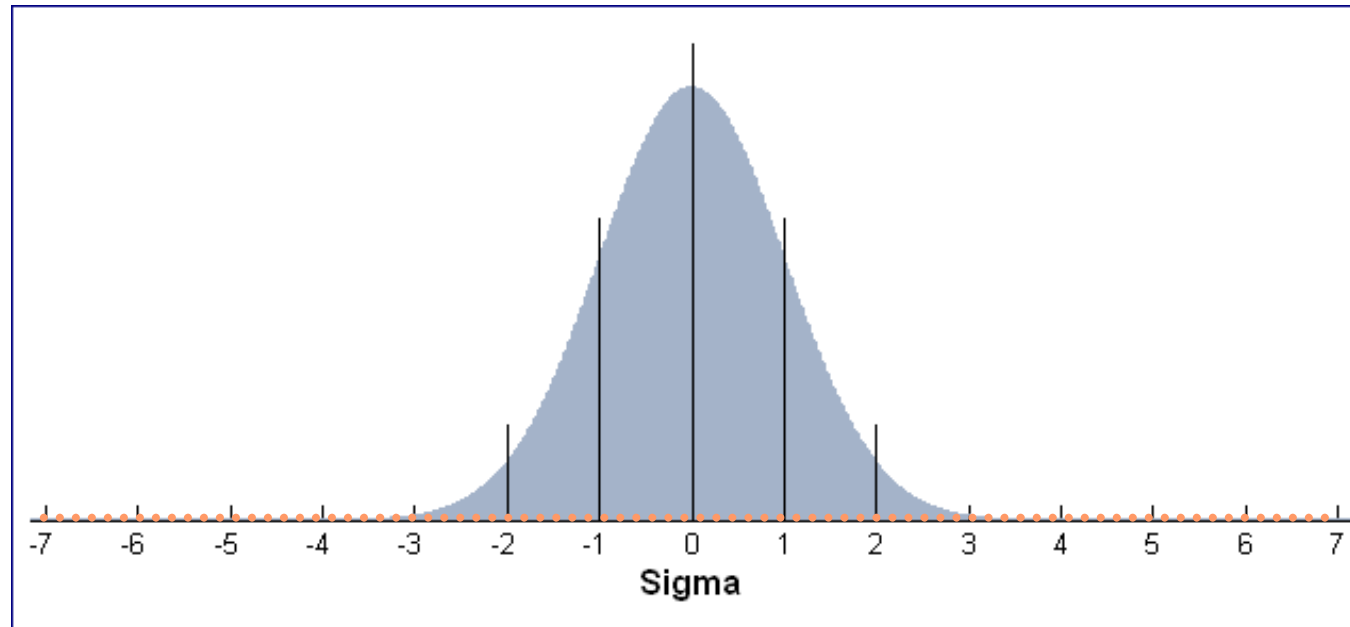
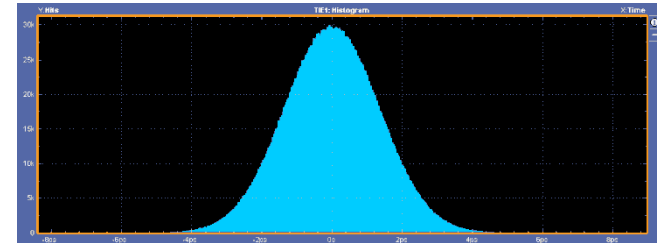
Common Terms

- Random Jitter (RJ)
 - Periodic Jitter (PJ)
 - Sinusoidal Jitter (SJ)
 - Duty Cycle Distortion (DCD)
 - Data-Dependent Jitter (DDJ)
 - Inter-Symbol Interference (ISI)
- Deterministic Jitter (DJ)
 - Periodic Jitter (PJ)
 - Sinusoidal Jitter (SJ)
 - Duty Cycle Distortion (DCD)
 - Data-Dependent Jitter (DDJ)
 - Inter-Symbol Interference (ISI)
- Bit Error Rate (BER)
- Total Jitter ~ (TJ or TJ@BER)
- Eye Width @BER
 - versus Actual or Observed Eye Width



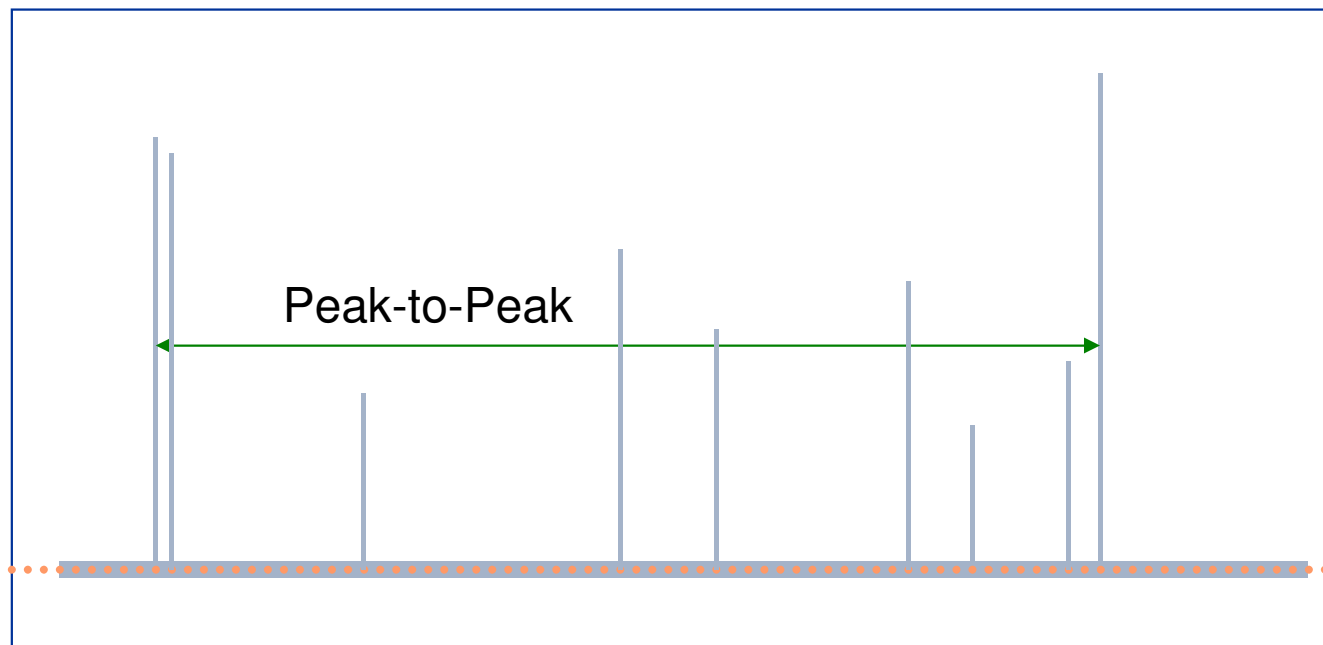
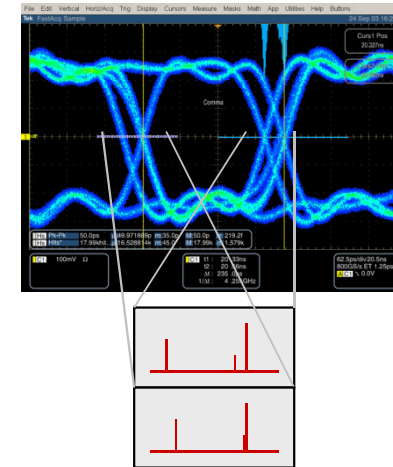
Random Jitter (RJ)

- Jitter of a random nature is assumed to have a Gaussian distribution (Central Limit Theorem)
- Histogram (estimate) \leftrightarrow pdf (mathematical model)
- Peak-to-Peak = ... unbounded!



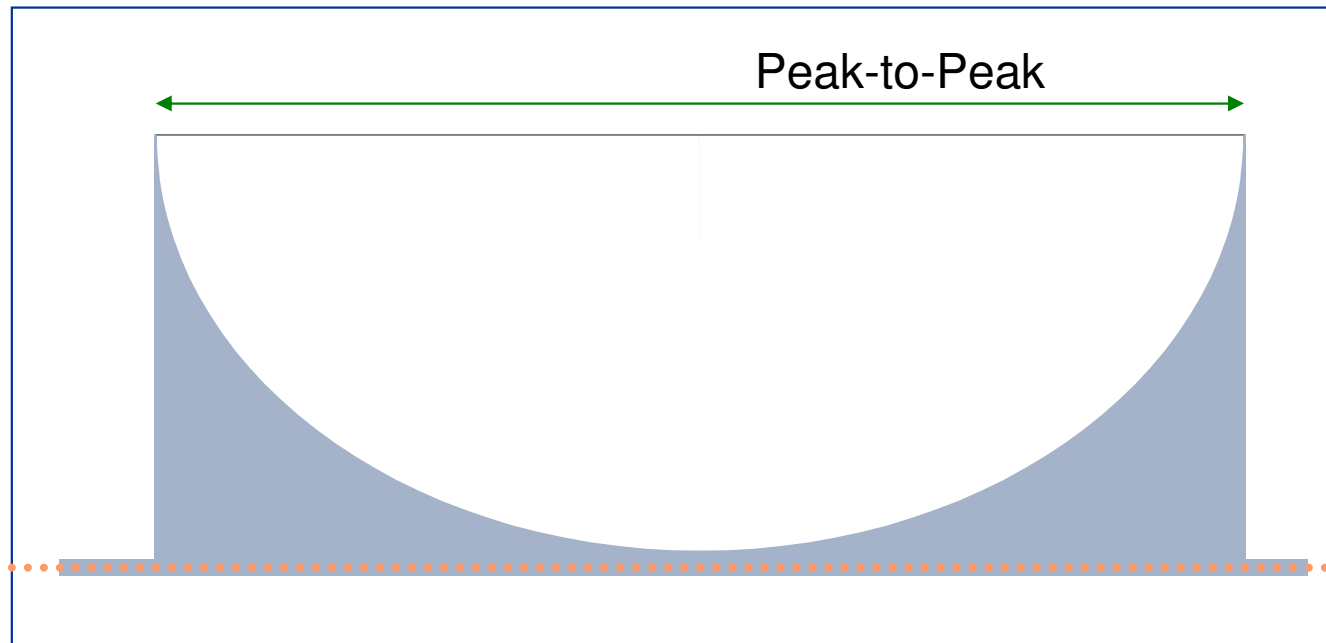
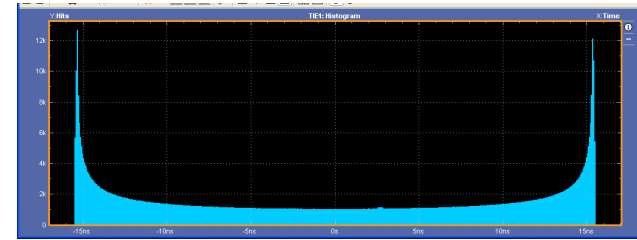
Deterministic Jitter (DJ)

- Deterministic jitter has a bounded distribution: the observed peak-to-peak value will not grow over time
- Histogram = pdf (close enough)



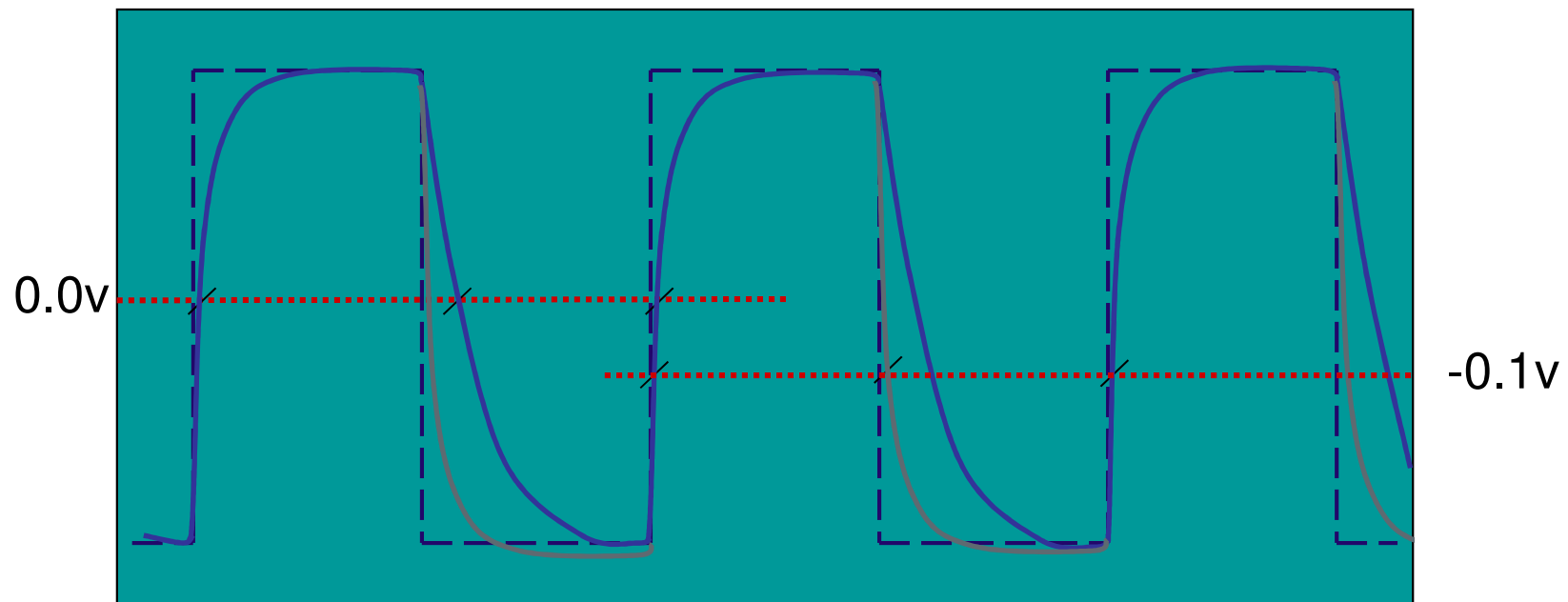
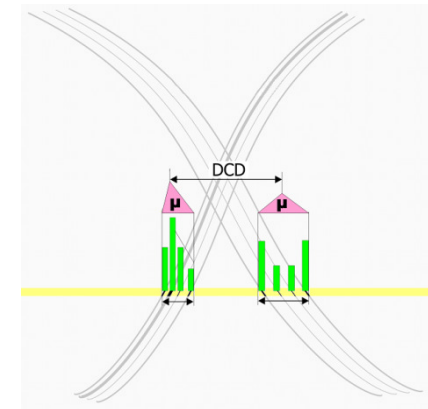
Periodic Jitter (PJ, SJ)

- TIE vs. time is a repetitive waveform
- Assumed to be uncorrelated with the data pattern (if any)
- Sinusoidal jitter is a subset of Periodic Jitter



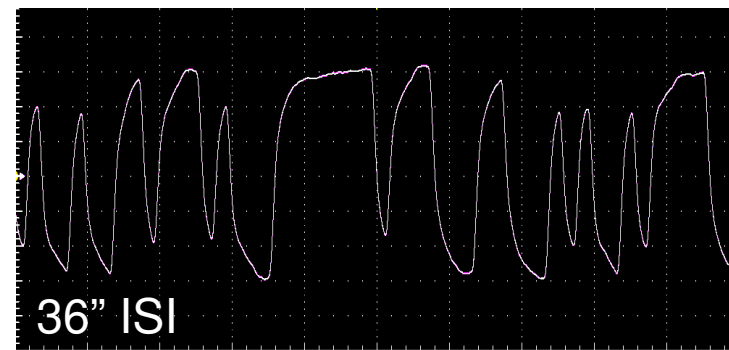
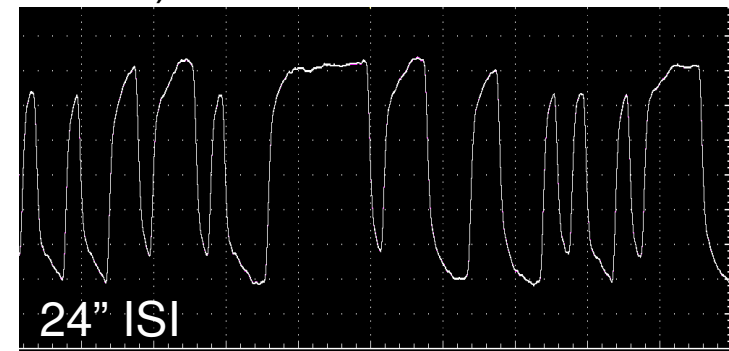
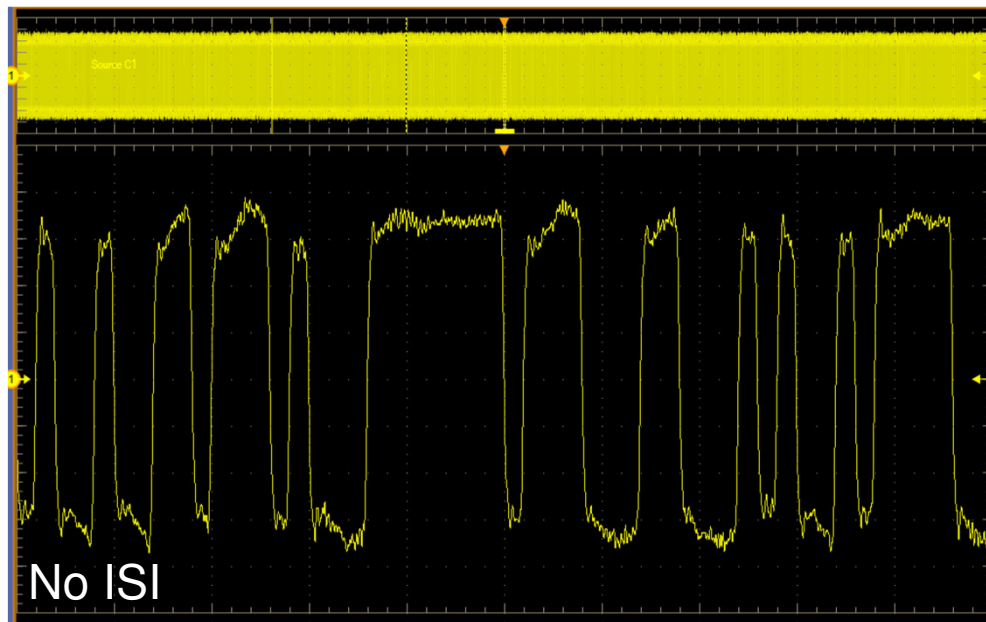
Duty Cycle Distortion (DCD)

- DCD is the difference between the mean TIE for rising edges and the mean TIE for falling edges
- Causes
 - Asymmetrical rise-time vs. fall-time
 - Non-optimal choice of decision threshold
- For a clock signal, the pdf consists of two impulses



Data-Dependent Jitter

- DDJ or ISI – used interchangeably
- ISI – usually considered to be the physical effect that causes DDJ
- Characterizes how the jitter on each transition is correlated with specific patterns of prior bits
 - Due to the step response of the system
 - Due to transmission line effects (e.g. reflections)



Bounded Uncorrelated Jitter

- Problem: Bounded but uncorrelated jittered components are accounted in RJ and thus cause larger TJ than actually in the system, incorrectly reflecting system performance.
- The implications of complex channel interaction can be observed and identified by examining the type and amount of Bounded Uncorrelated Jitter or BUJ.
- There is a strong Cause-and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

Table 4-6. Stressed Receiver Conditions

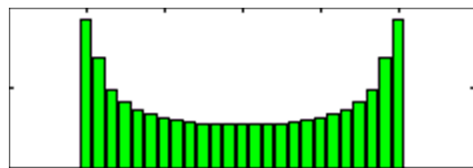
Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter



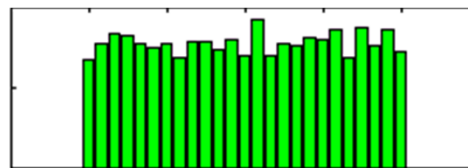
Bounded Uncorrelated Jitter (BUJ)

- Definitions of Jitter Properties:

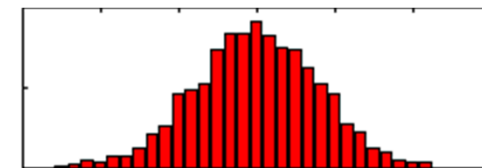
- **Bounded:** Having a PDF (histogram) that does not grow in width as the observation interval increases



Bounded



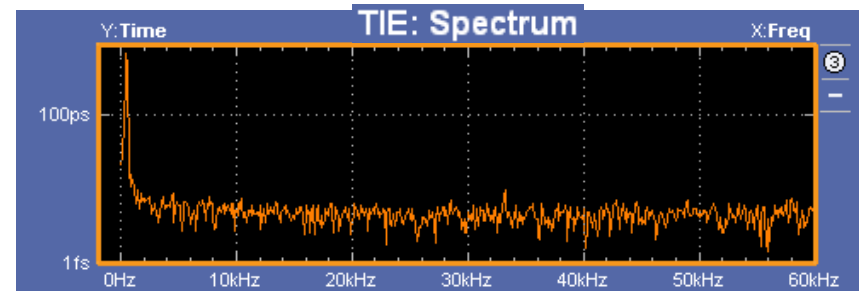
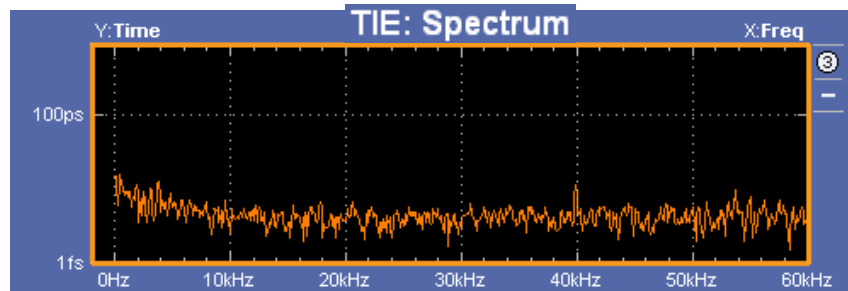
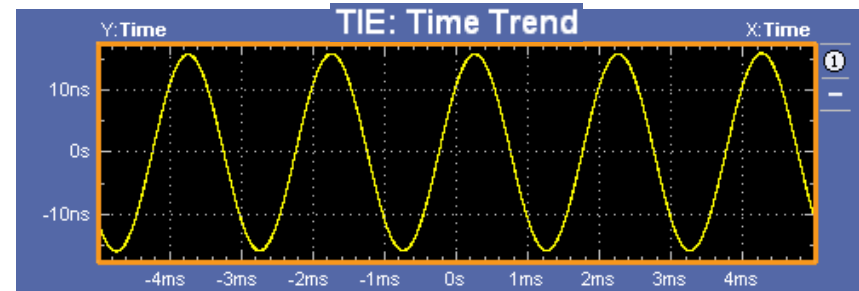
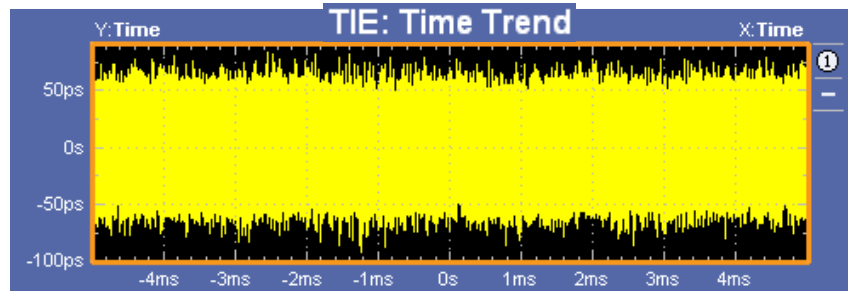
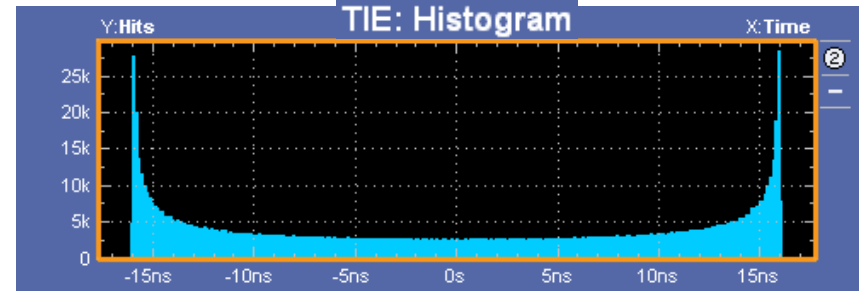
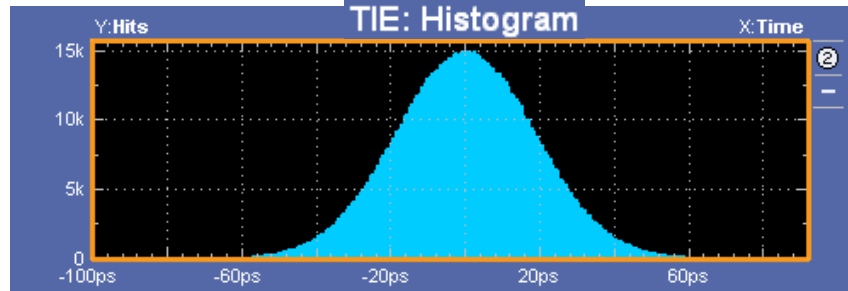
Bounded



Unbounded

- **Uncorrelated:** Specifically, not correlated to the pattern of data bits
 - Note that PJ (Periodic Jitter) is both bounded and uncorrelated → BUJ!
- **Deterministic:** Future behavior can be predicted based on observed past.
 - Deterministic jitter is always bounded
 - But... bounded jitter isn't necessarily deterministic
- **RJ:** By convention, random jitter with a Gaussian histogram
- **NPJ or NP-BUJ:** Non-Periodic (Bounded Uncorrelated) Jitter. This is basically random jitter with a bounded PDF

Jitter Visualization



Gaussian Random Noise

Sinusoidal Jitter



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TIE Jitter needs a Reference Clock

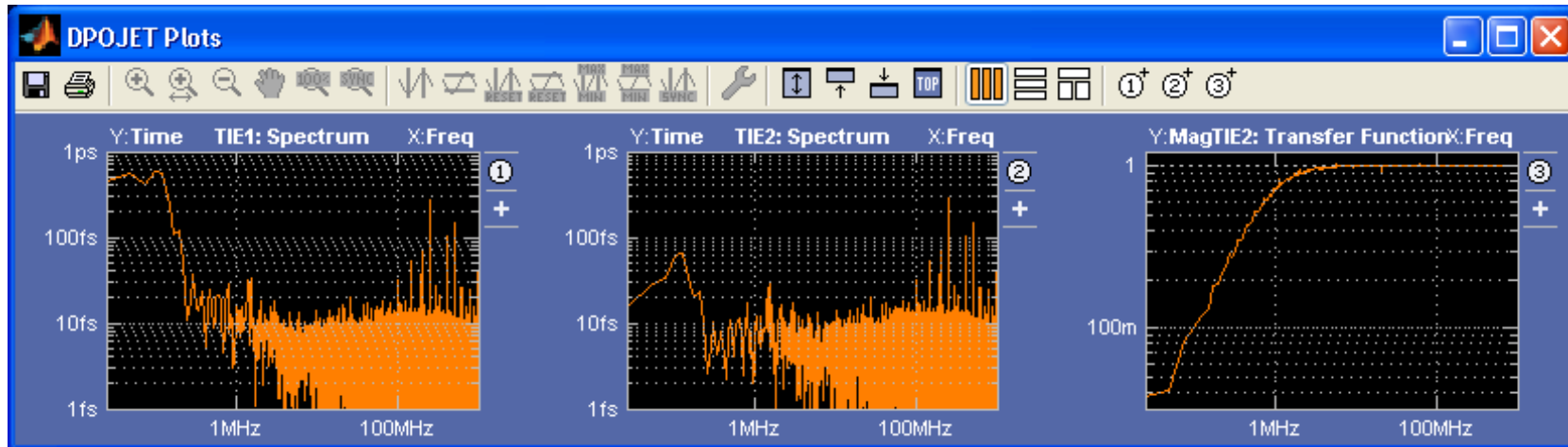
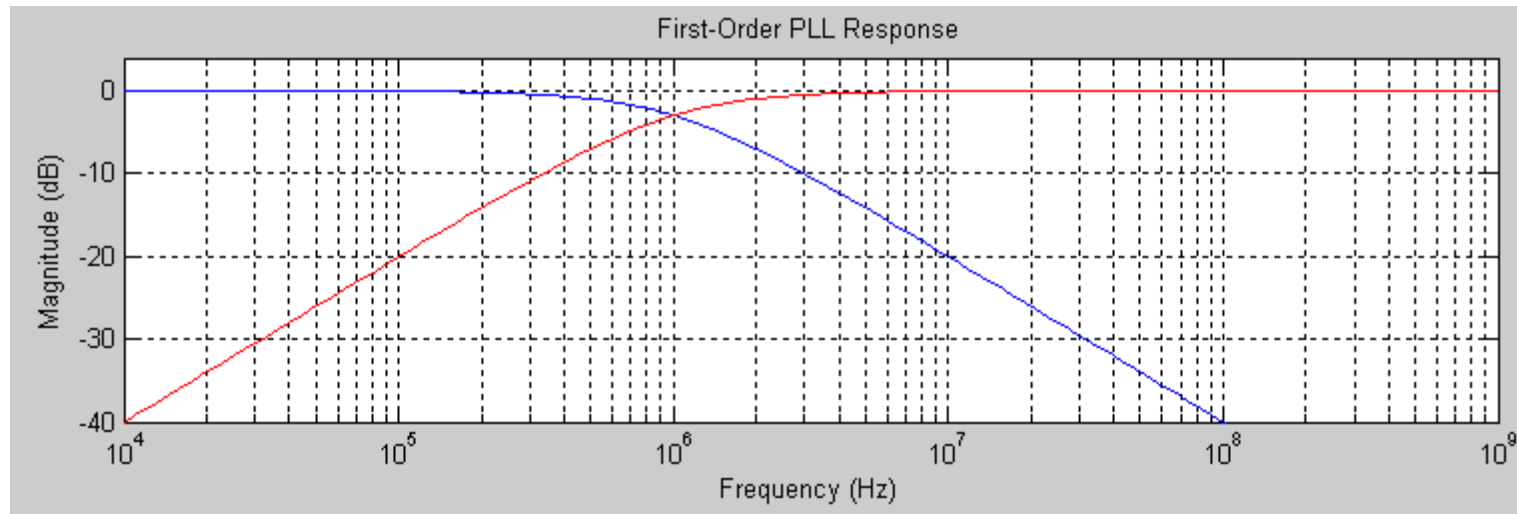
- The process of identifying the reference clock is called **Clock Recovery**.
- There are several ways to define the reference clock:
 - Constant Clock with Minimum Mean Squared Error
 - This is the mathematically “ideal” clock
 - But, only applicable when post-processing a finite-length waveform
 - Best for showing very-low-frequency effects
 - Also shows very-low-frequency effects of scope’s timebase
 - Phase Locked Loop (e.g. Golden PLL)
 - Tracks low-frequency jitter (e.g. clock drift)
 - Models “real world” clock recovery circuits very well
 - Explicit Clock
 - The clock is not recovered, but is directly probed
 - Explicit Clock (Subrate)
 - The clock is directly probed, but must be multiplied up by some integral factor
 - Example: PCI Express motherboard CEM testing



JTF vs PLL Loop Bandwidth

- Configuring the correct PLL settings is key to correct measurements
- Most standards have a reference/defined CR setup
 - For example, USB 3.0 uses a Type II with JTF of 4.9Mhz
- Type I PLL
 - Type I PLL has 20dB of roll off per decade
 - JTF and PLL Loop Bandwidth are Equal
- Type 2 PLL
 - Type II PLL has 40dB of roll off per decade
 - JTF and PLL Loop Bandwidth are not Equal
 - For example, USB 3.0 uses a Type 2 PLL with a JTF of 4.9Mhz. The corresponding loop bandwidth is 10.126 Mhz
 - Setting the Loop Bandwidth as opposed to JTF will lead to incorrect jitter measurement results

PLL Loop Bandwidth vs. Jitter Transfer Function (JTF)

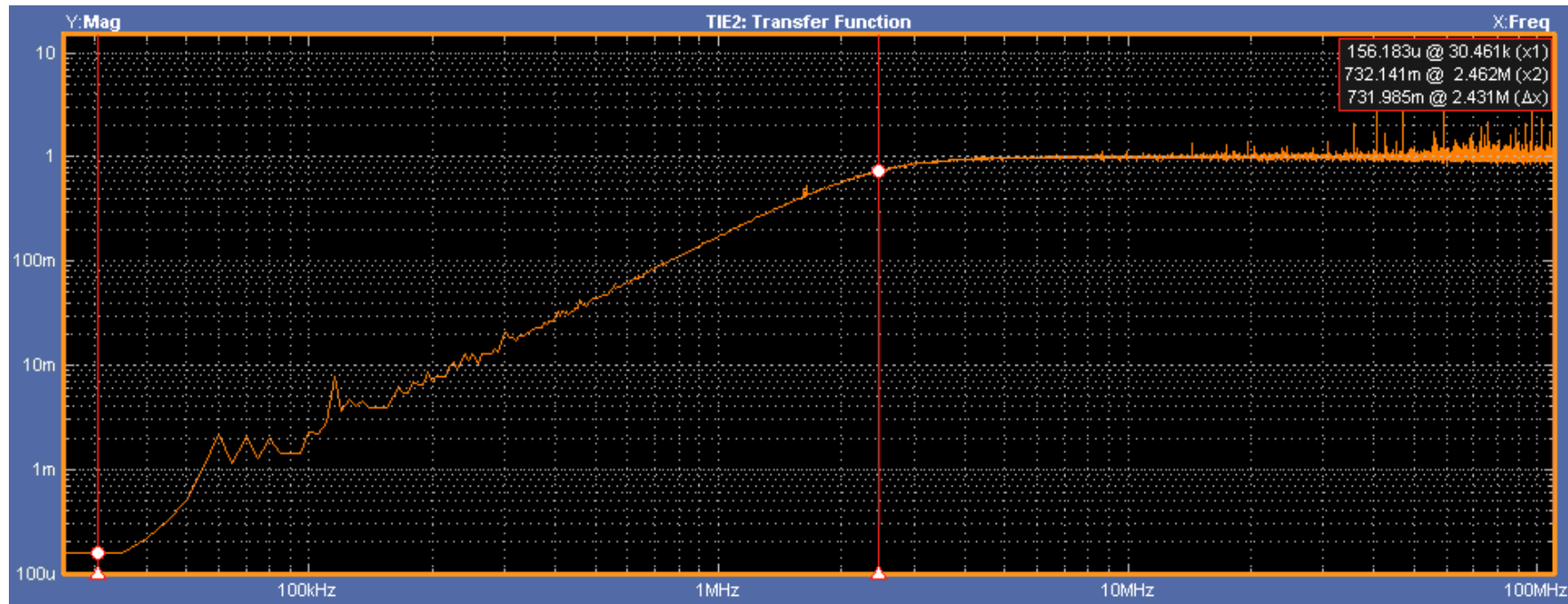
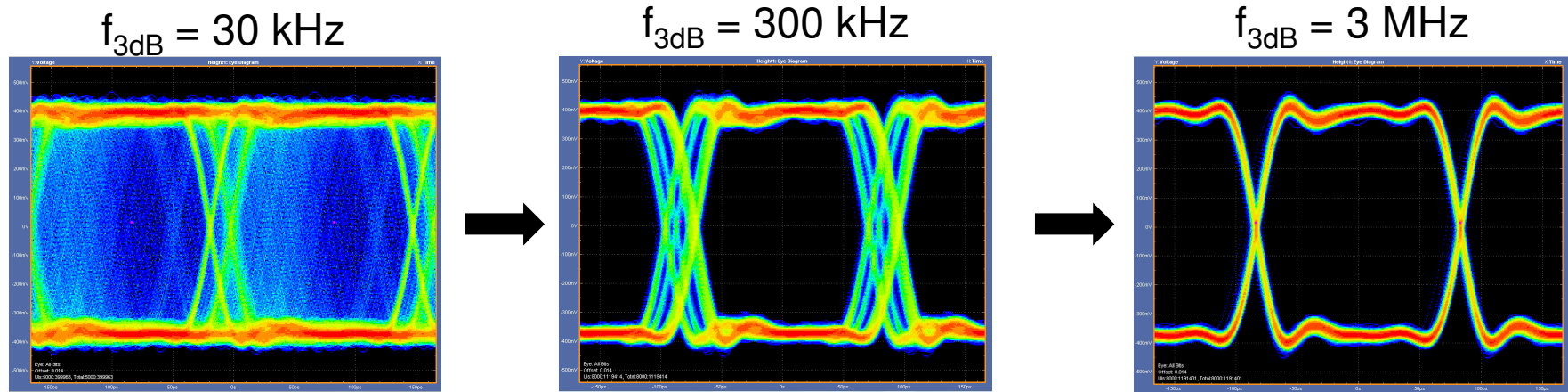


A: Constant Clock Recovery

B: PLL Clock Recovery

Ratio of B/A

JTF Filtering Effects based on different PLL bandwidths

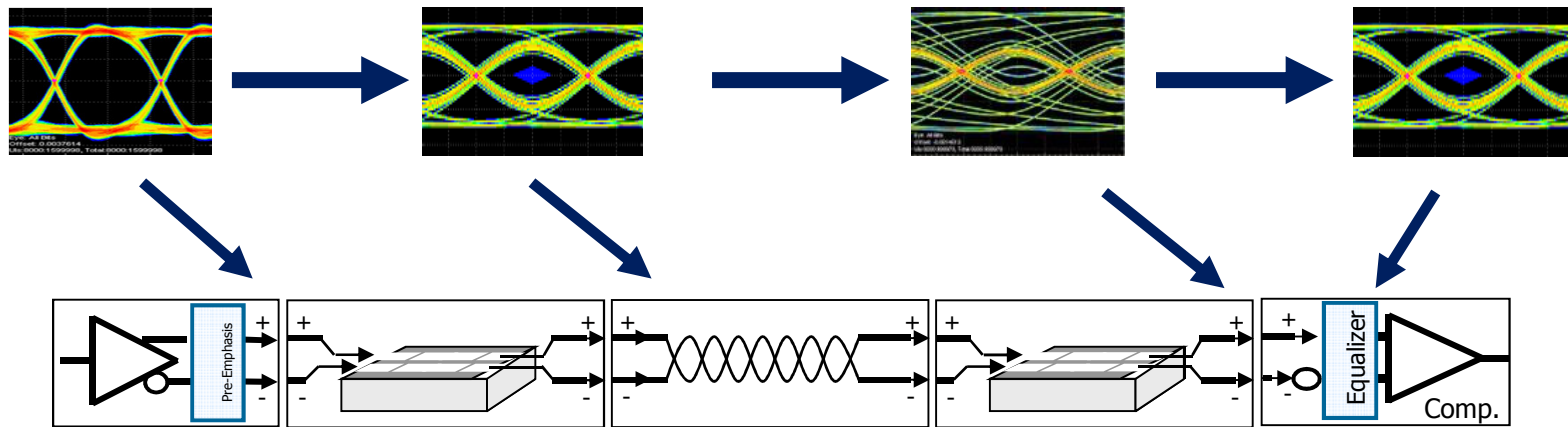




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Channel Effects on the Signal and Measurements



- ***As signal propagates through the model***
 - ***Eye closes both horizontally and vertically***
 - ***Jitter increases***
- ***Eye may be closed at the receiver pins (before equalization)***
- ***Equalization is needed to open the eye at the slicer (comparator) of the receiver***

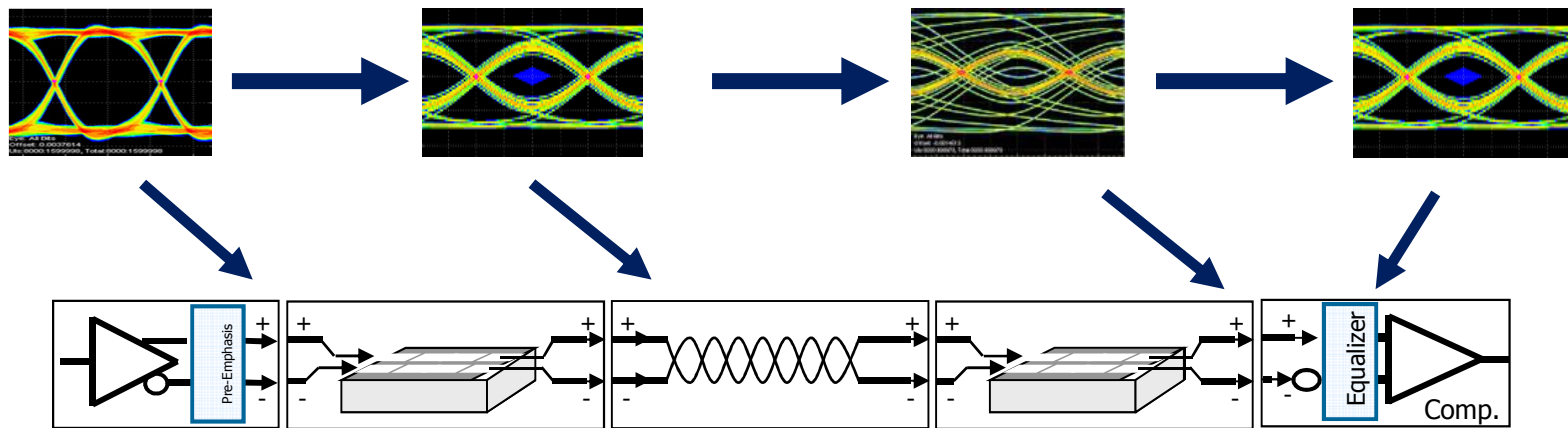
Terminology

- Transmitter equalization
- De-emphasis, Preshoot, Boost
- De-embedding
- CTLE – Continuous time linear equalizer
- FFE – Feed-forward equalizer
- DFE – Decision feedback equalizer

What is the difference?

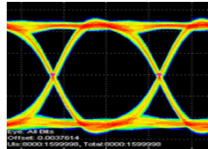
Vs.

- Channel loss
- Embedding

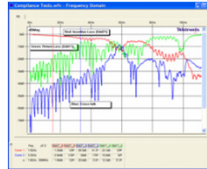


Fundamentals of Serial Data Link Analysis

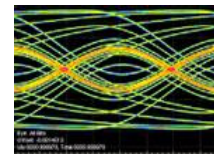
Transmitter Performance
after De-Embed



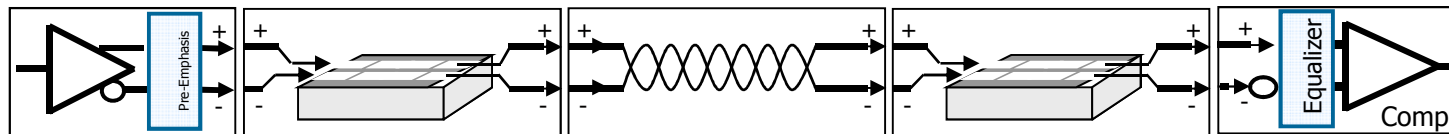
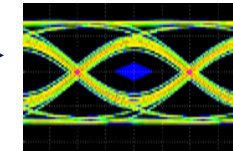
Embed Channel Characteristics
(S-parameters)



Result of Channel
Effects



After
Equalization



- **De-embed** measured circuit as needed, to remove the effects of the test fixture, cables and/or the channel to characterize the Transmitter
- **Embed** the simulation circuit: observe the waveform at the receiver pins
- Emulate the **Equalization inside the Rx**: observe the waveform at the comparator

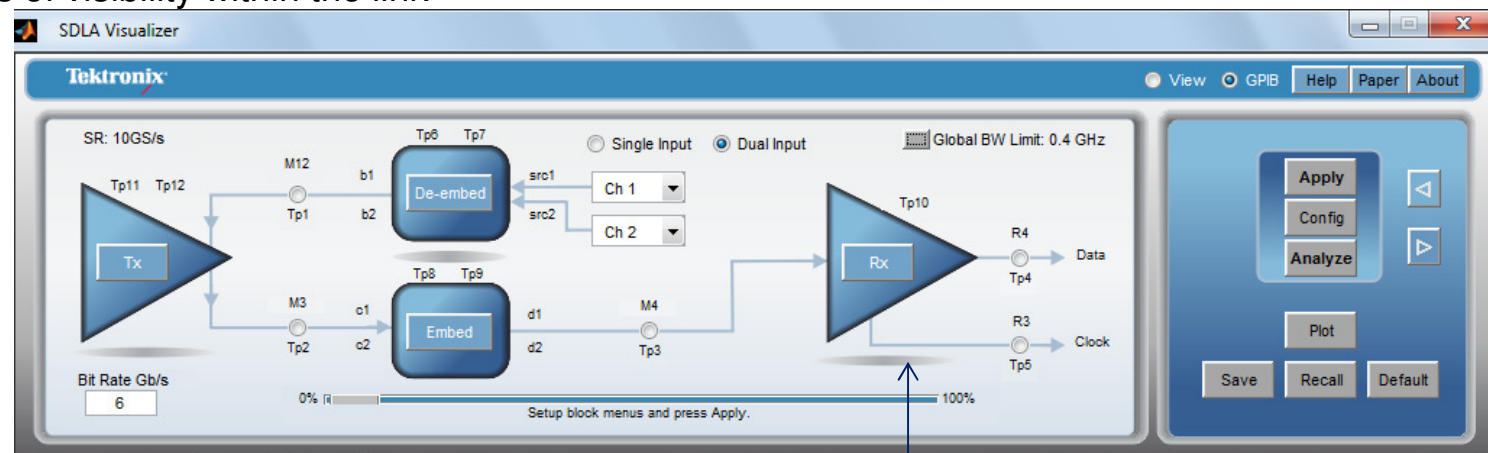
SDLA Visualizer

Tool for Channel Modeling

- Select Input Mode
 - Specifies operating mode of SDLA
- Configure Measurement Circuit (**De-Embed**)
 - The Measurement Circuit is used to define the TX output impedance and the physical test and measurement system used to acquire the signal
- Configure Simulation Circuit (**Embed**)
 - The Simulation Circuit is used to define the TX output impedance, embed a simulated channel and to specify a receiver load
- Configure RX Block (**Equalization**)
 - Rx Equalization can be specified as an IBIS-AMI model, OR CTLE and/or DFE/FFE.
- Select Test Points
 - Points of visibility within the link

Measurement Circuit →

Simulation Circuit →



Receiver Equalizer



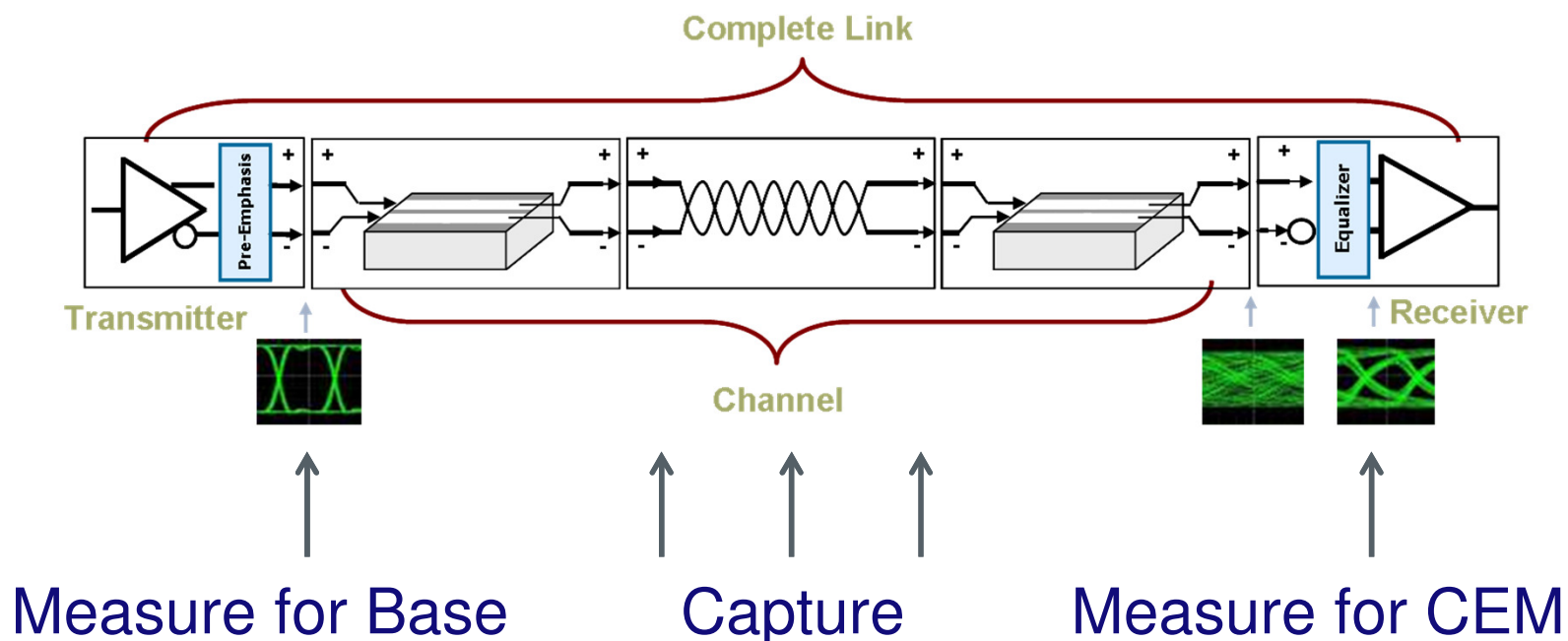


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PCI Express 3.0 Example

- Base vs CEM Testing
- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?



Capture where you can - Measure where you need!

System (Base Spec) Tx Testing

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see how the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel

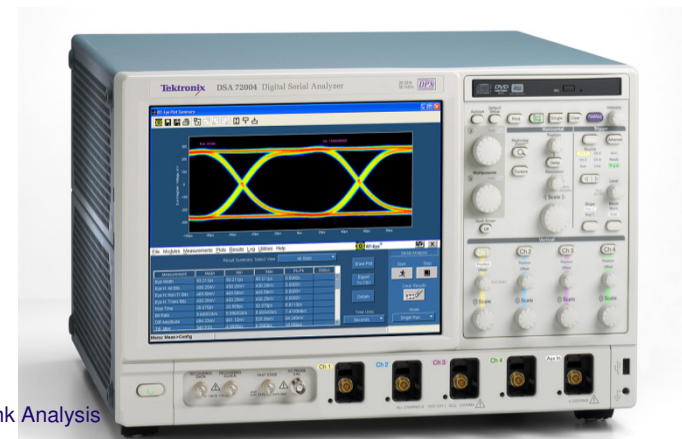
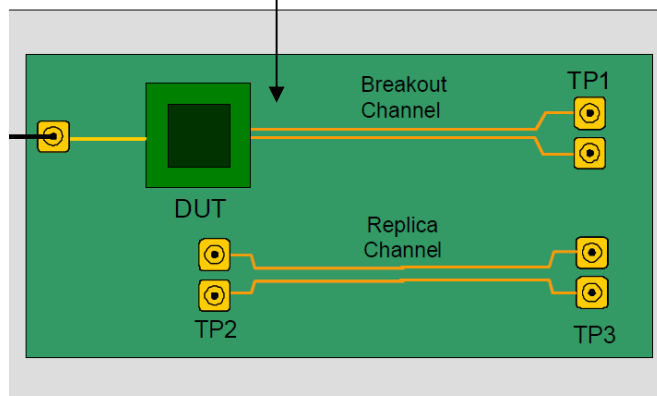


Signal at Tx Pins

Measured Signal at TP1

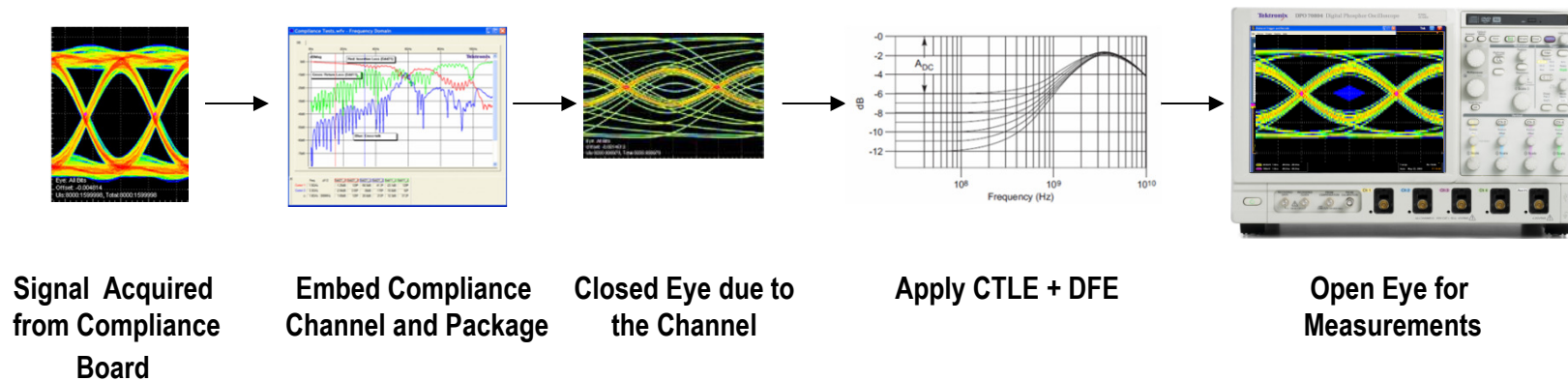
De-embed using S-Parameters

Signal with Channel Effects Removed



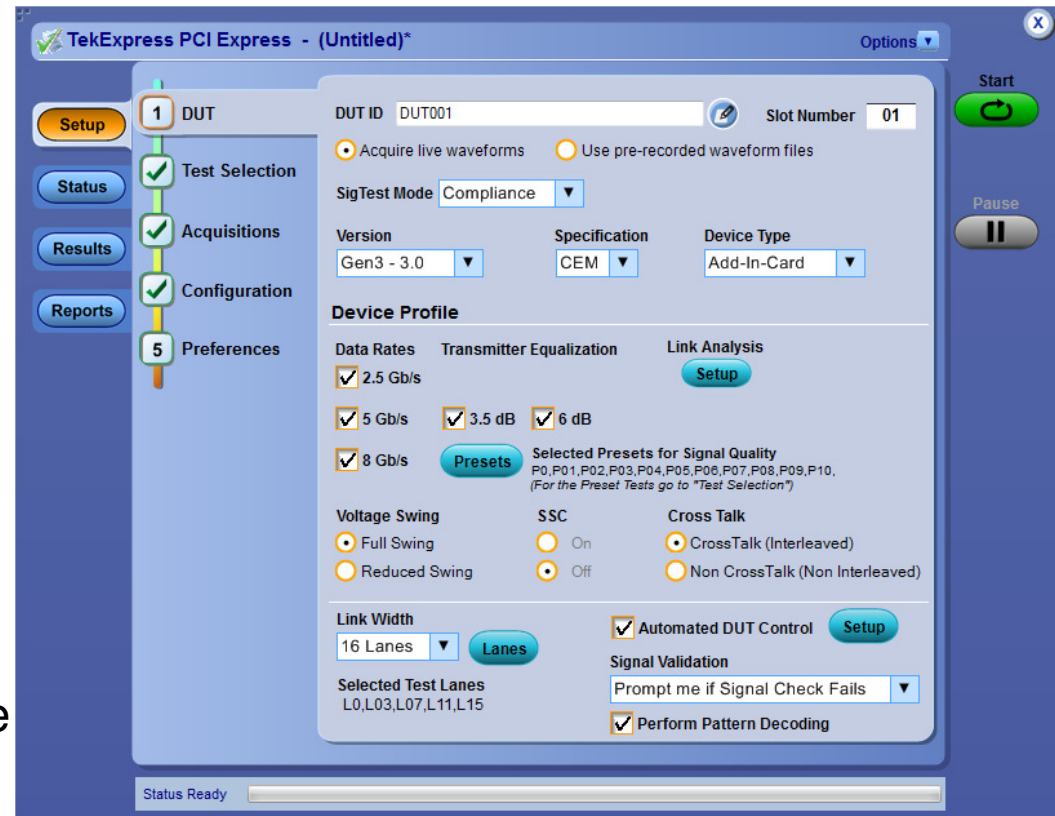
Add-In Card (CEM Spec) Tx Testing


- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible either
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



Tektronix option PCE3

- TekExpress Automation for Tx Compliance with unique features including:
 - ✓ Sets up the Scope and DUT for testing
 - ✓ Toggles thru and verifies the different Presets and Bit Rates (2.5, 5, 8 GT/s)
 - ✓ Tests multiple slots and lanes
 - ✓ Processed with PCI-SIG SigTest
 - ✓ Provides custom reporting
 - ✓ Optionally removes test fixture effects by using de-embedding

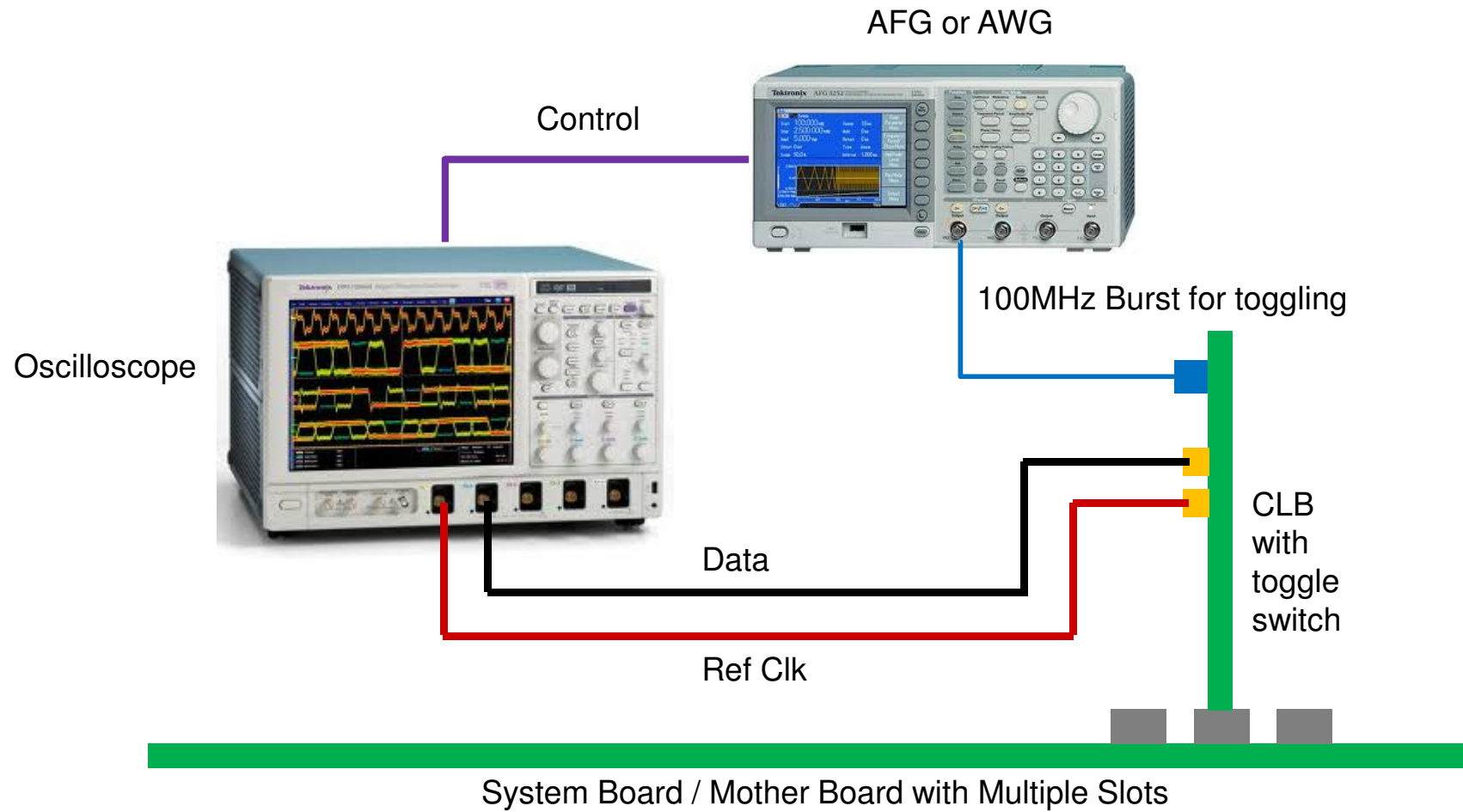




Option PCE3 for DPOJET

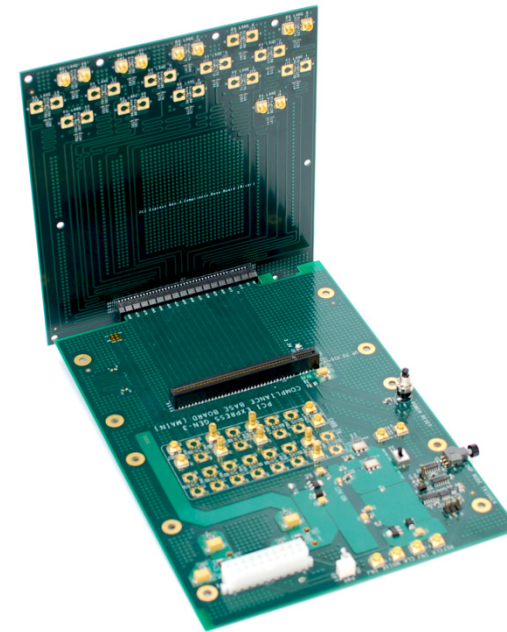
- SigTest.exe (Command-Line) integration
 - Supports PCI-SIG recommended SigTest.exe utility
 - User can switch between DLL and Command-Line (.exe) modes
 - All result are populated in Tektronix result/report format in command line mode
- Support the latest versions of SigTest
 - User can optionally choose a different version and run
- Uses AWG/AFG for automatic DUT toggle (*Min 2ch & 100MHz Burst mode*)
 - AFG3252/C
 - AWG5002B/C, AWG5012B/C, AWG5014B/C
 - AWG7082B/C, AWG7122B/C
 - AWG70001A/2A

Automated DUT Control

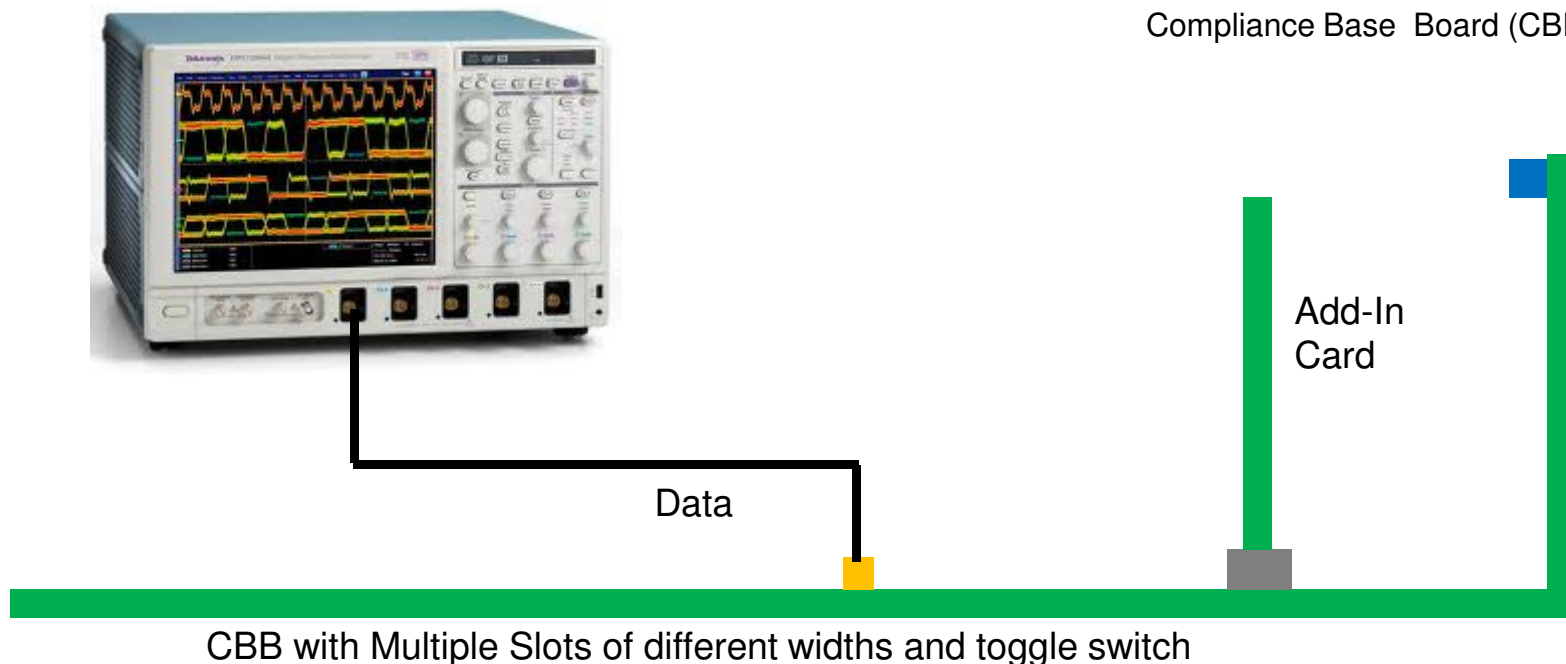


Add-In Card Test Fixture

- Compliance Base Board (CBB)
 - Used for Testing Add-In cards
 - All Tx / Rx Lanes are routed to SMP
 - Compliance Mode Toggle Switch
 - Low Jitter Clean Reference Clock
 - Separate CBB for Gen 1/2/3



Compliance Base Board (CBB)



CBB with Multiple Slots of different widths and toggle switch



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Hints for Successful Jitter Analysis

- Verify that signal integrity (i.e. probing) is reasonable
 - Reflections due to mid-bus probing can cause “duplicate” edges
- Check (and consider overriding) your autosets
 - Reference levels are appropriate to the signal
 - If the input signal is differential, consider locking the mid ref to 0 V.
 - A strongly bi-modal histogram often signals a reference level problem.
 - Is the signal noisy enough to require more hysteresis?
 - Explicitly set the signal type to Clock or Data
- Use only the bandwidth you need
 - If the scope BW exceeds the BW of the device being tested, you are adding some scope noise to the measurement results
- Check your RJ/DJ settings
 - Repeating-pattern vs arbitrary-pattern
 - Check that your pattern length is correct



More Hints for Successful Jitter Analysis

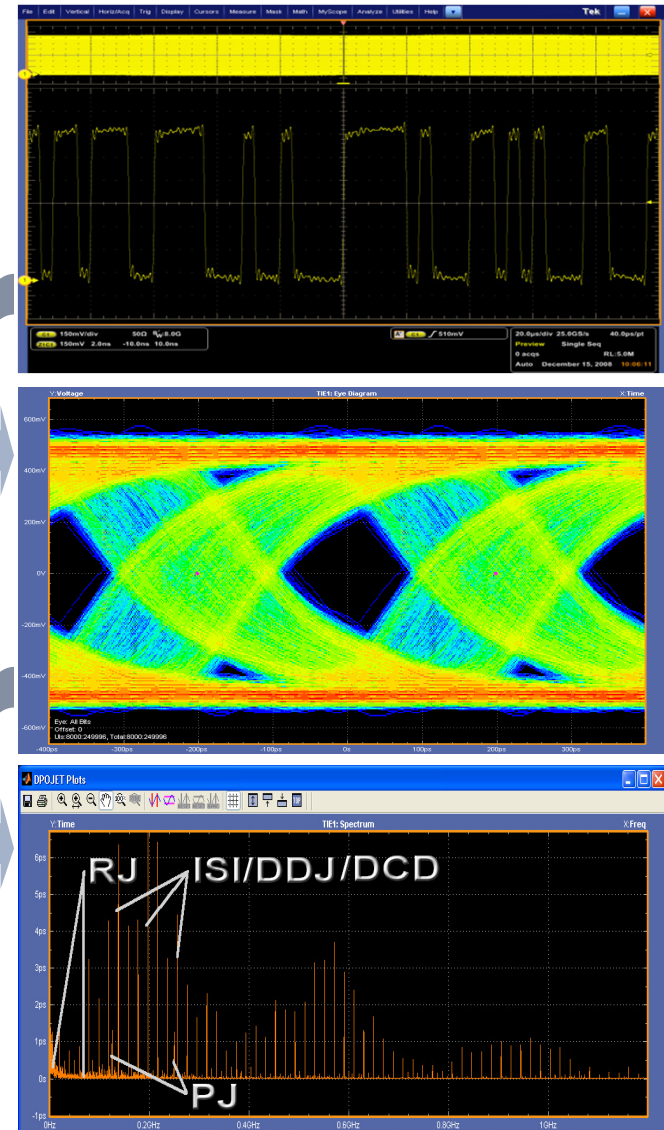
- Clock Recovery has a great deal of influence on jitter results. Think about what you're trying to accomplish.
 - Constant-Clock is the most “unbiased”
 - Often best if you're trying to see very-low-frequency effects
 - But it can also show wander in the scope's timebase
 - PLL recovery can model what a real data receiver will see
 - It can track and remove low-frequency effects, allowing you to “see through” to the jitter that really contributes to eye closure
 - Explicit-Clock is appropriate if your design uses a forwarded clock
 - Make sure your probes are deskewed

Hints for looking at Spread-Spectrum Clock

- If you don't want to see the SSC effects, use **TIE** and PLL clock recovery with a bandwidth of at least 1 MHz. A Type-II (2nd-order) PLL will track out the SSC more effectively than a Type-I PLL.
- If you do want to observe the SSC profile:
 - Use a **Period** measurement and turn on a 3rd-order **low-pass filter** (in DPOJET) with a bandwidth of 200 kHz
 - Because Period trends accentuate high frequency noise, the low-frequency SSC trend will be obscured if you don't use a filter
 - You can't use a Frequency measurement directly. The combination of filtering and the reciprocal operation ($\text{Freq} = 1/\text{Per}$) cause distortion in the resulting waveshape.
 - If you use a TIE measurement, you'll see modulation that looks like a sine wave. This is normal. It's because TIE measures phase modulation, which is the integral of frequency. It turns out that the integral of a triangle wave looks very much like a sine wave.

Additional Ideas for Resolving of Jitter Issues

- Deep memory capture
 - Long records needed for low frequency events (SSC, periodic jitter, low speed clocks)
 - Frequency window related to time capture
 - 1 SSC cycle (33kHz) => Need 30us time record
- Eye Diagram Analysis
 - Quick visual indicator of voltage and timing performance
 - Related to Bit Error Rate (BER)
- Debugging Jitter
 - Knowledge of jitter types and sources aids in debug
 - Common jitter sources
 - Power supply coupling
 - PLL (tracking or overshoot)
 - Limited channel bandwidth and reflections (ISI)
 - Driver imbalance (Rise/fall time asymmetry)
- Check Reference Levels and Clock Recovery parameters





Conclusions

- Jitter decomposition and measurements allow proper evaluation of system performance
- Use Serial Data Link Analysis (SDLA) to emulate or compensate for losses in the channel
- Use specific measurement solutions (DPOJET, TekExpress) to evaluate compliance with the specification
- Use tools that provide most flexibility and comprehensive analysis capability
- Thank you for attending!

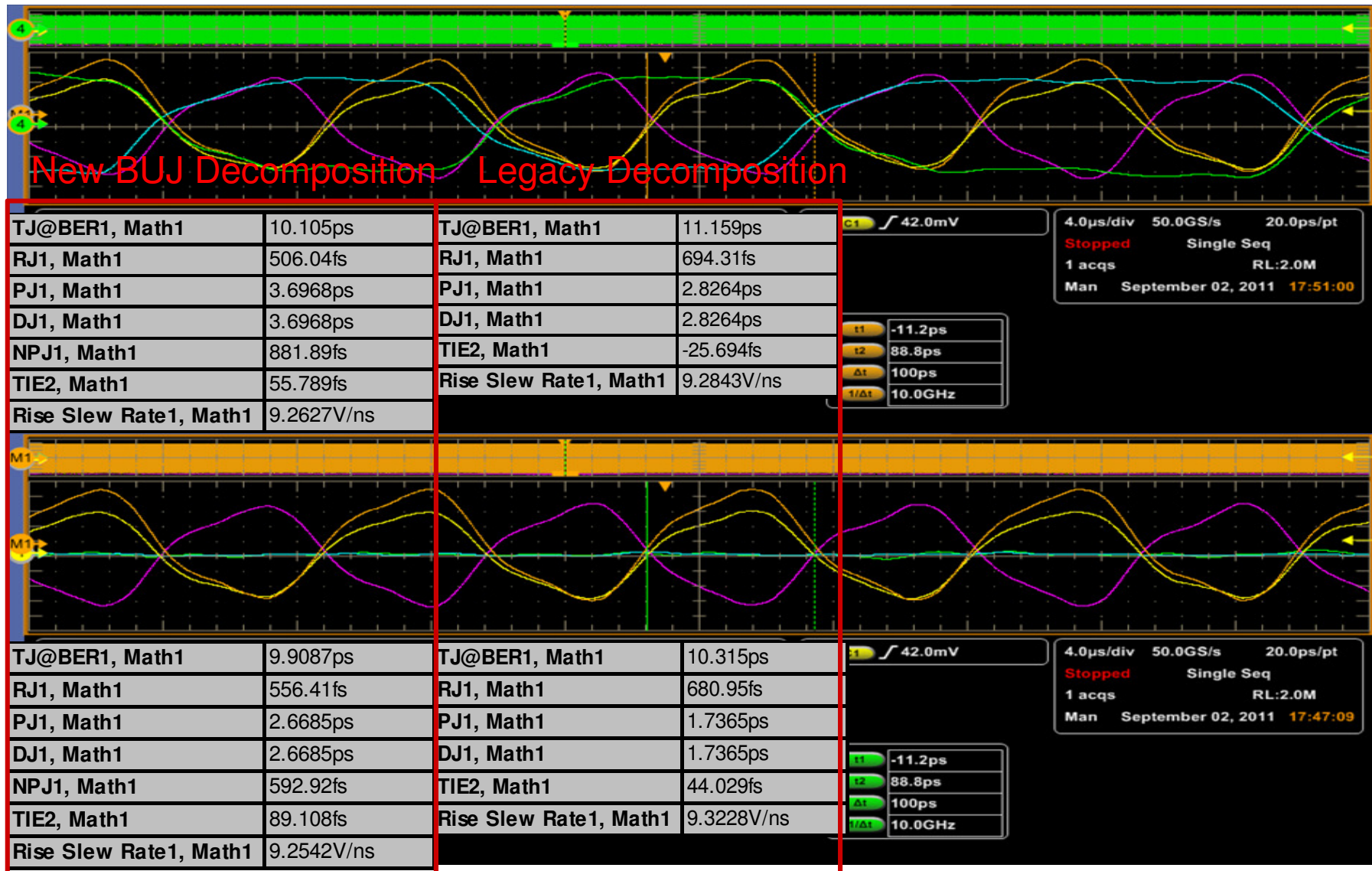
Jitter Measurement in the Presence of Crosstalk: Problem Summary

- Crosstalk-caused jitter typically is Bounded Uncorrelated Jitter (BUJ); depending on the spectra this should be separated as either
 - PJ (Periodic BUJ)
 - or
 - NPJ (Non-Periodic BUJ)
- In traditional oscilloscope-based jitter measurement methodology the more spectrally diffuse BUJ components (i.e. NPJ) are not distinguished from RJ.
 - The inflated RJ is multiplied by a factor, thereby grossly inflating TJ.

$$\text{Example: } TJ = DJ + 14 * RJ \quad (\text{at BER} = 1e-12)$$

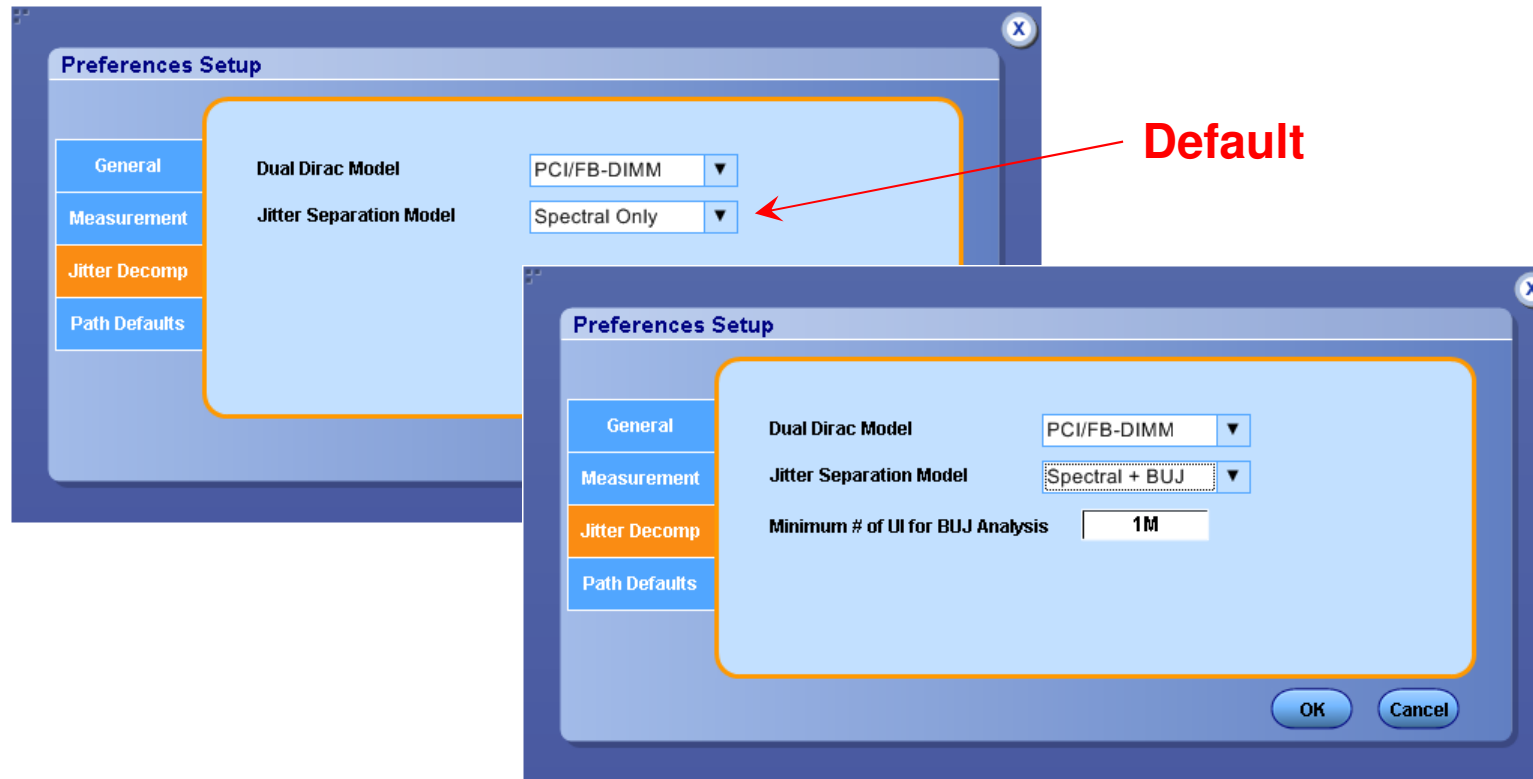
- This is well known and was documented e.g. in *“Method of BER Analysis of High Speed Serial Data Transmission in Presence of Jitter and Noise”*, Zivny at all, DesignCon 2007.

BUJ vs. Legacy Jitter Decomposition Results



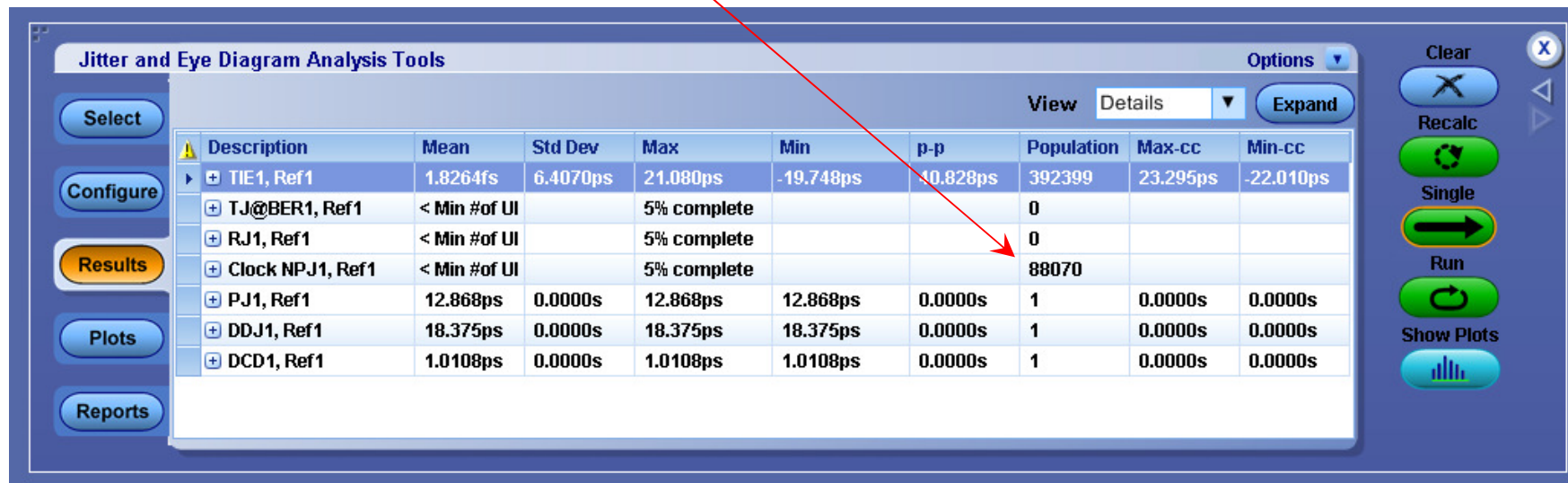
DPOJET Setup for BUJ / NPJ Measurements

- **Enable** Spectral+BUJ either through the Preferences Setup or the Jitter Map
- **Minimum # of UI** control is only available via Preferences Setup
 - Default is 1M but it can be reduced as low as 10k.



DPOJET Results for BUJ / NPJ Measurements

- Until the population requirement has been met, dependent measurements say “< Min # of UI”
- Clock NPJ measurement shows actual progress toward the population requirement



Jitter and Eye Diagram Analysis Tools

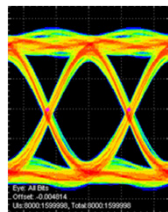
Options ▾ View Details ▾ Expand

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
⊕ TIE1, Ref1	1.8264fs	6.4070ps	21.080ps	-19.748ps	40.828ps	392399	23.295ps	-22.010ps
⊕ TJ@BER1, Ref1	< Min #of UI		5% complete			0		
⊕ RJ1, Ref1	< Min #of UI		5% complete			0		
⊕ Clock NPJ1, Ref1	< Min #of UI		5% complete			88070		
⊕ PJ1, Ref1	12.868ps	0.0000s	12.868ps	12.868ps	0.0000s	1	0.0000s	0.0000s
⊕ DDJ1, Ref1	18.375ps	0.0000s	18.375ps	18.375ps	0.0000s	1	0.0000s	0.0000s
⊕ DCD1, Ref1	1.0108ps	0.0000s	1.0108ps	1.0108ps	0.0000s	1	0.0000s	0.0000s

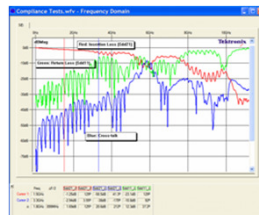
Clear X
Recalc
Single
Run
Show Plots

SDLA provides Complete Signal Visibility

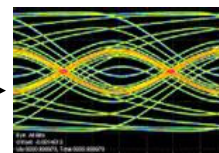
- SDLA provides all functionality relating to Serial Data Link modeling in a single package (embed, de-embed, equalization)
- With Tektronix SDLA you can view the waveform and/or eye diagram at all stages in the link
- Supports S-parameters and other linear model descriptions of a system as well as IBIS-AMI models (industry standard for behavioral modeling of links)



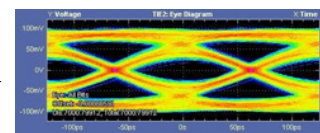
Signal Acquired from Compliance Board



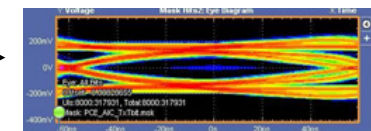
Embed the Add-In Card Compliance Channel



Closed Eye due to the Channel



Apply the CTLE



Apply the DFE