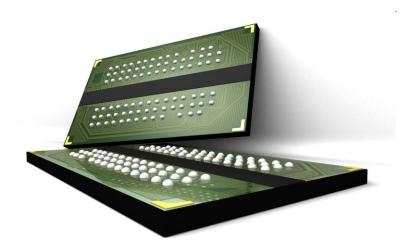
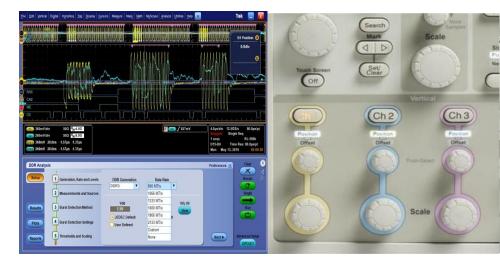
Memory Interface Verification and Debug

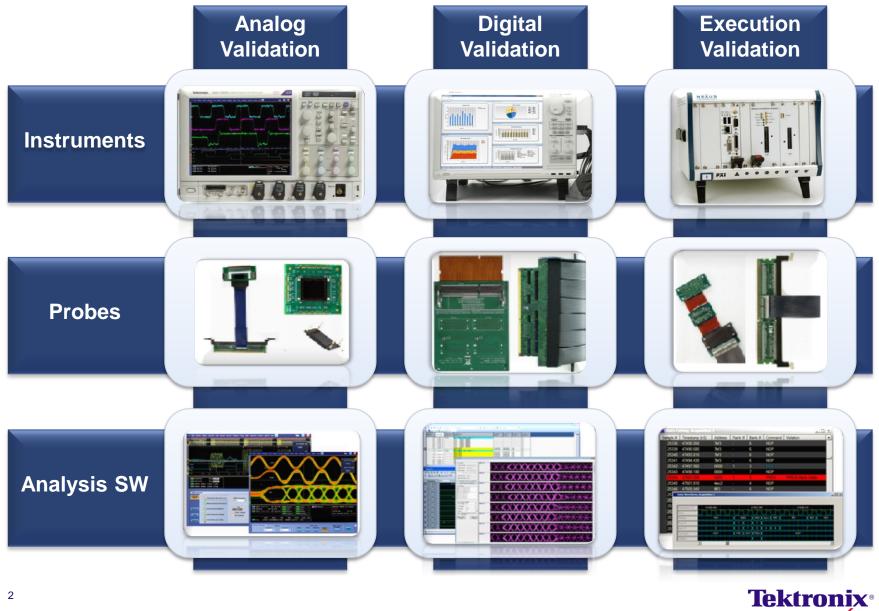
Customer Presentation Version 1.0







Memory Validation Continuum

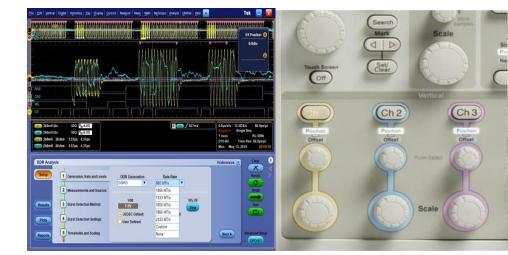


2

Memory Interface Analog Validation

Measure the analog signal characteristics; trtf, Vmin/max, jitter, eye size, crossover, strobe/clock alignment, etc.







DDRA Features and Benefits

Complete Solution for Memory Interface Physical Layer Test

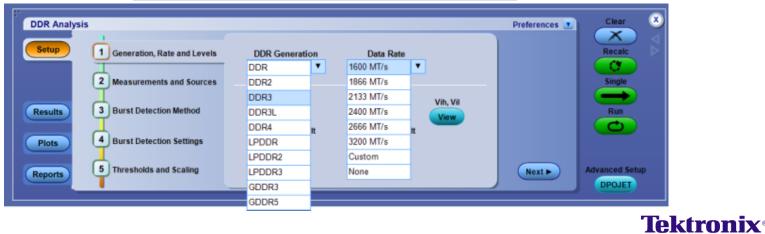


Feature	Benefits
Memory Validation and Debug	Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3 the newest standards targeted for Server/Computer and Mobile handsets.
Selectable Speed Grades	Support for various JEDEC specification defined speed grades as well as custom speeds
Auto Configuration Wizard	Easily set up the test configuration for performing the analysis.
Qualified Multi-Rank Measurements	Isolate measurements to a rank of interest by using the chip select signal in a multi rank configuration
Cycle Type Identification	Navigate and Timestamp all the READ and WRITE cycles in an acquired record using Search and Mark
Visual Trigger / Pin Point Triggering	Quickly trigger, isolate and capture events of interest with Pin-Point HW Triggering combined with Visual Trigger and Active Search and Mark capabilities in Tektronix Oscilloscopes, making them an indispensable tool for Memory Interface Validation.
De-embedding	De-embed the effects of the Interposers and Probes to provide more accurately representation of the signal.
Test Selection	Provides the ability to select the Memory specification and the Speed Grade against which the analysis needs to be done as well as individual tests or group of tests to perform targeted analysis.
Reporting	Automatically generate consolidated reports that include pass/fail results, statistical measurement information as well as details about the test setup
Conformance and Debug	Quickly switch into debug mode in case a system fails conformance tests and use the DPOJET jitter analysis package
Probing Solutions	P7500 Trimode Probe Family and Micro-Coax Tips combined with Nexus Technology Interposers for various memory standards and packaging types results in a complete probing system that provides easy access to memory interface signals and allows making differential, single-ended, and common mode measurements accurately and definitively
Digital Channels on MSO	Address/Command signals acquired on the digital channels of the Mixed Signal Oscilloscope can be used to precisely qualify bus cycles or events of interest as well as perform timing measurements
Analysis and Debug Tools	Tektronix provides a broad range of tools for Electrical Test, Logic Debug and Execution Validation.

Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings
- JEDEC Standards specify measurements & methods

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212



Test Setup and Configuration

- All the tests are logically grouped based on the input source requirement
 - READ
 - WRITE
 - CLOCK
 - ADDR/CMD
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.
- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.

DDR Analysis						Preferences 💽	Clear 🗴
Setup	Generation, Rate and Levels	Measurement Type Write Bursts		easureme Sources	ent		Recalc
	2 Measurements and Sources	Write Bursts Measurements Tota Eye Height	DQS DQ	Ch 1 Ch 2	•		Single
Results	3 Burst Detection Method	 ✓ Data Eye Width ⊕ ✓ Differential DQS 	СК	Ch3	•		Run
Plots	4 Burst Detection Settings	 ✓ Single Ended DQS ✓ Slew Rate DQ 				Prev	Show Plots
Reports	5 Thresholds and Scaling	Cannot select Diff and SE measurements at th	⊻ e same tii	ne		Next ►	Advanced Setup

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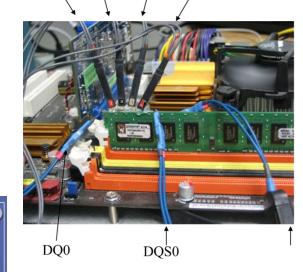
Burst Detection

- Read / Write bursts are automatically detected for analysis purposes
- Several different techniques are used for Read/Write Burst Separation
 - DQ/DQS phase alignment: DQ and DQS have different phase relationship in Read and Write bursts
 - CS, Latency + DQ/DQS Phase Alignment: CS is used to quality the occurrence of a burst, followed by DQ/DS phase relationship to distinguish between Read/Write
 - Logic State + Burst latency: The command bus probed using the digital channels on the MSO is used to identify Read/Write commands on the command bus are quality and distinguish Read and Write bursts
- Options are provided to adjust the levels to improve burst detection in systems with lower signal integrity

DDR Analysis			Preferences 💽	Clear
Setup	Generation, Rate and Levels	Burst Detection Method • DQ/DQS Phase Alignment		Recalc
	Measurements and Sources	 Chip Select, Latency + DQ/DQS Phase Alignment Logic State + Burst Latency 		Single
Results	3 Burst Detection Method			Run
Plots	4 Burst Detection Settings	Burst auto identified based on DQ\$/DQ phase relationship	< Prev	Show Plots
Reports	5 Thresholds and Scaling	Measurement results may vary as the Ref levels are changed	Next ►	Advanced Setup



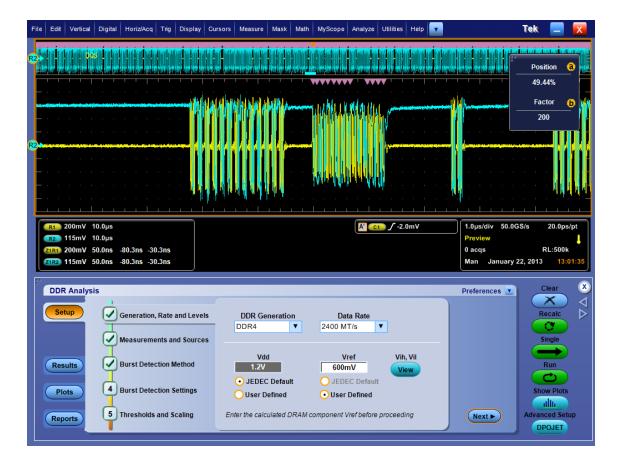
RAS# WE# CAS# CS#





Burst Detection

- Easily Identify, Mark & Measure all Read / Write bursts
 - Scroll through marked reads / writes across the entire waveform record
 - Measurements performed on ALL Reads/writes within an acquisition





Reports

- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes
 - Measurement results
 - Pass/Fail test results based on specification values
 - Summary and detail plots
 - Oscilloscope screenshots
 - Measurement and Instrument configuration summary
- Report contents are user definable content
- Provision to append more results later

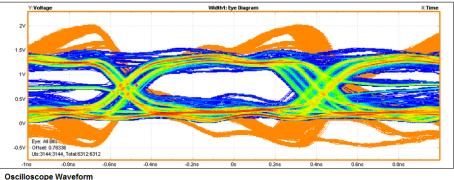
Measurement Results

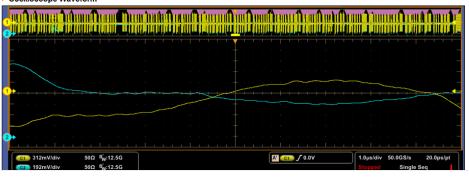
Description	Mean	Std Dev	Max	Min	р-р	Population	Max-cc	Min-cc
Data Eye Height, DQ, DQS	485.04mV	53.316mV	522.74mV	447.34mV	75.400mV	2	0.0000V	0.0000V
Current Acquisition	522.74mV	V0000.0	522.74mV	522.74mV	V0000.0	1	0.0000V	V0000.0
Data Eye Width, DQ, DQS	761.25ps	15.916ps	772.50ps	749.99ps	22.509ps	2	0.0000s	0.0000s
Current Acquisition	772.50ps	0.0000s	772.50ps	772.50ps	0.0000s	1	0.0000s	0.0000s

• Pass/Fail Summary There were no pass/fail limits defined for the selected measurement(s).

Plot Images

Measurement Plot(s)



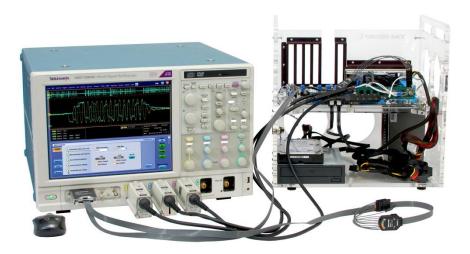


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Overall Test Result:	🕴 Fail				View	Summary	Expand	Recalc
Description	Pass/Fail	Mean	Std Dev	Max	Min	р-р	Population	
🛨 Data Eye Width, DQ		277.69ps	0.0000s	277.69ps	277.69ps	0.0000s	1	
🛨 tDH-Diff(base), DQS	. 📀 Pass	517.93ps	78.008ps	908.52ps	214.20ps	694.32ps	856	Single
🛨 tDQSH, DQS	Pass	1.2500ns	6.7707ps	1.2692ns	1.2249ns	44.286ps	898	
🛨 tDQSL, DQS	Pass	1.2479ns	6.6527ps	1.2663ns	1.2240ns	42.297ps	783	Run
🗖 tDS-Diff(base), DQS	. 🔞 Fail	581.49ps	132.47ps	929.69ps	6.8603ps	922.83ps	951	
High Limit								Show Plots
Low Limit	🔞 Fail				75.000ps			
Current Acquisition		581.49ps	132.47ps	929.69ps 🔍	6.8603ps 🔍	922.83ps	951	Advanced Setup
	 Description 	Description Pass/Fail Data Eye Width, DQ tDH-Diff(base), DQS	Description Pass/Fail Mean Data Eye Width, DQ 277.69ps tDH-Diff(base), DQS	Description Pass/Fail Mean Std Dev 	Description Pass/Fail Mean Std Dev Max 	Description Pass/Fail Mean Std Dev Max Min 	Description Pass/Fail Mean Std Dev Max Min p-p 	Description Pass/Fail Mean Std Dev Max Min p-p Population

Beyond DDRA

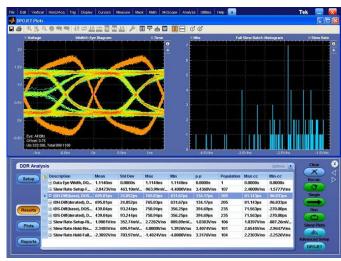
- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
 - DPOJET advanced Jitter analysis toolkit
 - PinPoint Triggering
 - Visual Trigger
 - Mask Testing
 - Advanced Search and Mark



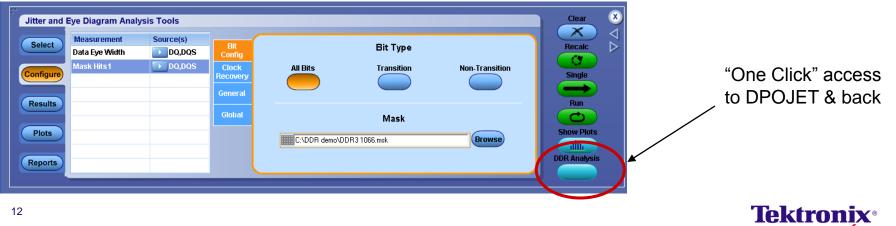


Signal Analysis & Debug DDRA + DPOJET

- DDRA is not a closed tool seamlessly links directly to DPOJET for measurement analysis
- Opportunity to change or fine-tune settings, add new measurements as needed

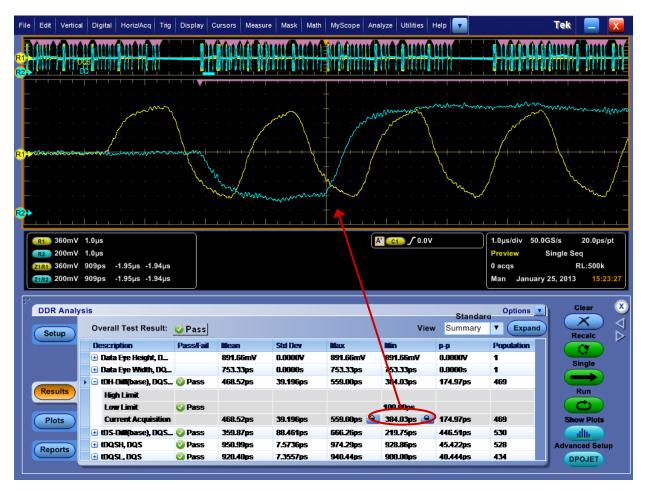


- DPOJET powerful measurement engine for DDRA
- All settings are explicit you can see them and change them.



DPOJET Debug Tools

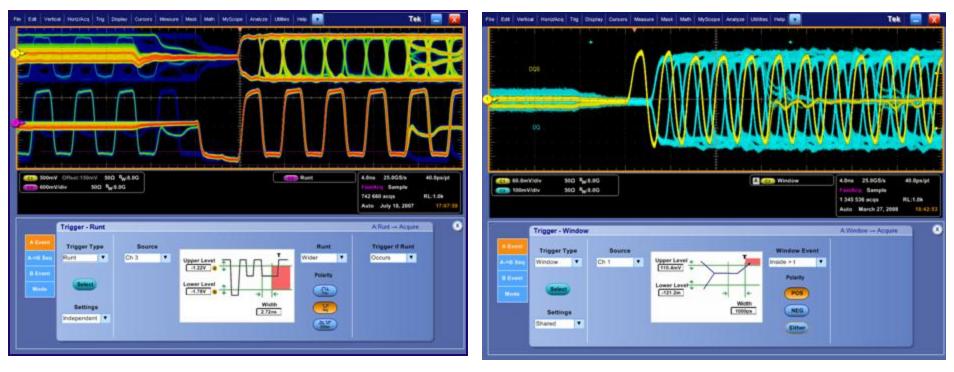
- "Find Worst Case Events" feature
 - Zoom to waveform from Min / Max for each measurement





Pinpoint Triggering

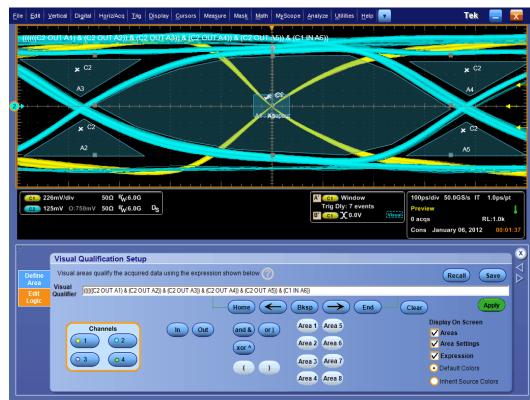
- Fastest way to solve sophisticated Memory signaling issues
 - Superior real-time insight into the complex signaling
 - DPX (FastAcq) and Pinpoint Triggering gives you "the power to see what others can't"
 - FastAcq shows any disparities on signals, like infrequent glitch's



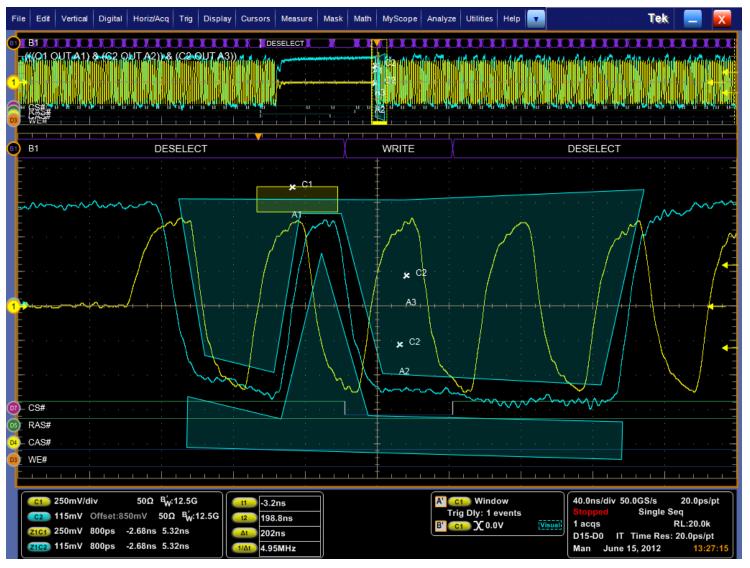


Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 verticies
- Areas are "keep in" or "keep out" and can be applied to either trigA or trigB.
- Can be used to
 - Separate Read / Write Bursts
 - Separate ranks
 - Look for pattern dependencies
 - Enable persistence eye diagrams



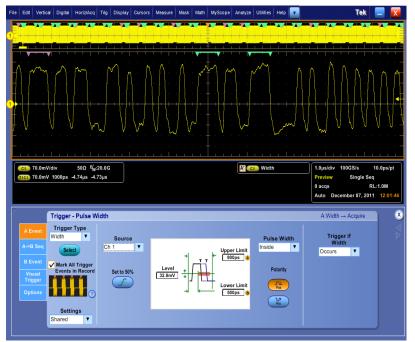
Visual Trigger Used For DQ Pattern Detection 010000X Pattern

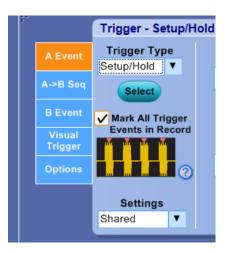


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Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
 - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
 - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA







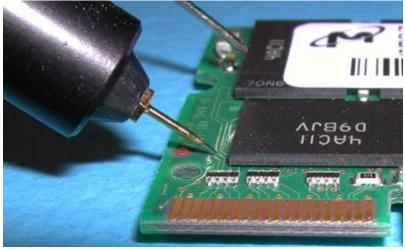
Advanced Search and Mark

- Tabular Results and Navigation
 - Events by Type read/write or other events _
 - Time stamps, delta-times between events —
 - Intuitive navigation Zoom on the burst of interest _
- 'Stop on Found' works as a pseudo-trigger mode

Select Infigure	1 2	DD	T ype IR Read R Write	12221473	12	Count 130 157							
	Re	sult	ts: Ma	rk Table				_					
Select			Index	Туре	Src	Location		Ti	me Del	ta		Description	
Scieut			Constant's			CREASE ADD DOL	sec	ms	us	ns	ps		
		_	1	DDR Write	C1	-8.579us						DDR3 - WRITE - 1.066G	
Configure		Z2	2	DDR Write	C1	-8.496us	000	000	000	082	480	DDR3 - WRITE - 1.066G	
		74	3	DDR Write	C1	-8.414us	000	000	000	082	520	DDR3 - WRITE - 1.066G	
Results		Z1	4	DDR Write	C1	-8.331us	000	000	000	082	500	DDR3 - WRITE - 1.066G	
			5	DDR Write DDR Write	C1 C1	-8.29us	000	000	000	041	240	DDR3 - WRITE - 1.066G DDR3 - WRITE - 1.066G	
View			0	DDR Wille	IQ1	-8.208us	000	the state of the s	000	-		DDR3- WRITE - 1.0000	8
Mode			Total	Marks: 2	87	ΔZ1,Z2 ΔZ2,Z3 ΔZ1,Z3	000	000	000	164	000		
-		_	> 6	ch Marks	_	_	_			-		All Marks	View
		Sav	e) (S	ave All) Cle	ar)	(Digits :	>>)			(<<	Digits	Export Clear	Count
		Jun			_	bigits	2			0	Figits	Contract Contract	Count

Memory Probing

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- Memory Components use BGA or PoP Packages
 - Reduces the parasitics, enabling performance at higher speeds
 - Mandate from JEDEC
- Probing a BGA or PoP package is Difficult
 - Unable to probe at the Balls of the Device
 - Probing at a connector, trace, or a via is not the same as probing at the device
 - Not a true representation of the signal

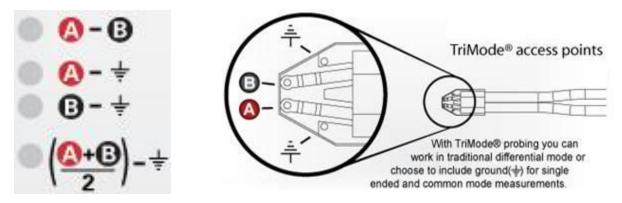


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*Courtesy Micron Technologies

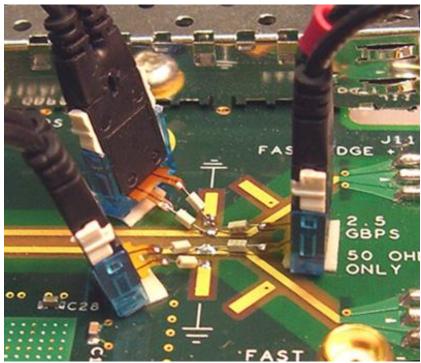
TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
 - Traditional differential measurements: V+ to V-
 - Independent single ended measurements on either input
 - V+ with respect to ground
 - V- with respect to ground
 - Direct common mode measurements: ((V+) + (V-))/2 with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!





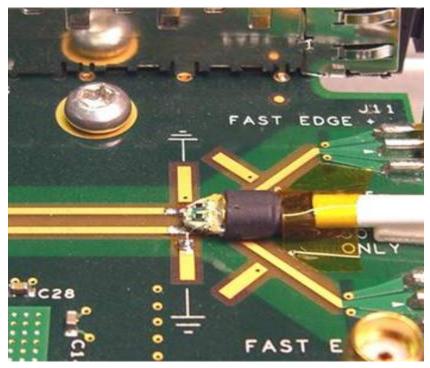
Before and After



Before TriMode Probing

Probe for Differential
 Probes for SE and Common Mode
 or

1 Probe Soldered and Re-soldered 3 times 2 Probes for Common Mode



After TriMode Probing

1 Probe and 1 setup for Differential, SE and Common Mode



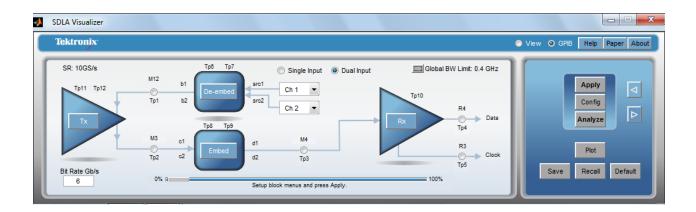
Memory Component Interposers

- Provide easy access to signals of Interest
- Controller Impedance path with embedded resistor for good signal Integrity
- De-embed filters to remove effects of interposer tap trace
- SPICE model available upon request for simulation and analysis

	Memory Standard	Supported Form Factors	Interposer Types
	DDR2	- BGA	Socketed InterposerDirect Attach Interposer
	DDR3	- BGA	 Socketed Interposer Direct Attach Interposer MSO DIMM Interposer Instrumented DIMM
	DDR4	- BGA	 Socketed Interposer Direct Attach Perimeter Interposer MSO DIMM Interposer Instrumented DIMM
	LPDDR2	- BGA - PoP	Socketed InterposerPoP Interposer
	LPDDR3	- BGA - PoP	Socketed InterposerPoP Interposer
22	GDDR5	- BGA	Socketed InterposerDirect Attach Interposer

De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will available for the interposers upon request.
 These de-embedding filters are developed assuming nominal values
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used





Memory Interface Digital Validation

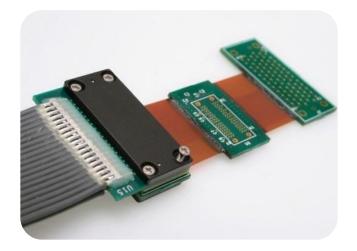
Measure the digital logic state and cycle based timing characteristics for diagnostic and troubleshooting purposes

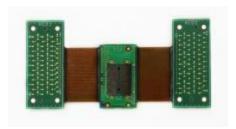




DDR4 Memory Component Interposers

- MCI's are used for probing signals from individual Memory Components
- Comes with a Custom Socket that needs to be soldered to Target system
- Quickly swap TLA & oscilloscope interposers on the same target. Quickly move interposers to different target.
- No special footprints or special routing requirements
- Memory Component Interposer Types
 - Logic Analyzer and Oscilloscope
 - Direct Attach or Socketed interposers
 - x4/x8 and x16 Memory Component types

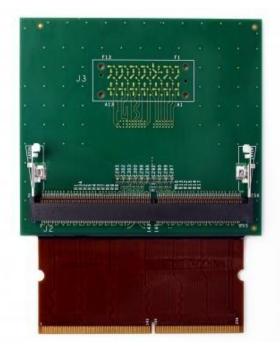






DDR4 ACC Interposers

- Protocol / Execution Validation
 - DIMM and SODIMM Interposers
 - Targeted for protocol compliance analysis
 - Automated Setup
 - Use with Nexus Compliance Analysis S/W
 - Compatible with P6960HCD or NEX-PRB1XL







Introducing New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

Gain Unprecedented Visibility Into Your DDR3/4 Signal Activity





SODIMM Interposer

Collaborative design combining years of Logic Analyzer acquisition and DDR3 probing experience between Tektronix and Nexus Technology



New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

- Provides significant performance improvements to DDR3 probing
 - Integrates Tektronix ultra-high performance SiGe Hybrid ASIC technology
 - Compensation for platform trace loss on writes
- Improved interposer input impedance (5.2k to 0.73V)
 - Reduces load on target with minimal effect on bus
 - Provides an accurate representation of the signal on the target
- Enables probing DDR3/4 speeds at 2400MT/s and beyond
- Enables probing lower voltage signals on LVDDR3/4
- Interposers compatible with UDIMM, RDIMM, LRDIMM

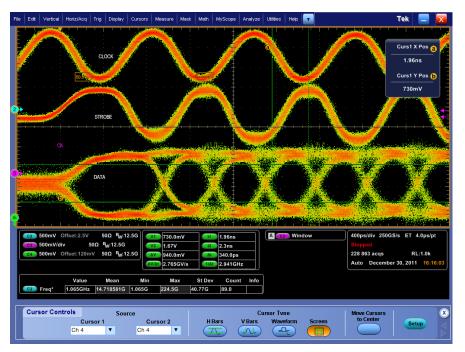


Scope Screenshots at DDR3 2133MT/s – Writes

OLD Interposer

File E	dit V	'ertical	Horiz/Acq	Trig	Display	Cursors	Measure	Mask M	ath MyScop	e Analyze	Utilities	Help		DSA71254	Tek	📃 💌
						CLOCK			^		`				2.38	Y Pos (b
E						منغن سنه		and the second					in in the second second			
						STROBE							Alter and A			
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2	and the second	Si Si	and Longenham					2000	6. 			Street,		Neta: San tan Kuta	See .	
			Offset:110r		DΩ ^B W:12		1 3.67V		1 2.38ns		A C3	Trans		400ps/div 2500	GS/s ET	4.0ps/pt
			Offset:1.86 Offset:2.41		0Ω ^B W:1; 0Ω ^B W:1;		V2 3.781 V 110.5 VA1 708.3	-	12 2.536r ▲t 156ps 1/∆t 6.41G					Stopped 2 903 acqs Auto January		L:1.0k 10:58:52
C	🗩 Fr	eq*	Value 1.067GH		Mean 882707G	Min 1.041G	Ma 11.83G		Dev Cou 3M 211.0							
f c	urso	r Cont		rsor 1	Sour		ursor 2		H Bars	Ca V Bars	ursor Tvo Wavef		creen	Move Cursors to Center	Se	

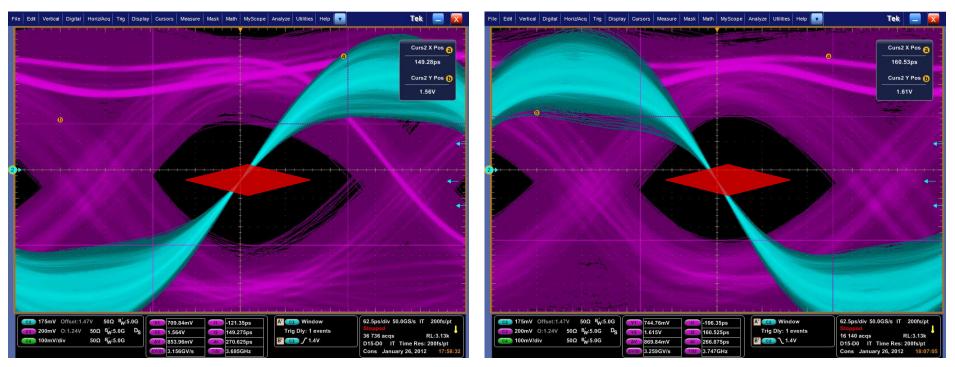
NEW Interposer







Write Data Eye - DDR3 2400MT/s



Write data eye, rising strobe edge, 853mV x 270ps Write data eye, falling strobe edge, 869mV x 266ps



Represents minimum TLA7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.



Scope Screenshots at DDR3 2133MT/s - Reads

OLD Interposer

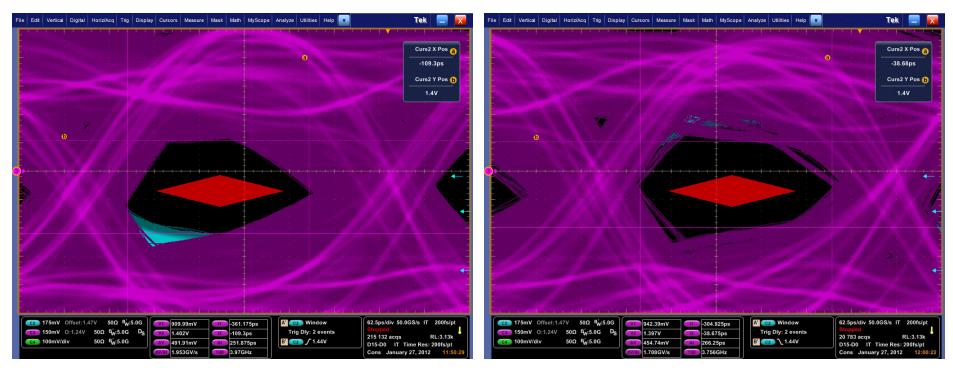
NEW Interposer





Tektronix®

Read Data Eye - DDR3 2400MT/s



Read data eye, rising strobe edge, 492mV x 252ps Read data eye, falling strobe edge, 454mV x 266ps



Represents minimum 7BB4 eye size, 180ps x 200mV

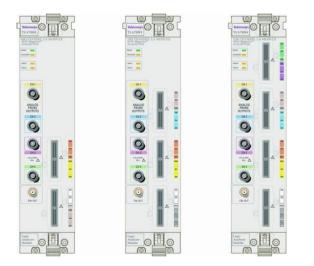
NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.



TLA7BBx Logic Analyzer Modules

Proven Technology for Analyzing DDR3 SDRAM

DIGITAL CHARACTERISTICS	TLA7BB2	TLA7BB3	TLA7BB4			
Digital Channels	68	102	136			
High Speed Timing (MagniVu)	50GS/s (20ps)					
Deep Memory Timing	Up to 6.4GS/s					
State Speed	Up to 1.4GHz/3.0Gbps					
Memory Depth	Standard 2Mb, Maximum 64Mb					
Probes	All P68xx and P69xx					
iCapture (Analog Mux)		3 GHz				

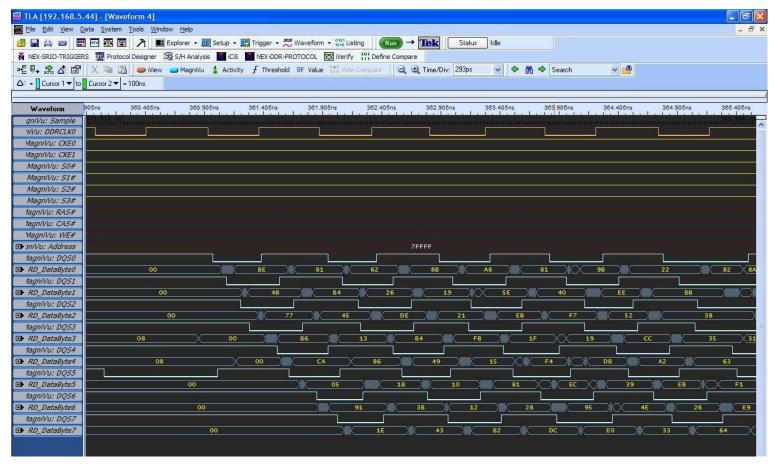


- Preserve investment in TLA7BBx modules
- Enable higher DDR3 speed support with new interposer



MagniVu 20ps (50 GS/s) High Speed timing

Industry Leading Sampling Resolution

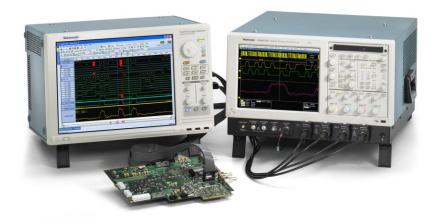


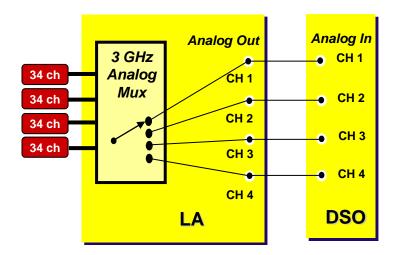
- 50GHz timing analysis on every channel
- Acquired simultaneously and time-correlated with state acquisition data
- Enables acquisition and debug of S/H violations, glitches, and other timing violations
- Reveals fly-by command/address/control bus timing



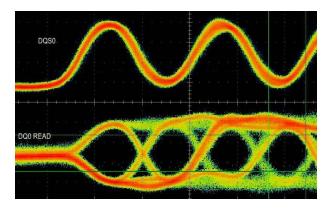
Analog Mux, iCapture

Enables Signal Integrity Troubleshooting





- Unrivaled capability of the TLA that provides single-point digital and analog probing
- No need to separately probe with a scope, as probing done through the interposer
- Walk through all the signals on your DDR bus in less than 15 minutes to review channel behavior and isolate any potential problems
- Quickly perform detailed analog characterization on signals of interest using a scope component interposer

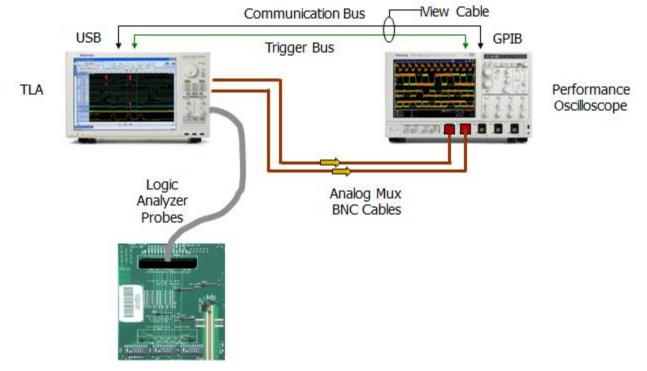




iView

View Correlated Analog & Digital Characteristics in the Same Display

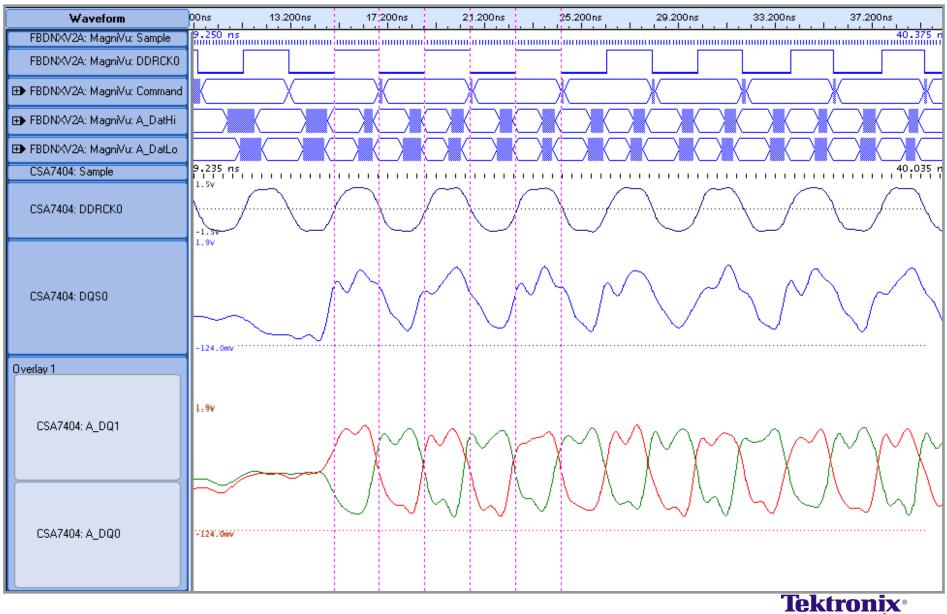
- Unique capability on the TLA that provides time correlated state acquisition, high-speed MagniVu timing acquisition, and analog scope capture results on the same screen.
- Capture events that occur in analog or digital domain through cross triggering
- Enables cross domain analysis by quickly capturing and isolating potential problems





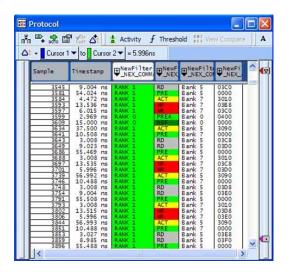
iView

Correlated High-Speed MagniVu Acquisition & Scope Capture Data Example



TLA - Initial Setup

- New Fast & Easy Setup
 - Quick and easy connection
 - Fast software setup
 - No calibration needed for CMD/ADDR/CTRL
 - Automated and graphical DQ data calibration
 - Up and running acquiring ALL data in 15-30 minutes!
 - Identify problem channels at the same time!



- Load the TLA Software
- Load the Support Package
- Ready to Acquire CMD / ADDR / CTRL!

File Edit View System Too		
🙆 📑 📇 📼 👘 📰 📼		
NEX-SRIO-TRIGGERS 🗟 S/H	Analysis 🐯 iVerify 111 Define Compare Run → TEK	
	System: TLA78B4+8B4 Looic June Bayer See 5.9 Diable Ort See 5.9 Open Setup Window Ort Setup Trig Default Module Load Module Save Module 4.5 Load Support Package Rename Properties Duplicate Module Config Duplicate Module Config	



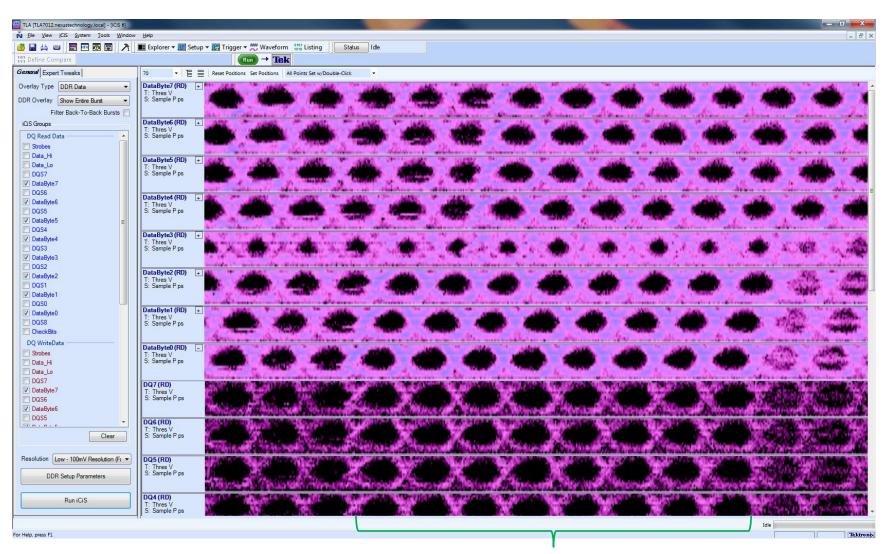
iCis Overview

- Goals of iCiS
 - Make LA memory tuning easier and quicker
 - Less dependency on platform specific DQ valid regions
 - Less dependency on DQS placement
 - Put more power in the users hands
 - Allow both Vth and sample point to be determined at same time
 - Quick check of signal integrity on the memory bus
 - Allow tuning of address and command signals
 - Simultaneous tuning of Read and Write sample points
 - Double mouse click method to set Vth and sample point for all signals
 - Single tuning tool leveraged for DDR3, DDR4, LPDDR2/3
- User control
 - DDR bus parameters
 - Voltage sweep step size
 - Voltage sweep range
 - Which signals to tune
 - Address bit(s)
 - Command bit(s)
 - DQ-byte lane or individual DQ
 - Read & Write, read only, write only



DDR3 Sweep

100mV Resolution, Full Burst Mode / 8 DQ Eyes, Reads



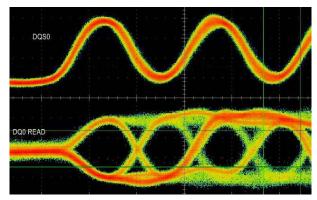
8 valid DQ eyes

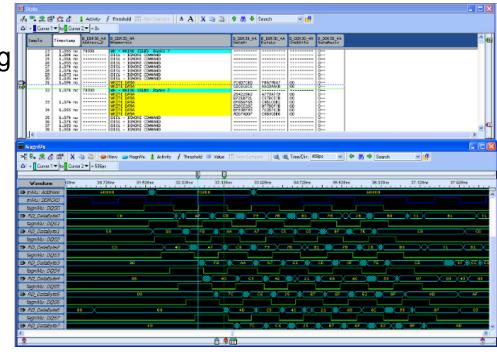


TLA Data Analysis

- State, MagniVu timing, & analog mux at your fingertips
- Compliance analysis tools
 - Fast setup
 - Comprehensive coverage and violation detection

-					
	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. v
R2 R1 R0	NA	NA	NA	NA	959,880
R2 R1 R0		10,273,985	2,106,353		26,250
e re ri <mark>ro</mark>	7,441	878,808	123,227	3.3	7,200
3 R2 R1 R0					5,625
B R2 R1 R0	NA	NA	NA	NA	70,200,000
3 R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
B R2 R1 <mark>R0</mark>	114,121	8,169,101	6,001,631	3.7	110,000
3 R2 R1 <mark>R0</mark>	42,969	2,839,180	267,945	14.6	
B R2 R1 <mark>R0</mark>	42,969	2,839,180	267,945	-99.9	70,200,000
3 R2 R1 <mark>R0</mark>			20,254		
RE RI RO	13,066	316,308	170,537	16.1	11,250
2 RI RO					20,625
T. RO	37,383	326,054	162,946	10.8	33,750







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TLA- Example State / MagniVu Display

- Command / Address / Control
- DQ Read and Write Data
- Up to 64M-sample state memory
- Simultaneous
 50GHz MagniVu timing

III. State				
👬 🍄 🍰 🖼 🎎 🔥 🚦 Activity 🖌 Threshold 👯 View Compare 🛛 A 🗛 🗶 🐚 👪	🔶 🔥 🕹 Searc	rch 🔽 🍱		
Sample Timestamp B_DDR3D_4A B_DDR3D_4A Address_D Mnemonics	B_DDR3D_4A B_D DataHi Dat	DDR 3D_4A B_DDR 3D_4A taLo ChekBits	B_DDR3D_4A DataMasks	
23 1.055 ns 70308 PML = WAITE (SL#) Pan/Ls 7 25 1.054 ns	7C4D7C4D FBA C6C5C6C5 AAC 25422542 A77 B721B721 C57 6F686F68 C0B E26CE2C 0F7 BF93BF93 7E2 AD07AD07 C6B	A7FBA7 CDA4CD 00 278479 00 784579 00 784579 00 28578 00 20578 00 2	0 0 0 0 0 0 0 0 0 0	× (C
Magni¥u ≫E ♥+ 歳 ☆ @ X => @ ● Mew ■ Magni¥u ≵ Activity ƒ Threshold OF Value } △t +] Cursor 1 ▼ o] Cursor 2 ▼ = 536ps	View Compare	्रे 🔍 Time/Div: 4	08ps 💌	◆ 例 ◆ Search
ĮĮ				
Waveform 28ns 30.728ns 31.528ns 32.328ns 33.128n	ns 33.928r	ins 34.728ns	35.528	3ns 36.328ns 37.128ns 37.928ns
miVu: Address 60000 70300 70300				60000
IniVu: DDRCKO				
1agniVu: DQS0				
RD_DataByte0 C0 A7 C0 A7 C0	X (<u>79</u> X	<u>78</u> <u>B1</u>	K <u>78</u> X	X 28 80 X 31 X B1 X 31
1agniVu: DQS1				
RD_DataByte1 S0 10 FB A	A A7	<u> </u>		
1agniVu: DQS2				
RD_DataByte2 C0 A7	<u></u> 7	<u>9 X 78 XX </u>	81 7	
1agniVu; DQS3				
RD_DataByte3		<u>A7 X C5 X</u>		
1agniVu: DQS4				
RD_DataByte4		42 21	68	6C 93 07 03 43 03
1agniVu: DQS5				
	rc C6	25 87	6F	
1agniVu: DQS6				
RD_DataByte6 88 08	40 X C	C5 42 XX	21	68 C C 93 C 07 C 03
1agnIVu: DQS7				
RD_DataByte7 40	7C	C6 25	87	GF E2 BF AD
<				
	m			A

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Memory Interface Execution Validation

Measure the bus command and control timing sequences, and compare them to a specification or evaluate them as indicators of bus utilization or performance

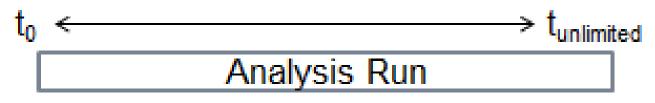


tat	Num.	Name	Occurences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
)	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
	23	MRS Settle			RT RE RE RE RE RE RE RO	NA	NA	NA	NA	22,500
	24	MRS Burst			R7 R6 R5 R4 R3 R2 R1 R0					
	25	sSREF Time			RT RE RE RE RE RE RE RE					7,500
	26	WR Burst			R7 R6 R5 R4 R3 R2 R1 R0					
	27	RD to WR(A) Separation	13,386		RT RE RE RE RE RE RE RI RO			64,028	70310809855578300.0	13,118
	28	PDX Slow Exit			R7 R6 R5 R4 R3 R2 R1 R0					
	29	Rank DLL Reset to RD(A)			RT R5 R5 R4 R3 R2 R1 R0					959,700
	30	WR to RD(A) Separation			R7 R6 R5 R4 R3 R2 R1 R0					
	31	RD Burst	22,075		RT RE RE RE RE RE RE RI RO			164,742	128102389400761000.0	7,200
		sPD Time Min.			R7 R6 R5 R4 R3 R2 R1 R0					
	33	sPD Time Max.			R7 R6 R5 R4 R3 R2 R1 R0					70,200,000
	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
	35	sREF Time			RT RG R5 R4 R3 R2 <mark>R1 R0</mark>			5,297,689	8384883669867880.0	110,000
	36	sACT Time Min.			R7 R6 R5 R4 R3 R2 R1 R0					
	37	sACT Time Max.	19,499		RT RE RE RE RE RE R1 RO			265,733	13138706605106.2	70,200,000
	38	ACT to RD(A)/WR(A)			R7 R6 R5 R4 R3 R2 R1 R0					
	39	RD to PRE(A)	15,227		RT RG RS R4 R3 R2 R1 R0			175,659	82029278164841400.0	11,244
	40	RD to ACT			R7 R6 R5 R4 R3 R2 R1 R0					
	41	WR to PRE(A)	4,217	00	RT RS RS R4 R3 R2 R1 R0	00	00	164,649	27343092721613700.0	33,732
	42	WR to ACT			R7 R6 R5 R4 R3 R2 R1 R0					
	43	CKEx Signal After DLL Reset	00	00	RT RE RE RE RE RE RE RO	NA	NA	NA	NA	959,700



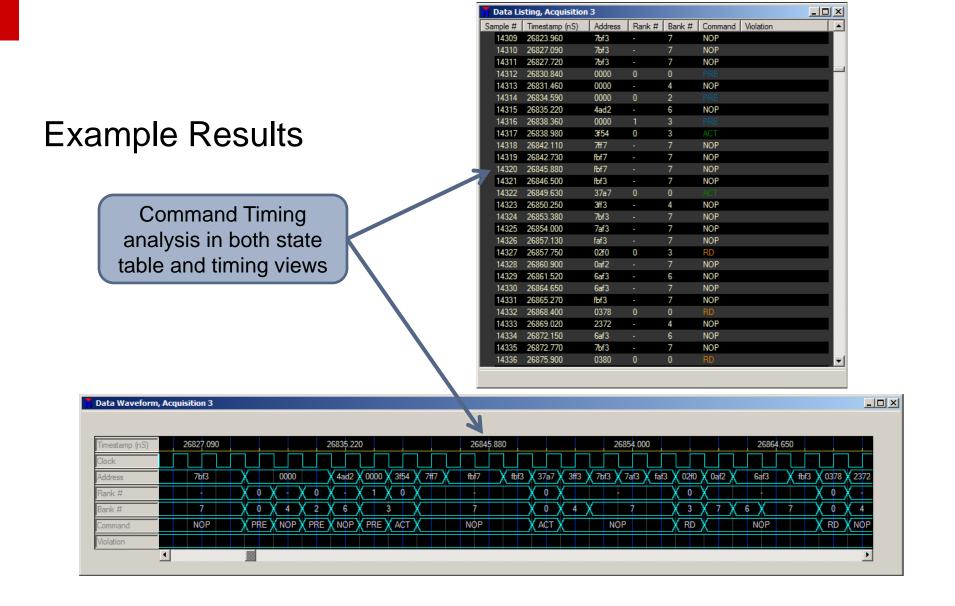
What's unique about Execution Validation

- Typical instrument use a post-capture model
 TRIGGER → ACQUIRE → ANALYZE
- Execution Validation use model



- Two equipment options
 - 1. Logic Analyzer S/W automates acquisitions
 - 2. Memory Compliance Analyzer Real-time Analysis







Specifications Published in JEDEC Standards

JEDEC STANDARD



DDR3 SDRAM Specification

JESD79-3E

192	Pages
118	Figures
80	Tables



What specs are checked?

Num.	Name	Description
1	CMD w/sSREF Rank	Sequential check. A non-NOP/DES command can not occur on a self-refreshing rank.
2	SRE w/sACT Rank	Sequential check. A Self-Refresh Entry (SRE) command can not occur on an active rank.
3	MRS w/sACT Rank	Sequential check. An Mode Register Set (MRS) command can not occur on an active rank.
4	RD(A)/WR(A) during MRS	Sequential check. A read (RD or RDA) or write (WR or WRA) command can not occur during rank MRS cycle.
5	CMD w/sPD Rank	Sequential check. A non-NOP/DES command can not occur on a powered-down rank.
6	RD(A)/WR(A) w/sREF Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during bank refresh.
7	ACT/REF w/sACT Bank	Sequential check. A activate (ACT) or refresh (REF) command can not occur on an active bank.
8	REF w/sACT Bank	Sequential check. A refresh (REF) command can not occur on an active bank that is reading or writing.
9	RD(A)/WR(A) to sPRE Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during on an inactive (precharged) bank.
10	d4ACT	The minimum time between any four activate (ACT) commands to the same rank must meet tFAW.
11	PDX Fast Exit	Power-Down Exit (PDX/PRX) to any valid command (PRE(A)/REF/ACT/MRS) must meet tXP.
12	SRX Exit	Self-Refresh Exit (SRX/PRX) to any command not requiring a locked DLL (PRE(A)/REF/ACT/MRS/SRE) must meet tXS.
13	dACT	The minimum time between two activate (ACT) commands must meet tRRD.
14	PRE(A) Rank Settle	Minimum time from a PRE(A) command to any valid command on the same rank (MRS/SRE) must meet tRP.
15	REF Before SRE	Sequential check. At least one refresh (REF) command is required between self refreshed (SRX to SRE).
16	SRE Separation from PRE(A)	If the last valid command received before a self-refresh entry (SRE) was any precharge PRE(A), then the separation between these two commands must meet tPREPDEN.
17	SRE Separation from REF	If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two commands must meet tREFPDEN.
18	SRE Separation from ACT	If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two commands must meet tACTPDEN.
19	SRE Separation from MRS	If the last valid command received before a self-refresh entry (SRE) was a mode register set(MRS), then the separation between these two commands must meet tMRSPDEN.
20	SRE Separation from WR	If the last valid command received before a self-refresh entry (SRE) was a write (WR), then the separation between these two commands must meet tWRPDEN.
21	SRE Separation from WRA	If the last valid command received before a self-refresh entry (SRE) was a write w/auto-precharge (WRA), then the separation between these two commands must meet tWRAPDEN.
22	SRE Separation from RD(A)	If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two commands must meet tRDPDEN.
23	MRS Settle	Minimum time from an mode register set (MRS) command to any other valid command that is not an MRS must meet tMOD.
24	MRS Burst	Minimum from the first to the next and subsequent mode register set (MRS) commands must meet tMRD.
25	sSREF Time	The minimum amount of time in self-refresh must meet tCKESR.
26	WR Burst	The minimum amount of time between write (WR(A)) commands must meet tCCD.
27	RD to WR(A) Separation	The minimum amount of time between read (RD) and write (WR(A)) commands must meet tNRTW.
28	PDX Slow Exit	Power-Down Exit (PDX/PRX) Slow Exit (MRS_A12 bit low) to read (RD(A) command must meet tXPDLL.
29	Rank DLL Reset to RD(A)	Read (RD(A)) must wait tDLLK after reset.
30	WR to RD(A) Separation	The minimum amount of time between write (WR) and read (RD(A)) commands must meet tNWTR.
31	RD Burst	The minimum amount of time between read (RD(A)) commands must meet tCCD.
32	sPD Time Min.	The minimum amount of time a rank must stay in power-down (PDE to PDX) must meet tPDmin.
33	sPD Time Max.	The maximum amount of time a rank can stay in power-down (PDE to PDX) must meet tPDmax.
34	PRE(A) Bank Settle	Minimum time from a PRE(A) command to any valid command on the same bank must meet tRP.
35	sREF Time	The minimum amount of time in refresh must meet tRFC.
36	sACT Time Min.	The minimum amount of time a bank must stay active (ACT to PRE(A)) must meet tRASmin.
37	sACT Time Max.	The maximum amount of time a bank can stay active (ACT to PRE(A)) must meet tRASmax.
38	ACT to RD(A)/WR(A)	The minimum amount of time from a activate (ACT) command to a read (RD(A)) or write (WR(A)) command must meet tNARW.
39	RD to PRE(A)	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet tNRP.
40	RD to ACT	The minimum amount of time from a read (RD) command to a activate (ACT) command must meet tNRA.
41	WR to PRE(A)	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet tNWP.
42	WR to ACT	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tNWA.
43	CKEx Signal After DLL Reset	Rank CKEx must remain high tDLLK time after a DLL Reset.



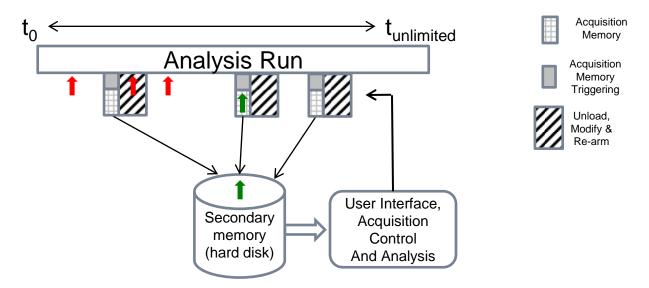
How are the event values set?

DDR System Setup	×	🔡 Complian	ice Timing Paramete	rs						
System Name DDR3-1600	Add Del Rename	Timing Para	meters DDR3-800D			▼ Add	Del	Rename		
	/Writes	tACTPDEN	1	ck	tRASmin	37500	ps	tWRAPDEN	Derived	ck
DDR3-1600 DDR Spec. 0 800 MHz DDR Gock	Additive Latency	tCCD	4	ck	tRCD	12500	ps	tWTR	7500	ps
	Additive Latency Reserved (AL)	tCKESR	10	ns	tRDPDEN	Derived	ck	tXP	7500	ps
(Chip Selects)	CAS Write Latency (CWL)	tDLLK	512	ck	tREFPDEN	1	ck	tXPDLL	25	ns
Space	Burst Length	tFAW_1Kb	40	ns	tRFC_512Mb	90	ns	tXS	Derived	ck
× 8 Addressing Length	↔ Write Recovery (WR)	tFAW_2Kb	50	ns	tRFC_1Gb	110	ns	tNARW	Derived	ck
J High Temp. Env. (85C-95C)	egistered	tMOD	12	ck	tRFC_2Gb	160	ns	tNRA	Derived	ck
CKE Mapping		tMRD	4	ck	tRFC_4Gb	300	ns	tNRP	Derived	ck
8	# of Banks	tMRSPDEN	12	ck	tRFC_8Gb	350	ns	tNRTW	Derived	ck
536 M		tPDmin	7500	ps	tRP	12500	ps			ck
2144 I 1 KB	MB System Memory (64-bit) Page Size	tPDmax	70200	ns	tRRD_1Kb	10	ns	1		ck
Setup is valid 11	Read Latency (RL)	tPDmax_H	T 35100	ns	tRRD_2Kb	10	ns	1		ck
8	Write Latency (WL)	tPREPDEN	1	ck	tRTP	7500	ps			
13	Row Address Length (bits)	tRASmax	70200	ns	tWR	15	ns			
10	Column Address Length (bits)	tRASmax_H	HT 35100	ns	tWRPDEN	Derived	ck			Save
24	WRA Precharge Delay									
	Min. RDA Precharge Delay									
	Save									

- Standard system setups are provided, and can then be modified
- Once the memory system is setup, any timing parameter can be modified

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Post-Capture Protocol Compliance Analysis



- LA Memory Compliance Analysis Package enables automated sweeps of multiple transitions, which would result in violation detection over many acquisitions.
- When violations are occurring frequently the likelihood of capture increases and the analysis time decreases.
- However, near the edge of margin envelopes, intermittency increases, resulting in difficulty to observe and capture the event.



Results per Session & per Acquisition

Con	Compliance Parameters									
Stat	Num.	Name	Occurences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
?	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
?	23	MRS Settle	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	24	MRS Burst			R7 R6 R5 R4 R3 R2 R1 R0					22,500
?	25	sSREF Time	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	7,500
٥	26	WR Burst	13,386		R7 R6 R5 R4 R3 R2 R1 R0			168,523	128102389400761000.0	
@	27	RD to WR(A) Separation	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	64,028	70310809855578300.0	13,118
?	28	PDX Slow Exit			R7 R6 R5 R4 R3 R2 R1 R0					24,000
?	29	Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700
۰	30	WR to RD(A) Separation	22,075		R7 R6 R5 R4 R3 R2 R1 R0			910,959	35155404927789100.0	26,236
۰	31	RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,742	128102389400761000.0	7,200
?	32	sPD Time Min.			R7 R6 R5 R4 R3 R2 R1 R0					5,625
?	33	sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
8	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
۰	35	sREF Time	1,527	00	R7 R6 R5 R4 R3', R1 R0	00	00	5,297,689	8384883669867880.0	110,000
۰	36	sACT Time Min.	19,499		R7 R6 R5 P R3 R2 R1 R0				24595658764946000.0	37,500
۰	37	sACT Time Max.	19,4° 9	00	R7 R6 7 AR4 R3 R2 R1 R0	00	00	265,733	13138706605106.2	70 2.0,000
۲	38	ACT to RD(A)/WR(A)	19 36		R7 .6 R5 R4 R3 R2 R1 R0			19,999	70273310756988700.0	13,125
۰	39	RD to PRE(A)	17 ,227	00	A7 R6 R5 R4 R3 R2 R1 R0	00	00	175,659	820292781648414.0.0	11,244
?	40	RD to ACT	0	00	R7 R6 R5 R4 R3 R2 R1 R0				NA	20,614
e	41	WR to PRE(A)	4,217	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,649	27342252721613700.0	33,72
?	42	WR to ACT	00	50	R7 R6 R5 R4 R3 R2 R1 R0				A	20 ,14
?	43	CKEx Signal After DLL Res ² .	00	00	RT RE RE RE RE R1 R0	NA	NA	NA	NA	59,700

Event occurrences and details per Acquisition

Total Event Occurrences

Indiv	Individual Appraisition Details									
Stat	Run #	lime	Occurences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)		
8	1	10/10/2011 1:38:00 PM	2501	2	RT RE RE RE RE RE RE RI	00	00	1,038,534		
8	2	10/10/2011 1:38:05 PM			R7 R6 R5 R4 R3 R2 R1 R0			950,031		
	3	10/10/2011 1:38:11 PM	2545		R7 R6 R5 R4 R3 R2 R1 R0	00	00	1,029,172		
2	4	10/10/2011 1:38:16 PM	2722		R7 R6 R5 R4 R3 R2 R1 R0			936,685		
	5	10/10/2011 1:38:22 PM	2670		R7 R6 R5 R4 R3 R2 <mark>R1</mark> R0	00	00	970,402		
8	6	10/10/2011 1:38:28 PM			R7 R6 R5 R4 R3 R2 R1 R0			890,874		
8	7	10/10/2011 1:38:33 PM	2543	2	R7 R6 R5 R4 R3 R2 <mark>R1 R0</mark>	00	00	980,858		
8	8	10/10/2011 1:38:39 PM			R7 R6 R5 R4 R3 R2 R1 R0			896,071		
	9	10/10/2011 1:38:44 PM	2697	7	RT RE RS R4 R3 R2 R1 R0	00	00	880,706		
۰	10	10/10/2011 1:38:50 PM			R7 R6 R5 R4 R3 R2 R1 R0			920,762		

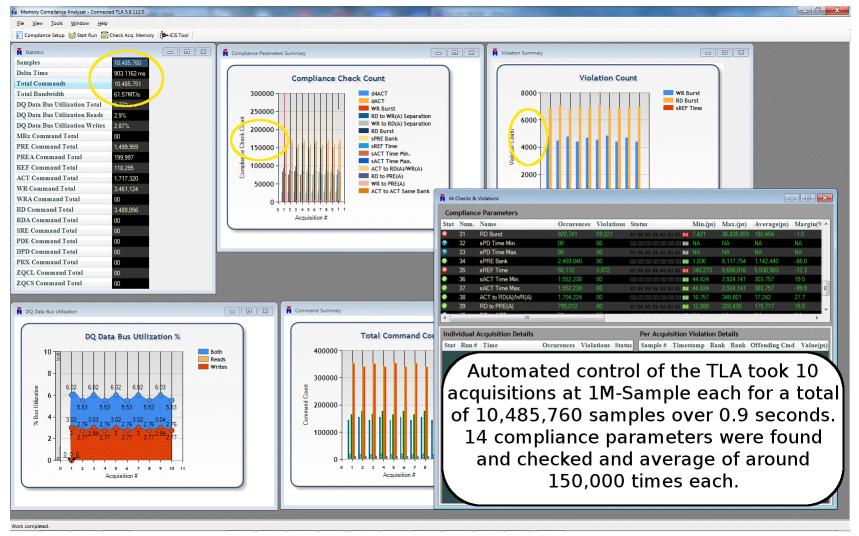


Individual Event Analysis

	All Checks & Violations								
	Compliance Parameters		_						
	Name O	Individual	- · · · ·	Average(ps) Mai		Spec. Value	(ps)		
	WR Burst 13 RD to WR(A) Separation 13	o oquicition and			02389400761000.0 0809855578300.0	7,200 13,118			
	PDX Slow Exit 00	acquisition and		NA NA	00000070000.0	24,000			
	Rank DLL Reset to RD(A) 00	event selection		NA NA		959,700			
	WR to RD(A) Separation 22, RD Burst 22,075	0.0 A 76]R5]R4]R3 R2 R1 R0			5404927789100.0 02389400761000.0	26,236 7,200	State of	nd Timina	
	sPD Time Min. 00			NA NA	102303400701000.0	5,625	State a	nd Timing	J
	sPD Time Max. 00			NA NA		70,200,0	before	and after	
	PRE(A) Bank Settle 26,733	29 R7 R6 R5 T R3 R2 R1 R0 (73310756988700.0	13,125			
	sREF Time 1,527 sACT Time Min. 19,499	00 R7 R6 R5 R4 3 R2 R1 R0 0			1883669867880.0 15658764946000.0	110,000 37,500	an	event	
	sACT Time Max. 19,499				38706605106.2	70,200,000	T	7	
	•								
	Individual Acquisition Details		Per Acquisition Vi	olation Details					
	Stat Run # Time	Occurences Violations Status	Sample # Timesta	mp Rank Banl	k Offending Cr	a Value(ps)	Margi		
	1 10/10/2011 1:38:00 PM	2501 2 RT R5 R5 R5	25344 4986080	1 1 3	PRE	3,731	-71,9		
	😒 2 10/10/2011 1:38:05 PM		114431 21690519	95 0 7	PRE	11,894	-9 4		
	3 10/10/2011 1:38:11 PM								
	 4 10/10/2011 1:38:16 PM 5 10/10/2011 1:38:22 PM 	_							
	 6 10/10/2011 1:38:28 PM 				Data Listing, Ac	mp (nS) Addr	ess Rank # Ban	k # Command Violati	
	7 10/10/2011 1:38:33 PM	2543 2 R7 R6 R5 R4 R5			25338 47490.0			NOP	
Data Wave	form, Acquisition 1				25339 47490.6			NOP	
					25340 47493			NOP	
		K			25341 474 44 25342 4497.5			NOP PRE	
Timestamp (n	(S) 47490.680	47501.290	47509.410		25343 7498.1			NOP	
Clock					25344 47501.2				A) Bank Settle
Address	7bf3 ¥	0000 X 0400 X 4ec2 X 6ff3 X	fff3 X fbf3 X	7bf3	25345 47501.9)10 4ec2	- 4	NOP	
Rank #					25346 47505.0		- 6	NOP	
			7		25347 47505.6		- 7	NOP	
Bank #		3 <u>X 7 X 0 X 4 X 6 X</u>			25348 47508.7 25349 47509.4		- 7	NOP NOP	
Command	<u>NÓP X</u> P		NÓP		25350 47512.5		- 7	NOP	
Violation					25351 47513.1			NOP	
				Þ	25352 47516.2	270 7bf3	- 7	NOP	
					25353 47516.8	390 7bf3	- 6	NOP	-
					00000 100000			100	

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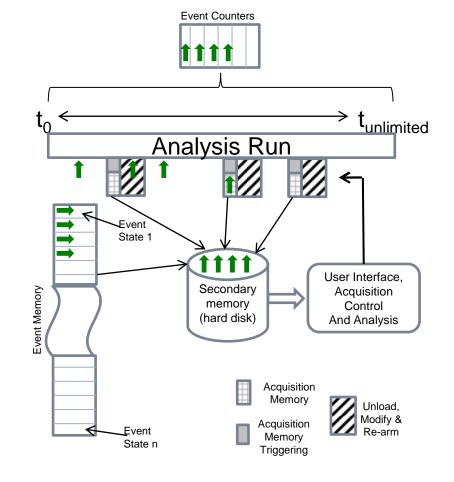
Multi-acquisition Automation Session



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Real-time Protocol Compliance Analysis

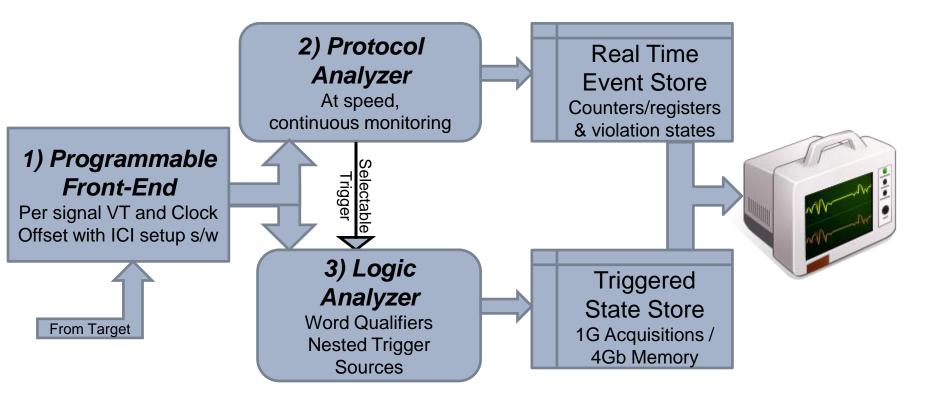
Event Counters and State Memory continue to update *AT-SPEED*, with results displayed in *REAL-TIME*, *While....*



...the Acquisition Memory is unloaded, analyzed and trigger re-armed



Real-time Memory Compliance Analyzer



DUAL INSTRUMENT PLUS PROGRAMMABLE FRONT-END



Memory Compliance Analyzer

REAL-TIME PROTOCOL COMPLIANCE ANALYSIS

- Analysis 160+ categories of JEDEC spec parameters
- Includes Power up/down, self-refresh and autoprecharge (RDA/WRA) analysis
- Timing and State analysis
- HTML reports / XML exporting



Real-time AND Post Capture Compliance Analysis

Command/Address



Programmable Front-End / High Speed Eye Diagrams

i¤ ≁icis			
iCiS Setup	0 ▼ 匡 ≣ Reset Positions Set Positions A	All Points Set w/Double-Click 🔻	
	-2,002ps -1,342ps -	682ps -22ps 638ps 1,298ps	1,9
	Bank Address – T: 0.900-0.938 V S: -31911 pSec		
Left Boundary -2000 ps	BA2 T: 0.900 V S: -319 pSec	BA2	
Right Boundary 2000 ps	BA1 T: 0.938 V	BA1	
Remember Previous Acquisitions Clear Previous Acquisitions	S: -11 pSec	BAO	
iCiS Groups (Double-click to select)	S: -154 pSec		
 ✓ Bank Address (3) ✓ Chip Select (2) 	S: -77 pSec	CS1	
Clock Enable (2) Control (3)	S: -77 pSec	CS0	
	T: 0.938 V S: -77 pSec		
iCiS Sweep Voltages From Voltage 0.3 V	T: 0.881-0.975 V S: -34111 pSec	WE	
To Voltage 1.3 V	T: 0.919 V S: -341 pSec		
Resolution 0.01 V Repeat 0 Times	T: 0.975 V S: -11 pSec	CAS	
Above settings will require sweep of 100 acquisitions.	RAS T: 0.881 V S: -165 pSec	RAS	



Automated Analysis Sessions

- One or Many Acquisitions / One or Both Analyzers
- Protocol Analysis Session
 - Protocol Analyzer runs until stopped
 - Violations and statistics are reported
- Single Acquisition Session
 - Protocol Analyzer runs until the state analyzer is triggered
 - Violations and statistics are reported.
 - State/Timing data is acquired and available for analysis
- Multi-Acquisition Session
 - Protocol Analyzer runs until the state analyzer is triggered
 - Results are stored in disk memory and analysis is restarted
 - Trigger conditions can be modified mid-session.



Compliance Timing and Parameter Selection

- Spec timing included
- Customize timing per target and margin
- Enable one, some or all violations

			🥔 Session	Setup		
🕒 Target Corr	npliance Timing				Wrap Violation Storag	
Compliance Tim	ning (Speed-Bin)	DR3-2133H	GoliathR1.1	▼ Add	Enable Compliance Para	
ACTPDEN	1	ck	tRASmin	36 ns	■ Table Compliance Faran	neter 🔺
łCCD	2	ck	tRCD	13500 ps	▼ 10.07AW	
tCKESR	7125	ps	tRDPDEN	Derived ck		
łDLLK	512	ck	tREFPDEN	1 ck	📝 13: tRRD	
tFAW_1Kb	30	ns	tRFC_512Mb	90 ns	📝 14: tRP (MRW/SR	E)
tFAW_2Kb	45	ns	tRFC_1Gb	110 ns	📝 15: REF Before SR	E
tMOD	18	ns	tRFC_2Gb	76 ck	📝 16: tPREPDEN	E
tMBD	4	ck	- tRFC_4Gb	300 ns	📝 17: tREFPDEN	
tMRSPDEN	18	ns	RFC_8Gb	350 ns	📝 18: KACTPDEN	
	5625		-		V 19: tMRSPDEN	
tPDmin		ps	tRP		📝 20: tWRPDEN	
tPDmax	70200	ns	tRRD_1Kb	6 ns	21: tWRAPDEN	
tPDmax_HT	35100	ns	tRRD_2Kb	7500 ps	📝 22: tRDPDEN	
tPREPDEN	1	ck	tRTP	7500 ps	📝 23: tMOD	
tRASmax	70200	ns	ťWB	15 ns	📝 24: tMRD	
tRASmax_HT	35100	ns	(WRPDEN	Derived ck	25: tCKESR	
		_			🔽 26: tCCD WR	-
					۰ III	•
					Sel. None Sel. All	



Logic Analyzer Acquisition Control

- 8 IF/THEN/ELSE States
- Each State supports multiple AND/OR clauses
- 1 Global Storage qualifier
- 4 Word Recognizers
- 2 Counters

Acquisitio	n Control					• 🛛	
Setup Nam	ne Goliath						
Storage Co		Word Recognizers					
Post-Trigger Delay 1,000 🚔		Signal	Bank Addr Command		I Address Rank		
Pre-Trigg		WR1 🗾 👻	7 🔹	ACT 🔻	****	Rank 1	
	igger In Off 🚽	WR2 💽	7 🔹	PRE 🔻	××××	Rank 1	
		WR3 🗖	•		××××		
Violation C	ontrol	WR4			****		
Edit	Violations	Counter Load Values	S			_	
Automa i	/iolation Store	Counter 1 1000	d Value 🔻				
	voiation store	Counter 2 2222	-				
Trigger Con	trol						
Trigger Stau		Edit Add	Insert	Delete C	lause Logic	Else If	
Global							
	Anything					- 11	
Then	Store					-	
1]					=	
State 1	State 1						
If Anything							
Then	Load Counter 1 AND Go To Sta	te 2				-	
1	1						
State 2	State 2					_	
lf	WR2 Matches					-	
	Increment Counter 2 AND Go To State 3						
Then	Else If Anything						
<u> </u>	Anything					-	



Real-time Compliance Results

Compliance Parameters										
Stat	Num.	Name	Occurences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
?	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
?	23	MRS Settle	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	24	MRS Burst			R7 R6 R5 R4 R3 R2 R1 R0					22,500
?	25	sSREF Time	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	7,500
٢	26	WR Burst	13,386		R7 R6 R5 R4 R3 R2 R1 R0			168,523	128102389400761000.0	7,200
•	27	RD to WR(A) Separation	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	64,028	70310809855578300.0	13,118
?	28	PDX Slow Exit			R7 R6 R5 R4 R3 R2 R1 R0					24,000
?	29	Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700
۰	30	WR to RD(A) Separation	22,075		R7 R6 R5 R4 R3 R2 R1 R0			910,959	35155404927789100.0	26,236
۰	31	RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 <mark>R1 R0</mark>	00	00	164,742	128102389400761000.0	7,200
?	32	sPD Time Min.			R7 R6 R5 R4 R3 R2 R1 R0					5,625
?	33	sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
3	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
۰	35	sREF Time	1,527	00	R7 R6 R5 R4 R3 R2 <mark>R1 R0</mark>	00	00	5,297,689	8384883669867880.0	110,000
۰	36	sACT Time Min.	19,499		R7 R6 R5 R4 R3 R2 R1 R0		00	265,733	24595658764946000.0	37,500
۰	37	sACT Time Max.	19,499	00	R7 R6 R5 R4 R3 R2 <mark>R1 R0</mark>	00	00	265,733	13138706605106.2	70,200,000
٢	38	ACT to RD(A)/WR(A)	19,636		R7 R6 R5 R4 R3 R2 R1 P	00		19,999	70273310756988700.0	13,125
۰	39	RD to PRE(A)	15,22	00	R7 R6 R5 R4 P* «2 R1 R0	00	00	175,659	82029278164841400.0	11,244
?	40	RD to ACT	00		R7 P5 R4 R3 R2 R1 R0					20,614
۰	41	WR to PRE(A)	,217	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,649	27343092721613700.0	33,732
?	42	WR to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0					20,614
?	43	CKEx Signal After DLL Reset	00	00	R7 R6 R5 R4 R5 R2 R1 R0	NA	NA	NA	NA	959,700

Real-time event statistics



Violations and Acquisitions Must Be Time Correlated

							tion Listing					
mestamp (nS).	Bank Address	Rank(s)	Violations	Acquisition Sample	_ Tir	estamp (nS)	Address	Rank #	Bank #	Command	Violation	
51,015.32	-		tRFC	33982	=	90,179.50	-	-	0	NOP		
01,390.17	-		tRFC	54366		90,191 00	-	-	0	NOP		
90,182.50) -		t RFC	60099		90,182.50	OOF6D	1	6	ACT		
100,701.05	-		tRFC	125819		90.184.00	-	-	0	NOP		
197,279.24	-		tRFC	131491		90,185.50	-	-	0	NOP		
3,322,501.00	-		tRFC			90,187.00	-	-	0	NOP		
3,606,275.50	-		tRFC			90,188.50	-	-	0	NOP		
3,666,592.00	-		tRFC			90,190.00	OOFOD	1	0	ACT		
3,675,070.50	-		tRFC			90,191.50	-	-	0	NOP		
3,704,818.00	-		tRFC			90,193.00	-	-	0	NOP		
3,713,274.50	-		tRFC			90,194.50	-	-	0	NOP		
3,735,281.50	-		tRFC			90,196.00	00248	1	6	RD		
				Þ	+ (
												_
MCA Direct Acquisiti	on Waveform											
MCA Direct Acquisiti	on Waveform 90,181.00		90,188.50	90,196.00		9	0,203.50		90,21	1.00		
	90,181.00					30	0,203.50		90,21	1.00		
Timestamp (nS)			10,1\$8.50	90,196.00		90 200250 X	0,203.50		90,21	1.00		
Timestamp (nS)	90,181.00						0,203.50		90.21	1.00		
Timestamp (nS) Clock Address	90,181.00						0.203.50		90.21 X			
Timestamp (nS) Clock Address Rank #	90,191.00 X00F6D	X X X 1	- X00F0DX	- X00248X		X00250 X			X			L X X
Timestamp (nS) Clock Address Rank # Bank #	90.191.00 - X00F6D - X 1 X 0 X 6 X			X00248X		X00250 X			X · ·		X X00236	L X X



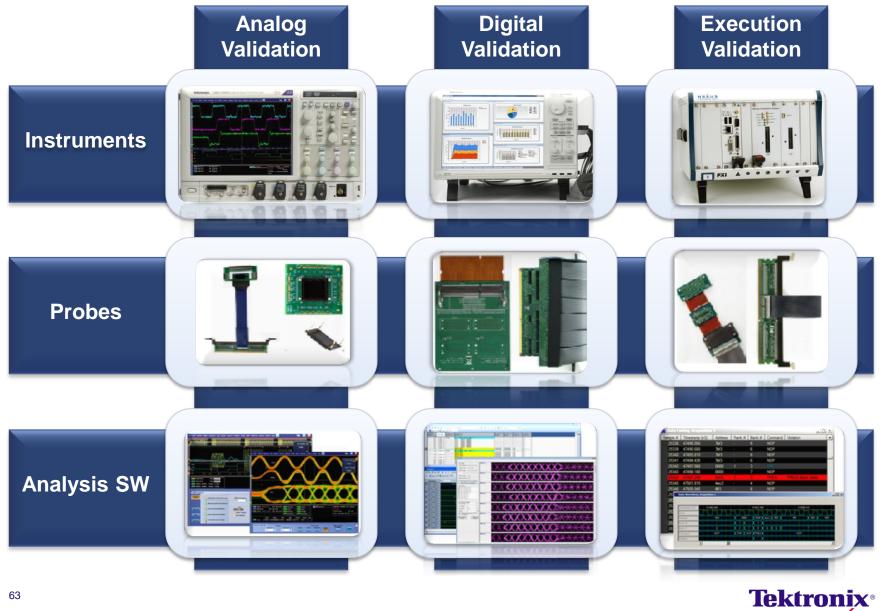
Benefits of Real-Time + Post Capture

	ACC (Address/Command/Control)	ACC+DQ (Address/Command/Control/Data)
At-Speed / Real-Time	MCA	MCA+LA
Post Capture		LA

MCA Advantages	LA Advantages
Capture Depth 1Gcycles	State Capture of ALL DDR Signals
Cost	20ps High Speed Timing / MagniVu
PA Real Time + LA State Analysis	Analog Mux
	Multi Bus Cross Correlation



Memory Validation Continuum



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