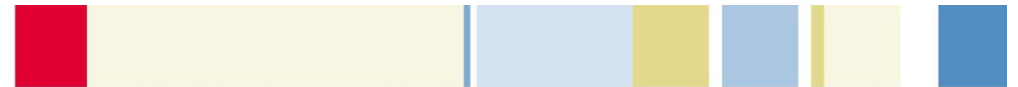


# Memory Solutions

Industry Trends and Solution Overview



## Tektronix Innovation Forum

Leading Solutions for Today,  
Tomorrow and Beyond

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# Outline

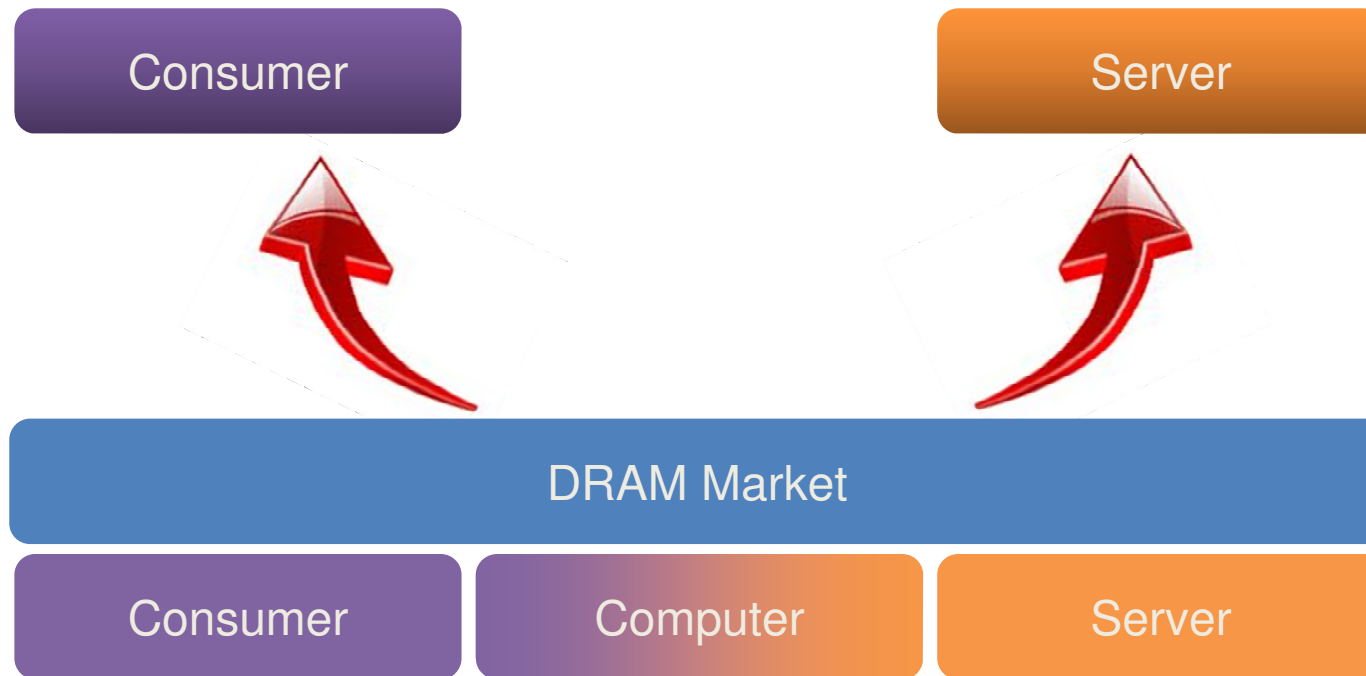
- Industry Trends & Market Status
- Existing SDRAM Technologies
  - DDR3, DDR3L, DDR3U
    - DDR3 Signaling
  - LPDDR2/LPDDR3
    - LPDDR3 Signaling
  - DDR4
    - DDR4 Signaling
- “Emerging” SDRAM Technologies
  - LPDDR4
  - WideIO2
  - HBM (High Bandwidth Memory)
  - HMC (Hybrid Memory Cube)
  - Bandwidth and Pin Count
- Memory Validation Continuum – Solution Overview



# Industry Trends & Market Status

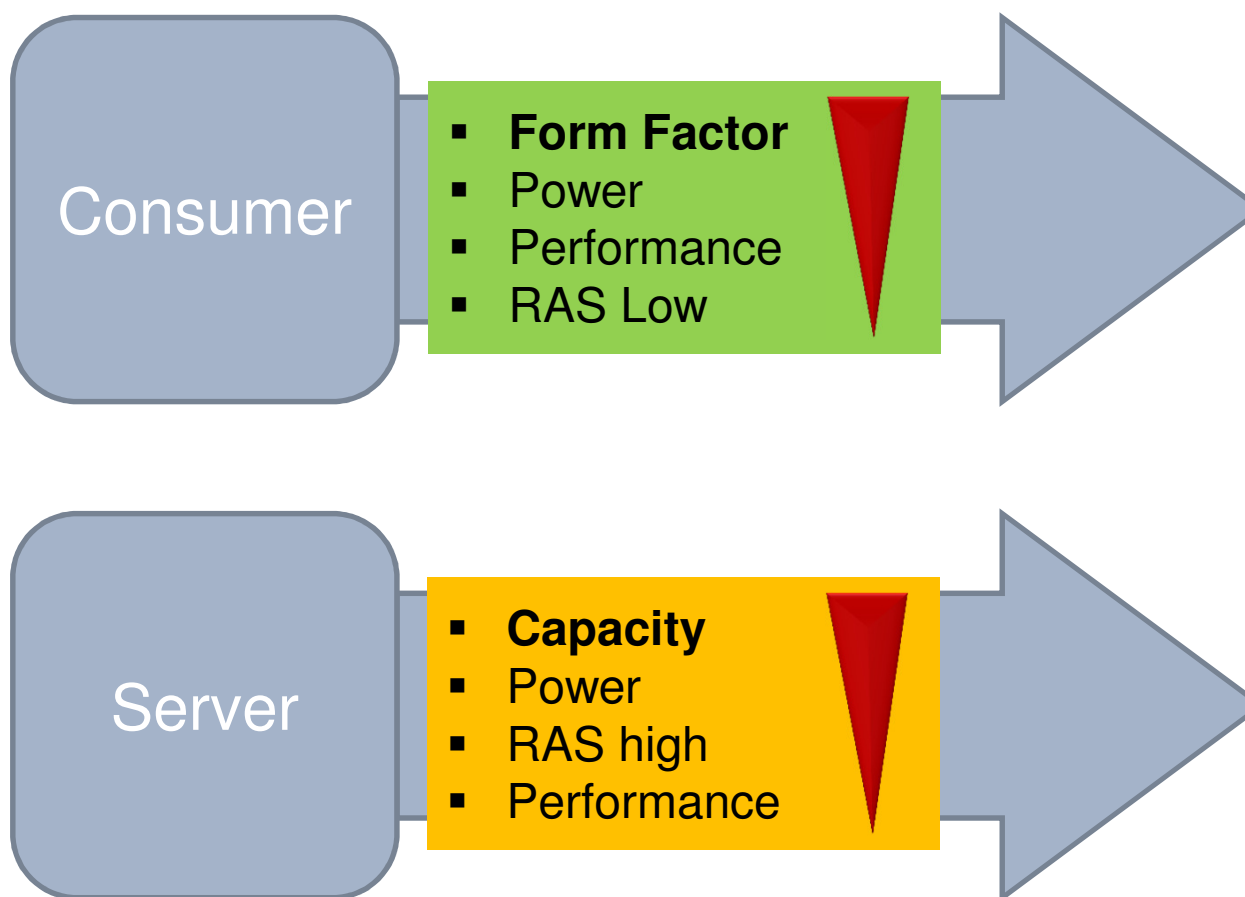


# DRAM Market Status

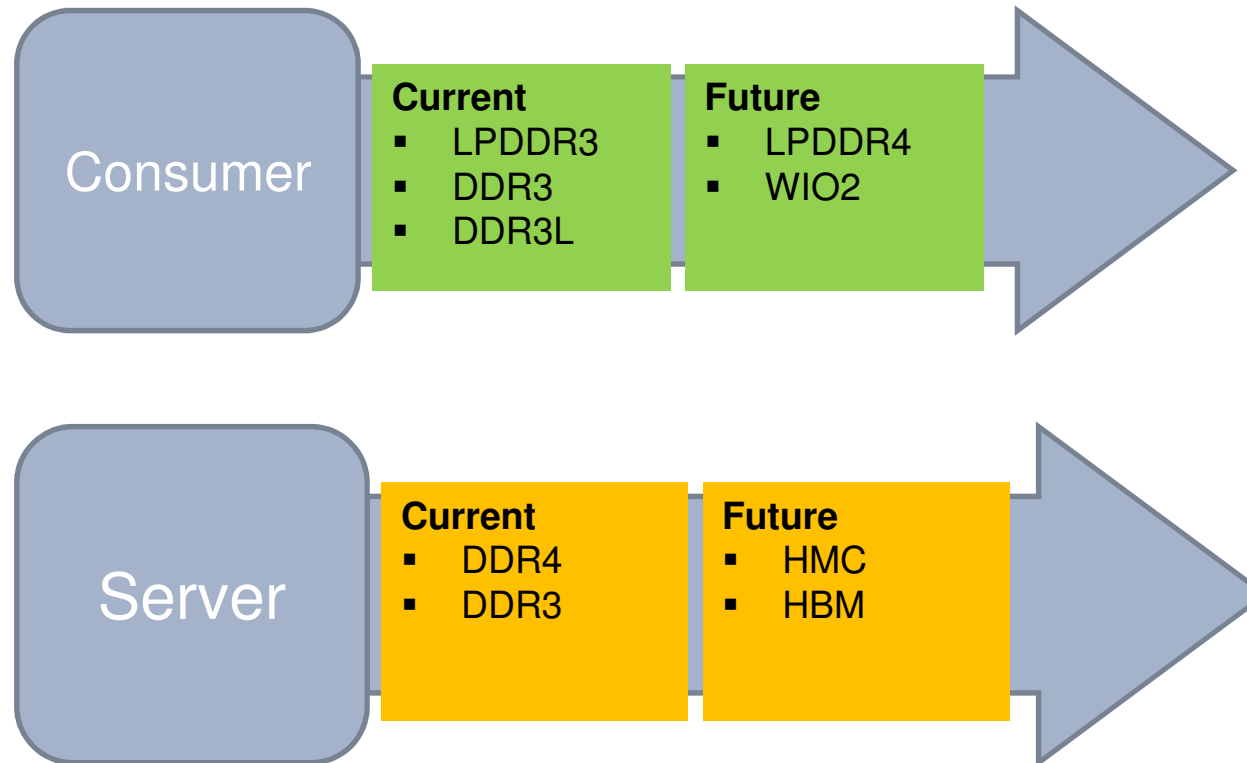


- Three Sub segments all focused on single standard
- Computer segment disappearing and market bi-furcation into Server and Consumer

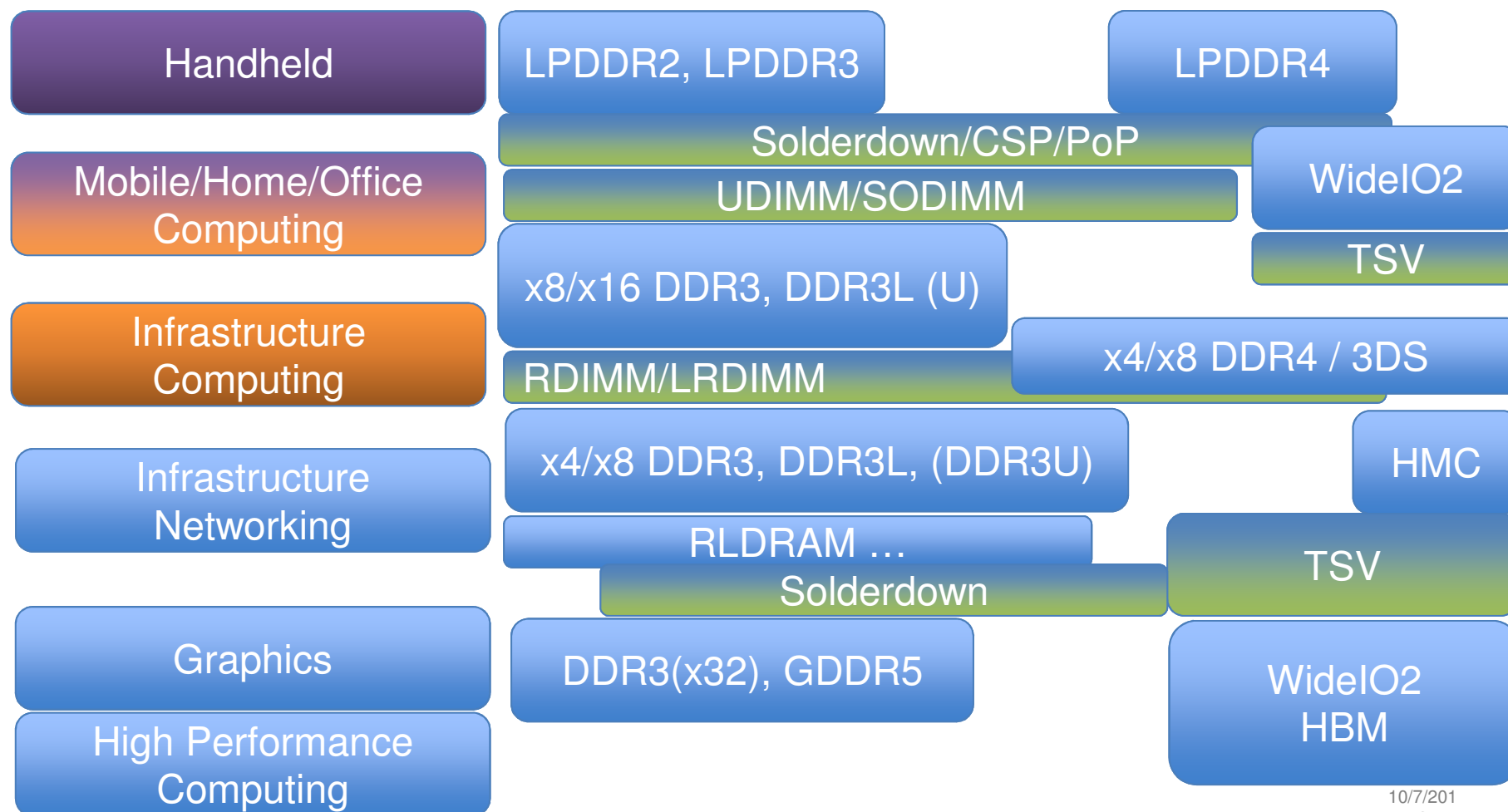
# DRAM Industry Trends



## Consumer DRAM Market status



# DRAM Applications Overview



10/7/201  
3

7



# Existing SDRAM Technologies

- DDR3, DDR3L, DDR3U
- LPDDR2/LPDDR3
- DDR4



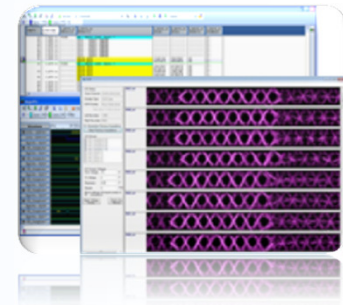


# DDR3/DDR3L(/DDR3U)

*Server and Desktop/Mobile Computing*

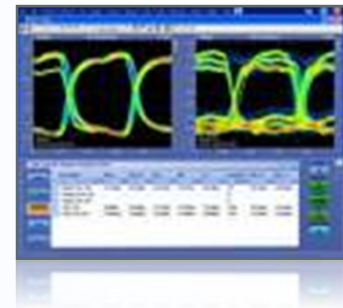
## Protocol Layer

- Command based interface
- Separate Command/Address and data bus
- Power state management via CKE
- No dedicated connectivity test mode
- Clock/Strobe calibration (write leveling)



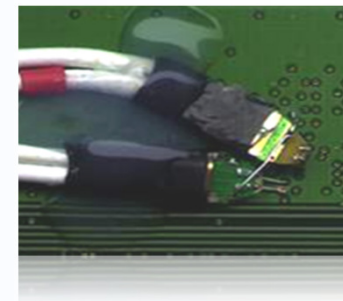
## Physical Layer

- DDR Signaling, Midlevel Referencing (VREFCA, VREFDQ)
- SDR CA-bus, differential clock
- Bidirectional single ended data bus (800 – 2133 Mbps/pin), differential strobe
- programmable Midlevel ODT, ZQ calibrated
- programmable Drive Strength, ZQ calibrated



## Packaging Technology

- Typical DIMM with 8...36 single SDP's (or DDP, QDP, 3DS)
- x4/x8 (server) x8/x16 (mobile computing) x32 (low end graphics)
- E.g. x8 has 44 active signals, window BGA (CSP), 0.8 mm ball pitch
- UDIMM, RDIMM, LRDIMM socket 240-pins 1.0 mm pitch
- X64/x72 DIMM has 6.4 GBps ... 14.1 GBps per channel

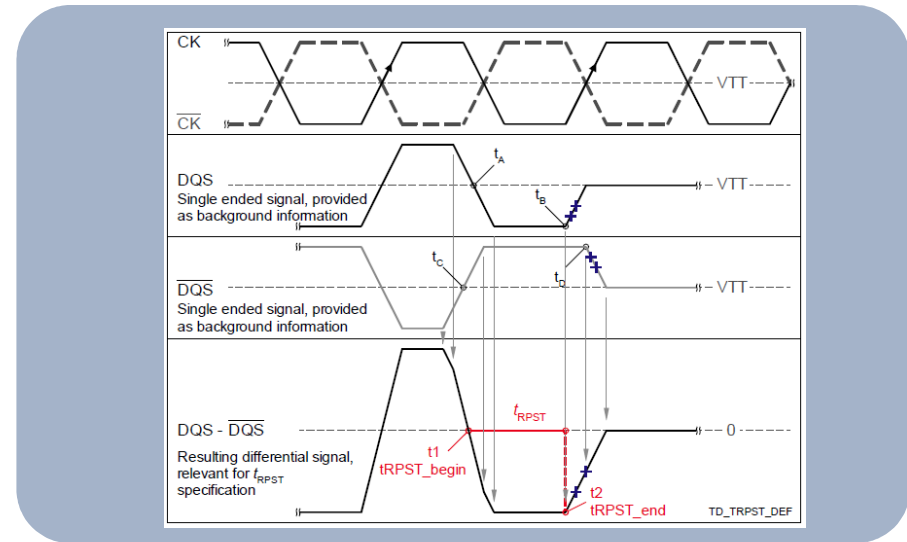
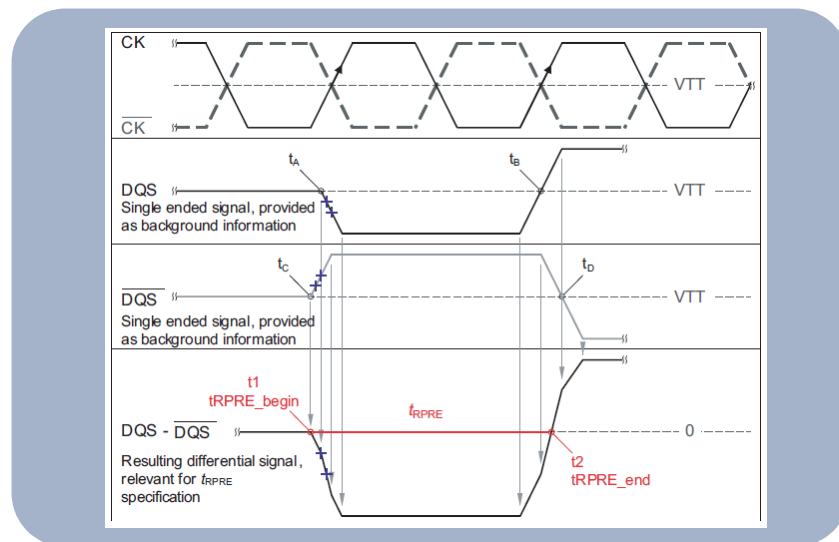
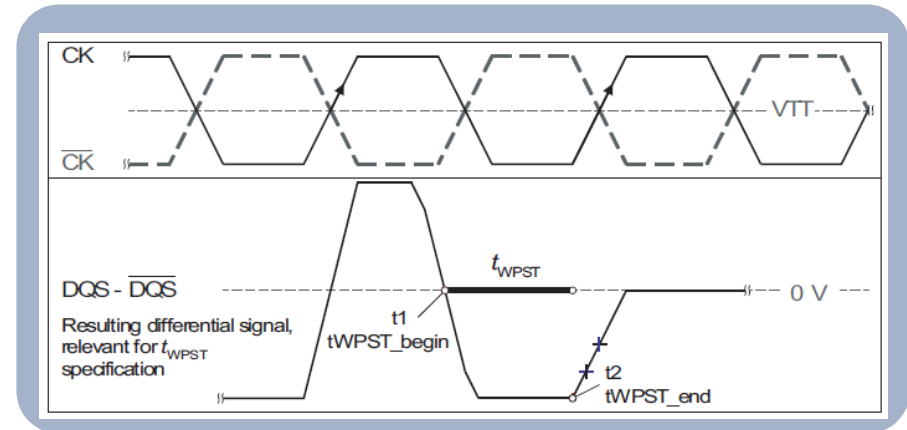
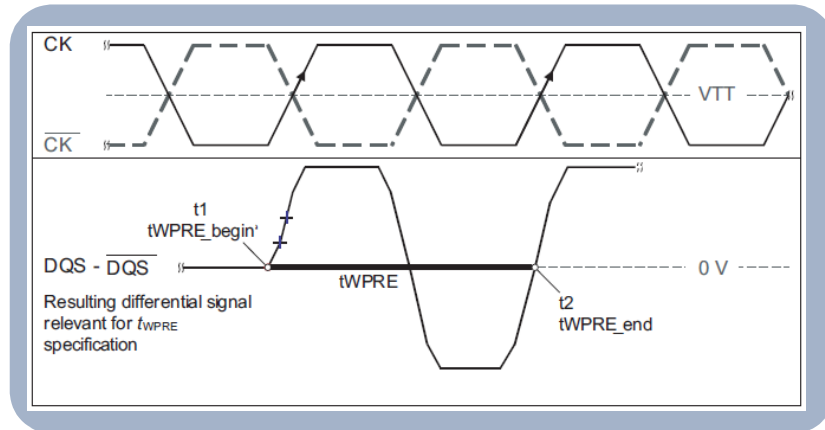


## DDR3/DDR3L(/DDR3U): Signaling Details (1)

- VDD = VDDQ: 1.5V, L=1.35V, (U=1.25 V)
- AC-Input Levels:  
+/-175 mV...+/- 125 mV around VREF(dc)
- DC-Input levels:  
+/- 100 mV .... +/-90 mV around VREF(dc)
- Strobe crossing centered in data eye for Write;  
Rising strobe edge centered between two falling clock edges  
 $t_{DSS} = +/- \frac{1}{4} t_{CK}$
- Strobe edge aligned with clock for Reads;  
 $t_{DQSCK} = +/- 10\% t_{CK}$   
Data aligned with strobe for Reads
- Slew rate dependent setup/hold (derating)
- ADD/CMD – eye centered around rising clock edges (SDR)

# DDR3/DDR3L(/DDR3U): Signaling Details (5)

## Preamble/Postamble Read/Write

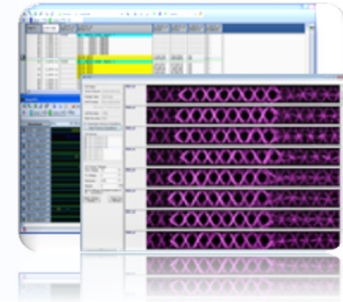


# LPDDR2 and LPDDR3

## Handheld

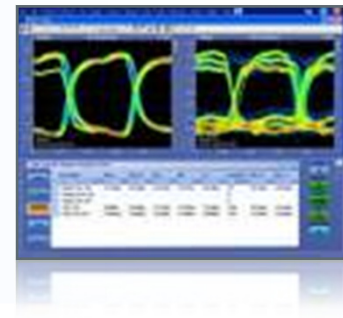
### Protocol Layer

- DDR Command/Address (10xCA-)bus; 2-halfcycle commands
- Different Prefetch LPDDR2: S2, S4; LPDDR3 S8
- LPDDR2 also supports NVM, **LPDDR3 does NOT**
- No dedicated connectivity test mode
- Clock/Strobe calibration (write leveling); LPDDR3: **Clock/CA training**



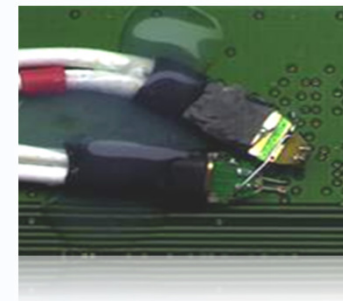
### Physical Layer

- DDR Signaling, Midlevel Referencing (VREFCA, VREFDQ)
- **DDR** CA-bus, differential clock, SDR CS#
- Bidirectional single ended data bus (400 – 1066 - 2133 Mbps/pin) differential strobe, **unterminated** HSUL, **LPDDR3 adds VDD term option**
- programmable Drive Strength, ZQ calibrated



### Packaging Technology

- PoP or side-by-side CSP solder-down, 0.4, 0.5, 0.65x0.8 mm ball pitch
- MCP in with separate NVM (eMMC, UFS) channel(s)
- Edge-pad die with wire-bonded DDP/QDP, very thin
- Typ. one or two channels; x32 DQ per channel; 1.6 – 7.0 GBps per ch.
- ~60 active pins per (x32) channel



## LPDDR2/3: Signaling Details

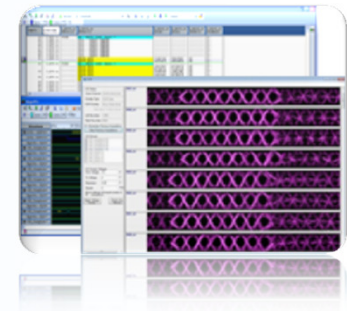
- VDDQ: 1.2V
- AC-Input Levels:  
LPDDR2: +/-300 mV...+/- 220 mV around VREF  
LPDDR3: +/-150 mV...+/- 135 mV around VREF
- With VDDQ termination VREF may be off-centered!
- CA bus DDR, eye centered around clock crosspoint
- CS\_n is SDR, only latched with rising clock edges
- Strobe centered in data eye for Writes,
- Strobe aligned with clock for Writes  
 $t_{DQSS} = \pm \frac{1}{4} t_{CK}$
- Strobe edge aligned with data for Reads;
- No DLL: strobe NOT aligned with clock for Reads;  
 $t_{DQSCK} = 2.5 \dots 5.5 \text{ ns}$
- Slew rate dependent setup/hold (derating)  
referenced to clock/strobe crosspoint
- $t_{QH}$  (while defined the same way as in LPDDR2) has much larger value (in %UI)  
compared to LPDDR2

# DDR4

## *Server (and Mobile Computing)*

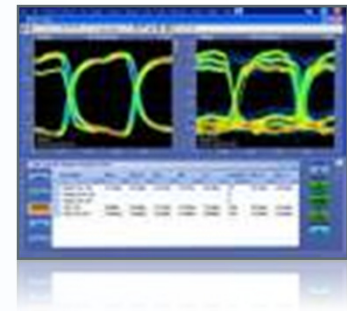
### Protocol Layer

- Command based interface like DDR3
- CA parity, Data CRC (for higher data rate), DBI(dc)
- Dedicated connectivity test mode (mandatory for x16/x32)
- Clock/Strobe calibration (write leveling); 'internal VREFCA' training
- DQS/DQ training; 'internal VREFDQ' training;



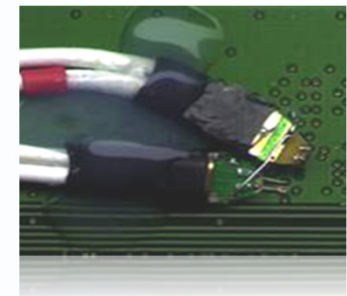
### Physical Layer

- DDR Signaling, Internally programmable VREFCA, VREFDQ/bytelane
- SDR CA-bus (~23x), differential clock
- Bidirectional single ended data bus (1600 – 3200 Mbps/pin), diff. strobe
- Databus VDDQ terminated, programmable ODT, ZQ calibrated
- programmable Drive Strength, ZQ calibrated



### Packaging Technology

- Typical DIMM with 8...36 single SDP's (or DDP, QDP) or 2H, 4H, 8H 3DS
- x4/x8 (server) x8/x16 (mobile computing) x32 (low end graphics)
- E.g. x8 has xx active signals, window BGA (CSP), 0.8 mm ball pitch
- UDIMM, RDIMM, LRDIMM socket 288-pins 0.85 mm pitch
- X64/x72 DIMM has 12.8 GBps ... 25.6 GBps per channel



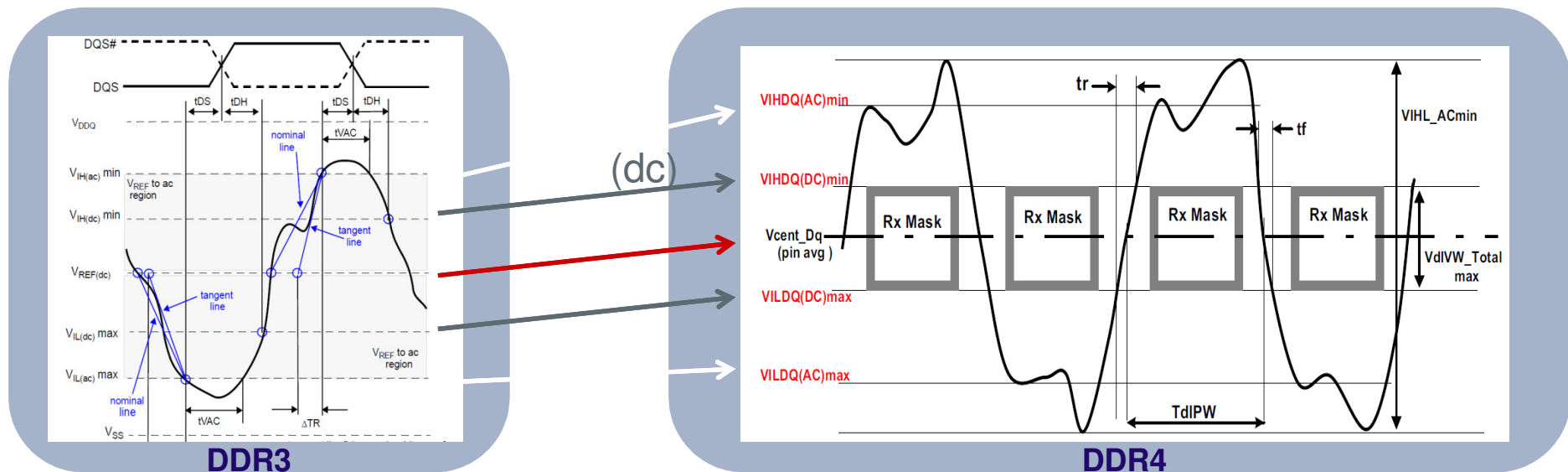
## DDR4: Signaling Details

- VDD = VDDQ: 1.2V, (maybe → 1.1V → 1.0 V in the future)
- Generally like DDR3; except:
  - No external VREF.  
Replaced by internally trained VREF and virtual “VCENT”
  - Mask type data valid window  
mask height ~+/- 68 mV ... xxx mV  
(corresponds to DDR3 dc-levels)  
VIHL\_ac = +/- 93 mV  
(corresponds to DDR3 ac-levels)
  - VDDQ Termination



# DDR4 Rx Data Eye Detail: ac/dc levels -- mask

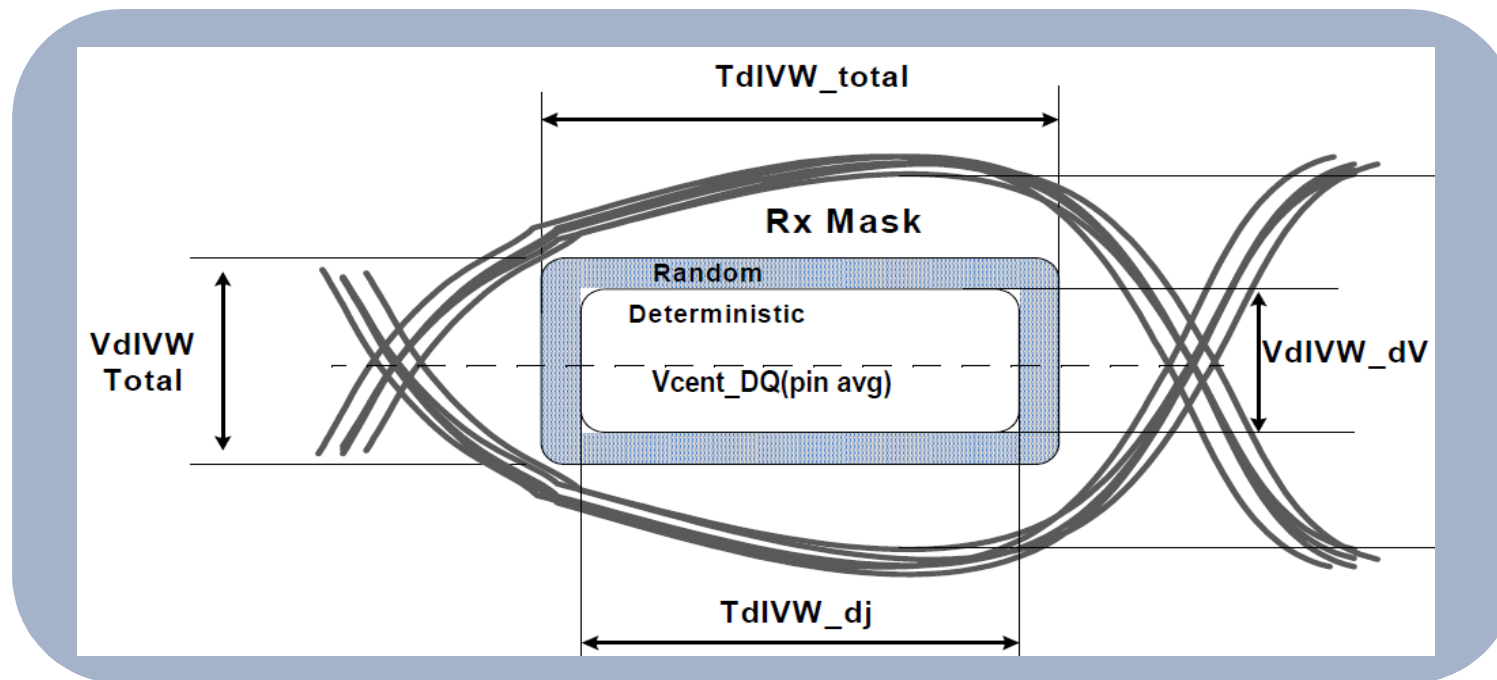
- Redefinition from (min) ac/dc levels that must be applied externally (as system requirement)  
→ (max) mask height (VdIVW) that receiver is allowed to require (as receiver property)
- VREF is internal and trained in DDR4 system → only virtual Vcent externally
- AC-level has to be reached, but at no particular time





# DDR4 Rx Data Eye Detail: Statistical Mask

- TdIVW (max) is centered around the strobe crossing (replaces min setup/hold)
- VdIVW (max) is centered around Vcent
- Vcent is calculated to be the widest eye-opening
- Allow VdIVW and TdIVW to have bounded (deterministic) and gaussian (random) properties.

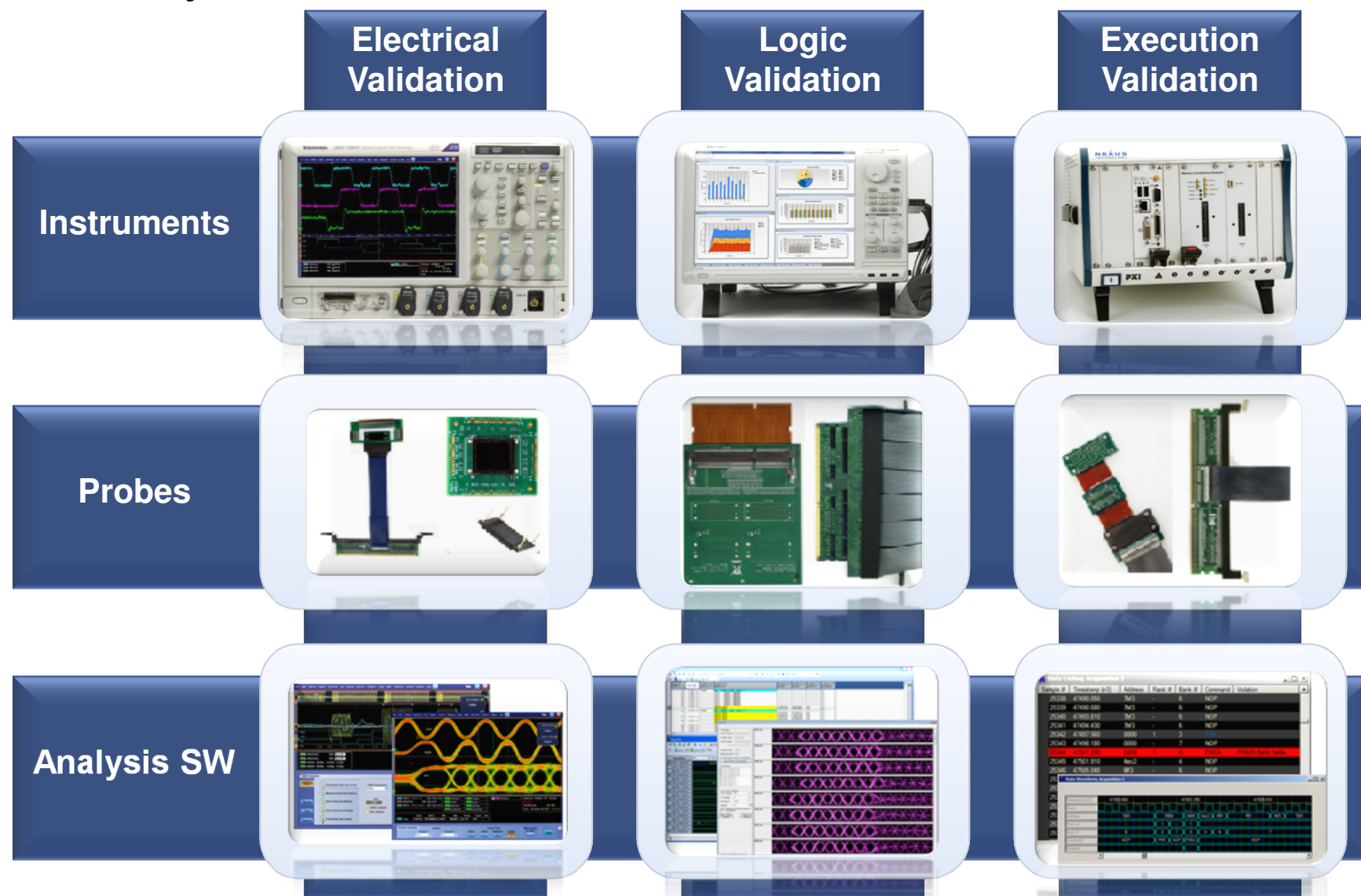




# Memory Validation Continuum



# Memory Validation Continuum





## Memory Validation Continuum

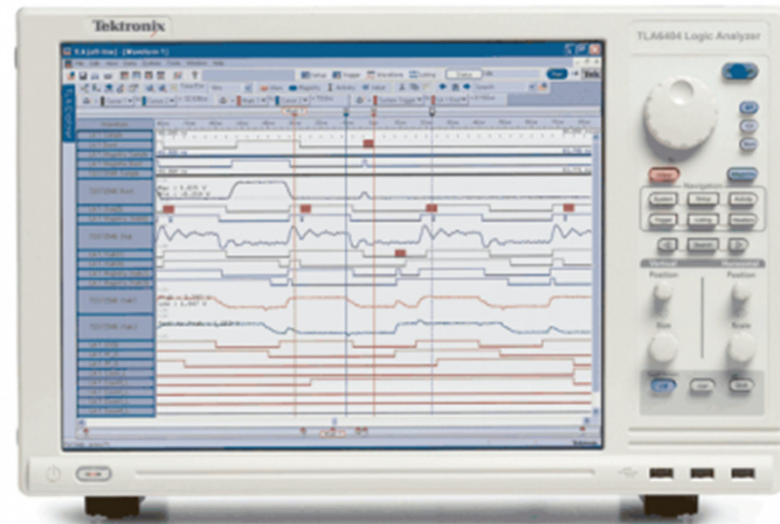
- Complete Solution for the Memory Application Space
- Best in class solutions for Electrical, Logic and Execution Validation plus correlation and time-to-data capabilities unique to Tektronix
  - iCapture and iView Capability
  - Socketed interposers
  - iCis
  - Shared Interposers
  - Common compliance software
  - Single probing multiple views
  - MSO Slot+MCI probing combination

# iCapture / iView

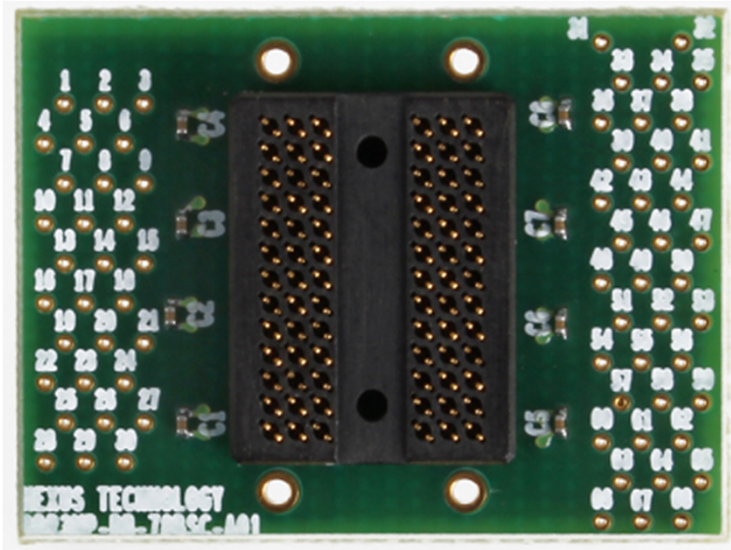


MSO

TLA

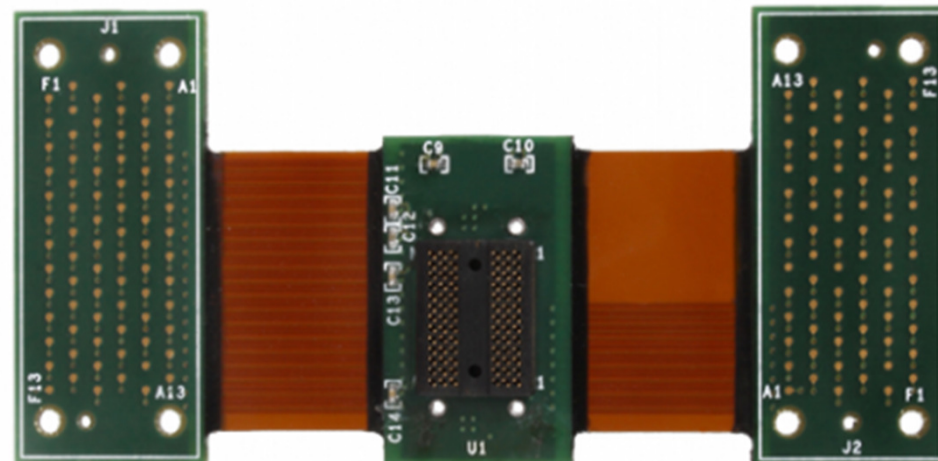


# Socketed Interposers



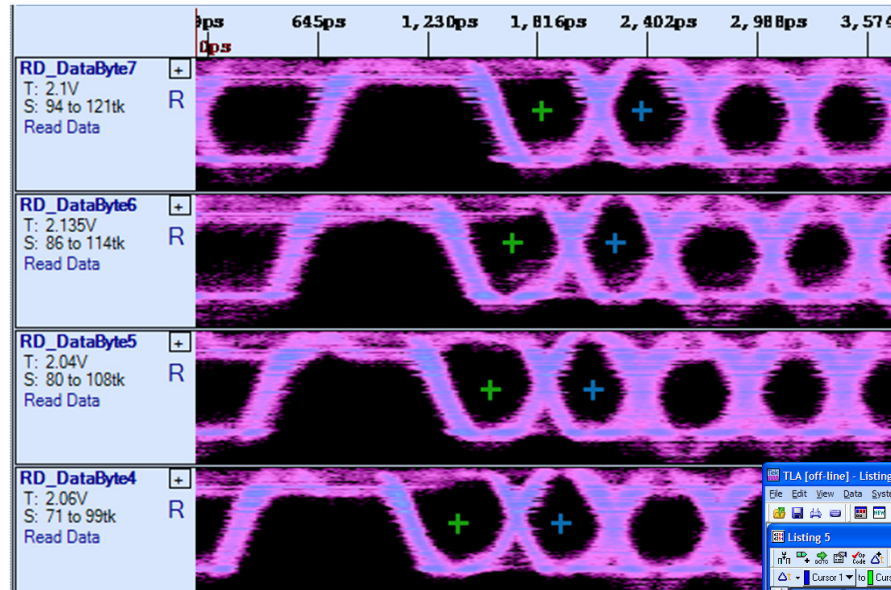
Socketed  
Scope Interposer

Socketed  
LA Interposer



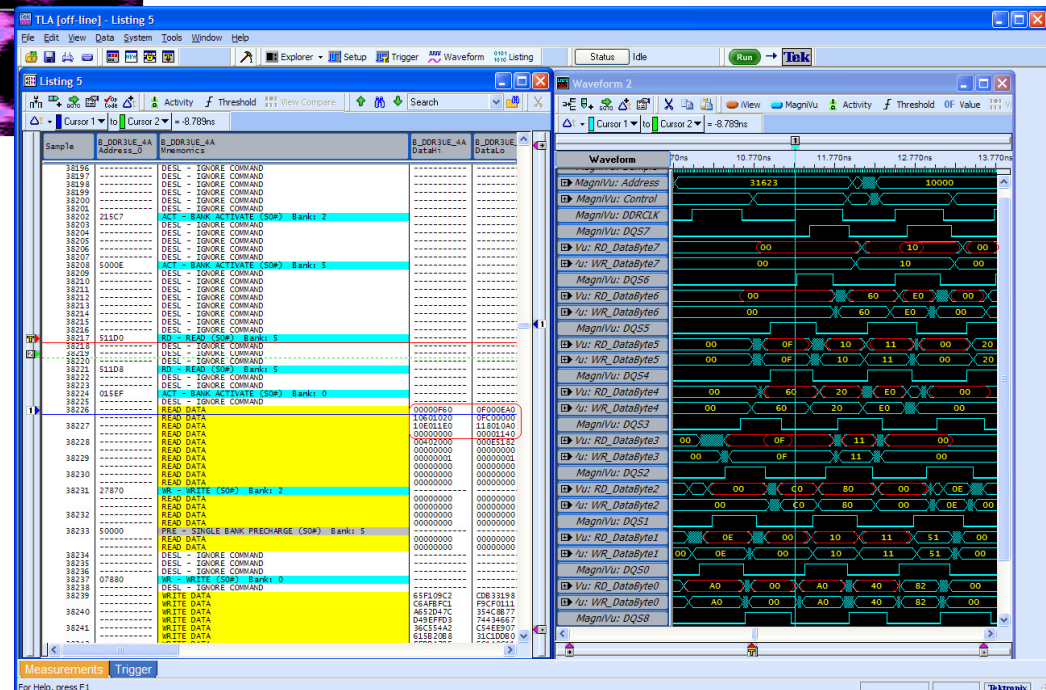


# Data Displays

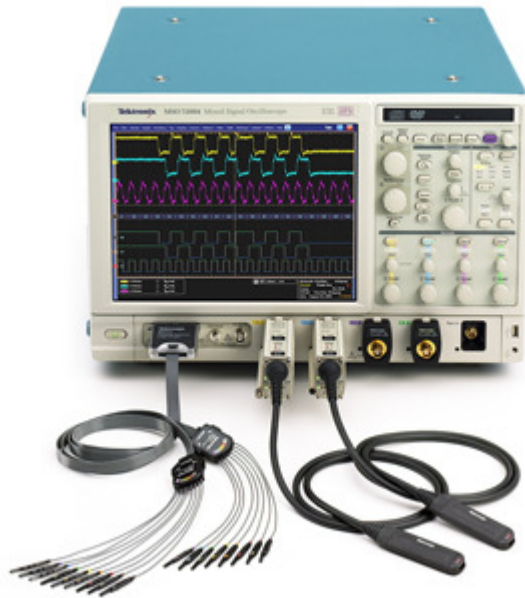


iCi's

Traditional LA Display

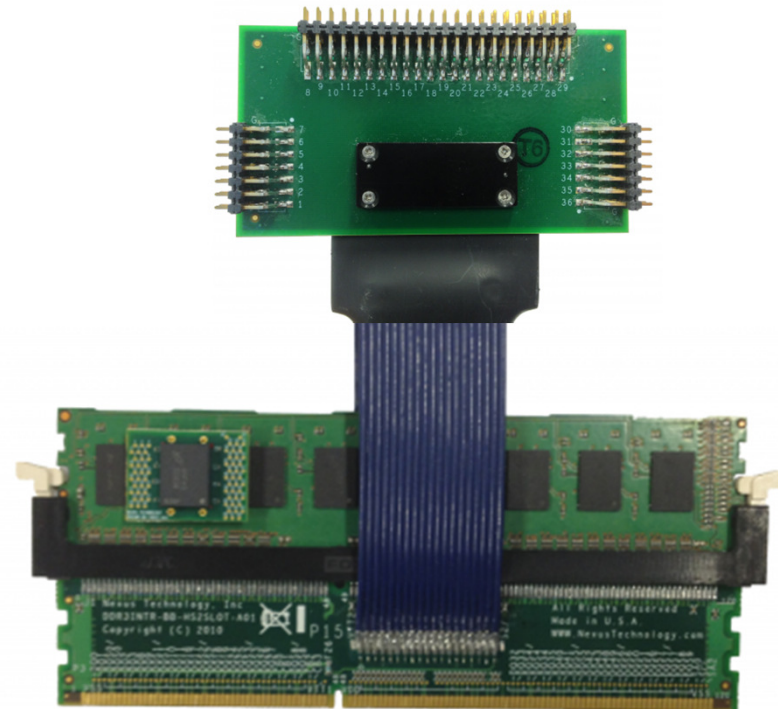


# MSO Interposer Combination



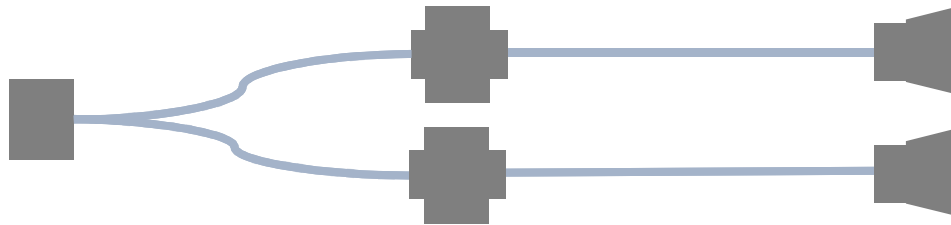
**MSO Interposers**

**MSO**





# Shared Probing



LA Probes

Interposers



# Protocol Compliance

All Checks & Violations									
Compliance Parameters									
Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)	
WR Burst	13,385	00	00 00 00 00 00 00 00 00 00 00	00	00	168,522	12810238400/761000.0	7,200	
RD to WR(A) Separation	13,385	00	00 00 00 00 00 00 00 00 00 00	00	00	64,028	70310809855/78300.0	13,118	
PDX Slow Exit	00	00	00 00 00 00 00 00 00 00 00 00	NA	NA	NA	NA	24,000	
Rank DLL Reset to RD(A)	00	00	00 00 00 00 00 00 00 00 00 00	NA	NA	NA	NA	959,700	
WR to RD(A) Separation	22,075	00	00 00 00 00 00 00 00 00 00 00	00	00	910,958	3518540527/768100.0	26,236	
RD Burst	22,075	00	00 00 00 00 00 00 00 00 00 00	00	00	164,742	12810238400/761000.0	7,200	
sPD Time Min.	00	00	00 00 00 00 00 00 00 00 00 00	NA	NA	NA	NA	5,595	
sPD Time Max.	00	00	00 00 00 00 00 00 00 00 00 00	NA	NA	NA	NA	70,200,000	
PRE(A) Bank Settle	26,733	00	00 00 00 00 00 00 00 00 00 00	00	00	947,526	70273310756386/700.0	13,125	
sREF Time	1,527	00	00 00 00 00 00 00 00 00 00 00	00	00	5,297,689	83848836696/7880.0	110,000	
sACT Time Min.	19,499	00	00 00 00 00 00 00 00 00 00 00	00	00	265,733	24959538764945000.0	37,500	
sACT Time Max.	19,499	00	00 00 00 00 00 00 00 00 00 00	00	00	265,733	13138706605106.2	70,200,000	

Individual Acquisition Details									
Stat	Run #	Time	Occurrences	Violations	Status	Per Acquisition Violation Details			
						Sample #	Timestamp	Rank	Bank
1	10/10/2011 1:38:00 PM	2601	2	00 00 00 00 00		25344	49860801	1	3
2	10/10/2011 1:38:05 PM	2644	3	00 00 00 00 00		114431	216905195	0	7
3	10/10/2011 1:38:11 PM	2545	3	00 00 00 00 00					
4	10/10/2011 1:38:16 PM	2722	3	00 00 00 00 00					
5	10/10/2011 1:38:22 PM	2670	4	00 00 00 00 00					
6	10/10/2011 1:38:28 PM	2800	4	00 00 00 00 00					
7	10/10/2011 1:38:33 PM	2543	2	00 00 00 00 00					
8	10/10/2011 1:38:38 PM	2605	1	00 00 00 00 00					
9	10/10/2011 1:38:44 PM	2697	7	00 00 00 00 00					
10	10/10/2011 1:38:50 PM	2805	0	00 00 00 00 00					

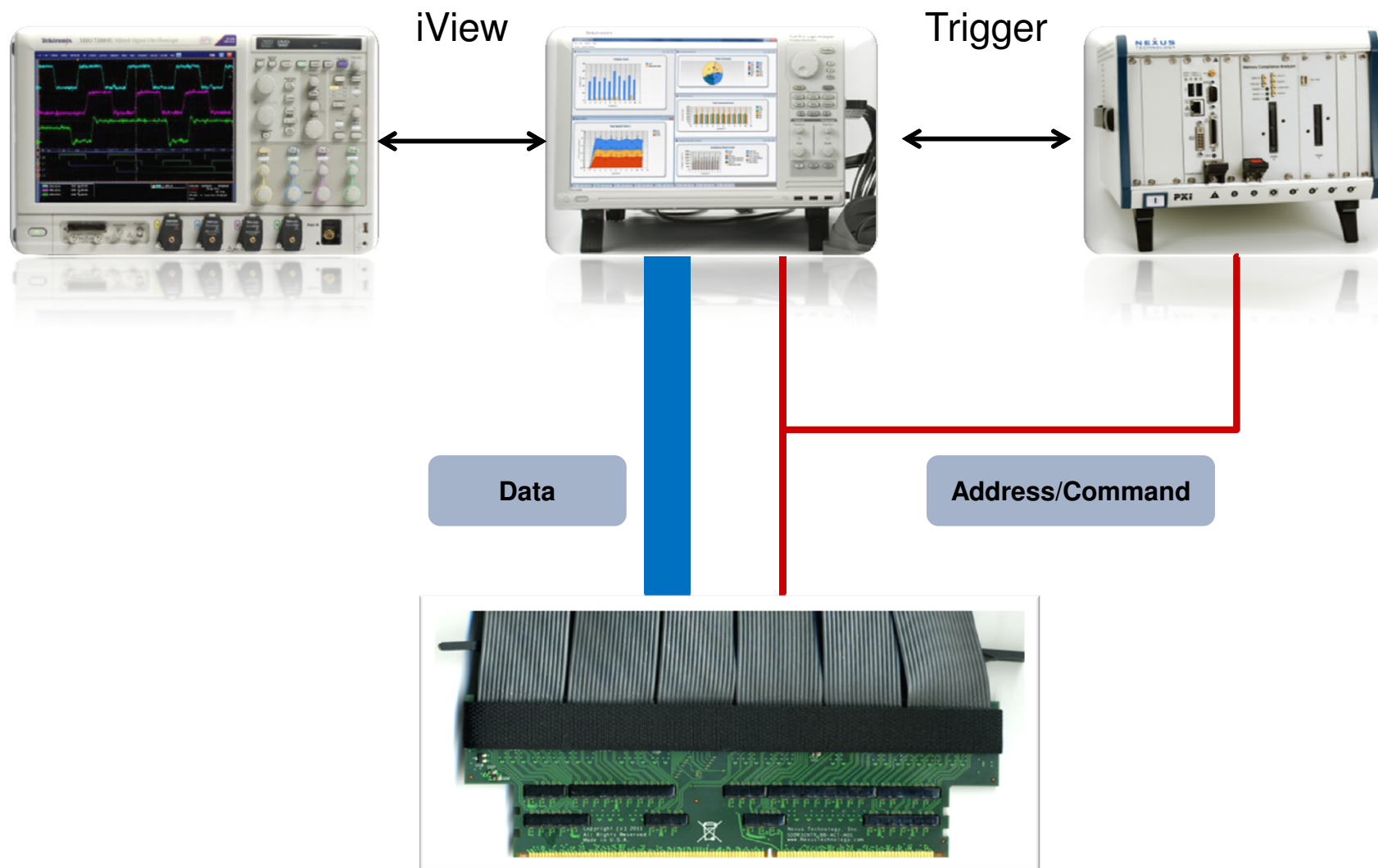
Offline Protocol Compliance

Real-Time Protocol Compliance



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# Single Probe Multiple Views



# Memory Interface Electrical Validation

*Measure the analog signal characteristics; trtf, Vmin/max, jitter, eye size, crossover, strobe/clock alignment, etc.*



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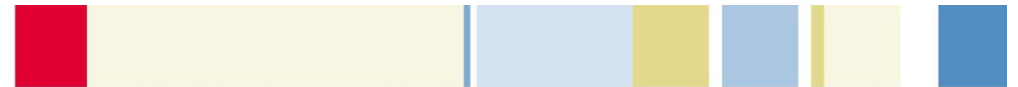
# Memory Validation Continuum





# Signal Access

Probing



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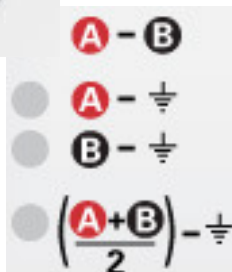
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# Probing



**P7300 Probes**



**P7500 Probes**



51W-29204-0 How To Guide P7500 Tip Selection Solder Guide.pdf

# Interposer Types

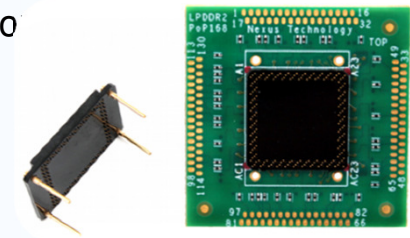
## Socketed Interposers

- Comes with a Custom BGA Socket that needs to be soldered to Target
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target



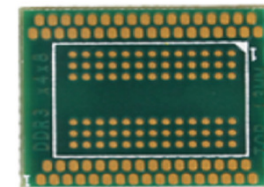
## PoP Interposers

- Comes with a Custom BGA Socket that needs to be soldered to Application
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target



## Direct Attach Interposers

- Interposer is soldered to Target
- Memory Component is soldered to Interposer
- Full BGA visibility
- No Special design or routing requirements needed

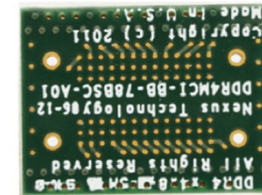




# Interposer Types

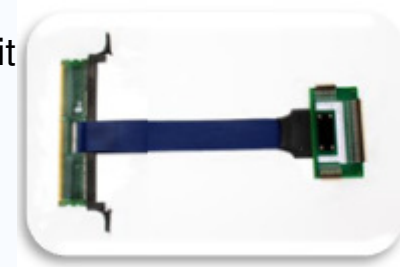
## Direct Attach Perimeter Interposers

- Interposer is soldered to the Target
- Memory component is soldered to Interposer
- Signals are brought to pads on edge of the Interposer
- KoV of the interposer is the same size as the BGA component
- Because of limited space around the edge not all signals can be probed
- Choose between wide / narrow Address or data



## MSO Interposers

- Provides a quick and easy access of the Addr/CMD signals to MSO digit
- Allows the Addr/cmd triggers to correlate Analog Inputs
- Combine with Component Interposers for high fidelity analog analysis

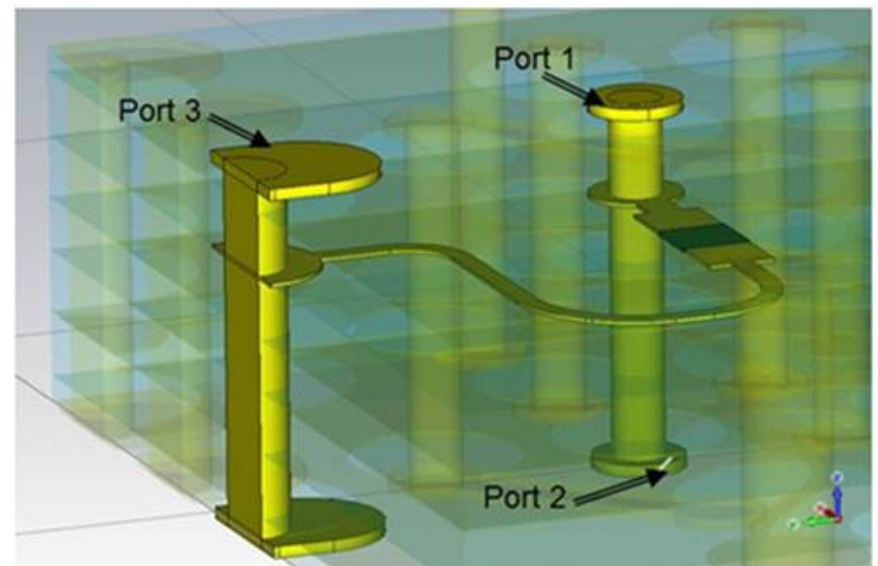
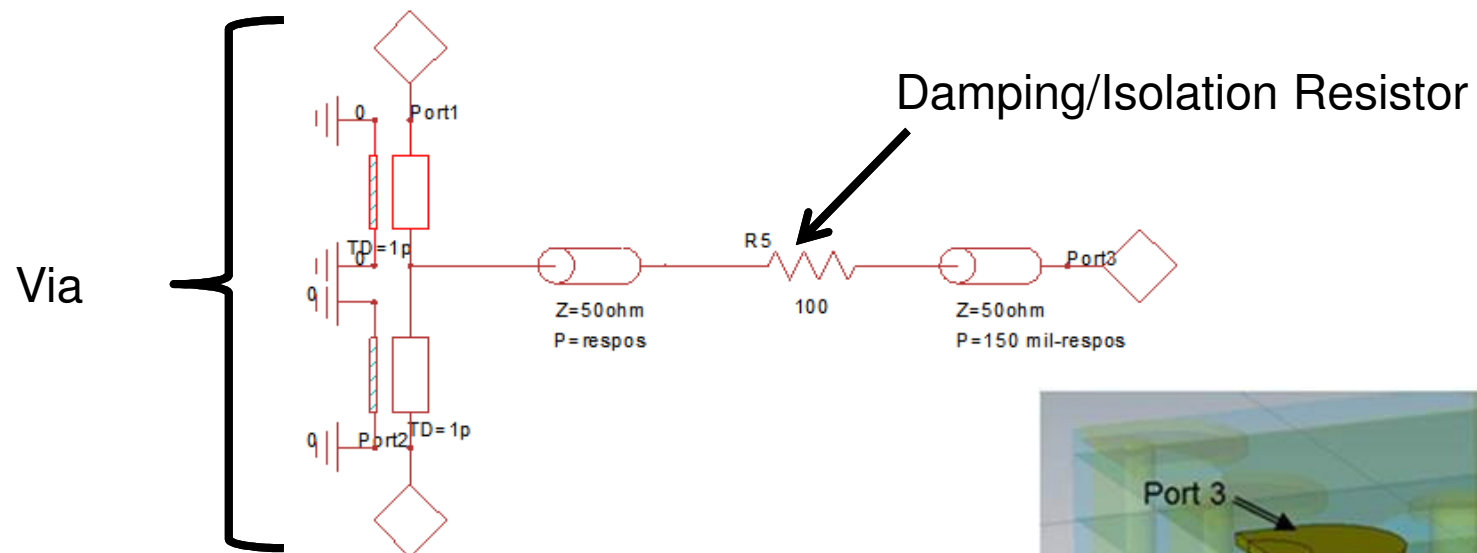


# Interposer Availability

Technology	Package / Form Factor
DDR2	Socketed – 60 Ball/ 84 Ball Solder-down – 60 Ball/ 84 Ball
DDR3	Socketed – 78 Ball/ 96 Ball Solder-down – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball – Coming soon! DIMM Interposer for MSO SO-DIMM Interposer for MSO
DDR4	Socketed – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball Edge Probe – 144 Ball – Coming soon! DIMM Interposer for MSO
LPDDR	Socketed – 60ball
LPDDR2	Socketed – 136 ball/168 ball/216 ball/240 ball
LPDDR3	Socketed – 216 ball Solder-down – 178 ball
GDDR5	Socketed – 170 ball Solder – down – 170 ball

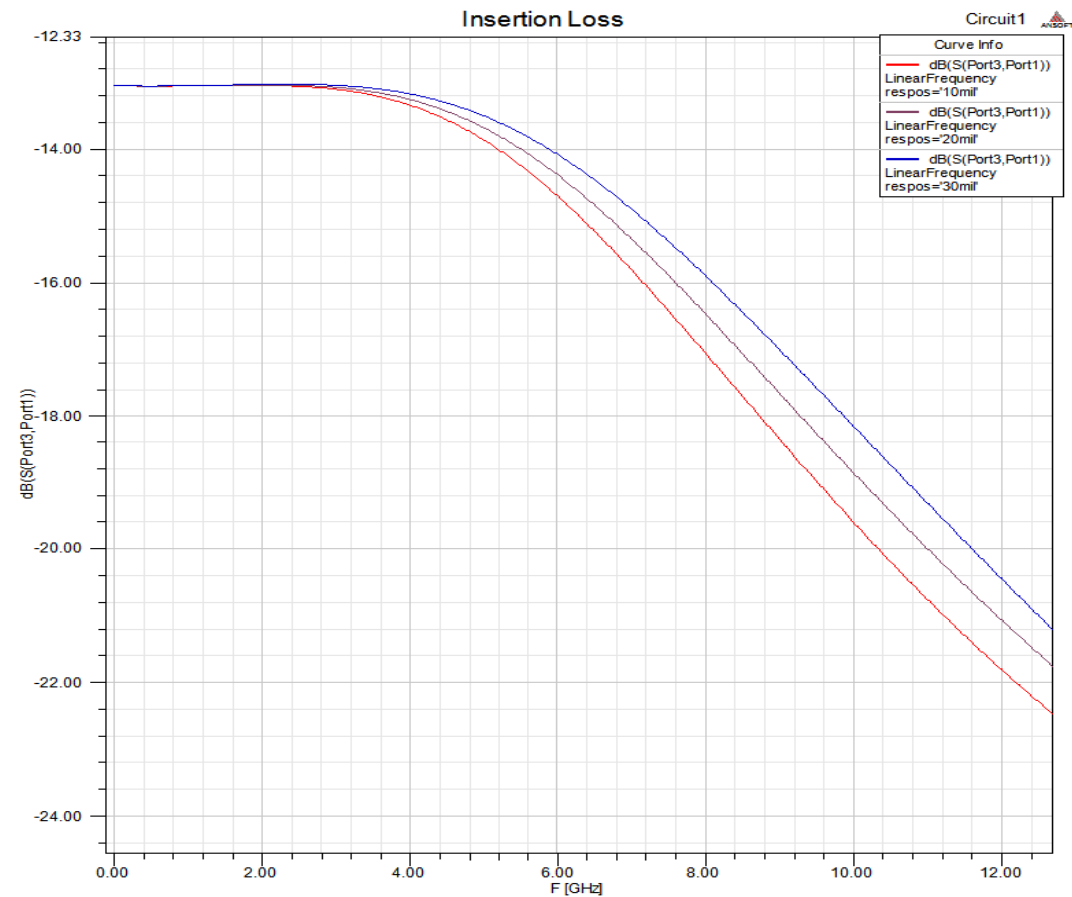


# Probe Modeling



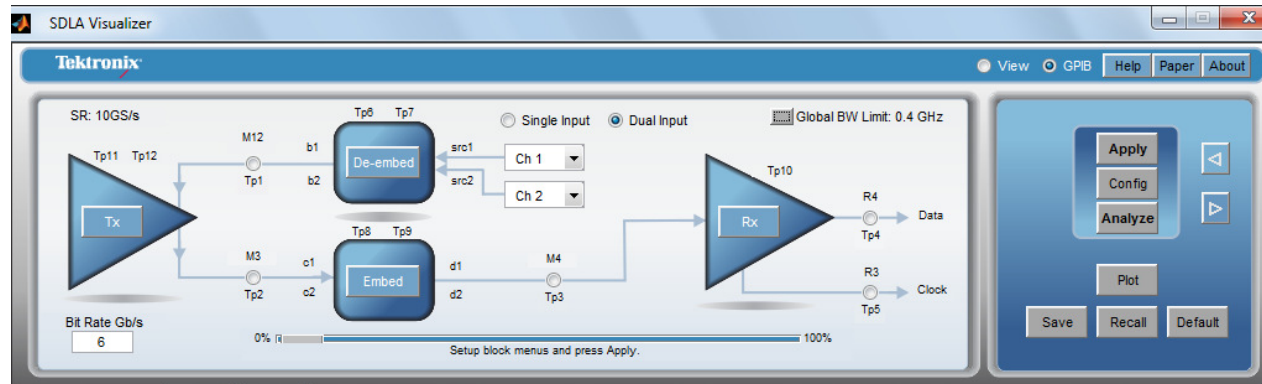
# Frequency Response

- Models the insertion loss based on placement of Isolation resistor
- Resistor closer to Via has better response than the one further away



# De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will be available for the interposers upon request. These de-embedding filters are developed assuming nominal values
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used



# Signal Acquisition and Analysis

Triggering, ASM, DDRA and DPOJET



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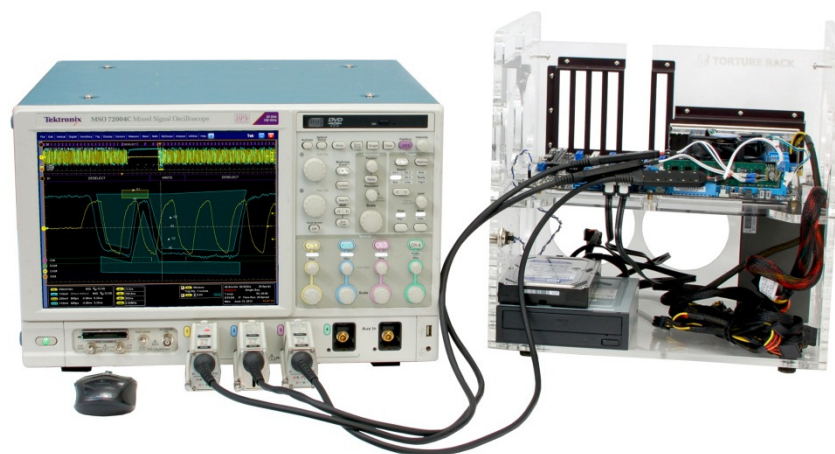
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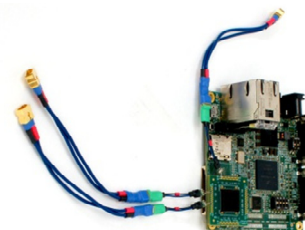
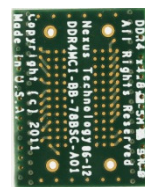
# Oscilloscope Bandwidth Requirement

Memory Technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s
Max slew rate	5	5	5	10	12	12	8	18
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8
20-80 risetime (ps)	216	150	150	60	50	45	45	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0
Recommended Scope BW (Max Performance)	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16
Recommended Scope BW (Typ Performance)	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 and LPDDR3 is supported only on DSA/MSO/DPO70000C/D models only

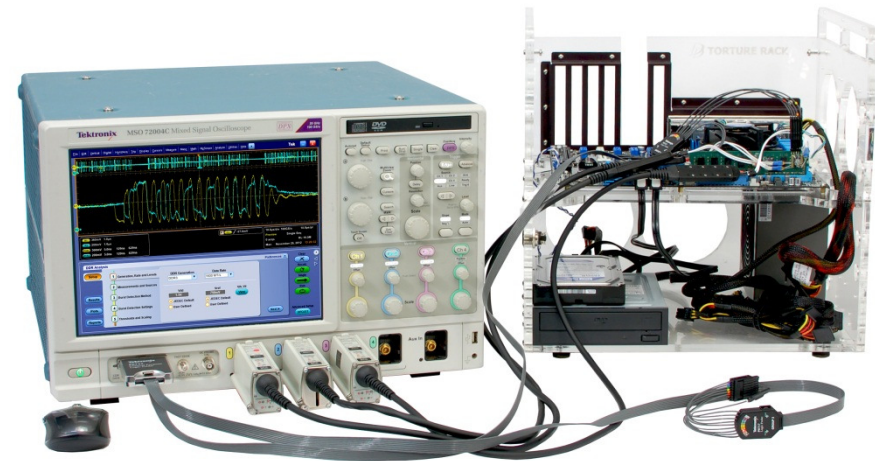


Microsoft Excel  
Worksheet



# Debug and Analysis Tools

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark
  - DDRA

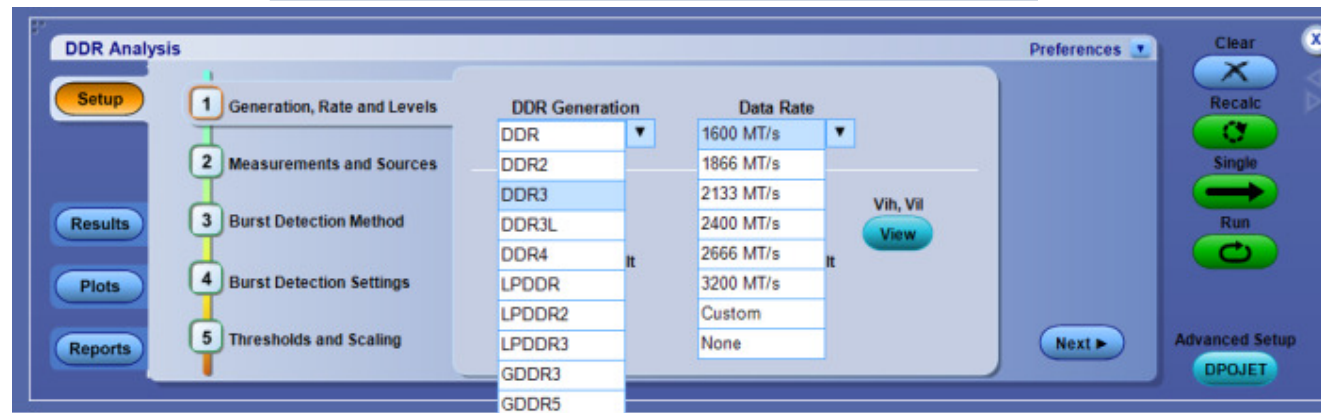




# Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212





## DDRA Measurement Process

DDRA Inputs

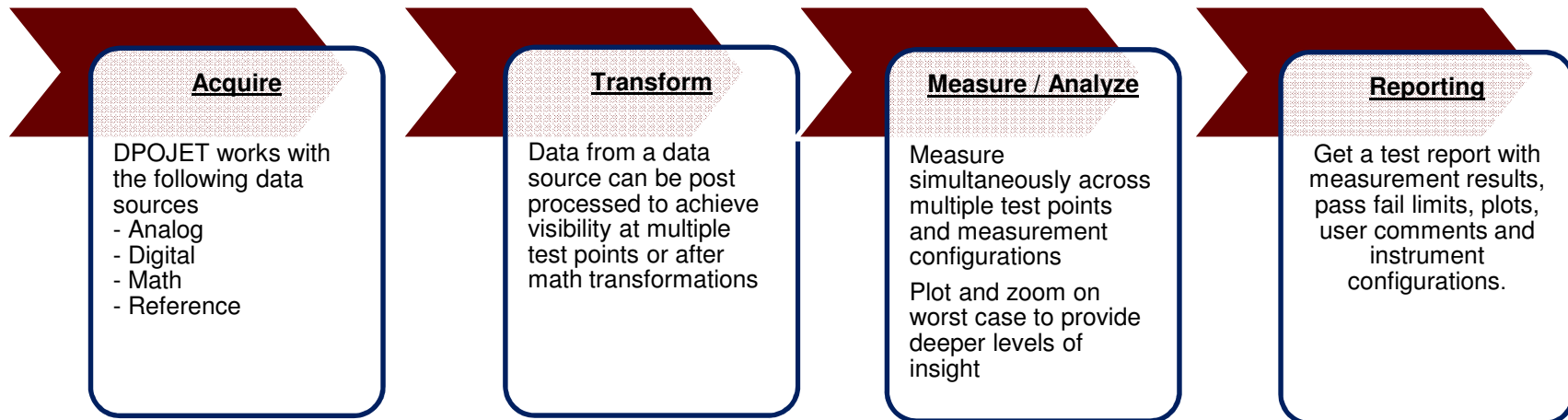
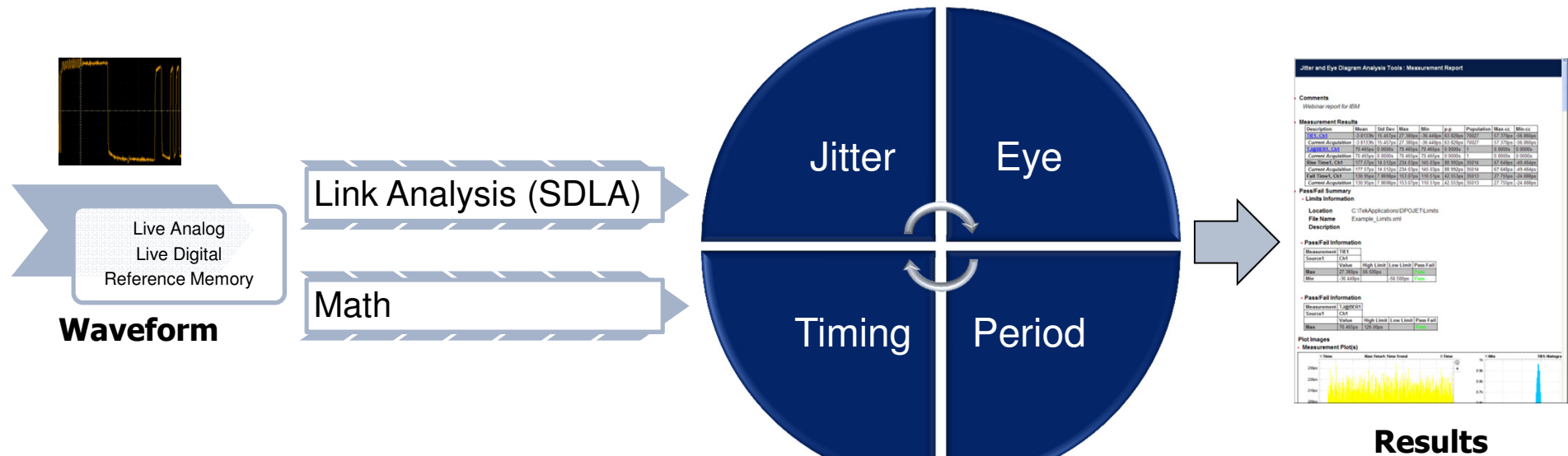
ID reference levels

Search and Mark relevant sections

Perform Measurements

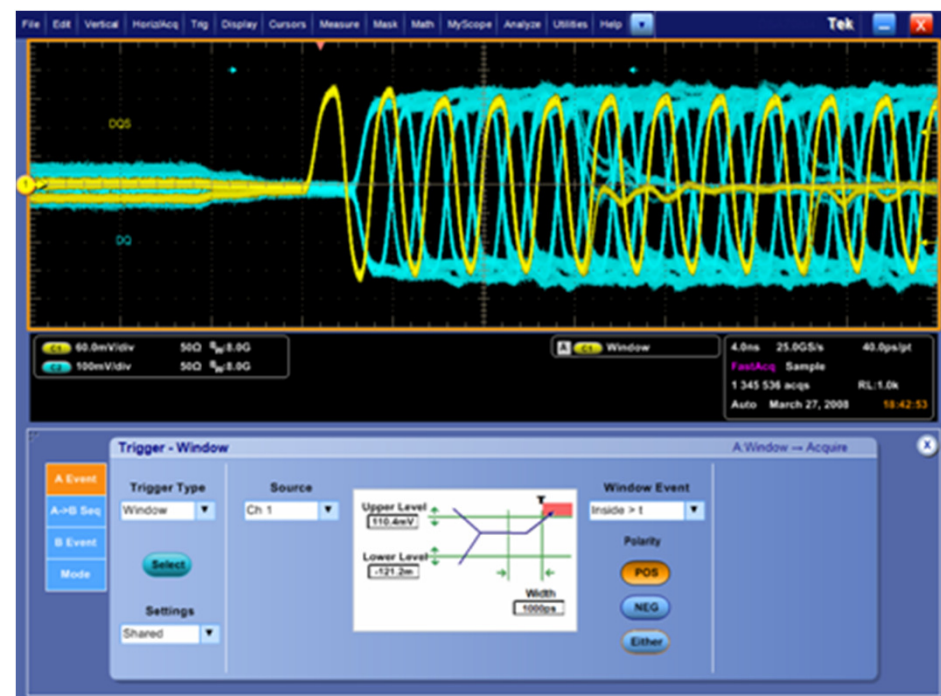
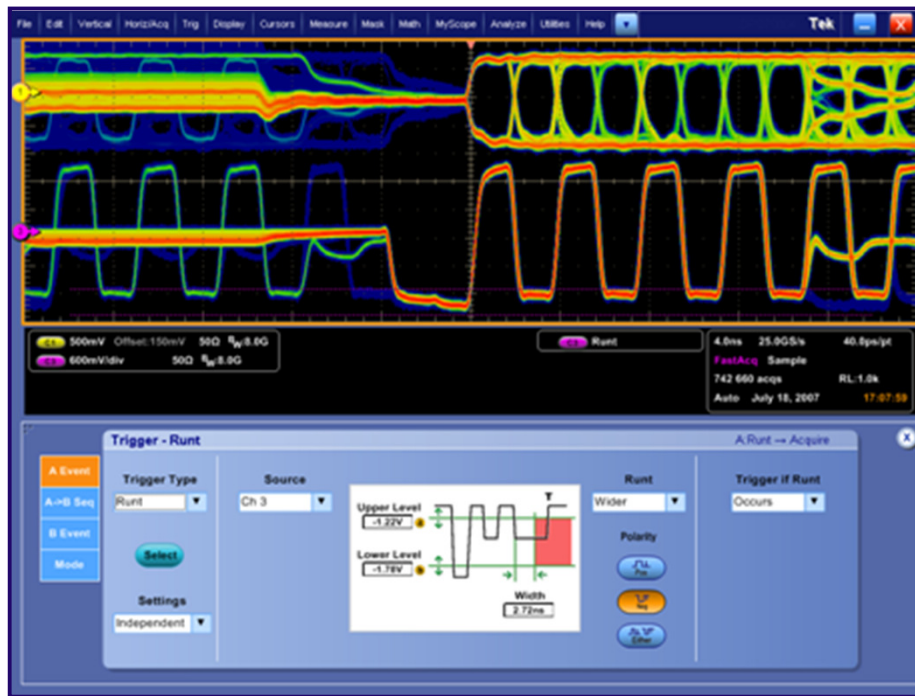
Generate Reports / Plots

# DPOJET Analysis Overview



# Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
  - FastAcq shows any disparities on signals, like infrequent glitch’s



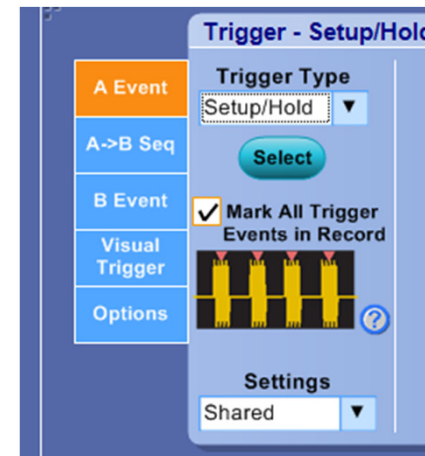
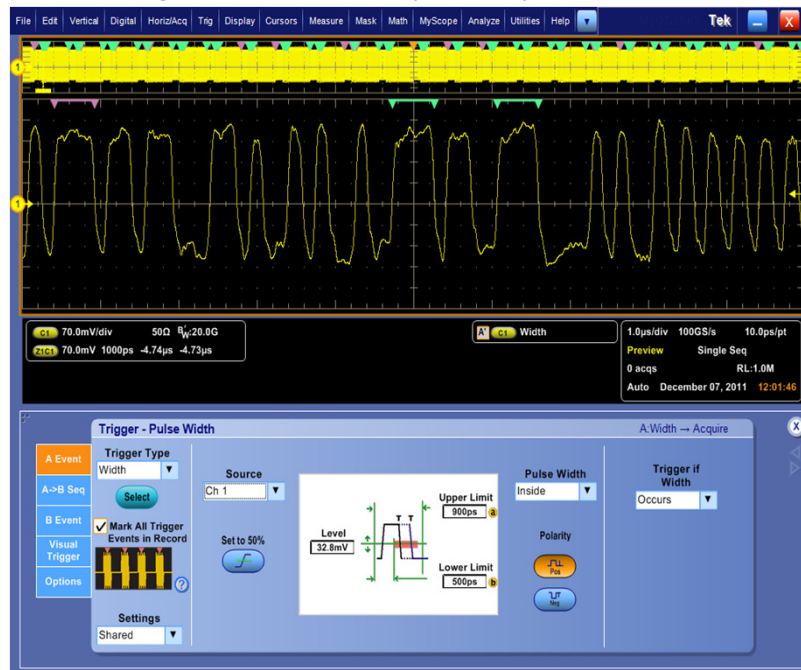


## Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Option VET required
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 vertices
- Areas are “keep in” or “keep out”
- Apply to either trigA or trigB, whichever is last
- Used to
  - Separate Read bursts from Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams

# Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
  - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
  - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA



# Advanced Search and Mark

- Tabular Results and Navigation
  - Events by Type – read/write or other events
  - Time stamps, delta-times between events
  - Intuitive navigation – Zoom on the burst of interest
- 'Stop on Found' works as a pseudo-trigger mode

The screenshot displays the Tektronix Advanced Search and Mark interface. It features a sidebar with navigation buttons: Select, Configure, Results (highlighted), View, and Mode. The main area is divided into two sections: 'Results: Counts' and 'Results: Mark Table'.

**Results: Counts**

	Type	Source	Count
1	DDR Read	Ch 1,Ch 2	130
2	DDR Write	Ch 1,Ch 2	157

**Results: Mark Table**

	Index	Type	Src	Location	Time Delta					Description
					sec	ms	us	ns	ps	
	1	DDR Write	C1	-8.579us						DDR3 - WRITE - 1.066G
Z2	2	DDR Write	C1	-8.496us	000	000	000	082	480	DDR3 - WRITE - 1.066G
	3	DDR Write	C1	-8.414us	000	000	000	082	520	DDR3 - WRITE - 1.066G
Z1	4	DDR Write	C1	-8.331us	000	000	000	082	500	DDR3 - WRITE - 1.066G
	5	DDR Write	C1	-8.29us	000	000	000	041	240	DDR3 - WRITE - 1.066G
	6	DDR Write	C1	-8.208us	000	000	000	082	500	DDR3 - WRITE - 1.066G
Total Marks: 287					ΔZ1,Z2					000 000 000 164 000
					ΔZ2,Z3					
					ΔZ1,Z3					

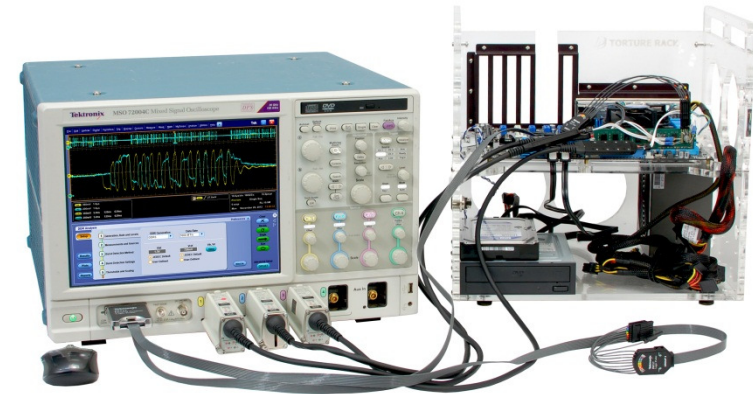
At the bottom, there are buttons for 'Search Marks' (Save, Save All, Clear, Digits >>) and 'All Marks' (Export, Clear). A 'View Count' button is also present.



# Summary – World's Best Memory Test Solution

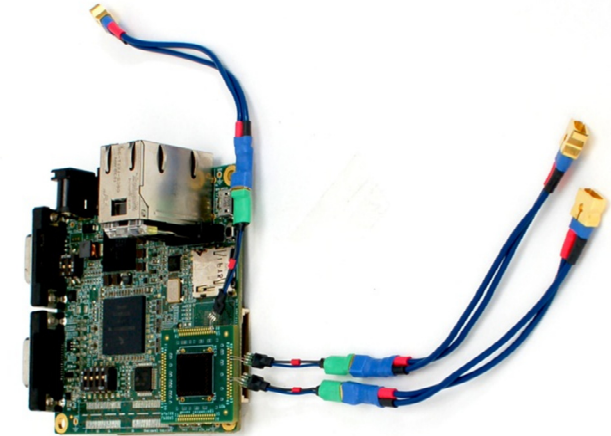
## Complete

- Provides JEDEC validation, characterization and full measurement support
- Comprehensive coverage of multiple memory standards in one single package



## Performance

- Based upon high performing oscilloscopes and software analysis tools
- TriMode probing that enables three measurements with a single probe connection
- Read/Write burst identification on all bursts
- Automated setup with JEDEC pass/fail limits



**Comprehensive Analog Verification and Debug Tools for Memory Interface**



Q &A

**Tektronix®**