Memory Solutions

Industry Trends and Solution Overview

Tektronix Innovation Forum

Leading Solutions for Today, Tomorrow and Beyond
Outline

- Industry Trends & Market Status
- Existing SDRAM Technologies
  - DDR3, DDR3L, DDR3U
    - DDR3 Signaling
  - LPDDR2/LPDDR3
    - LPDDR3 Signaling
  - DDR4
    - DDR4 Signaling
- “Emerging” SDRAM Technologies
  - LPDDR4
  - WideIO2
  - HBM (High Bandwidth Memory)
  - HMC (Hybrid Memory Cube)
  - Bandwidth and Pin Count
- Memory Validation Continuum – Solution Overview
Industry Trends & Market Status
DRAM Market Status

- Three Sub segments all focused on single standard
- Computer segment disappearing and market bifurcation into Server and Consumer
DRAM Industry Trends

- Consumer
  - Form Factor
  - Power
  - Performance
  - RAS Low

- Server
  - Capacity
  - Power
  - RAS high
  - Performance
Consumer DRAM Market status

**Consumer**
- **Current**
  - LPDDR3
  - DDR3
  - DDR3L
- **Future**
  - LPDDR4
  - WIO2

**Server**
- **Current**
  - DDR4
  - DDR3
- **Future**
  - HMC
  - HBM
DRAM Applications Overview

- **Handheld**
  - LPDDR2, LPDDR3
  - LPDDR4
  - Solderdown/CSP/PoP

- **Mobile/Home/Office Computing**
  - WideIO2
  - TSV
  - Solderdown/CSP/PoP
  - UDIMM/SODIMM

- **Infrastructure Computing**
  - x8/x16 DDR3, DDR3L (U)
  - x4/x8 DDR4 / 3DS
  - RDIMM/LRDIMM

- **Infrastructure Networking**
  - x4/x8 DDR3, DDR3L, (DDR3U)
  - HMC
  - RLDRAM ...

- **Graphics**
  - DDR3(x32), GDDR5

- **High Performance Computing**
  - WideIO2
  - HBM
  - TSV
  - Solderdown
Existing SDRAM Technologies

- DDR3, DDR3L, DDR3U
- LPDDR2/LPDDR3
- DDR4
DDR3/DDR3L(/DDR3U)
Server and Desktop/Mobile Computing

Protocol Layer
- Command based interface
- Separate Command/Address and data bus
- Power state management via CKE
- No dedicated connectivity test mode
- Clock/Strobe calibration (write leveling)

Physical Layer
- DDR Signaling, Midlevel Referencing (VREFCA, VREFDQ)
- SDR CA-bus, differential clock
- Bidirectional single ended data bus (800 – 2133 Mbps/pin), differential strobe
- programmable Midlevel ODT, ZQ calibrated
- programmable Drive Strength, ZQ calibrated

Packaging Technology
- Typical DIMM with 8…36 single SDP’s (or DDP, QDP, 3DS)
- x4/x8 (server) x8/x16 (mobile computing) x32 (low end graphics)
- E.g. x8 has 44 active signals, window BGA (CSP), 0.8 mm ball pitch
- UDIMM, RDIMM, LRDIMM socket 240-pins 1.0 mm pitch
- X64/x72 DIMM has 6.4 GBps … 14.1 GBps per channel
DDR3/DDR3L(/DDR3U): Signaling Details (1)

- VDD = VDDQ: 1.5V, L=1.35V, (U=1.25 V)
- AC-Input Levels:
  +/-175 mV…+/- 125 mV around VREF(dc)
- DC-Input levels:
  +/- 100 mV …. +/-90 mV around VREF(dc)
- Strobe crossing centered in data eye for Write;
  Rising strobe edge centered between two falling clock edges
  tDSS = +/- ¼ tCK
- Strobe edge aligned with clock for Reads;
  tDQSCCK = +/- 10% tCK
  Data aligned with strobe for Reads
- Slew rate dependent setup/hold (derating)
- ADD/CMD – eye centered around rising clock edges (SDR)
DDR3/DDR3L/DDR3U: Signaling Details (5)

Preamble/Postamble Read/Write
LPDDR2 and LPDDR3

**Handheld**

**Protocol Layer**
- DDR Command/Address (10xCA-) bus; 2-halfcycle commands
- Different Prefetch LPDDR2: S2, S4; LPDDR3 S8
- LPDDR2 also supports NVM, **LPDDR3 does NOT**
- No dedicated connectivity test mode
- Clock/Strobe calibration (write leveling); LPDDR3: *Clock/CA training*

**Physical Layer**
- DDR Signaling, Midlevel Referencing (VREFCA, VREFDQ)
- DDR CA-bus, differential clock, SDR CS#
- Bidirectional single ended data bus (400 – 1066 - 2133 Mbps/pin)
- Differential strobe, unterminated HSUL, **LPDDR3 adds VDD term option**
- Programmable Drive Strength, ZQ calibrated

**Packaging Technology**
- PoP or side-by-side CSP solder-down, 0.4, 0.5, 0.65x0.8 mm ball pitch
- MCP in with separate NVM (eMMC, UFS) channel(s)
- Edge-pad die with wire-bonded DDP/QDP, very thin
- Typically one or two channels; x32 DQ per channel; 1.6 – 7.0 GBps per channel
- ~60 active pins per (x32) channel
LPDDR2/3: Signaling Details

- VDDQ: 1.2V
- AC-Input Levels:
  - LPDDR2: +/-300 mV…+/- 220 mV around VREF
  - LPDDR3: +/-150 mV…+/- 135 mV around VREF
- With VDDQ termination VREF may be off-centered!
- CA bus DDR, eye centered around clock crosspoint
- CS_n is SDR, only latched with rising clock edges
- Strobe centered in data eye for Writes,
- Strobe aligned with clock for Writes
  \[ tDQSS = +/­ 1/4 \text{ tCK} \]
- Strobe edge aligned with data for Reads;
- No DLL: strobe NOT aligned with clock for Reads;
  \[ tDQSCK = 2.5…5.5 \text{ ns} \]
- Slew rate dependent setup/hold (derating) referenced to clock/strobe crosspoint
- \( tQH \) (while defined the same way as in LPDDR2) has much larger value (in %UI) compared to LPDDR2
**DDR4**

*Server (and Mobile Computing)*

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**Protocol Layer**
- Command based interface like DDR3
- CA parity, Data CRC (for higher data rate), DBI(dc)
- Dedicated connectivity test mode (mandatory for x16/x32)
- Clock/Strobe calibration (write leveling); 'internal VREFCA' training
- DQS/DQ training; 'internal VREFDQ' training;

**Physical Layer**
- DDR Signaling, Internally programmable VREFCA, VREFDQ/bytelane
- SDR CA-bus (~23x), differential clock
- Bidirectional single ended data bus (1600 – 3200 Mbps/pin), diff. strobe
- Databus VDDQ terminated, programmable ODT, ZQ calibrated
- Programmable Drive Strength, ZQ calibrated

**Packaging Technology**
- Typical DIMM with 8…36 single SDP’s (or DDP, QDP) or 2H, 4H, 8H 3DS
- x4/x8 (server) x8/x16 (mobile computing) x32 (low end graphics)
- E.g. x8 has xx active signals, window BGA (CSP), 0.8 mm ball pitch
- UDIMM, RDIMM, LRDIMM socket 288-pins 0.85 mm pitch
- X64/x72 DIMM has 12.8 GBps … 25.6 GBps per channel
DDR4: Signaling Details

- VDD = VDDQ: 1.2V, (maybe $\rightarrow$ 1.1V $\rightarrow$ 1.0 V in the future)

- Generally like DDR3; except:
  - No external VREF. Replaced by internally trained VREF and virtual “VCENT”
  - Mask type data valid window
    mask height $\sim$ +/- 68 mV … xxx mV
    (corresponds to DDR3 dc-levels)
    VIHL_ac = +/- 93 mV
    (corresponds to DDR3 ac-levels)
  - VDDQ Termination
DDR4 Rx Data Eye Detail: ac/dc levels -- mask

- Redefinition from (min) ac/dc levels that **must be applied** externally (as system requirement)
  - (max) mask height (VdIVW) that receiver is **allowed to require** (as receiver property)
- VREF is internal and trained in DDR4 system → only virtual Vcent externally
- AC-level has to be reached, but at no particular time
DDR4 Rx Data Eye Detail: Statistical Mask

- $T_{dIVW} (\text{max})$ is centered around the strobe crossing (replaces min setup/hold)
- $V_{dIVW} (\text{max})$ is centered around $V_{\text{cent}}$
- $V_{\text{cent}}$ is the calculated to be the widest eye-opening
- Allow $V_{dIVW}$ and $T_{dIVW}$ to have bounded (deterministic) and gaussian (random) properties.
Memory Validation Continuum
Memory Validation Continuum

- **Electrical Validation**
- **Logic Validation**
- **Execution Validation**

**Instruments**

**Probes**

**Analysis SW**
Memory Validation Continuum

- Complete Solution for the Memory Application Space
- Best in class solutions for Electrical, Logic and Execution Validation plus correlation and time-to-data capabilities unique to Tektronix
  - iCapture and iView Capability
  - Socketed interposers
  - iCis
  - Shared Interposers
  - Common compliance software
  - Single probing multiple views
  - MSO Slot+MCI probing combination
iCapture / iView

MSO

TLA
Socketed Interposers

Socketed Scope Interposer

Socketed LA Interposer
Data Displays

iCi’s

Traditional LA Display
MSO Interposer Combination
Shared Probing

LA Probes

Interposers
Protocol Compliance

Offline Protocol Compliance

Real-Time Protocol Compliance
Single Probe Multiple Views
Memory Interface Electrical Validation

Measure the analog signal characteristics; trtf, Vmin/max, jitter, eye size, crossover, strobe/clock alignment, etc.
Memory Validation Continuum

- **Instruments**
  - Analog Validation
  - Digital Validation
  - Execution Validation

- **Probes**

- **Analysis SW**
Signal Access

Probing

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Probing

P7300 Probes

P7500 Probes

51W-29204-0 How To Guide P7500 Tip Selection Solder Guide.pdf
Interposer Types

**Socketed Interposers**
- Comes with a Custom BGA Socket that needs to be soldered to Target
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

**PoP Interposers**
- Comes with a Custom BGA Socket that needs to be soldered to Application Processor
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

**Direct Attach Interposers**
- Interposer is soldered to Target
- Memory Component is soldered to Interposer
- Full BGA visibility
- No Special design or routing requirements needed
Interposer Types

**Direct Attach Perimeter Interposers**
- Interposer is soldered to the Target
- Memory component is soldered to Interposer
- Signals are brought to pads on edge of the Interposer
- KoV of the interposer is the same size as the BGA component
- Because of limited space around the edge not all signals can be probed
- Choose between wide / narrow Address or data

**MSO Interposers**
- Provides a quick and easy access of the Addr/CMD signals to MSO digital
- Allows the Addr/cmd triggers to correlate Analog Inputs
- Combine with Component Interposers for high fidelity analog analysis
## Interposer Availability

<table>
<thead>
<tr>
<th>Technology</th>
<th>Package / Form Factor</th>
</tr>
</thead>
</table>
| **DDR2**   | Socketed – 60 Ball/ 84 Ball  
Solder-down – 60 Ball/ 84 Ball |
| **DDR3**   | Socketed – 78 Ball/ 96 Ball  
Solder-down – 78 Ball/ 96 Ball  
Edge Probe – 78 Ball/ 96 Ball – Coming soon!  
DIMM Interposer for MSO  
SO-DIMM Interposer for MSO |
| **DDR4**   | Socketed – 78 Ball/ 96 Ball  
Edge Probe – 78 Ball/ 96 Ball  
Edge Probe – 144 Ball – Coming soon!  
DIMM Interposer for MSO |
| **LPDDR**  | Socketed – 60ball  |
| **LPDDR2** | Socketed – 136 ball/168 ball/216 ball/240 ball |
| **LPDDR3** | Socketed – 216 ball  
Solder-down – 178 ball |
| **GDDR5**  | Socketed – 170 ball  
Solder – down – 170 ball |
Probe Modeling

Via

Damping/Isolation Resistor

35
Frequency Response

- Models the insertion loss based on placement of Isolation resistor
- Resistor closer to Via has better response than the one further away

![Graph showing frequency response with insertion loss on the y-axis and frequency on the x-axis.](image)
De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will available for the interposers upon request. These de-embedding filters are developed assuming nominal values.
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used.
Signal Acquisition and Analysis
Triggering, ASM, DDRA and DPOJET
# Oscilloscope Bandwidth Requirement

<table>
<thead>
<tr>
<th>Memory Technology</th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR3</th>
<th>DDR3L</th>
<th>LPDDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>all rates</td>
<td>to 400MT/s</td>
<td>to 800MT/s</td>
<td>to 1600MT/s</td>
<td>to 2400MT/s</td>
<td>to 1600MT/s</td>
<td>to 1600MT/s</td>
<td>to 3200MT/s</td>
</tr>
<tr>
<td>Max slew rate</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>8</td>
<td>18</td>
</tr>
<tr>
<td>Typical V swing</td>
<td>1.8</td>
<td>1.25</td>
<td>1.25</td>
<td>1</td>
<td>1</td>
<td>0.9</td>
<td>0.6</td>
<td>0.8</td>
</tr>
<tr>
<td>20-80 risetime (ps)</td>
<td>216</td>
<td>150</td>
<td>150</td>
<td>60</td>
<td>50</td>
<td>45</td>
<td>45</td>
<td>27</td>
</tr>
<tr>
<td>Equivalent Edge BW</td>
<td>1.9</td>
<td>2.7</td>
<td>2.7</td>
<td>6.7</td>
<td>8.0</td>
<td>8.9</td>
<td>8.9</td>
<td>15.0</td>
</tr>
<tr>
<td>Recommended Scope BW (Max Performance)</td>
<td>2.5</td>
<td>3.5</td>
<td>4.0</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>16</td>
</tr>
<tr>
<td>Recommended Scope BW (Typ Performance)</td>
<td>2.5</td>
<td>2.5</td>
<td>3.5</td>
<td>8.0</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
</tr>
</tbody>
</table>

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 and LPDDR3 is supported only on DSA/MSO/DPO70000C/D models only
Debug and Analysis Tools

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark
  - DDRA
Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>JEDEC Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>JESD79E</td>
</tr>
<tr>
<td>DDR2</td>
<td>JESD79-2F</td>
</tr>
<tr>
<td>DDR3</td>
<td>JESD79-3F</td>
</tr>
<tr>
<td>DDR3L</td>
<td>JESD79-3-1</td>
</tr>
<tr>
<td>DDR4</td>
<td>JESD79-4</td>
</tr>
<tr>
<td>LPDDR</td>
<td>JESD209A</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>JESD209-2E</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>JESD209-3</td>
</tr>
<tr>
<td>GDDR5</td>
<td>JESD212</td>
</tr>
</tbody>
</table>
DDRA Measurement Process

- DDRA Inputs
- ID reference levels
- Search and Mark relevant sections
- Perform Measurements
- Generate Reports / Plots
DPOJET Analysis Overview

DPOJET works with the following data sources:
- Analog
- Digital
- Math
- Reference

Data from a data source can be post processed to achieve visibility at multiple test points or after math transformations.

Measure / Analyze:
Measure simultaneously across multiple test points and measurement configurations.
Plot and zoom on worst case to provide deeper levels of insight.

Reporting:
Get a test report with measurement results, pass fail limits, plots, user comments and instrument configurations.
Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
  - FastAcq shows any disparities on signals, like infrequent glitch's
Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Option VET required
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 verticies
- Areas are “keep in” or “keep out”
- Apply to either trigA or trigB, whichever is last
- Used to
  - Separate Read bursts from Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams
Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
  - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
  - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA
Advanced Search and Mark

- **Tabular Results and Navigation**
  - Events by Type – read/write or other events
  - Time stamps, delta-times between events
  - Intuitive navigation – Zoom on the burst of interest

- ‘Stop on Found’ works as a pseudo-trigger mode
Summary – World’s Best Memory Test Solution

Complete
- Provides JEDEC validation, characterization and full measurement support
- Comprehensive coverage of multiple memory standards in one single package

Performance
- Based upon high performing oscilloscopes and software analysis tools
- TriMode probing that enables three measurements with a single probe connection
- Read/Write burst identification on all bursts
- Automated setup with JEDEC pass/fail limits

Comprehensive Analog Verification and Debug Tools for Memory Interface
Q &A