高速串行测试方案介绍

泰克华南区技术支持工程师  余岚
High-Speed Serial Data Test Solutions

Design > Verification > Compliance Test

- PCI EXPRESS
- SERIAL ATA
- USB
- ddr3
- GbE DisplayPort
- HDMI
- MHL...

Tx + Interconnect → Rx

Transmitter Testing

System Integration
Digital Validation & Debug

Receiver Test Margin Testing

Interconnect Test

Real-time Scopes

Logic Analyzers

Arbitrary Waveform Generator

Sampling Scopes

Compliance Test

Compliance Test Software

Probing Fixtures
Storage Timelines and Solutions Development

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<th>Year</th>
<th>Gen 2 - Silicon Phase</th>
<th>Gen 3 - Silicon Phase</th>
</tr>
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<tr>
<td>2008</td>
<td>Draft Spec</td>
<td>Public Spec 6G Release</td>
</tr>
<tr>
<td>2009</td>
<td>6G Integration Phase</td>
<td>6G Deployment Phase</td>
</tr>
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<td>Gen 3 (12Gb/Sec)</td>
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<td>2011</td>
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<td>6G Deployment Phase</td>
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<td>2012</td>
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<td>6G Deployment Phase</td>
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<td></td>
<td>Gen 3 (12Gb/Sec)</td>
<td>Gen 2 - Silicon Phase</td>
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<td></td>
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<td>6G Deployment Phase</td>
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<td>2013</td>
<td>6G Integration Phase</td>
<td>6G Deployment Phase</td>
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<td>Gen 3 (12Gb/Sec)</td>
<td>Gen 2 - Silicon Phase</td>
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<td>2014</td>
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<td>6G Deployment Phase</td>
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<td>Gen 3 (12Gb/Sec)</td>
<td>Gen 2 - Silicon Phase</td>
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<tr>
<td></td>
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<td>6G Deployment Phase</td>
</tr>
</tbody>
</table>

- **Draft Spec**
- **Public Spec 6G Release**
- **6G Integration Phase**
- **6G Deployment Phase**
- **Gen 3 (12Gb/Sec)**
- **Gen 2 - Silicon Phase**
- **Gen 3 - Silicon Phase**

**Timeline Details**

- **2008**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - Public Spec 6G Release

- **2009**:
  - Gen 3 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase
  - Gen 3 (12Gb/Sec)

- **2010**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase

- **2011**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase

- **2012**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase

- **2013**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase

- **2014**:
  - Gen 2 - Silicon Phase
  - 6G Integration Phase
  - 6G Deployment Phase

**Events**

- **2009**: First official testing of Gen3 products in June
- **2009**: Commercial Gen3 product deployment.
- **2009**: Envelope of SATA IO Unified Test Definition 1.4
- **2009**: SAS3 first Spec Draft
- **2009**: IOL SAS (12) Interop
- **2009**: ATA test specification of SAS released.

**Interoperability**

- **2010**: ATA test specification of SAS released.

**Public Spec 6G Release**

- **2010**: Draft Spec
- **2010**: Public Spec Release
- **2010**: 6G Integration Phase
- **2010**: 6G Deployment Phase
- **2010**: Gen 3 (12Gb/Sec)

**6G Sata Express Integration Phase**

- **2014**: 8G (Spec 3.2) SATA-Express Deployment Phase
- **2014**: 8G SATA-Express Integration Phase
- **2014**: 12G Deployment Phase
- **2014**: Gen 3 (12Gb/Sec)
- **2014**: Gen 2 - Silicon Phase
- **2014**: Gen 3 - Silicon Phase

**Conference Dates**

- **IW#9/PF#1**: Taipei 11/16
- **IW#10/PF#15**: Milpitas CA 05/16
- **IW#11/PF#16**: Taipei 03/23
- **IW#12/PF#18**: Milpitas CA 10/14
- **IW#13/PF#19**: Taipei 05/15
- **IW#14/PF#19**: Taipei 05/15
- **IW#15/PF#22**: Milpitas CA 10/15

**Other Events**

- **2009**: Gen 2 - Silicon Phase
  - SCSI Trade Association Plugfest (UNH IOL)
  - STA test specification of SAS released.
<table>
<thead>
<tr>
<th>Tests</th>
<th>UTD 1.4.2</th>
<th>UTD 1.4.3</th>
<th>UTD 1.5</th>
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</thead>
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<tr>
<td>PHY-01 : Unit Interval</td>
<td>Normative</td>
<td>Normative</td>
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<tr>
<td>PHY-02 : Frequency Long Term Stability</td>
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<td>Normative</td>
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<td>PHY-03 : Spread-Spectrum Modulation Frequency</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>PHY-04 : Spread-Spectrum Modulation Deviation</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>TSG-01 : Differential Output Voltage</td>
<td>Normative</td>
<td>Informative</td>
<td>Informative</td>
</tr>
<tr>
<td>TSG-02 : Rise/Fall Time</td>
<td>Normative</td>
<td>Informative</td>
<td>Informative</td>
</tr>
<tr>
<td>TSG-03 : Differential Skew</td>
<td>Normative</td>
<td>Informative</td>
<td>Informative</td>
</tr>
<tr>
<td>TSG-04 : AC Common Mode Voltage</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative/Update</td>
</tr>
<tr>
<td>TSG-05 : Rise/Fall Imbalance</td>
<td>Obsolete</td>
<td>Obsolete</td>
<td>Obsolete</td>
</tr>
<tr>
<td>TSG-06 : Amplitude Imbalance</td>
<td>Obsolete</td>
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<td>Obsolete</td>
</tr>
<tr>
<td>TSG-07 : Gen1 (1.5 Gbps) TJ at Connector, Clock to Data, fBAUD/10</td>
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<tr>
<td>TSG-08 : Gen1 (1.5 Gbps) DJ at Connector, Clock to Data, fBAUD/10</td>
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<tr>
<td>TSG-09 : Gen1 (1.5 Gbps) TJ at Connector, Clock to Data, fBAUD/500</td>
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<tr>
<td>TSG-10 : Gen1 (1.5 Gbps) DJ at Connector, Clock to Data, fBAUD/500</td>
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<tr>
<td>TSG-11 : Gen2 (3 Gbps) TJ at Connector, Clock to Data, fBAUD/500</td>
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<tr>
<td>TSG-12 : Gen2 (3 Gbps) DJ at Connector, Clock to Data, fBAUD/500</td>
<td>Normative</td>
<td>Normative</td>
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<tr>
<td>TSG-14 : Gen3 (6 Gbps)TX Maximum Differential Voltage Amplitude</td>
<td>Normative</td>
<td>Normative</td>
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<tr>
<td>TSG-16 : Gen3 (6 Gbps) Tx AC Common Mode Voltage</td>
<td>Normative</td>
<td>Normative</td>
<td>Obsolete</td>
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<tr>
<td>OOB-01 : OOB Signal Detection Threshold</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-02 : UI During OOB Signaling</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-04 : COMINIT/RESET Transmit Gap Length</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-05 : COMWAKE Transmit Gap Length</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-06 : COMWAKE Gap Detection Windows</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
<tr>
<td>OOB-07 : COMINIT/COMRESET Gap Detection Windows</td>
<td>Normative</td>
<td>Normative</td>
<td>Normative</td>
</tr>
</tbody>
</table>
SATA UTD 1.5 TSG/PHY/OOB Measurements

- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - New OOB patterns
  - TSG ECN additions
# SATA/SAS: Test Report

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Pattern Name</th>
<th>Interface Speed</th>
<th>Measurement Details</th>
<th>Low Limit</th>
<th>Measured Value</th>
<th>High Limit</th>
<th>Margin</th>
<th>Units</th>
<th>Test Result</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test 5.2.1-TX SSC Modulation Type</strong></td>
<td>HFTP</td>
<td>6.0 Gbps</td>
<td>Center-spread SAS</td>
<td>-NA-</td>
<td>-NA-</td>
<td>-NA-</td>
<td>-NA-</td>
<td>-NA-</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>Test 5.2.2-TX SSC Modulation Frequency</strong></td>
<td>HFTP</td>
<td>6.0 Gbps</td>
<td>SSC Modulation Frequency</td>
<td>&gt;= 30</td>
<td>30.0000</td>
<td>&lt;= 33</td>
<td>0 , 3</td>
<td>kHz</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>Test 5.2.3-TX SSC Modulation Deviation and Balance</strong></td>
<td>HFTP</td>
<td>6.0 Gbps</td>
<td>Max Deviation</td>
<td>-NA-</td>
<td>-2109.6500</td>
<td>-NA-</td>
<td>-NA-</td>
<td>-NA-</td>
<td>Informative</td>
</tr>
<tr>
<td><strong>Test 5.2.4-TX DQDT (informative)</strong></td>
<td>HFTP</td>
<td>6.0 Gbps</td>
<td>dQ/dt</td>
<td>&gt;= -850</td>
<td>-389.3082</td>
<td>&lt;= 850</td>
<td>-NA-</td>
<td>ppm/us</td>
<td>Informative</td>
</tr>
<tr>
<td><strong>Test 5.3.1-TX Physical Link Rate Long Term Stability</strong></td>
<td>HFTP</td>
<td>6.0 Gbps</td>
<td>Mean Period</td>
<td>&gt;= -100</td>
<td>-2109.6501</td>
<td>&lt;= 100</td>
<td>-NA-</td>
<td>Informative</td>
<td></td>
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<tr>
<td><strong>Test 5.3.2-TX Common Mode RMS Voltage Limit</strong></td>
<td>CJT1a-Gen2</td>
<td>6.0 Gbps</td>
<td>Common-mode RMS voltage at IT (mV)-SAS 2.0</td>
<td>-</td>
<td>42.9227</td>
<td>&lt;= 30</td>
<td>-</td>
<td>mV</td>
<td>Fail</td>
</tr>
<tr>
<td><strong>Test 5.3.3-TX Common Mode Spectrum</strong></td>
<td>CJT1a-Gen2</td>
<td>6.0 Gbps</td>
<td>Common-mode spectrum (dBm) at 100kHz-SAS 2.0</td>
<td>-</td>
<td>-33.5689</td>
<td>&lt;= 12.7</td>
<td>46.2689</td>
<td>mv</td>
<td>Pass</td>
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<tr>
<td><strong>Test 5.3.4-TX Peak-to-Peak Voltage</strong></td>
<td>D30.3-Gen2</td>
<td>6.0 Gbps</td>
<td>Peak to Peak voltage (mVppd)-SAS 2.0</td>
<td>&gt;= 850</td>
<td>1240.0000</td>
<td>&lt;= 1200</td>
<td>390.40</td>
<td>mV</td>
<td>Fail</td>
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<tr>
<td><strong>Test 5.3.5-TX VMA and EQ</strong></td>
<td>D30.3-Gen2</td>
<td>6.0 Gbps</td>
<td>Transmitter equalization (dB)-SAS 2.0</td>
<td>&gt;= 2</td>
<td>2.0684</td>
<td>&lt;= 4</td>
<td>-</td>
<td>dB</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>Test 5.3.6-TX Rise and Fall Times</strong></td>
<td>D10.2</td>
<td>6.0 Gbps</td>
<td>Rise time in ps</td>
<td>&gt;= 41.6</td>
<td>55.7616</td>
<td>&lt;= 14.1610</td>
<td>-</td>
<td>ps</td>
<td>Pass</td>
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<tr>
<td><strong>Test 5.3.7-TX Random Jitter (RJ)</strong></td>
<td>D24.3-Gen2</td>
<td>6.0 Gbps</td>
<td>RJ before CIC</td>
<td>-</td>
<td>0.7056</td>
<td>&lt;= 25</td>
<td>24.2531</td>
<td>ps</td>
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</tr>
</tbody>
</table>

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**SATA/SAS Physical Layer Validation**
Enabling the New SATA Express Ecosystem

Desktop Connector Concept

Accept only a x2 PCIe, or a x1 PCIe cable

Accept a x2 PCIe, or a x1 PCIe, or two SATA cables

Keys that reject the SATA cables
Enabling the New SATA Express Ecosystem

Desktop Cables **Concept**

- SATA devices will coexist with next generation PCIe devices
- SATA cost/performance benefits
- Requires a connector that supports both PCIe and SATA
  - Allows a single motherboard (backplane) connector to support both interfaces
- HDD-compatible form factors to be defined for PCIe devices
  - Enables system-level mechanical compatibility
  - Preserves high-capacity storage

SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives
SATA Express Signal Access

- Recommend Luxshare-ICT Dual Port SAS fixtures (SFF-8482)
- Similar dimensions but different pinout
- For device testing use plug fixture (TF-4R21) to mate with SATAe plug
  - Both ports accessible (29 pin)
- For cable testing use receptacle fixture (TF-4P22) to mate with SATAe receptacle
  - Only port A is accessible (22 pin)

SAS Dual Port Plug Test Fixture

SAS Dual Port Receptacle Test Fixture

http://www.luxshare-ict.com/
Tektronix Solutions for SATA Express Measurements

- DPOJET-based SATA Express setup (requires option PCE3)
- Support for Base/CEM spec measurements
- Supports all versions of PCI Express and includes SATA Express PLL configurations
10GBASE-T - Overview

- 10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)
- Baseband 16-level PAM signaling with a modulation rate of 800 Msymbols per second is used on each of the wire pairs.
- Supports full duplex operation only
- Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T
- Supports a BER of less than or equal to 10E-12 on all supported distances and Classes
- Provides a cost advantage over fiber

Next Big Thing
<table>
<thead>
<tr>
<th>Measurement</th>
<th>Test Mode</th>
<th>XGbT Features / Notes</th>
<th>Does XGbT cover this measurement?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Maximum output droop</td>
<td>Sub clause 55.5.3.1, Test Mode 6</td>
<td>Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests.</td>
<td>Yes</td>
</tr>
<tr>
<td>2 Transmitter timing jitter – Master</td>
<td>Sub clause 55.5.3.3, Test Mode 2</td>
<td>Measure Jitter down to just few picoseconds. Software Filters are designed and applied on the acquired data automatically while performing measurements.</td>
<td>Yes</td>
</tr>
<tr>
<td>3 Transmit clock frequency</td>
<td>Sub clause 55.5.3.5, Test Mode 2</td>
<td>Exact value PPM for measured clock frequency is provided</td>
<td>Yes</td>
</tr>
<tr>
<td>4. Transmitter timing jitter – Slave</td>
<td>Sub clause 55.5.3.3, Test Mode 1 and Mode 3</td>
<td>Measure Jitter down to just few picoseconds. Software filters are designed and applied on the acquired data automatically while performing measurements.</td>
<td>Yes</td>
</tr>
<tr>
<td>5 Transmitter linearity</td>
<td>Sub clause 55.5.3.2, Test Mode 4 and 5</td>
<td>Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL</td>
<td>Yes</td>
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<tr>
<td>6 Transmitter power spectral density (PSD) and power level</td>
<td>Sub clause 55.5.3.4, Test Mode 5</td>
<td>Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL</td>
<td>Yes</td>
</tr>
<tr>
<td>7 Return Loss</td>
<td>Sub clause 55.8.2.1, Test Mode 5</td>
<td>Return Loss is not part of XGbT solution for now, however it will finally be released in next version. For time gap arrangement please request product line for Return Loss utility</td>
<td>Yes**</td>
</tr>
</tbody>
</table>
Transmitter Power Spectral Density (PSD) and Power Level
发送端功率谱密度及功率值

- **目的**: 确保发送端功率谱密度和功率值满足规范要求。
- 功率值应在3.2dBm~5.2dBm范围内
- 功率谱密度曲线应介于规范要求的上下限曲线之间。
- 需进入**Test Mode 5**
- **IEEE 标准 802.3an-2006, 55.5.3.4**条目。
- **Test Mode 5**: 正常操作模式
TF-XGbT Test Fixture

- The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix’s XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss.
10G-KR  Typical Backplane Ethernet

Transmitter
1. Chip and package
2. Package to board via
3. Daughter card trace
4. Daughter card to connector via
5. Connector
6. Connector to backplane via
7. Backplane trace

Receiver
10G-KR自动化测试软件
Testing connection for 10G-KR
10Gigabit Ethernet Interface Evolution

MSA Form Factors
- XENPAK Transceiver
- X2 Transceiver
- XFP Transceiver
- SFP+ Transceiver
- SFP+ direct attach
- QSFP

10GBE Standards
- IEEE 802.3ae SR/LR/ER/LX4
- IEEE 802.3ak CX4
- IEEE 802.3an 10GBASE-T LRM
- SFF-8431 SFP+

Source: Ethernet Alliance

Next Big Thing
SFF-8431 SFP+
## Tektronix SFP-TX – Automation & DPOJET Option

<table>
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<th>SL No.</th>
<th>Measurement</th>
<th>Signal Type</th>
<th>Recommended</th>
<th>Min</th>
<th>Target</th>
<th>Max</th>
<th>Units</th>
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<tr>
<td>Host Transmitter output electrical Specifications:</td>
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<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>Single Ended Output Voltage Range</td>
<td>PRBS31</td>
<td>-0.3</td>
<td>4</td>
<td>V</td>
<td></td>
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<tr>
<td>2</td>
<td>Output AC Common Mode voltage (RMS)</td>
<td>PRBS31</td>
<td>15</td>
<td>mV(RMS)</td>
<td></td>
<td></td>
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<tr>
<td>Host Transmitter Jitter and Eye Mask specifications</td>
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<td>3</td>
<td>Crosstalk source rise/fall time (20%-80%) (Tr, Tf)</td>
<td>8180</td>
<td>34</td>
<td>ps</td>
<td></td>
<td></td>
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<td>4</td>
<td>Crosstalk source amplitude (p-p differential)</td>
<td>8180</td>
<td>1000</td>
<td>mV</td>
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<td>5</td>
<td>Signal rise/fall time (20%-80%) (Tr, Tf)</td>
<td>8180</td>
<td>34</td>
<td>ps</td>
<td></td>
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<tr>
<td>6</td>
<td>Total Jitter (p-p) (Tj)</td>
<td>PRBS31</td>
<td>0.28</td>
<td>UI(p-p)</td>
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<tr>
<td>7</td>
<td>Data Dependent Jitter (p-p) (DDJ)</td>
<td>PRBS9</td>
<td>0.1</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)</td>
<td>PRBS9</td>
<td>0.055</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Uncorrelated Jitter (RMS) (UJ)</td>
<td>PRBS9</td>
<td>0.023</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Transmitter Qs5</td>
<td>8180</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Eye mask hit ratio (Mask hit ratio of 5x10-5)</td>
<td>PRBS31</td>
<td>X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Host Transmitter output specifications for Cu (SFP+ host supporting direct)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Voltage Modulation Amplitude (p-p)</td>
<td>8180</td>
<td>300</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Transmitter Qs5 Output AC Common Mode voltage</td>
<td>8180</td>
<td>63.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Output AC Common Mode Voltage</td>
<td>PRBS31</td>
<td>12</td>
<td>mV(RMS)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Host Output TWDPC</td>
<td>PRBS9</td>
<td>10.7</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SFP test connection
SFP Eye Mask hit ratio : less than 5E10-5
Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements
Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can be used to cycle through various settings of compliance patterns to perform jitter, voltage, and timing measurements.

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Preshoot</th>
<th>De-emphasis</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 GT/s,</td>
<td></td>
<td>-3.5 dB</td>
</tr>
<tr>
<td>5.0 GT/s,</td>
<td></td>
<td>-3.5 dB</td>
</tr>
<tr>
<td>5.0 GT/s,</td>
<td></td>
<td>-6.0 dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P0 = 0.0</td>
<td>-6.0±1.5dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P1 = 0.0</td>
<td>-3.5±1.5dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P2 = 0.0</td>
<td>-4.4±1.5dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P3 = 0.0</td>
<td>-2.5±1dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P4 = 0.0</td>
<td>0.0dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P5 = 1.9±1dB</td>
<td>0.0dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P6 = 1.9±1dB</td>
<td>0.0dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P7 = 1.9±1dB</td>
<td>-6.0±1.5dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P8 = 1.9±1dB</td>
<td>-3.5±1dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P9 = 1.9±1dB</td>
<td>0.0dB</td>
</tr>
<tr>
<td>8.0 GT/s,</td>
<td>P10 = 1.9±1dB</td>
<td>Test Max Boost Limit</td>
</tr>
</tbody>
</table>
Automated DUT Control

System Board / Mother Board with Multiple Slots

Oscilloscope

Control

AFG or AWG

Ref Clk

100MHz Burst for toggling

CLB with toggle switch

Data
TekExpress Automation for Tx Compliance - Setup

- Run Analysis on Live or Pre-Recorded Data
- Type of test / device selection
- Test selection
- Automate DUT control
TekExpress Automation for Tx Compliance – Test

Test Selection

- 2.5Gbps
- 5Gbps
- 8Gbps
  - Unit Interval
  - Mask Bits (All Bits)
  - Composited Eye Height
  - Transition Eye Diagram
  - Non-Transition Eye Diagram
  - Min Eye Width
  - Min Time Between Crossovers
  - TJ @ E-12
  - Dl_0d
  - RJ(RMS)
  - Peak to Peak Jitter
# TekExpress Automation for Tx Compliance – Reports

Here is an example of a TekExpress Automation for Tx Compliance – Reports page showing a table and a diagram. The table contains test results and the diagram displays the user interface of TekExpress.

### Test Results

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
<th>Generation</th>
<th>Pass/Fail</th>
<th>Value</th>
<th>Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unit Interval</strong></td>
<td>Mean Unit Interval</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>125.0090 ps</td>
<td>L: 0.0465 ps H: 0.0235 ps</td>
</tr>
<tr>
<td><strong>High Limit</strong></td>
<td></td>
<td></td>
<td></td>
<td>125.0325</td>
<td></td>
</tr>
<tr>
<td><strong>Low Limit</strong></td>
<td></td>
<td></td>
<td></td>
<td>124.9625</td>
<td></td>
</tr>
<tr>
<td><strong>Mask Hits (All Bits)</strong></td>
<td>Mask Hits</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>0.0000 hits</td>
<td>H: 0.0000 hits</td>
</tr>
<tr>
<td><strong>Composite Eye Height</strong></td>
<td>Composite Eye Height</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>105.7689 mV</td>
<td>L: 71.7689 mV</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Min Transition Eye Height</td>
<td>8Gbps P07</td>
<td>Informative</td>
<td>107.2269 mV</td>
<td>N.A</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Min Transition Voltage</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>-0.1264 mV</td>
<td>L: 599.8736 mV</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Max Transition</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>0.1289 mV</td>
<td>H: 599.8711 mV</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Min Transition Top Margin</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>0.0259 mV</td>
<td>L: 0.0259 mV</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Min Transition Bottom Margin</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>-0.0314 mV</td>
<td>H: 0.0314 mV</td>
</tr>
<tr>
<td><strong>Transition Eye Diagram</strong></td>
<td>Transition Eye Mask Hits</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>0.0000 hits</td>
<td>H: 0.0000 hits</td>
</tr>
<tr>
<td><strong>Non Transition Eye Diagram</strong></td>
<td>Min Non Transition Eye Height</td>
<td>8Gbps P07</td>
<td>Informative</td>
<td>112.3181 mV</td>
<td>N.A</td>
</tr>
<tr>
<td><strong>Non Transition Eye Diagram</strong></td>
<td>Min Non Transition</td>
<td>8Gbps P07</td>
<td>Pass</td>
<td>-0.1274 mV</td>
<td>L: 599.8726 mV</td>
</tr>
</tbody>
</table>
TekExpress Automation for Tx Compliance – Reports

![TekExpress PCI Express Add-In-Card Test Report](image)

### Setup Information

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPOJET Version</td>
<td>6.0.1 Build 8</td>
</tr>
<tr>
<td>Scope Model</td>
<td>DPO73040D</td>
</tr>
<tr>
<td>Scope Serial Number</td>
<td>B241123</td>
</tr>
<tr>
<td>SPC, FactoryCalibration, PASS, PASS</td>
<td></td>
</tr>
<tr>
<td>Date/Time</td>
<td>2013-06-10 17:28:45</td>
</tr>
<tr>
<td>Scope F/W Version</td>
<td>8.7.4 Build 3</td>
</tr>
<tr>
<td>Device Type: PCIe</td>
<td></td>
</tr>
<tr>
<td>TekExpress Version: PCI Express 2.0.0.66 (Beta_Build) Framework: 3.0.0.16_RevD</td>
<td></td>
</tr>
<tr>
<td>Spec Version: Gen3 - 3.0</td>
<td></td>
</tr>
<tr>
<td>Sig Test Version: 3.2.0</td>
<td></td>
</tr>
<tr>
<td>Slot Number</td>
<td>01</td>
</tr>
<tr>
<td>Overall Execution Time</td>
<td>00:03:21</td>
</tr>
<tr>
<td>Overall Test Result</td>
<td>Pass</td>
</tr>
<tr>
<td>Probe1 Model: TCA292D</td>
<td></td>
</tr>
<tr>
<td>Probe1 Serial Number: N/A</td>
<td></td>
</tr>
<tr>
<td>Probe2 Model: TCA292D</td>
<td></td>
</tr>
<tr>
<td>Probe2 Serial Number: N/A</td>
<td></td>
</tr>
<tr>
<td>Probe3 Model: TCA292D</td>
<td></td>
</tr>
<tr>
<td>Probe3 Serial Number: N/A</td>
<td></td>
</tr>
<tr>
<td>Probe4 Model: TCA292D</td>
<td></td>
</tr>
<tr>
<td>Probe4 Serial Number: N/A</td>
<td></td>
</tr>
<tr>
<td>Signal Source Model: AFG3252</td>
<td></td>
</tr>
<tr>
<td>Signal Source Serial Number: C010856</td>
<td></td>
</tr>
</tbody>
</table>

![Transition Eye Diagram](image)

**Transition Eye Diagram**

- **Lane0 8Gbps P07**

![Non Transition Eye Diagram](image)

**Non Transition Eye Diagram**

- **Lane0 8Gbps P07**

### Test Name Summary Table

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Interval</td>
<td>Pass</td>
</tr>
<tr>
<td>Mask Hits (All Bits)</td>
<td>Pass</td>
</tr>
<tr>
<td>Composite Eye Height</td>
<td>Pass</td>
</tr>
<tr>
<td>Transition Eye Diagram</td>
<td>Pass</td>
</tr>
<tr>
<td>Non-Transition Eye Diagram</td>
<td>Pass</td>
</tr>
<tr>
<td>Min Eye Width</td>
<td>Informative</td>
</tr>
<tr>
<td>Min Time Between Crosstalks</td>
<td>Informative</td>
</tr>
<tr>
<td>Cmitter file: /X-PCI Express\Reports/DUT001.mhtx@F_E_12</td>
<td>Pass</td>
</tr>
<tr>
<td>Sig._ed</td>
<td>Informative</td>
</tr>
<tr>
<td>SUR(JSI)</td>
<td>Pass</td>
</tr>
<tr>
<td>Peak to Peak Jitter</td>
<td>Informative</td>
</tr>
</tbody>
</table>

### Unit Interval

<table>
<thead>
<tr>
<th>Measurement Details</th>
<th>Lane Name</th>
<th>Data Rate</th>
<th>Equalization</th>
<th>Measured Value</th>
<th>Test Result</th>
<th>Margin</th>
<th>Low Limit</th>
<th>High Limit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean Unit Interval</td>
<td>Lane0</td>
<td>8Gbps</td>
<td>P07</td>
<td>125.0090 ps</td>
<td>Pass</td>
<td></td>
<td>104.5625</td>
<td>125.0325</td>
<td></td>
</tr>
</tbody>
</table>
Gen4 Update

• Key attributes/requirements of PCIe 4.0
  o 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  o Maintains compatibility w/ PCIe installed base
  o Connector enhanced electrically (no mechanical changes)
  o Limited channel: ~12”, 1 connector; repeater for longer reach

• Uniform measurement methodology applied across all data rates

• New ‘SRIS’ independent RefClk modes
  o SRIS – Separate RefClk Independent SSC Architecture

• Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  o Rev 0.9 no earlier than 1H/2015
  o Rev 1.0 no earlier than 2H/2015
USB 3.0 Key Considerations

- **Receiver Testing Now Required**
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues

- **Channel Considerations**
  - Need to consider transmission line effects
  - Software channel emulation for early designs

- **New Challenges**
  - 12” Long Host Channel
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
  - Reference channel is embedded and CTLE is applied

- USB 3.0 Reference Channels
  - Host Reference Channel
    - 11” back panel is applied for device testing
  - Device Reference Channel
    - 5” device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels

- USB 3.0 Reference Equalizer
  - Attenuates the low frequency content of the signal to open the eye

Figure 6-14. Tx Normative Setup with Reference Channel
USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate

- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod

- SSC
  - Modulation Rate
  - Deviation
Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s (2000)**
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging

- **USB 3.0, 5 Gb/s (2008)**
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture

- **USB 3.0, 10 Gb/s (2013)**
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation
USB 3.1 Tx test challenges

- **Channel considerations**
  - Need to account for > 20 dB channel loss
  - 10 Gbps requires more complicated (EQ/repeaters) signal conditioning

- **New Challenges**
  - 4” Long Host Channels @ 10 Gbps
  - Closed Eye at Rx
  - Equalization
    - 3 tap EQ at Tx
    - Continuous Time Linear Equalizer (CTLE) & Decision Feedback equalization (DFE) at Rx

---

*Source: USB 3.1 Rev 1.0 Specification*
Interoperability Challenge

- **Goal**: Any certified host works with any certified hub or device

- **Short Channel**
  - 1" host PCB route
  - ¼ " device PCB route
  - Direct plug

- **Long Channel**
  - 4" host PCB route
  - 4" device PCB route
  - 1m cable
## USB 3.1 Comparison

<table>
<thead>
<tr>
<th></th>
<th>Gen1</th>
<th>Gen2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Rate</strong></td>
<td>5 Gb/s</td>
<td>10 Gb/s</td>
</tr>
<tr>
<td><strong>Encoding</strong></td>
<td>8b/10b</td>
<td>128b/132b</td>
</tr>
<tr>
<td><strong>Target Channel</strong></td>
<td>3m + Host/Device channels (-17dB, 2.5 GHz)</td>
<td>1m + board ref channels (-20dB, 5 GHz)</td>
</tr>
<tr>
<td><strong>LTSSM</strong></td>
<td>LFPS, TSEQ, TS1, TS2</td>
<td>LFPSPlus, SCD, TSEQ, TS1, TS2,</td>
</tr>
<tr>
<td><strong>Reference Tx EQ</strong></td>
<td>De-emphasis</td>
<td>3-tap (Preshoot/De-emphasis)</td>
</tr>
<tr>
<td><strong>Reference Rx EQ</strong></td>
<td>CTLE</td>
<td>CTLE + 1-tap DFE</td>
</tr>
<tr>
<td><strong>JTF Bandwidth</strong></td>
<td>4.9 MHz</td>
<td>7.5 MHz</td>
</tr>
<tr>
<td><strong>Eye Height (TP1)</strong></td>
<td>100 mV</td>
<td>70 mV</td>
</tr>
<tr>
<td><strong>TJ@BER</strong></td>
<td>132 ps (0.66 UI)</td>
<td>71 ps (0.714 UI)</td>
</tr>
<tr>
<td><strong>Backwards Compatibility</strong></td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td><strong>Connector</strong></td>
<td>Std A</td>
<td>Improved Std A with insertion detect</td>
</tr>
</tbody>
</table>
TekExpress USBSSP-TX Software

- Automates USB 3.1 gen1 & gen2 electrical tests
- Built-in control of LFPS generator for pattern toggle
  - CP0 – CP12
- Use preferred operating mode for your application
  - **Compliance**: Full automation of ping.LFPS, analysis and reporting
  - **User-defined**: Custom channel characterization and test limits
  - **Debug**: DPOJET based manual measurements with expanded jitter analysis and plotting capabilities
HDMI Basics
HDMI 测试方案-源端
HDMI Source Testing

- Rise/Fall Time
- Inter-pair Skew
- Clock Duty Cycle
- Clock Jitter
- Eye Diagram
- Voltage VL
- Intra-pair Skew
HEAC Software

![TEK EXPRESS HEAC AUTOMATED SOLUTION (EVALUATION VERSION) (UNTITLED) SCREENSHOT]

- **Select Device**: HEAC-Receiver
- **Select Test Suite**: Differential-Rx
- **Version**: CTS 1.4
- **DUT IP Address**: 255.255.255.255
- **Auto Detect MAC Address**: checked

### Test Description

This optional test verifies the receiver capability to respond to nominal amplitude, clock frequency and...
HDMI 2.0 Features

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60/50 Hz – 594Mcsc\(^{\text{a}}\) (Mega Characters per Second per Channel)
- Support 4K 2K 4:2:0 – 297Mcsc
- 3D; 21:9; Audio
- Low level Bit error rate testing
- Scrambling is introduced and mandatory for rates >340Mcsc.

\(^{\text{a}}\) Mega Characters per Second per Channel
HDMI 2.0 Source Testing - Advanced information
Source Testing 1.4b Vs 2.0

Eye Diagram test is changed

Rest of the tests is same

1.4b CTS test is a pre-requisite for HDMI 2.0

Min 8GHz scope to 16GHz scope

Fixtures and Probes
Likely Source Electrical tests

Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – $V_L$
Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – $T_{RISE}$, $T_{FALL}$
Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew
Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew
Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage
Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle
Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter
Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram
Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance
Source Testing

- Source Eye Diagram test is measured at TP2_EQ.
- TP2 is the signal after passing along a worst cable.
  - Worst cable has worst attenuation and skew of 112ps.
Source Eye Diagram Test

Include Reference Cable Emulator (s4p) and Reference Cable Equalizer

Tektronix Oscilloscope
DPO/DSA/MSO70000 Series
≥ 16GHz

HDMI Source

HDMI Plug Fixture with EDID Emulator

TIF - Validating Next Generation Display Interfaces
TP2 Source Eye for HDMI 2.0 6G signal

Single End Input eye rendered at Tek lab
HDMI 2.0 Tx Compliance Software
Tektronix HDMI Protocol Analyzer
MHL – An Introduction

- Why MHL interface?
  - Connector agnostic…. 

- Application

Source: MHL.org
MHL Introduction

MHL Consortium was formed in Sept 2009 with the following founding members:
- NOKIA
- SAMSUNG
- Silicon Image
- Sony
- Toshiba

The Specification 1.1 version was announced in Q1 2011, Specification 1.2 in Dec 2011, Specification 2.0 in Feb 2012, Specification 2.1 in March 2013 and MHL 3.0 Specification NOW.

The Consortium released CTS 1.1 version in June 2011, CTS 1.2 in Jan 2012, CTS 2.0 in Sept 2012, CTS 2.1 in April 2013, Phase 1 CTS 3.0 in Dec 2013 and MHL CTS 3.2 in July 2014

COMPLETE TEKTRONIX SOLUTION APPROVED in CTS1.1, CTS 1.2, CTS 2.0, CTS 2.1 solution, Phase 1 CTS 3.0 solution in Dec 2013 and MHL CTS 3.2 in July 2014

Tektronix is a Contributor adopter and actively involved in defining the MHL-NEXT
Tektronix MHL 2.1 Tx Solution with Direct Attach test support
Tektronix MHL Tx Setup

MHL Differential and CM Test Setup
7 tests

Single Ended and Intra Pair Skew Test Setup
3 Tests

Also same setup is used for MHL Protocol Testing

** C-Bus Sink and Source Board is needed for hand shaking and is available from Simplay Labs
MHL 2.1 Compliance Software for Automated Tx Tests: Option MHD
Tektronix MHL Protocol Analyzer

[Diagram showing the interface of the Tektronix MHL Protocol Analyzer with options for signal source, signal assignment, video format, and list of tests.]
MHL – 3.0 Spec/CTS 3.2

- MHL Consortium and Tektronix has worked together on the 3.0 version MHL specifications.

- **Data rate changes to 6Gbps.**

- **MHL Clock is no longer common mode but transmitted on eCBUS**
  - eCBUS has bi-directional ecbus data and clock

- New test procedures for Source, Sink and Dongle

- Most of the CTS 2.1 tests need to be used to ensure backward compatibility exists.
Tektronix MHL 3.2 Solution

- Tektronix has worked closely with MHL consortium to define the next CTS version 3.0 and MHL 3.0 TX SW.

- MHL 3.2 TX Software will be orderable as Option MHD3 (needs Opt MHD)
Tektronix MHL 3.2 CTS Transmitter Solution

Transmitter / Source Tests

- AV Link Data tests (TMDS)
- Clock Tests
- eCBUS FWD Tests
- eCBus BWD Tests
MIPI标准概述
移动终端方框图实例

显示单元 -> DSI -> 显示
驱动器IC

CMOS图像传感器 -> CSI -> 摄像机
驱动器IC

扬声器 -> SLIMbus

耳机

FM无线电

麦克风

扬声器

耳机

FM无线电

麦克风

基带IC

应用
处理器

Tx/Rx
处理器

存储器接口
(如移动DDR, 移动
SDRAM, 闪存, 等等)

存储器
(内存)

存储器
(SD卡)

定义

CSI = 摄像机串行接口

DSI = 显示器串行接口

SLIMbus = 串行低功率芯片间媒体总线

空中接口
(如WiMax)

RF接口, 不受
MIPI标准影响

RF IC
(WCDMA, GSM, WLAN, FM, 蓝牙, GPS, MobileTV, 等等)

DigRF

HSI

SLIMbus
D-PHY Tx测试解决方案 – 续

示波器
- **推荐**: DPO7354或DPO/DSA/MSO70404/B
  - 用来测量规范+/−5%误差范围内的上升时间(150ps)
  - 如果不考虑上升时间的测试，可以使用DPO7254

探头
- 探头考虑因素
  - 同时测量单端性能和差分性能
  - 动态范围必须>1.2V
  - 探头衰减要达到最小
    - 1X最好，2.5X或5X也行
- **推荐**:
  - DPO7000采用四只TAP3500；MSO/DPO/DSA70000/B采用四只P7240
  - (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
  - TAP2500也适合低数据速率的DUT
- 也可以使用:
  - 焊接式探头
    - DPO7000采用TDP3500，70000系列采用P73xx
    - (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ &Clk-)
New Opt.D-PHYTX

  - TekExpress option for Fully-Automated testing
  - Automation similar to Opt.USB-TX
  - Provides Conformance and Characterization Testing
  - Based on D-PHY Base Spec v1.0 and UNH’s Conformance Test Suite v0.98.
  - Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes

- Opt.TEKEXP is Pre-Requisite

- Differentiation
  - Un-parallel Automation (Auto-Cursors/ Regions)
  - For Conformance testing to Latest CTS (v0.98)
  - Based on Latest Base spec (v1.0)

- Value proposition
  - Custom-limits/ Limits-Editing on the fly
  - Test Reports
    - Zoom-in waveform captures at the Cursors/ Regions
    - Pass/Fail Summary with Margin details
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
    - i.e. unlike Agilent 4G scope at entry-level
D-PHY Rx : Test Solution Overview
Simple, Quick, Easy and Re-usable

- **100% Coverage to Rx CTS**
  - Meets all the requirements in UNH-IOL CTS document (v0.98)

- **Quick and Easy setup**
  - No complex VXI system, just standalone instruments, and a probe.

- **Cost effective solution**
  - 70% Lower list price vs Competition

- **Re-usable for Protocol tests**
  - PG3A is the Only 4 channel solution for CSI & DSI test

- **PG3A Pattern Generator**
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver

- **AWG7082C Generator**
  - Adds jitter and interference to the D-PHY signals

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**Recommended Setup**

- PGRemote Software*
- AWG7082C
- D-PHY Coupler**
- PG3ACAB
- P331 Probe*

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*These Moving Pixel products are available as Tektronix part number
**Tektronix part number not available yet. Expected Soon.

Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI & CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. *(Win7-OS only)*
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial--> Select MIPI DSI or CSI from the drop down list.

Probe using Mixed Channels

Analog Clock, Digital Data

Digital Clock, Analog Data

Probes using Mixed Channels
Memory Technology – Quick Overview

- DRAM - dominant memory technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 1600 (1.6Gb/s) data rates
    - DDR3 2000 emerging soon (overclocked)

- DRAM variants
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
    - Optimized for Speed - faster access
Automated Test Setup

Step #1

Select DDR Generation

Select DDR Rate

Step #2

Choose measurements (Read / Write / CLK / Addr & Command)
Effective Reporting / Archiving
Installation Process
BGA Chip Interposer for Oscilloscopes

- Available in socket and solder-in versions
  - Socket design allows for multiple chip exchanges
  - Solder-in best for single use
- Recommended probes: P7500 Series
  - P7504, P7506, P7508, P7513A
  - 020-3022-00 TriMode solder tips for Nexus Interposer
High-Speed Serial Data Test Solutions…

Design ➔ Verification ➔ Compliance Test

- PCI Express
- Serial ATA
- USB
- DDR3
- GbE DisplayPort
- HDMI
- MHL...

- Tx → Interconnect → Rx

- Real-time Scopes
- System Integration
  Digital Validation & Debug
- Transmitter Testing
- Receiver Test Margin Testing
- Interconnect Test
- Arbitrary Waveform Generator
- Sampling Scopes
- Compliance Test Software
- Logic Analyzers
- Probing Fixtures

Compliance Test Software