Tektronix

各种高速串行接口的最新规范以及测试方法

Yu Ocean

2014.5

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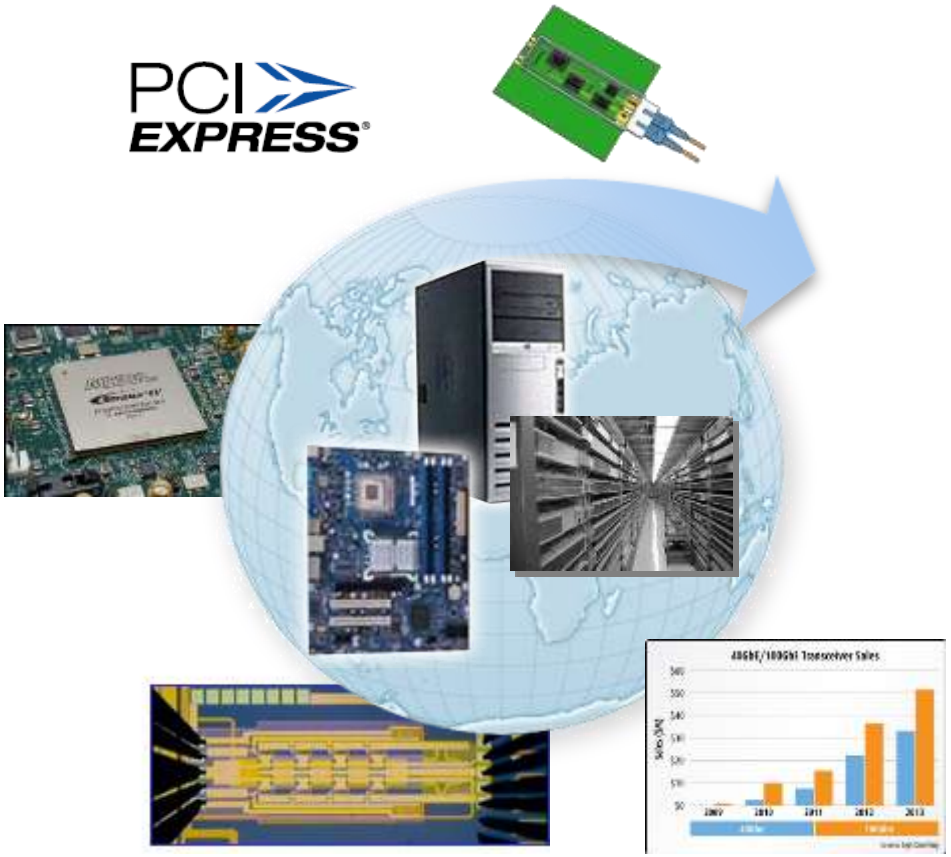
Agenda

- Industry Trend
- PCIe – Leading Data Rate in Industry
- HDMI – Introducing new HDMI 2.0
- MIPI – D-Phy to M-Phy, C-Phy is coming soon

High-Speed Serial Test

Trends and Implications



Industry/Technology Trends

- 100 GbE is becoming more relevant as data centers and communications networks ask for more bandwidth
- SAS 12G is needed by data centers for efficient transport of internet traffic (YouTube, Facebook, Smart Phone, etc)
- High-Speed FPGA's are increasing in complexity to support early designs above 28Gb/sec
- Proliferation of 10+ Gb/sec signaling in the communications network

Implications

- Closed data eyes requiring new techniques for transmitter and receiver equalization
- Higher data rate signals have less margin – requires de-embedding
- Edge/Slew rate speeds are difficult to characterize
- New Jitter Separation Measurements are required
- Complex 8b/10b signaling difficult to verify in PHY

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PCIe – Leading Data Rate in Industry

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Gen4 Update

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically (no mechanical changes)
  - Limited channel: ~12”, 1 connector; repeater for longer reach
- Uniform measurement methodology applied across all data rates
- New ‘SRIS’ independent RefClk modes
  - SRIS – Separate RefClk Independent SSC Architecture
- Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  - Rev 0.9 no earlier than 1H/2015
  - Rev 1.0 no earlier than 2H/2015

Gen4 Update

Latest Gen4 Update @ PCIe DevCon on Tue/Wed, June 25-26

- Tx Jitter – Analysis solution available today with PCE3.
- Tx EQ – CEM and Embedded will have limited change. Base might require Sampling solution.
- Rx – Similar approach at 16Gb/s.

Transmitter Jitter Spec

- PCIe 4.0 uses same jitter parameters as PCIe 3.0
  - ✓ $T_{TX-UPW-TJ}$, $T_{TX-UPW-DJDD}$, T_{TX-DDJ}, T_{TX-UTJ} and $T_{TX-UDJDD}$
  - ✓ Jitter will need to scale approximately with bitrate
  - ✓ De-embedding approach will likely remain the same
- PCIe 1.x and PCIe 2.x jitter parameters will be recast into the same form as the PCIe 3.0 parameters
  - ✓ Backward compatibility will be guaranteed
  - ✓ Some PCIe 1.x/2.x parameters will be effectively tightened
  - ✓ Example: PCIe 2.x $T_{MIN-PULSE}$ parameter will be converted into $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$

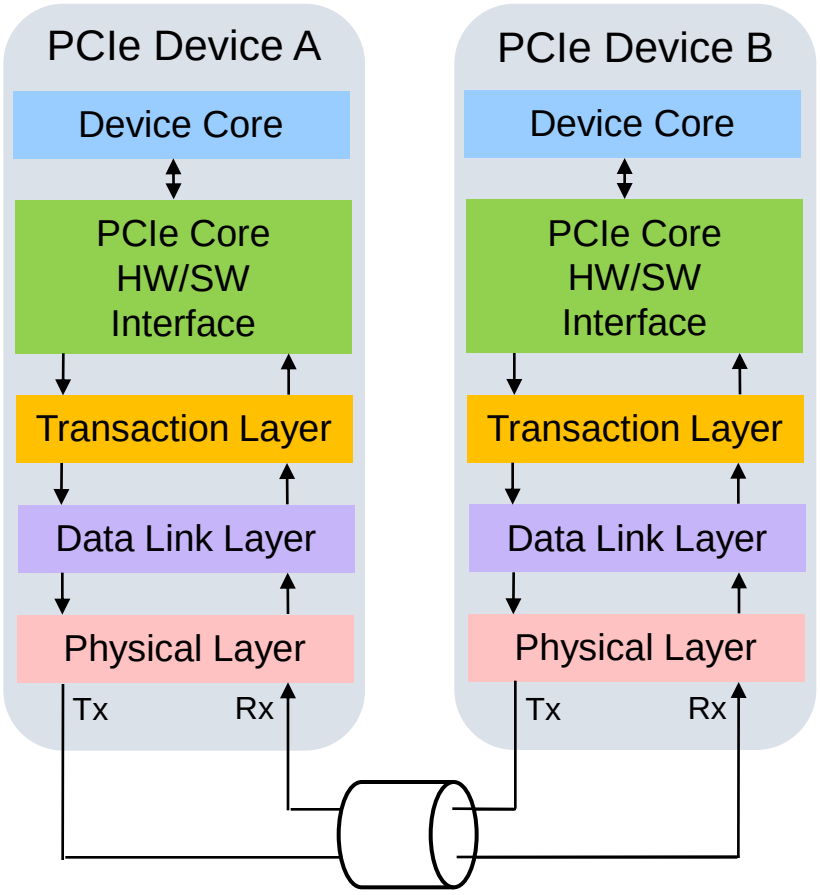
PCIe 4.0 Rx Specification

- Will continue to rely upon a stressed eye approach where both EH and EW are stressed
  - ✓ Calibration channels IL will need to be reduced to yield ~24 dB at 8 GHz
  - ✓ Behavioral package model needs to comprehend reduced C_{PAD} or include T-coil models
  - ✓ Behavioral DFE model to have increased number of taps, at least 2
  - ✓ More capable CTLE model

Transmitter Equalization

- Max PCIe 4.0 channel IL remains approx the same s for PCIe 3.0
- Plan is to retain same equalization presets
  - ✓ Training will require that only a subset of the presets be used (P7 and P8)
- Equalization coefficient range and resolution also are intended to remain unchanged
- EIEOS signaling will likely change such that no TxEQ is applied during the EIEOS interval

Testing Challenges with PCI Express 3.0



Logic Protocol Analyzer

Oscilloscope
Tx

BERTScope
Rx

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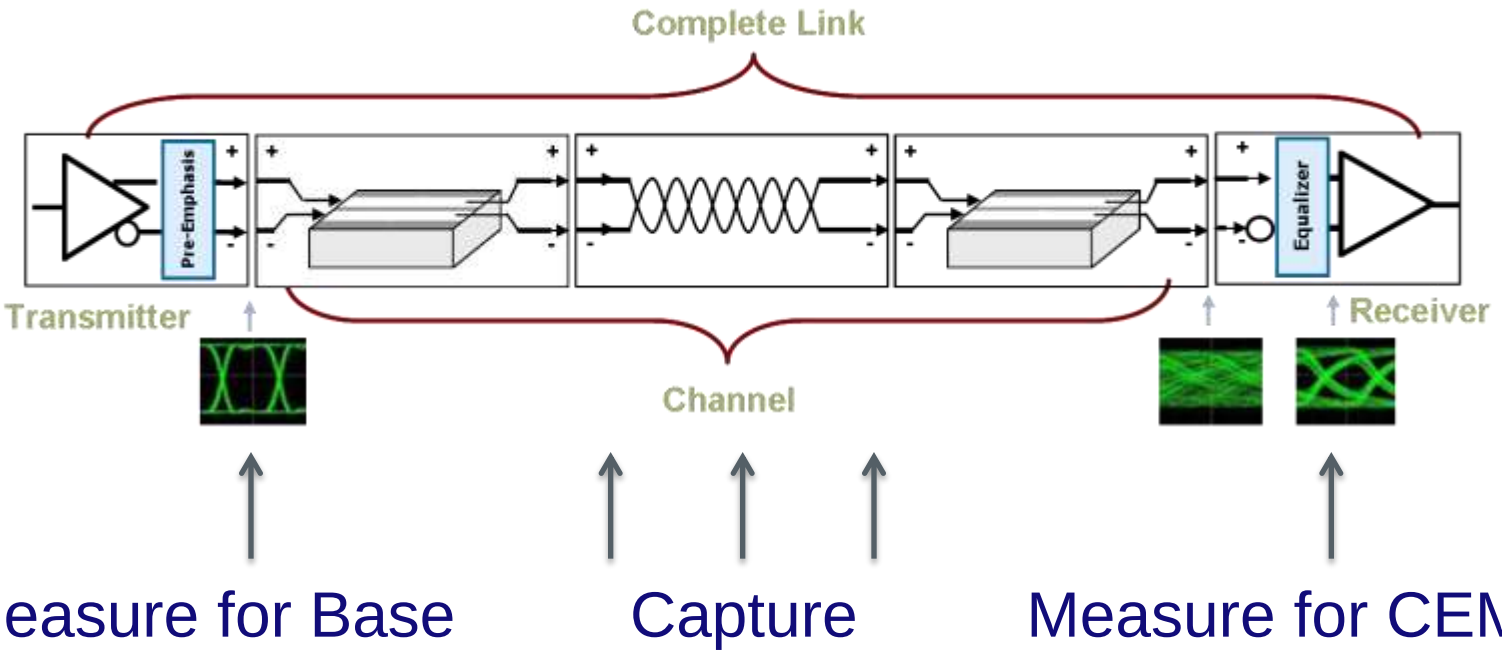
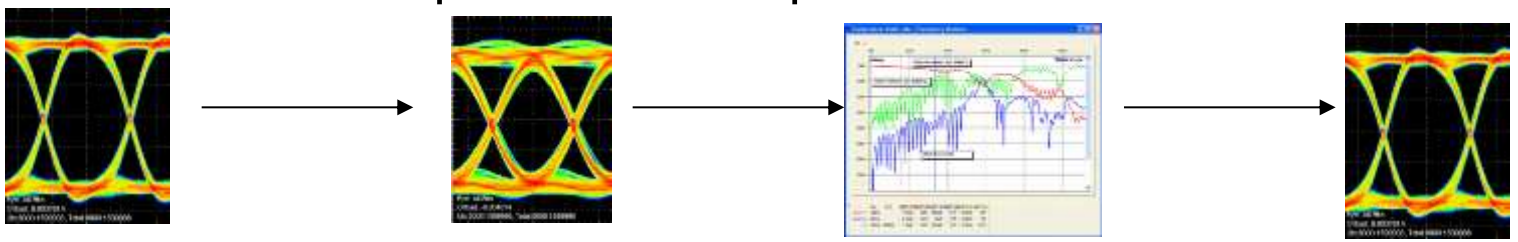
PCIe Base vs CEM Testing

- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?

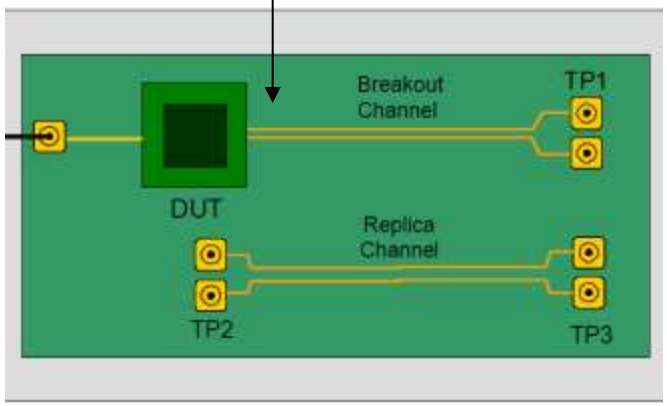


System (Base Spec) Tx Testing

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel

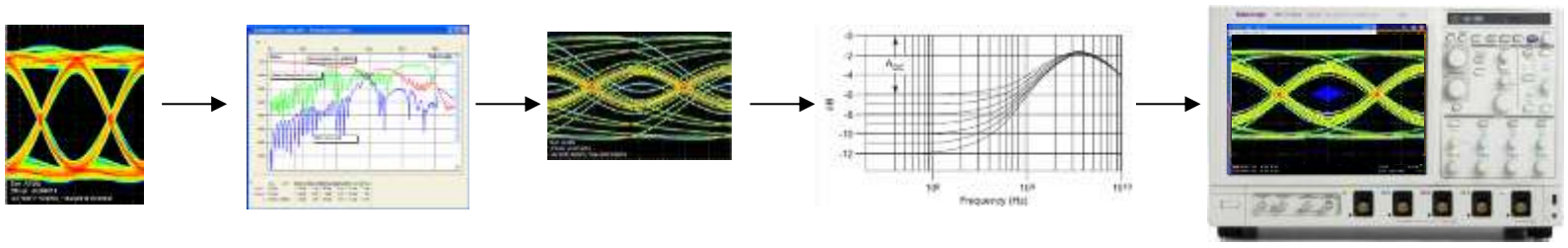


Signal at Tx Pins | Measured Signal at TP1 | De-embed using S-Parameters | Signal with Channel Effects Removed



Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



Signal Acquired from Compliance Board

Embed Compliance Channel and Package

Closed Eye due to the Channel

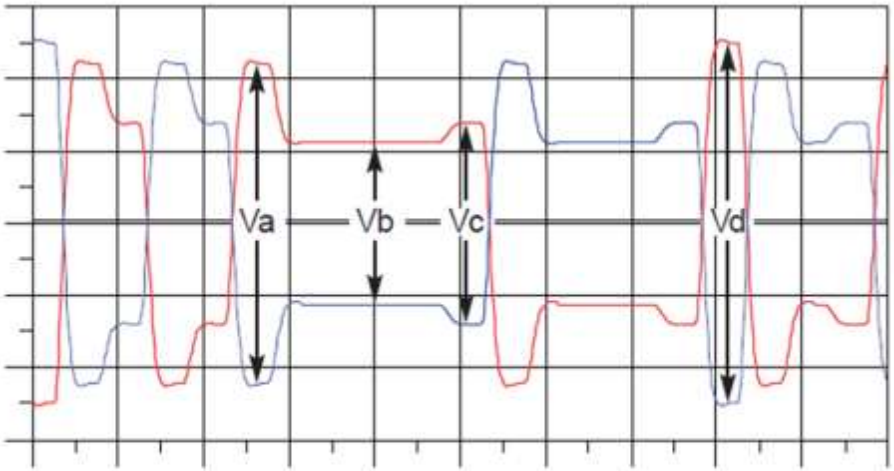
Apply CTLE + DFE

Open Eye for Measurements

Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

Data Rate	Preshoot	De-emphasis
2.5 GT/s,		-3.5 dB
5.0 GT/s,		-3.5 dB
5.0 GT/s,		-6.0 dB
8.0 GT/s,	P0 = 0.0	-6.0±1.5dB
8.0 GT/s,	P1 = 0.0	-3.5±1.5dB
8.0 GT/s,	P2 = 0.0	-4.4±1.5dB
8.0 GT/s,	P3 = 0.0	-2.5±1dB
8.0 GT/s,	P4 = 0.0	0.0dB
8.0 GT/s,	P5 = 1.9±1dB	0.0dB
8.0 GT/s,	P6 = 1.9±1dB	0.0dB
8.0 GT/s,	P7 = 1.9±1dB	-6.0±1.5dB
8.0 GT/s,	P8 = 1.9±1dB	-3.5±1dB
8.0 GT/s,	P9 = 1.9±1dB	0.0dB
8.0 GT/s,	P10 = 1.9±1dB	Test Max Boost Limit



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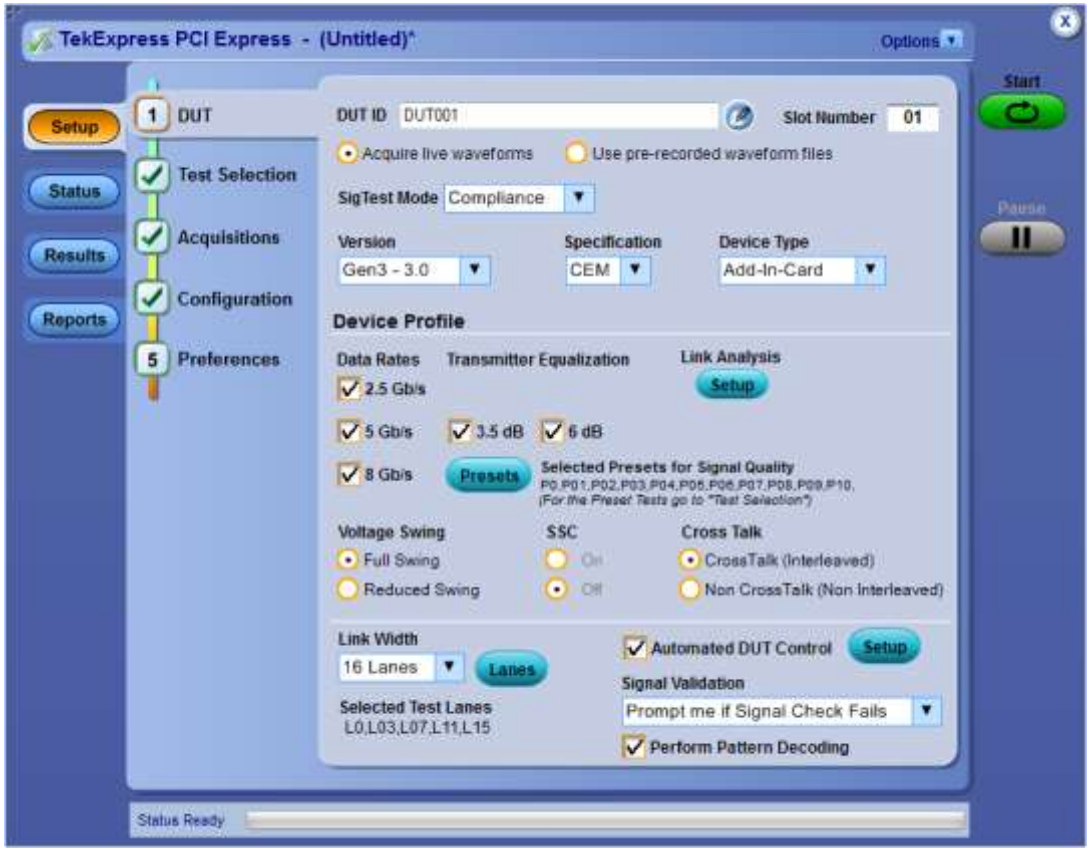
Introducing the NEW Opt PCE3

- TekExpress Automation for Tx Compliance with unique features including:
  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting



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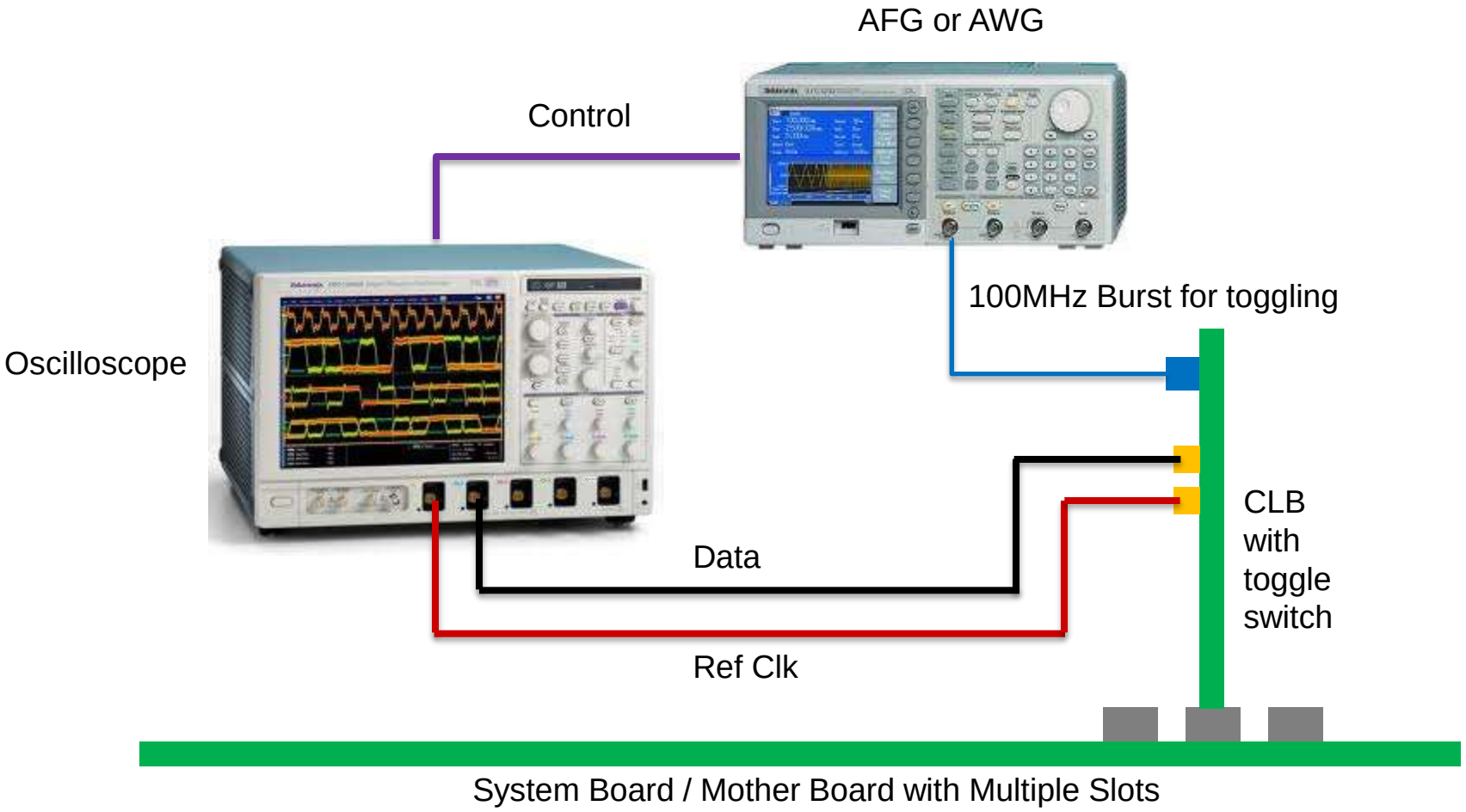
What's New in Option PCE3 Release 2?

- Supports a faster, Python-based sequencer
  - Much faster program launch with the test time reduced by ~50%
  - 64-bit only application (requires 70K C/D oscilloscopes with Win7 64-bit)
    - Will maintain earlier 32-bit release for 70K A/B oscilloscopes with WinXP 32-bit on www.tek.com
  - Smaller installer
- SigTest.exe (Command-Line) integration
  - Supports PCI-SIG recommended SigTest.exe testing
  - User can switch between DLL and Command-Line (.exe) modes
  - All result are populated in Tektronix result/report format in command line mode
- Support multiple versions of SigTest
  - User option to select required version and run
- Broader AWG/AFG support for automatic DUT toggle *(Min 2ch & 100MHz Burst mode)*
  - AFG3252/C
  - AWG5002B/C, AWG5012B/C, AWG5014B/C
  - AWG7082B/C, AWG7122B/C
  - AWG70001A/2A
- Incorporates customer & field feedback
  - Crosstalk option is added
  - Gen2 System-Board limit issue fixed
  - Addresses 6 customer-reported issues & ~30 PCIe Workshop-reported issues

Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

Automated DUT Control



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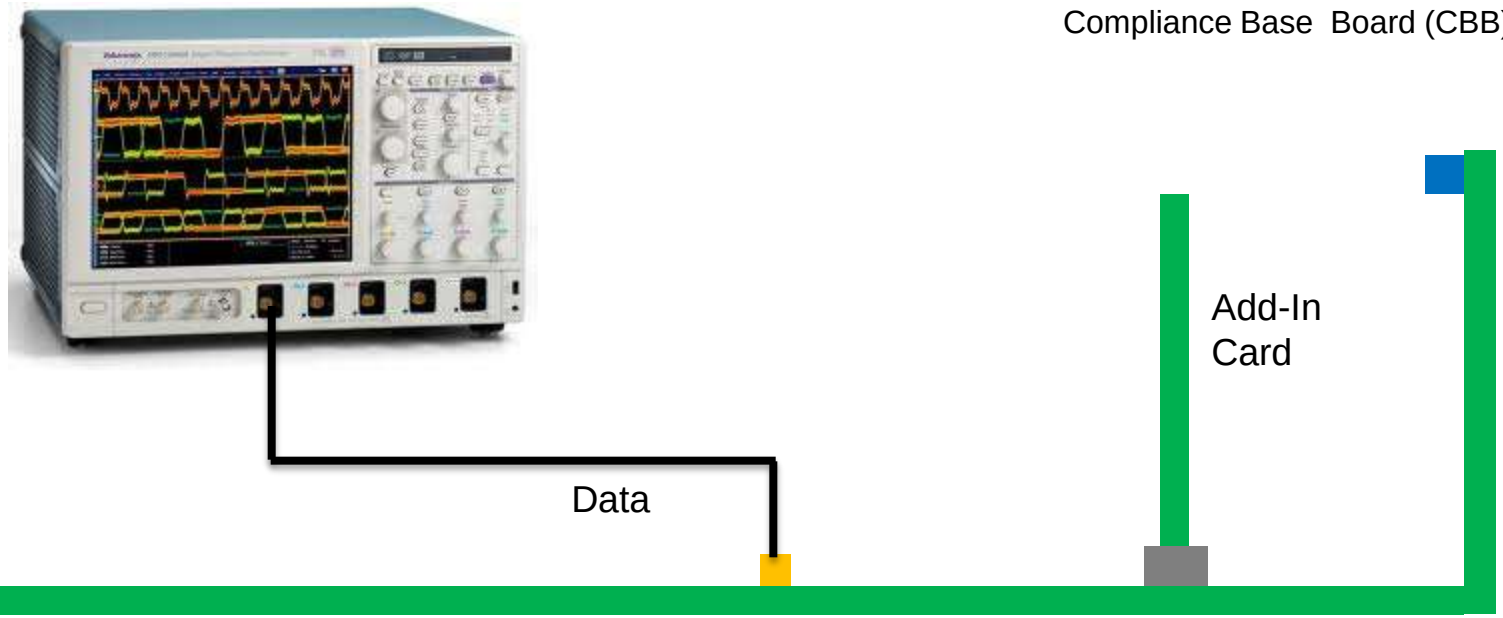
Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Compliance Base Board (CBB)



CBB with Multiple Slots of different widths and toggle switch

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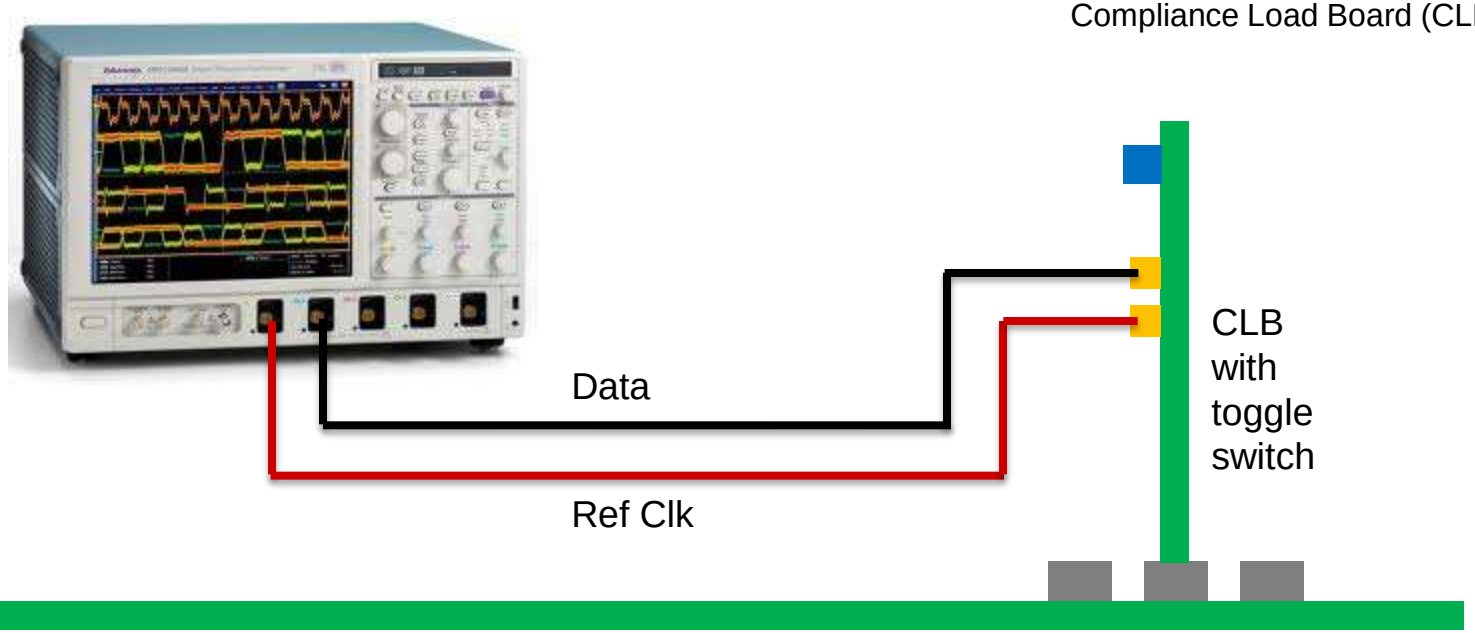
System Test Fixtures

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3

Compliance Load Board (CLB)



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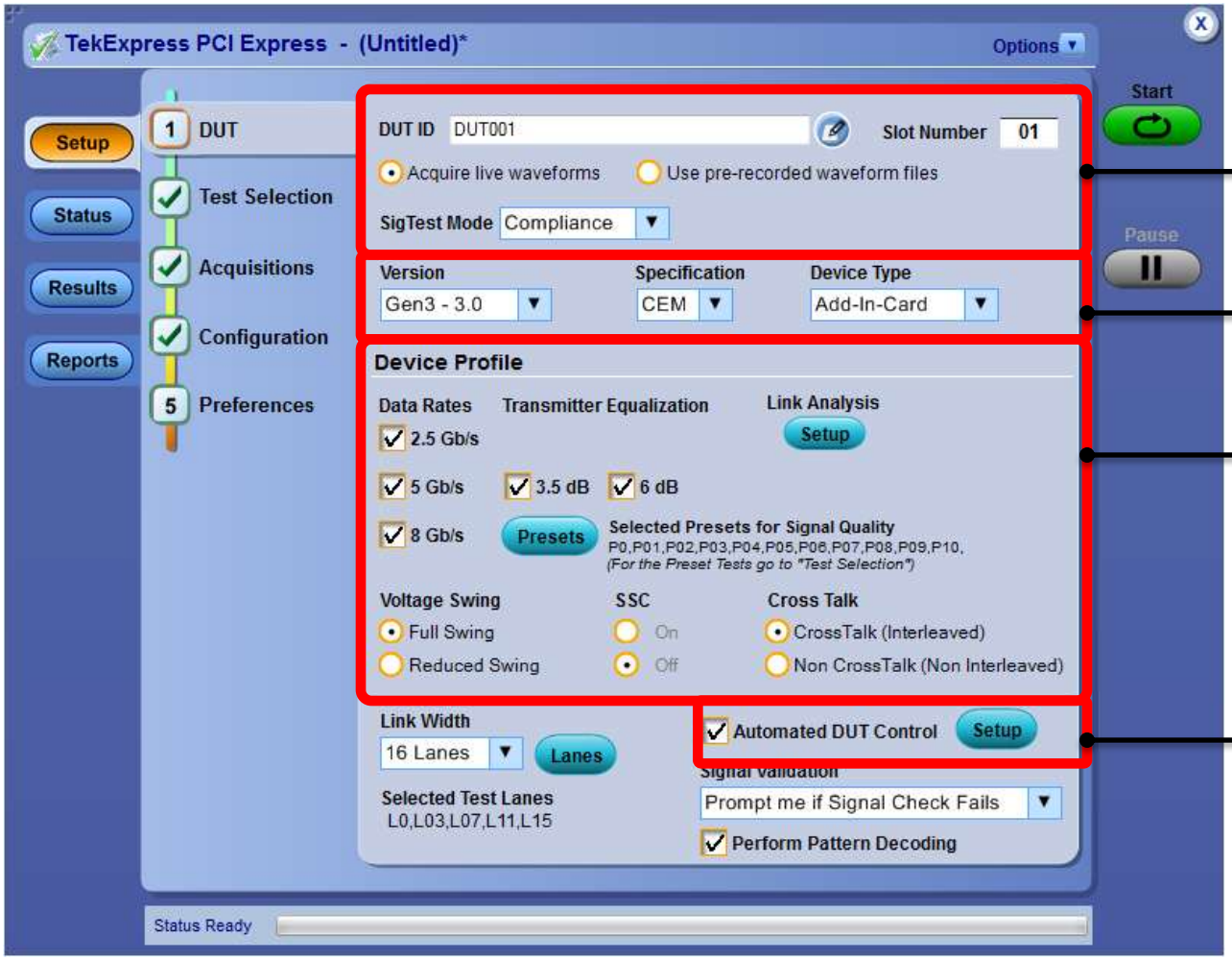
TekExpress Automation for Tx Compliance - Setup



Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

Automate DUT control

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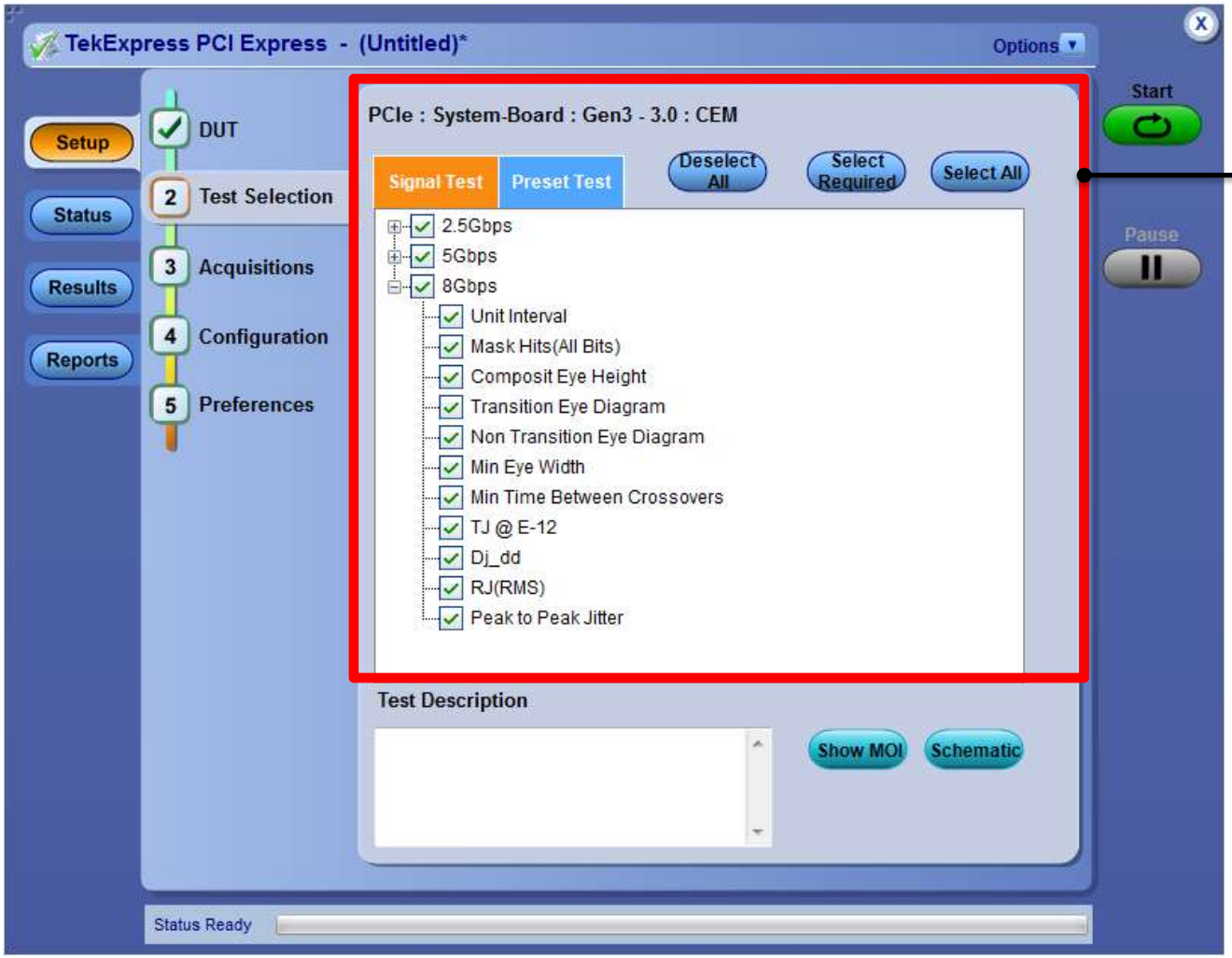
TekExpress Automation for Tx Compliance – Test



Test Selection

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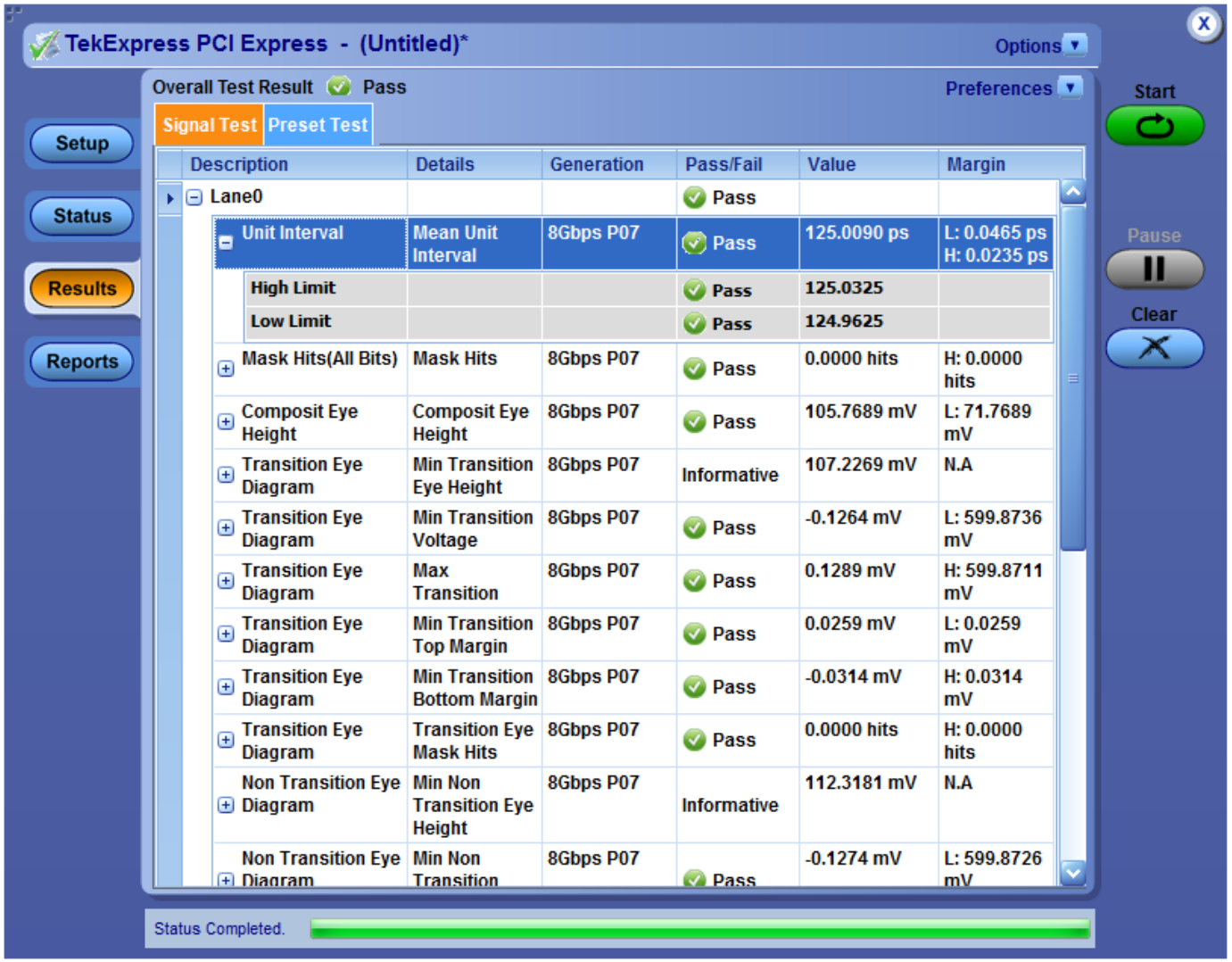
TekExpress Automation for Tx Compliance – Reports



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TekExpress Automation for Tx Compliance – Reports

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TekExpress PCI Express

Add-In-Card Test Report

Setup Information	
	DPOJET Version : 6.0.1 Build 8
	Scope Model : DPO73304D
	Scope Serial Number : B241123
DUT ID : DUT001	SPC, FactoryCalibration : PASS;PASS
Date/Time : 2013-06-10 17:28:45	Scope F/W Version : 6.7.4 Build 3
Device Type : PCIe	Probe1 Model : TCA292D
TekExpress Version : PCI Express:2.0.0.66 (Beta_Build) Framework:3.0.0.16_RevD	Probe1 Serial Number : N/A
Spec Version : Gen3 - 3.0	Probe2 Model : TCA292D
SigTest Version : 3_2_0	Probe2 Serial Number : N/A
Slot Number : 01	Probe3 Model : TCA292D
Overall Execution Time : 0:03:21	Probe3 Serial Number : N/A
Overall Test Result : Pass	Probe4 Model : TCA292D
	Probe4 Serial Number : N/A
	Signal Source Model : AFG3252
	Signal Source Serial Number : C010899
DUT Comment :DUT001	

Test Name:Summary Table	
Unit Interval	Pass
Mask Hits(All Bits)	Pass
Composit Eye Height	Pass
Transition Eye Diagram	Pass
Non Transition Eye Diagram	Pass
Min Eye Width	Informative
Min Time Between Crossovers	Informative
mhtml:file://X:\PCI Express\Reports\DUT081.mht#TJ @ E-12	Pass
Dj_dd	Informative
RJ(RMS)	Pass
Peak to Peak Jitter	Informative

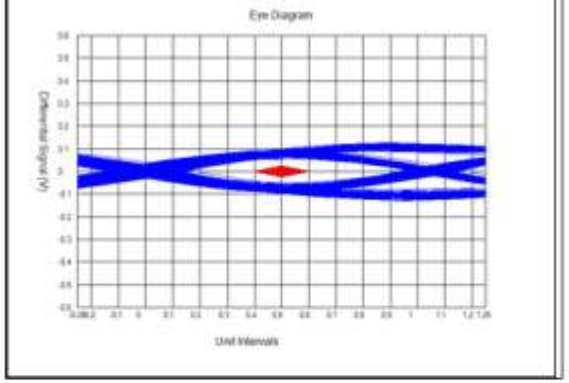
Unit Interval

Measurement Details	Lane Name	DataRate	Equalization	Measured Value	Test Result	Margin	Low Limit	High Limit	Comments
Mean Unit Interval	Lane0	8Gbps	P07	125.0090 ps	Pass	L: 0.0465 ps H: 0.0235 ps	124.9625	125.0325	

Back To Summary Table

Transition Eye Diagram

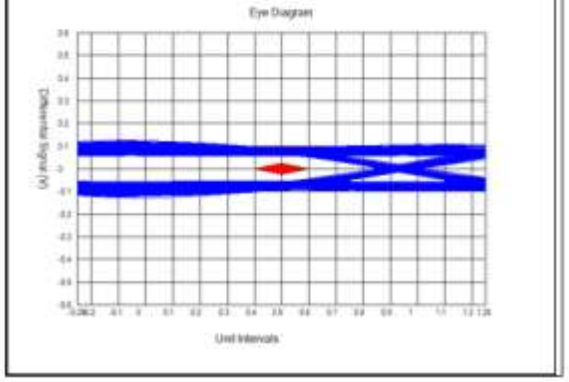
Transition Eye - Lane0 8Gbps P07



Back To Summary Table

Non Transition Eye Diagram

Non Transition Eye - Lane0 8Gbps P07



Back To Summary Table

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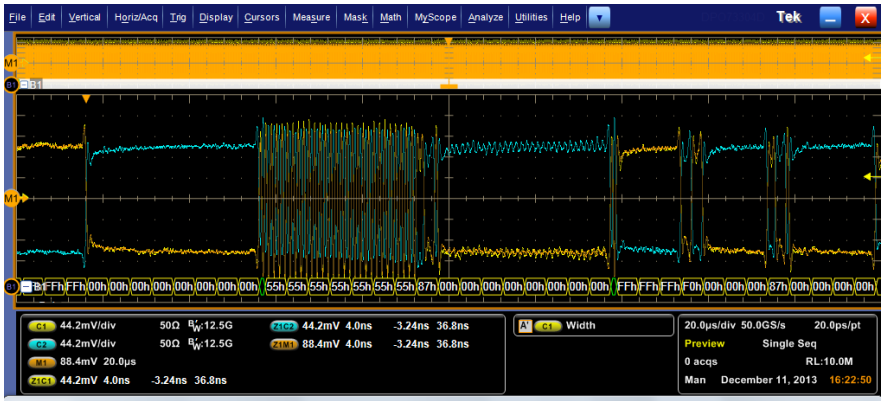
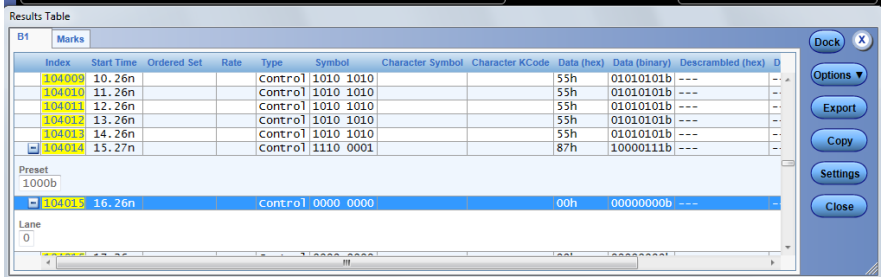
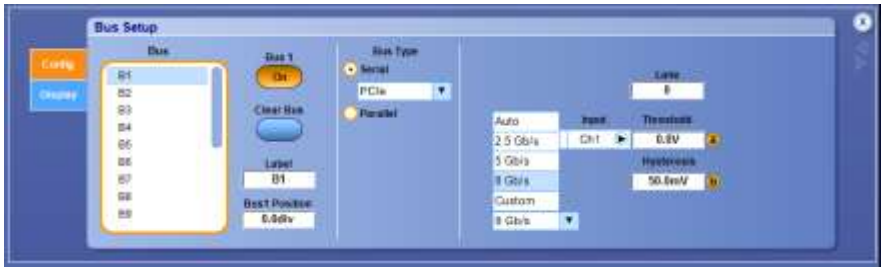
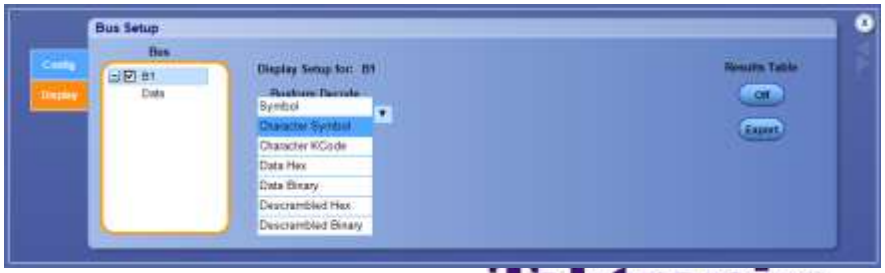
PCIe Decoder (Opt SR-PCIe)

- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- Triggering up to 6.25Gbs (Gen1 & Gen2 only)









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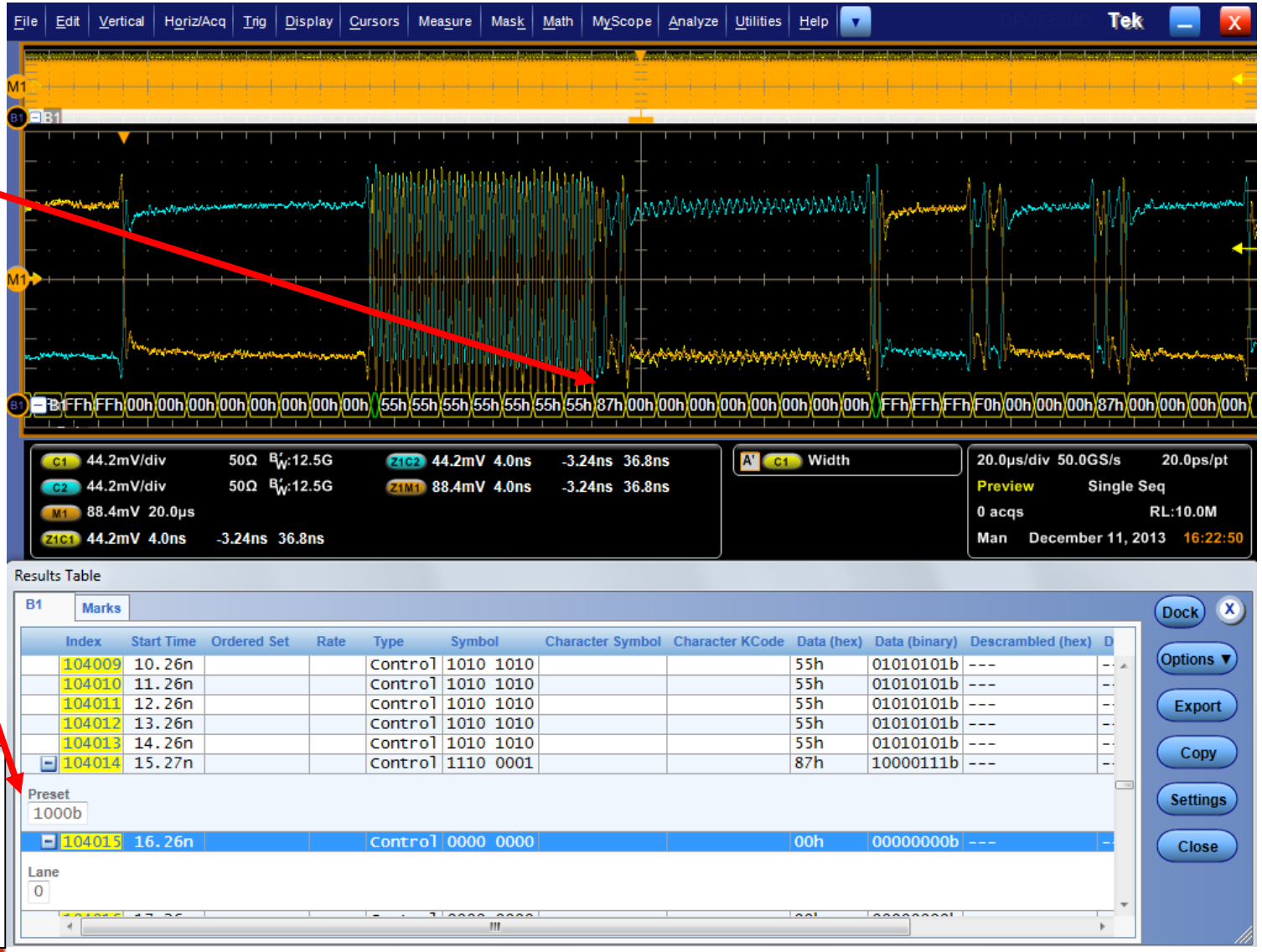
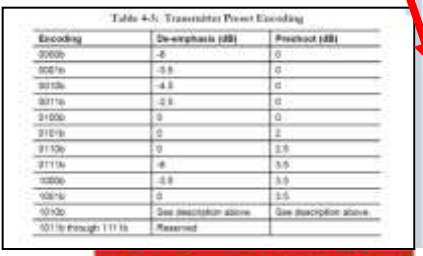
PCIe Decoder (Opt SR-PCIe)

Decoding of PCIe Gen3 compliance pattern Tx preset encoding

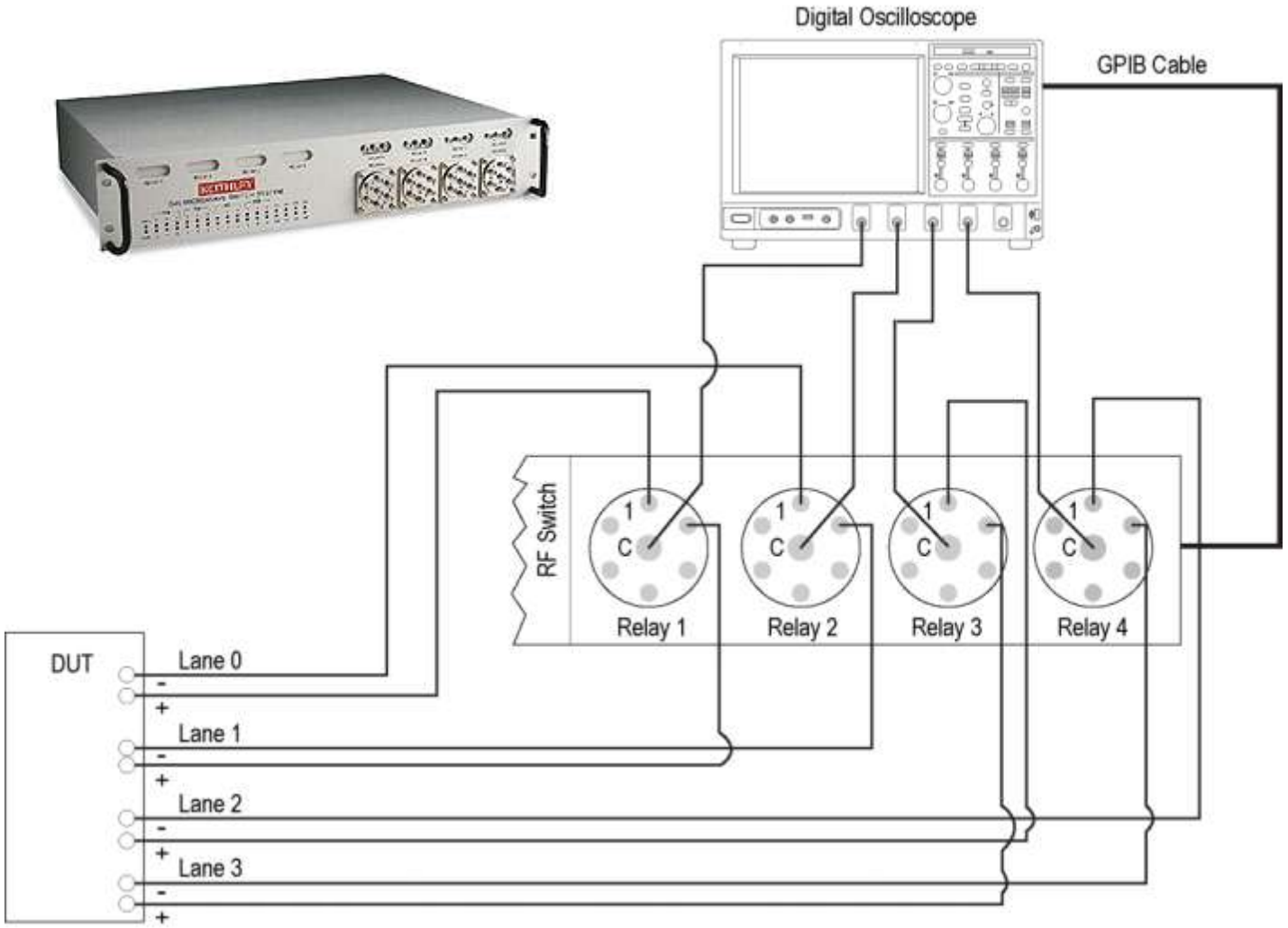
Decode results show correct value of “87h” or “1000b” (as shown in Results Table) for Transmitter Preset **P8** (-3.5dB de-emphasis with +3.5dB preshoot) on Lane 0





Reference: PCI Express Base Spec, Rev 3.0 (10-NOV-2010), Section 4.2.3.2 Encoding of Presets, p.225.

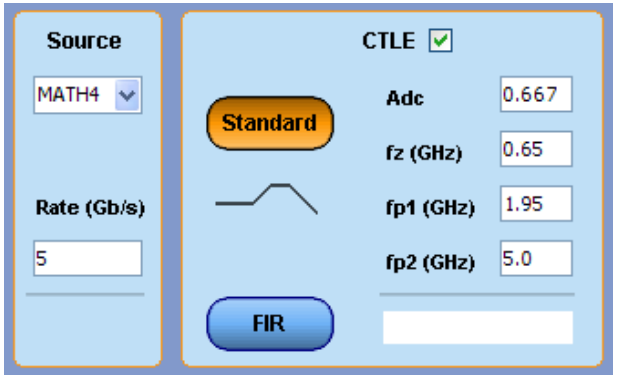
PCI Express Tx Test with RF Switch

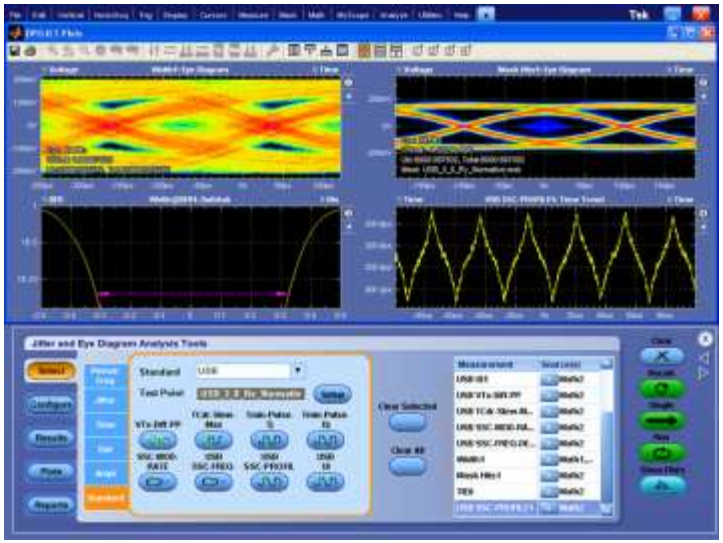


Cable and RF Switch De-embed

Testing Beyond Compliance

- What happens if a measurement fails Compliance ?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized RX setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance





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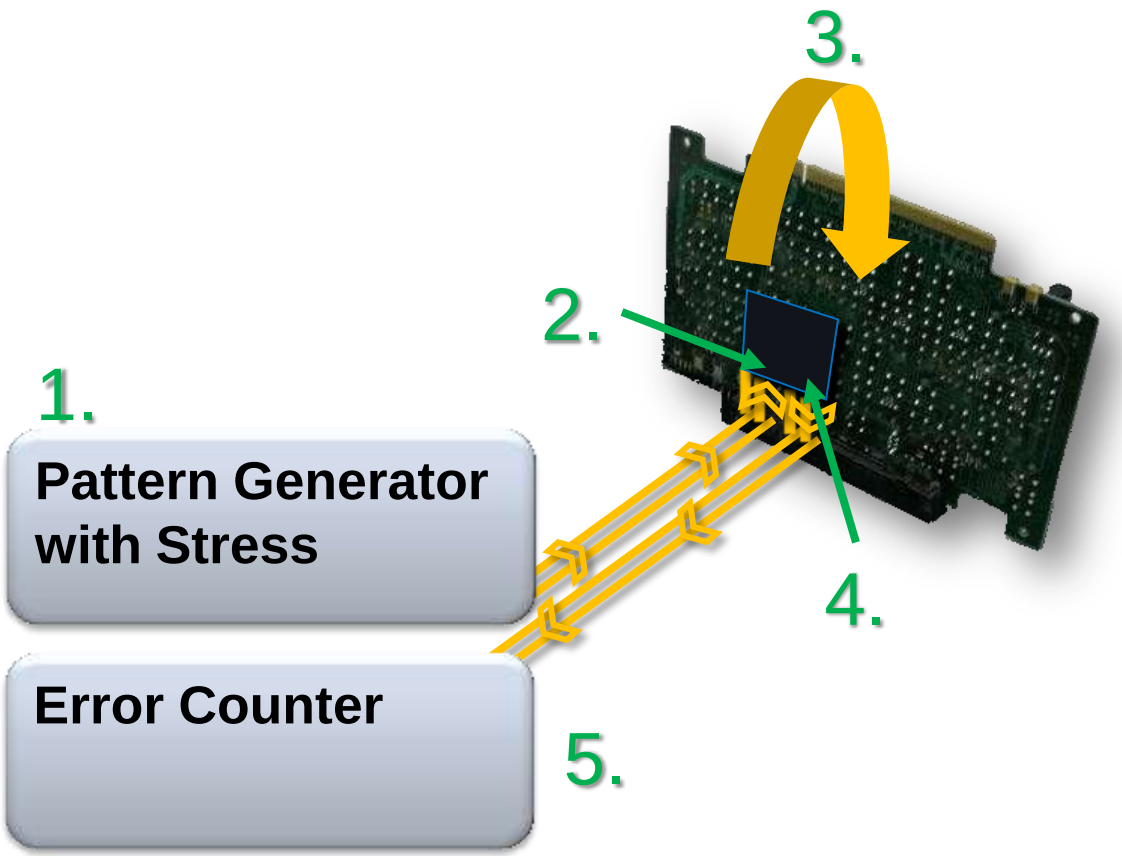
Essentials of Rx Testing

- PCIe 3.0 introduced formal Rx testing
- Based on stress testing of the DUT in loopback
  - Looped back data must be the same as stressed data
- DUT must support loopback initialization and **training**
- Impairments in stress must be **controlled** and **repeatable**
- DUT must receive stressed signals without errors (errors below specified ratio 10^{-12})

Testing Challenges in Rx

- Rx: Support of loopback
  - √ Loopback initialization
  - √ Proper training conditions
  - √ Correct stress and signal impairment levels
- How to achieve required confidence level and beyond?
  - √ Length of test (Rx)

Basic Receiver Testing



At the simplest level, receiver testing is composed of:

1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)

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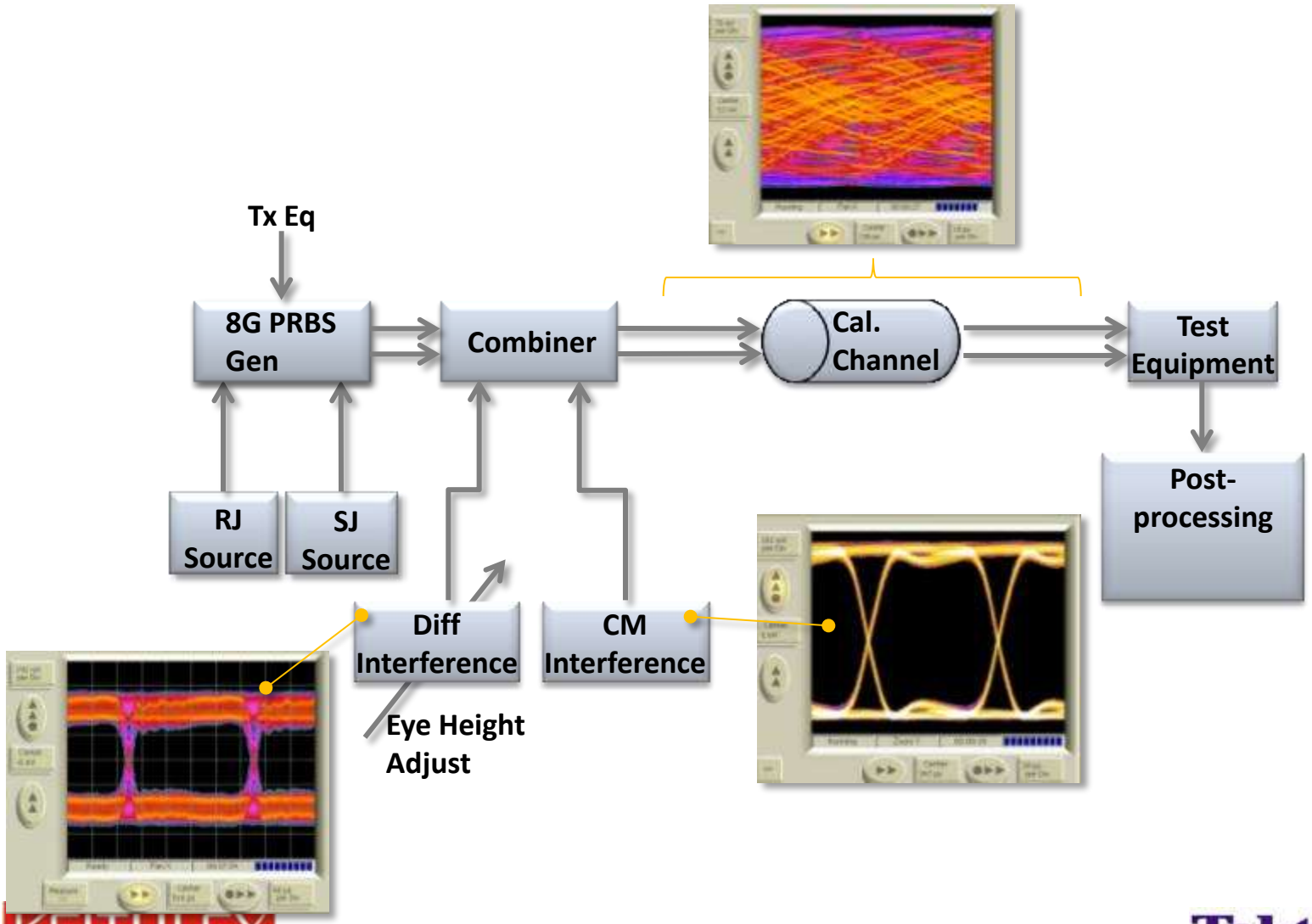
Stress Composition



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Components of a PCIe3 Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- New! DPP125C Option ECM
  - Eye opener, Clock doubler/Multiplier
- New! BSAITS125
  - CM/DM interference
  - ISI for Gen2 & Gen3
  - Option EXP for variable ISI
- New! CR125A Opt PCIE8G
  - PLL analysis for Gen1/2/3
- New! BSAPCI3 SW
  - Auto calibration, Link training, and test
- Cables, adapters, compliance boards
- DSA/DPO/MSO70K Series Oscilloscope
  - Stressed Eye Calibration

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DPP125C with Option ECM

- Integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz.
- Integrated eye opener functionality for testing DUTs with long channels.
- New microcontroller to provide more processing power.
- RS-232 interface enhancement to speed-up PCIe receiver equalization link training.
- SW to accommodate channel de-embedding and ISI fine adjustments.

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BSAITS125 Interference Test Set

- Programmable, variable ISI for automated testing and precision setting
- Built-in compliant PCIe2 and PCIe3 Medium and Long ISI channels
- Integrated PCIe3 CM and DM interference combiner
- Integrated PCIe3 Base Spec CM interference calibration
- Continuously Variable, Expanded ISI for automated testing of multiple standards with Option EXP

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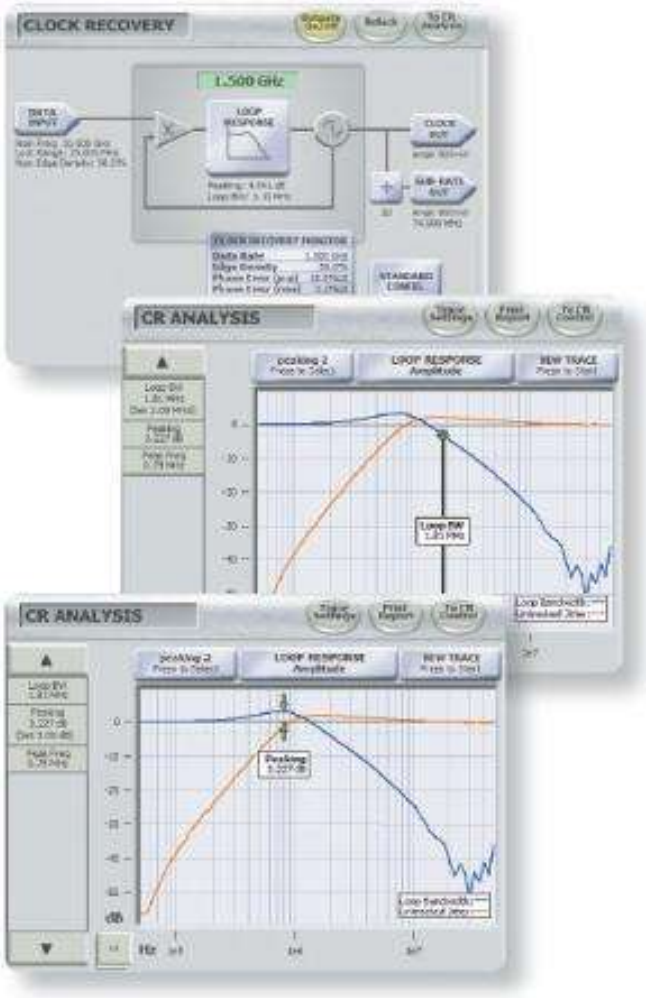
CR125A Opt PCIE8G



- PLL Loop BW Analysis for Gen1/2/3
- Uses CR125A and Test SW
  - Similar to Gen1/2 PLL Loop BW solution

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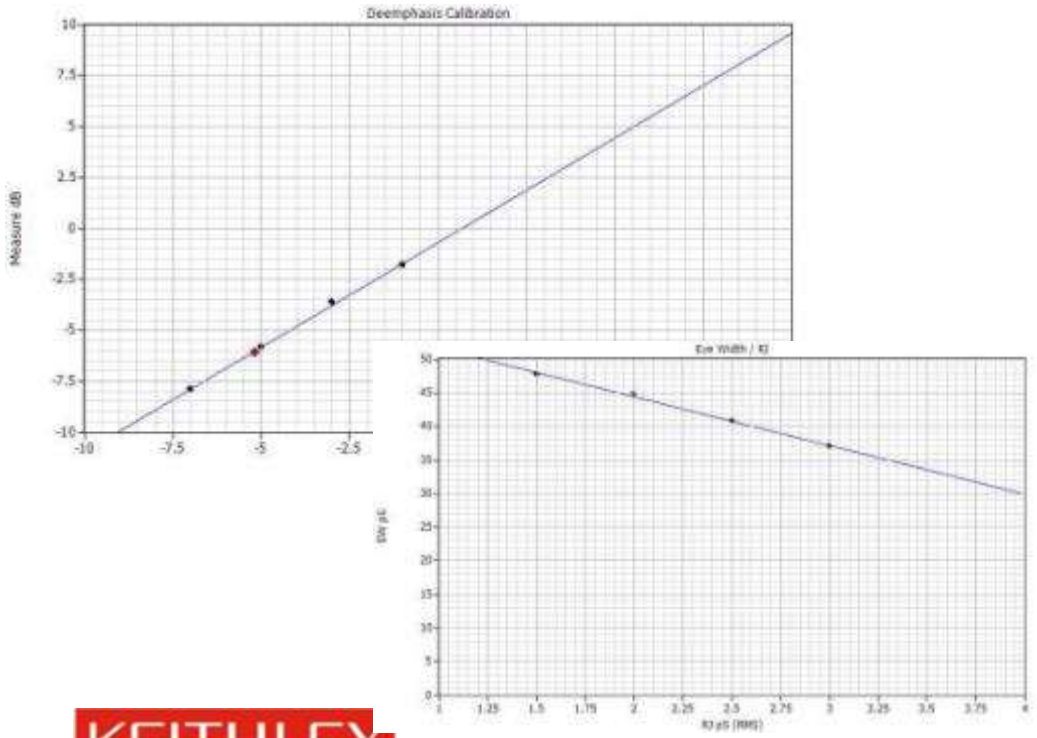
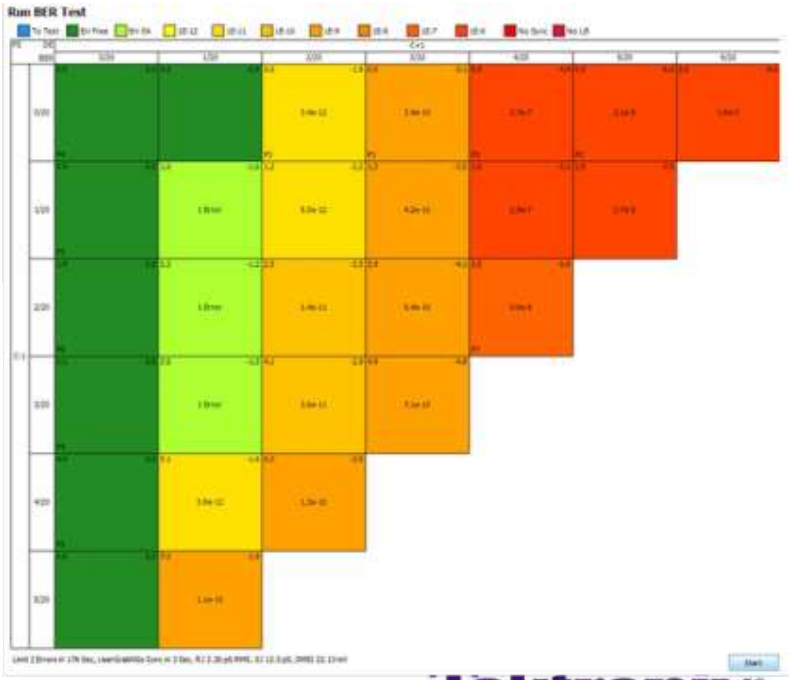
BSAPCI3 PCIe 3.0 Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.





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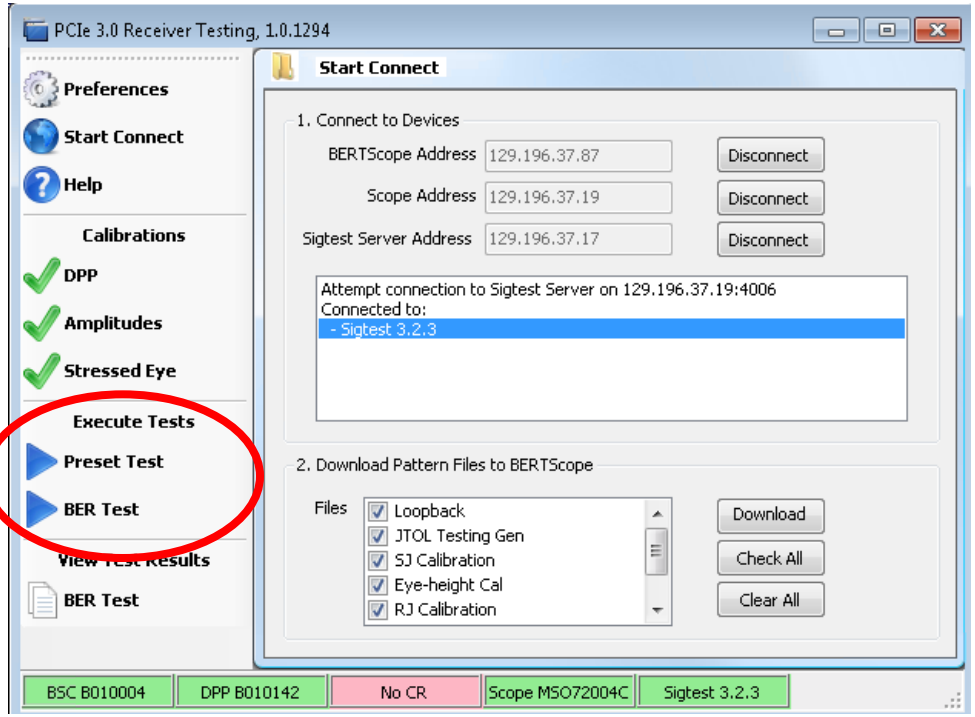
Automation test options

- Automation software provides two options for testing:
  1. “Preset test” uses either negotiated link equalization or user selected preset for test
  2. “BER test” provides the option to test a matrix of preshoot and de-emphasis settings



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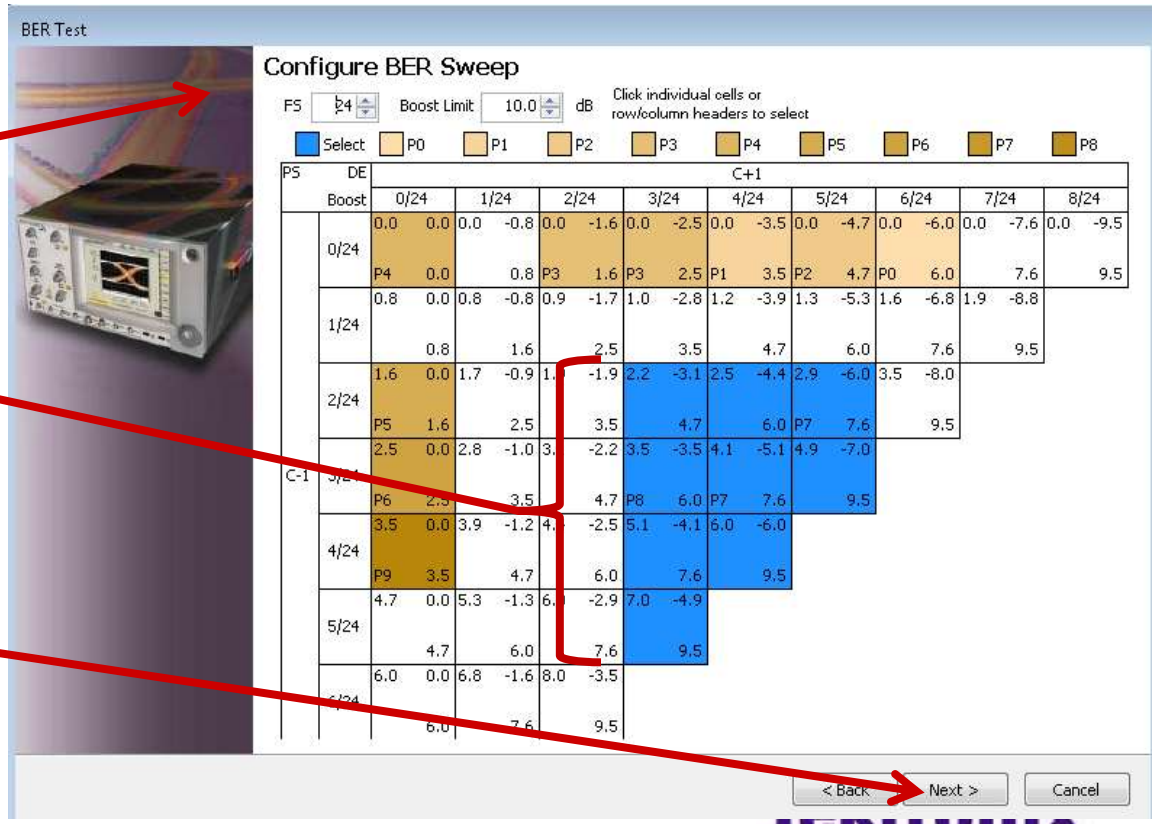
Automated Tx equalization matrix testing

- Automation software “BER test” provides the option to sweep a matrix of pre-shoot and de-emphasis settings
  - Quickly find the range of values that work well with the DUT
  - Ideal for debugging purposes

- Select test matrix resolution
- Click on equalization combinations desired for test
- Initiate test



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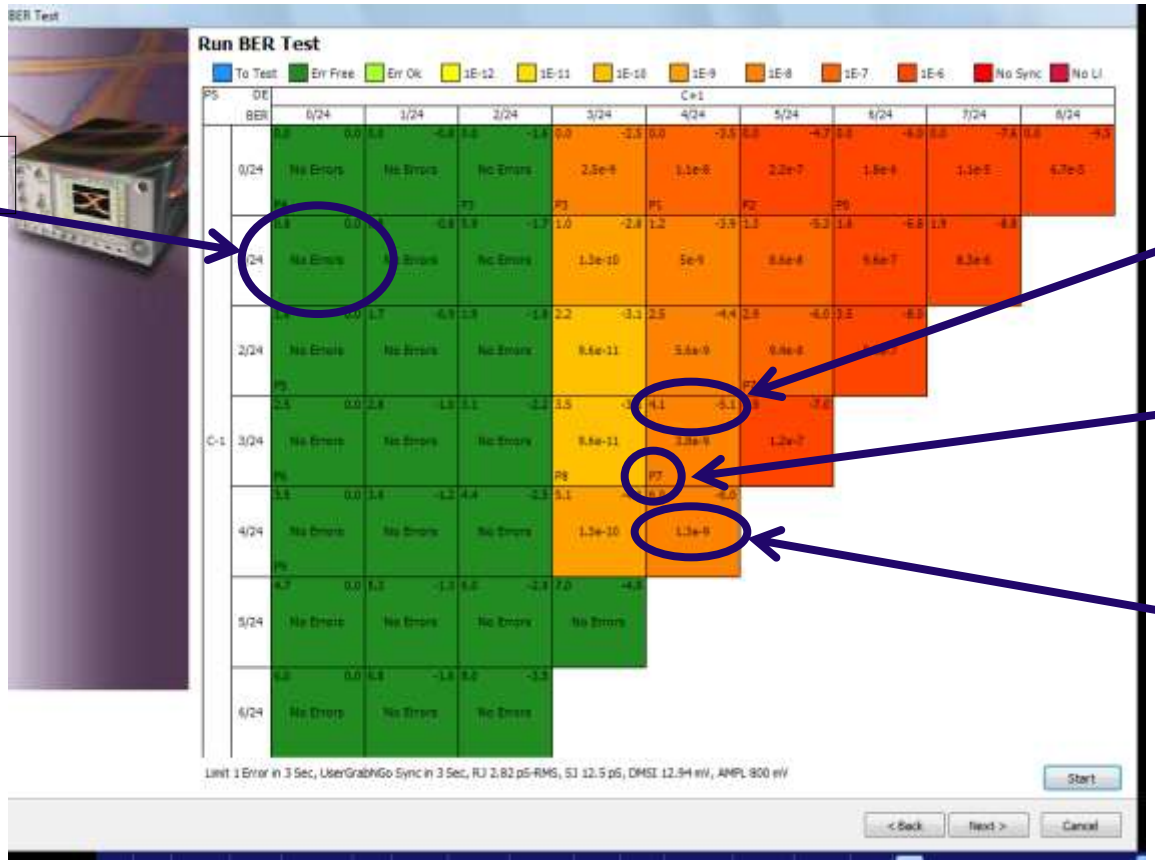
Automated Equalization Sweep testing

- BER results matrix for preshoot and de-emphasis settings provides an in-depth view of Rx sensitivity to Tx equalization



Green = pass

Preshoot and de-emphasis setting

Equivalent preset number

BER result for each combination of preshoot and de-emphasis

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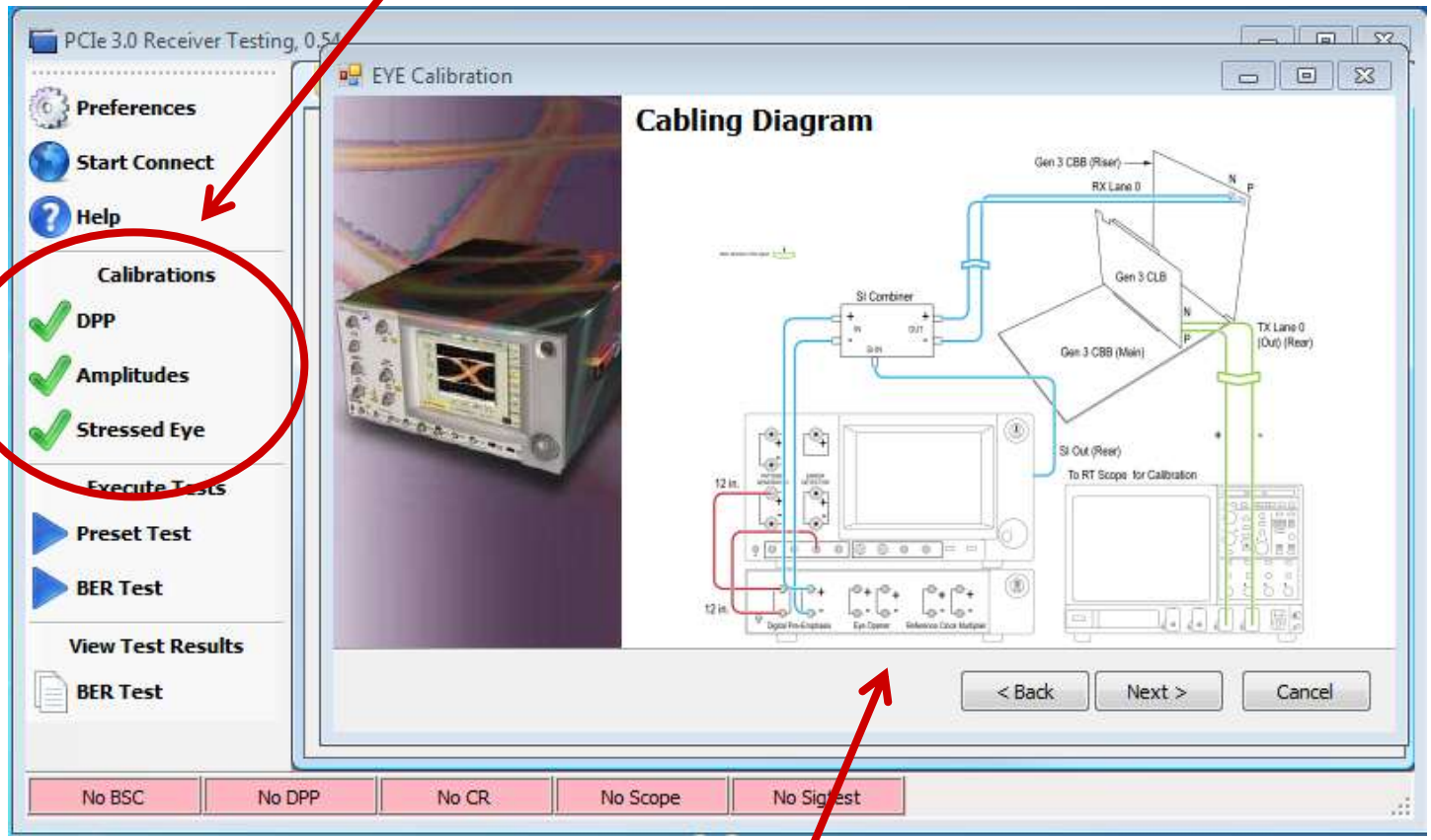
Automatic Calibration

- Due to complex test setup and variations in DUTs and test equipment just dialing up the settings on the signal source is not sufficient
- Stress must be measured and adjusted
- Automatic calibration is used to achieve the right amount of stress
- Margin testing complements the compliance testing
  - Help understand your device's margins.
  - How much additional stress does it tolerate?

Stressed Eye Calibration Setup

- Three required calibrations are fully automated



- Detailed cabling diagrams are provided for each calibration step

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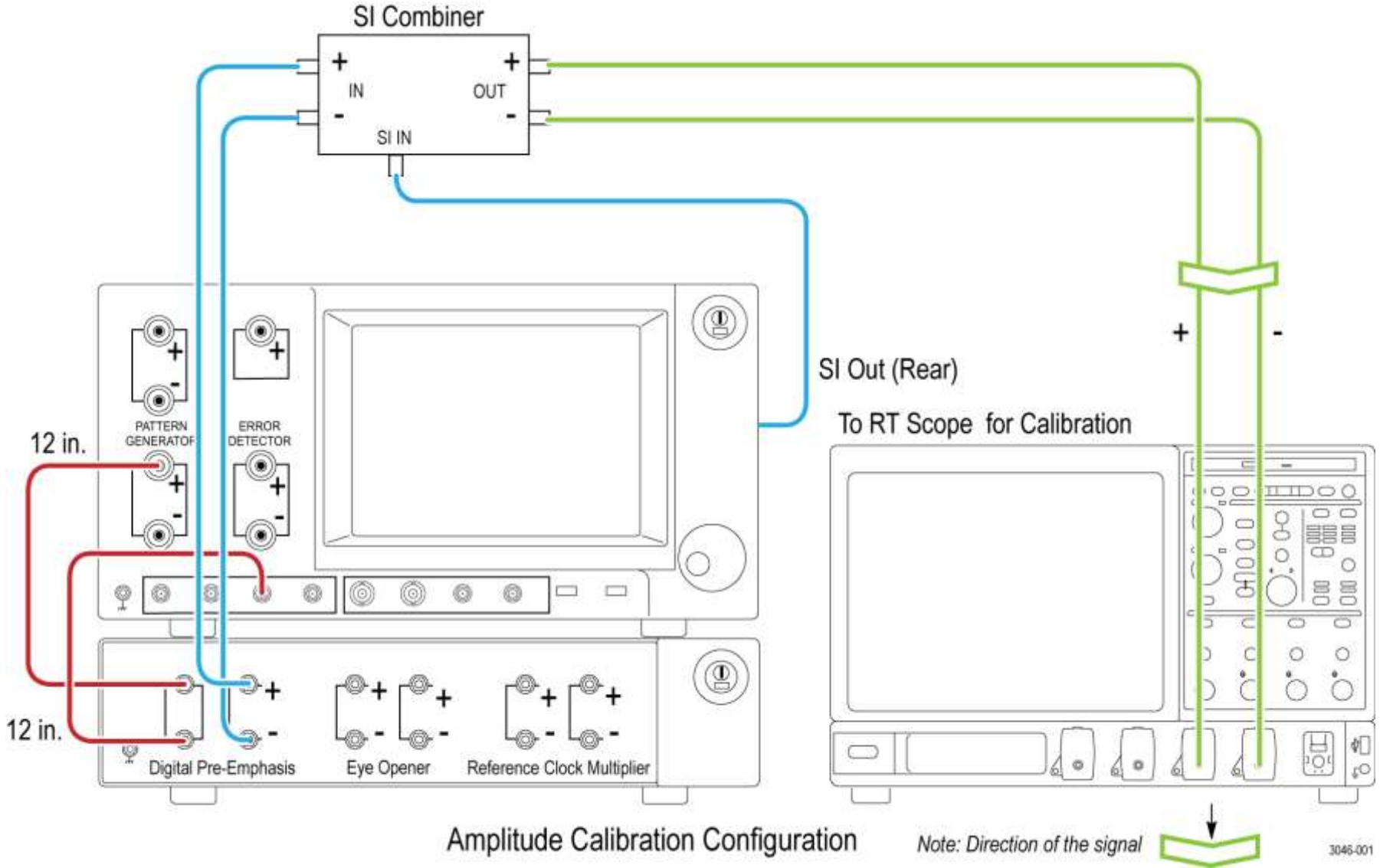
Amplitude Calibration Configuration



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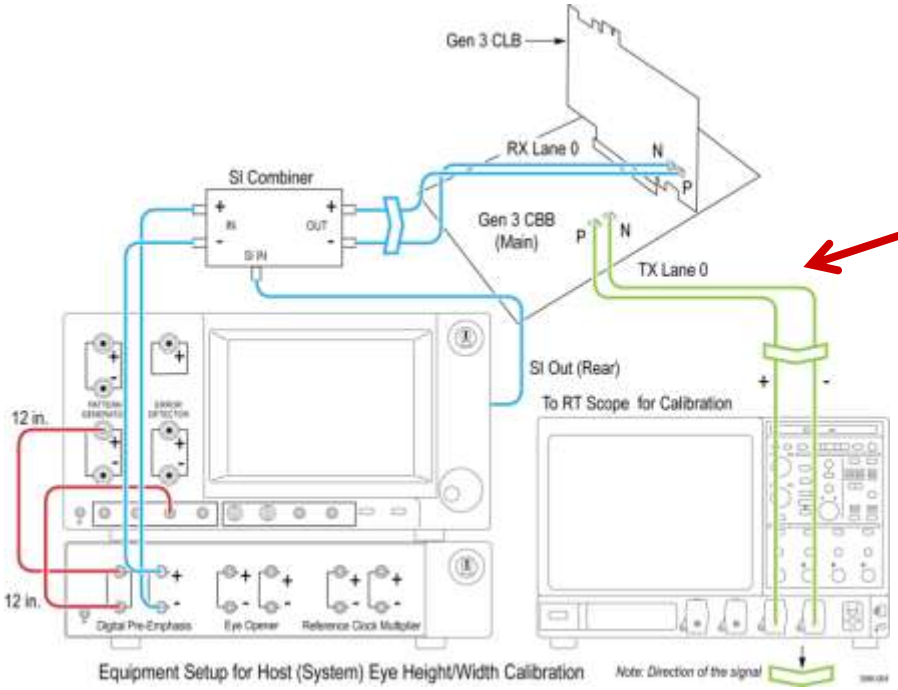
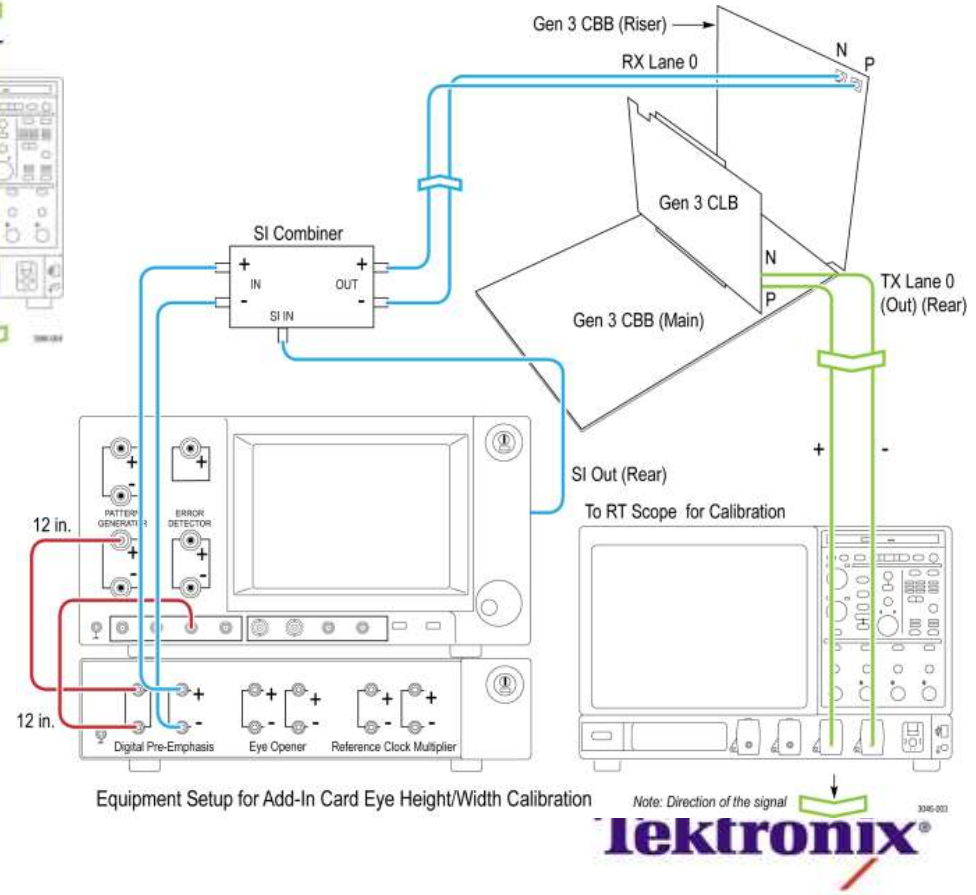
Eye Height/Width Calibration Connections

Host (System)

Add-In Card





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HDMI – Introducing new HDMI 2.0

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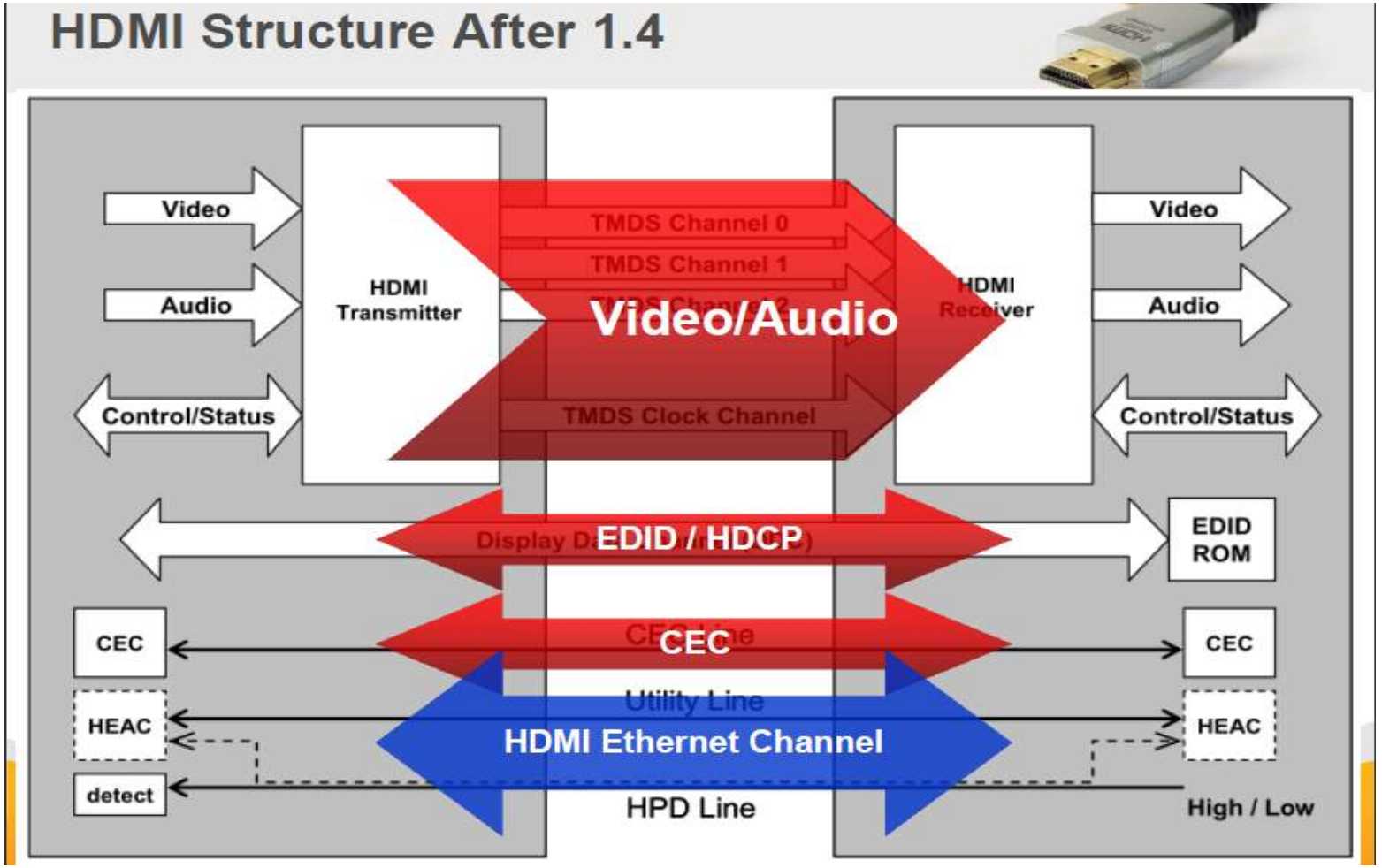
Overview of HDMI

- From 2003 till date and looking ahead…
  - Tek only solution provide for HDMI from 2003 to 2007
  - Contributor of SoftCRU method to the Specification
  - Innovative Sink solution leveraging Direct Synthesis method of AWG
- Hdmi 1.0 ---- 1.65GBps
- Hdmi 1.4—3.4GBps
- Hdmi 2.0….. 6GBps

HDMI™
HIGH-DEFINITION MULTIMEDIA INTERFACE

HDMI Basics

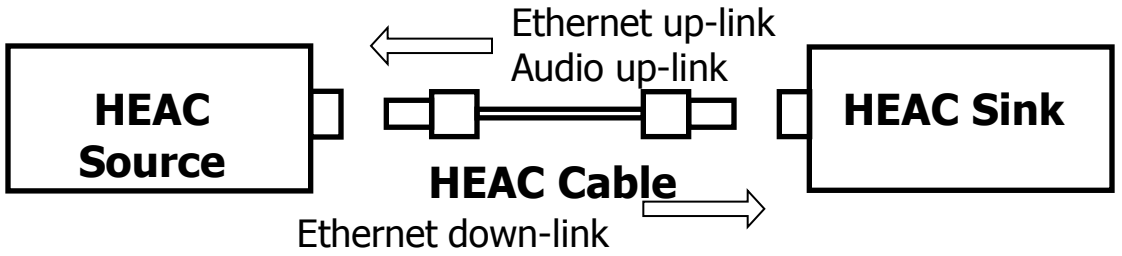

HDMI Structure After 1.4
Video
Audio
Control/Status
HDMI Transmitter
TMDS Channel 0
TMDS Channel 1
Video/Audio
TMDS Clock Channel
HDMI Receiver
Video
Audio
Control/Status
EDID / HDCP
EDID ROM
CEC
CEC
CEC
Utility Line
HEAC
HDMI Ethernet Channel
HEAC
detect
HPD Line
High / Low

HDMI Technology and solution status

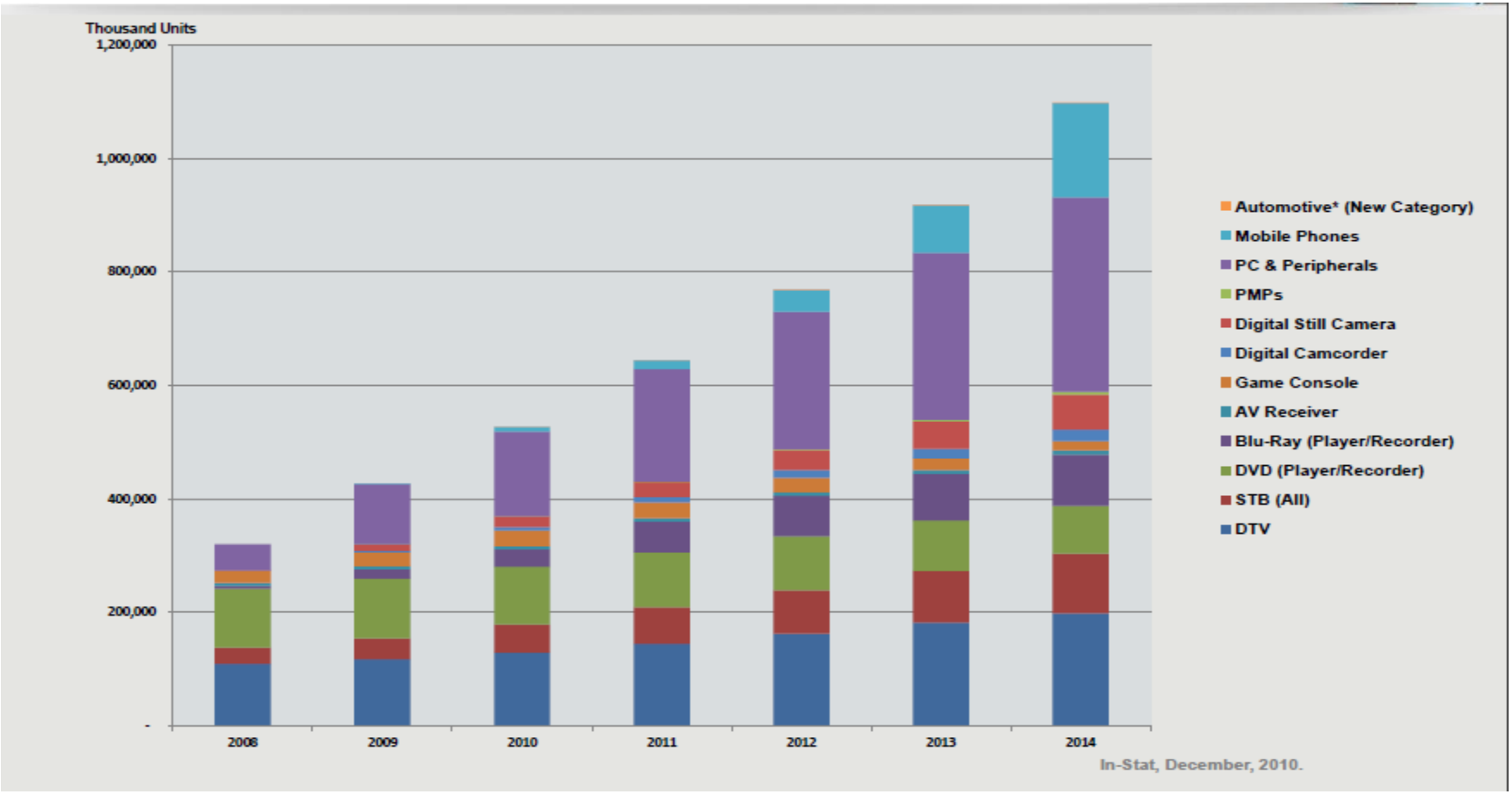
Source: HDMI LLC

- Over 1000+ adopters till date
- HDMI Expands Footprint
  - HDMI has made inroads into PC industry
    - New computer platforms have HDMI interfaces
  - Hand held devices with miniature HDMI devices
    - New connectors Type C and Type D introduced
  - HDMI Forays into Automotive – Type E
  - Year 2011 – 3D Year
  - Still camera
  - Advertising billboards

- HDMI NOW Truly Single Digital Interconnect for uncompressed Audio/Video
  - HEAC (A R C)



HDMI Market overview



Source: HDMI Forum

Tektronix HDMI 1.4b solution- Approved in CTS 1.4b

DPO/DSA/MSO
Real Time Oscilloscopes

AWG5K/B or AWG7K/B
Arbitrary Waveform Generators

DSA8200 Sampling Scope
with i-connect software

Common Set of test equipment for HDMI and HEAC

HDMI Fixtures:

1. Type A(TF-HDMI-TPA-S/-STX)
2. Type C(TF-HDMIC-TPA-S/-STX)
3. Type D(TF-HDMID-TPA-P/-R)
4. Type E(TF-HDMIE-TPA-KIT)
5. HEAC Fixtures(TF-HEAC-TPA-KIT)

Probes and accessories

HDMI Probes
HEAC Probes
HDMI Accessory Kit

GAME Changer - HDMI Protocol Analyser

Tektronix and HDMI Forum

- 89 companies in the HDMI forum as of date. source HDMI Forum

- Tektronix is member of this HDMI Forum. Actively participating in weekly/monthly calls and face-face meetings

- **Tektronix's U.N.Vasudev is co-chair for HDMI forum test sub-group**

- HDMI Forum released HDMI 2.0 specifications on Sept 4th 2013

  - Target

    - CTS 2013 Q4
    - MOI Q4 2013

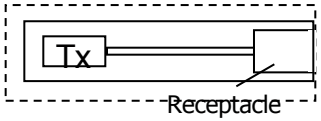
HDMI 2.0 features

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60 Hz – 594Mcsc**(Mega Characters per second per channel)**
- Support 4K 2K 4:2:0 – 297Mcsc
- 3D, 21:9 ; Audio
- Low level Bit error rate testing
- Scrambling is MUST for rates >340Mcsc.
- Direct Attach Device support
- HDMI 2.0 products must pass HDMI 1.4 CTS testing

Ecosystem update

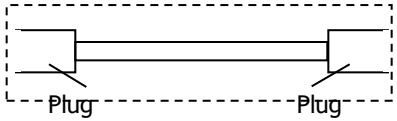
- Same HDMI customers for Source Devices, Sink Devices, Cable ,Repeater

Source Devices



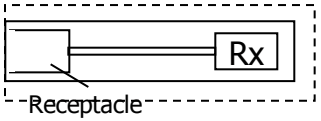
- Set-top Boxes, DVDs, Repeaters, Gaming devices

Cable Assemblies



- Cables

Sink Devices



- TVs, Monitors, Repeaters, etc.

- Direct Attach Devices – New category devices
  - Roku
  - Apple TV

HDMI 2.0 Solutions Portfolio (Source setup, Sink Setup, Protocol Decode, Probes)

Rise time Needs

Table 4-24 Source AC Characteristics at TP1

Item	Value
Rise time / fall time (20%-80%)	if attached Sink supports < 340MHz 75psec ≤ Rise time / fall time if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz 42.5psec ≤ Data Rise time / Data fall time 75psec ≤ Clock Rise time / Clock fall time

Table 4-30 TPT Direct Attach AC Characteristics at 6Gbps

Item	Value
Rise time / fall time (20%-80%)	if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz 42.5psec ≤ Data Rise time / Data fall time 75psec ≤ Clock Rise time / Clock fall time

- HDMI 1.4b, should be capable of measuring 75 psec, but no word about the System Rise time.
- **HDMI 2.0 should be capable of measuring 42.5 psec, but no word about System Rise time**.

- The Error contribution of RT measurement due to System and DUT generally not accounted when we refer to specification

What is the system bandwidth needed to measure 42.5 (20-80%)psec or less DUT Rise time

- System bandwidth should be around (42.5/1.5) 28psec
- Scope bandwidth of 16 Ghz and 16 Ghz DSP enhanced probe has System Rise time of about 23 psec. It can measure the DUT Rise time of 42.5 psec with error of 1%. And can measure DUT Rise time of 37 psec with error of 7%.
- We can indicate Pass or fail confidently only when the System band. width is close to 16 Ghz scope .
- Is it fact for all scope vender ??
  - Spec says it should not be less than 42.5psec.
  - Max Rise time is limited by Eye diagram slope.
  - Both scope and Probe rise time cannot be less or equal to the DUT rise time because it can measure the signal rise time accurately only if DUT RT is slower than system rise time by 1.5 X times.
- How it is handled in HDMI 1.4b today???
  - We recommend 8Ghz scope and 13 Ghz probe, then system rise time is 38 psec which is close 2X faster than 75 psec

Conclusion

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.

- HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps

Note: We also support 12.5GHz BW scope for HDMI 2.0 but will have a 10% error in RT/FT measurements

Source Testing 1.4b Vs 2.0

Eye Diagram and Clock Jitter test is now performed at TP2

Rest of the tests is same as HDMI 1.4b

1.4b CTS test is a pre-requsite for HDMI 2.0

Min 8GHz scope to 16GHz scope

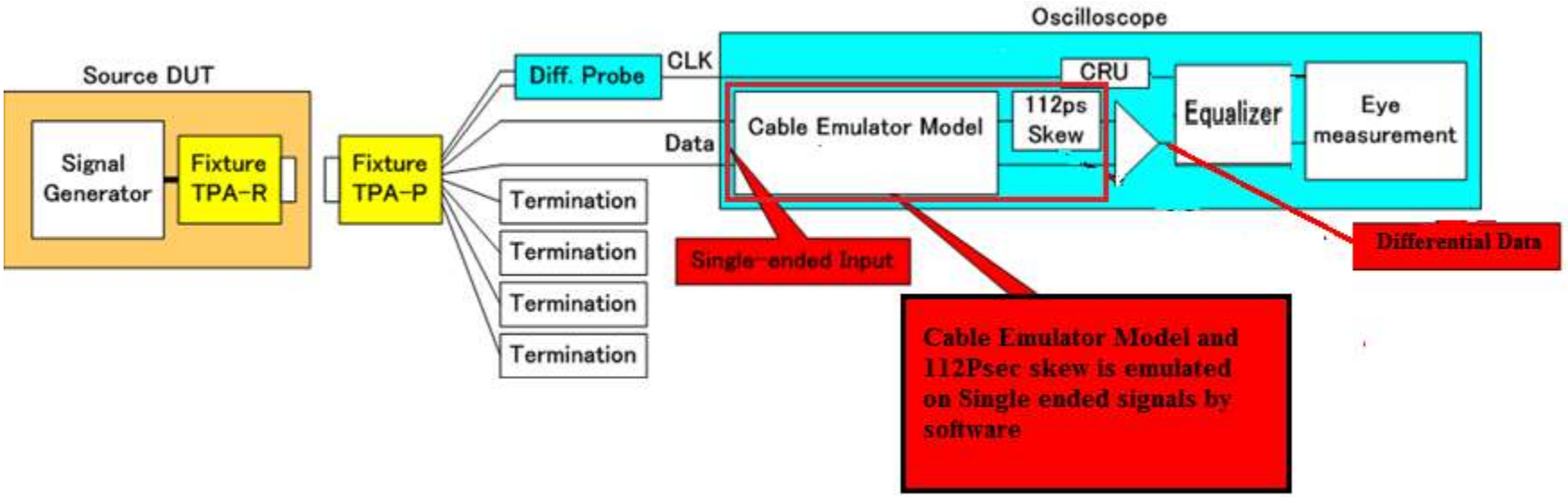
New Fixtures

Same Probes

HDM and HDM-DS Software

Source Testing

- Source Eye Diagram test is measured at TP2_EQ.
- TP2 is the signal after passing along a worst cable.
  - Worst cable has worst attenuation and skew of 112ps.



Source Electrical tests

Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – V_L

Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – T_{RISE}, T_{FALL}

Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew

Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage

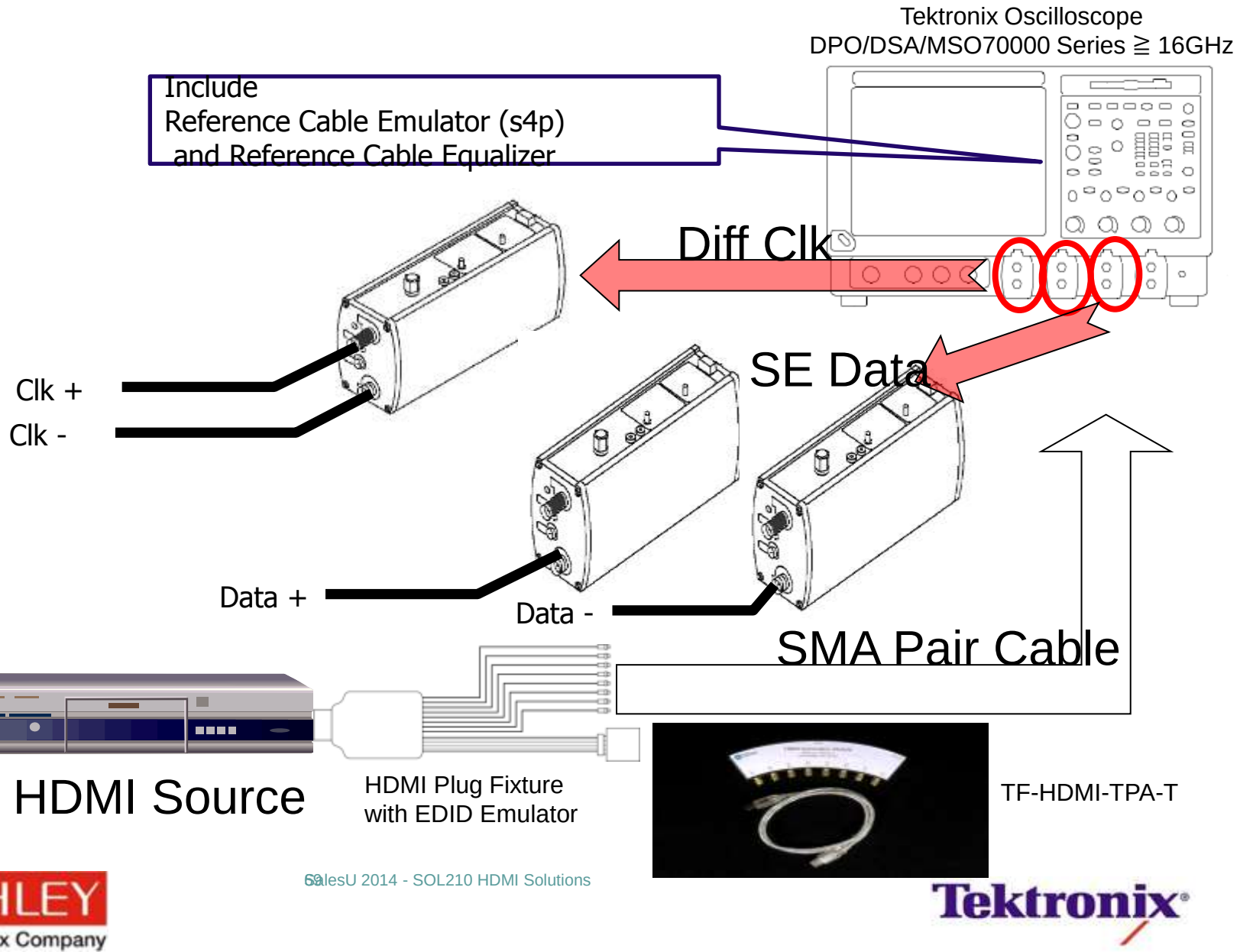
Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle

Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter

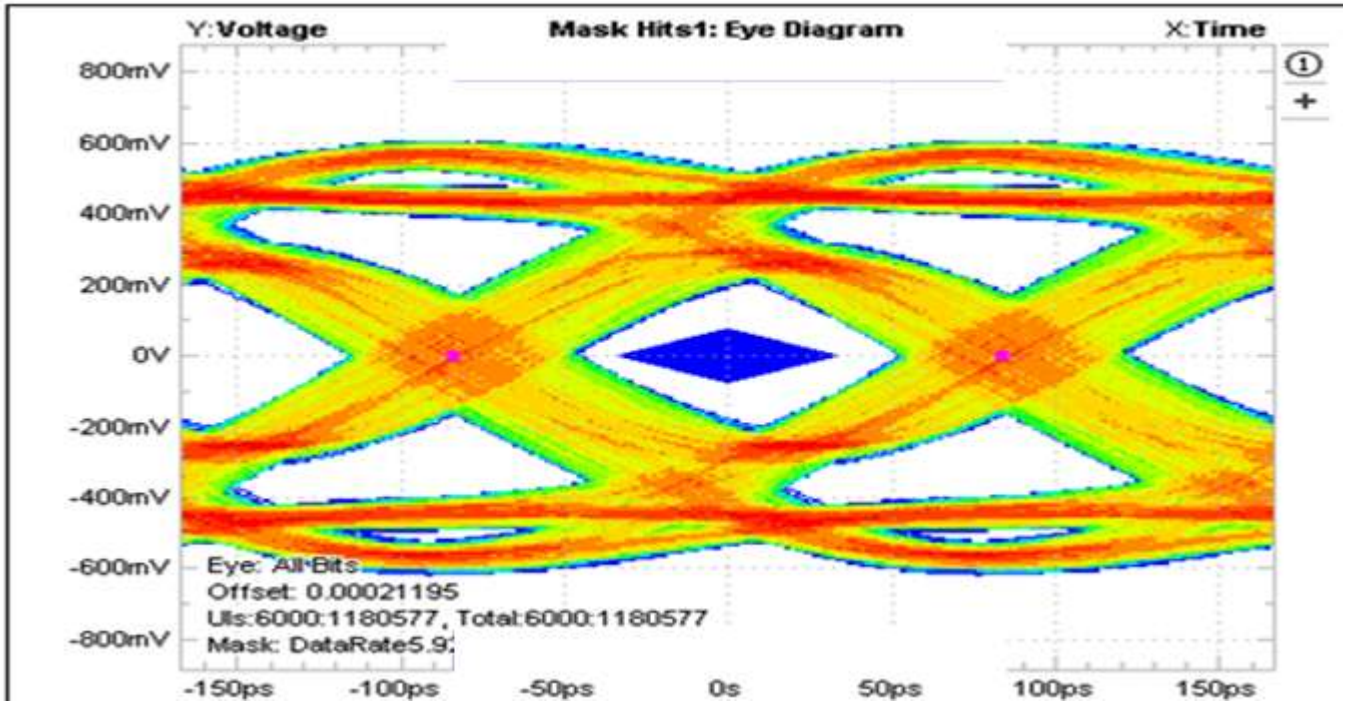
Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram

Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance

Source Eye Diagram Test

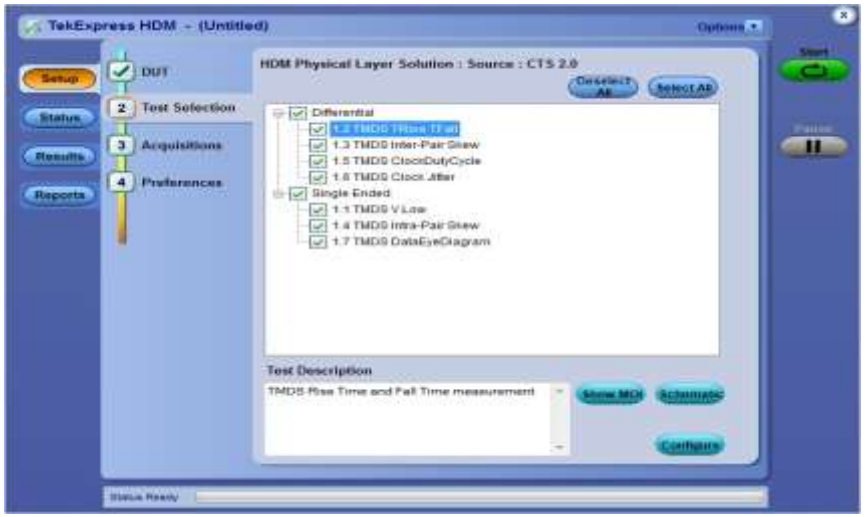


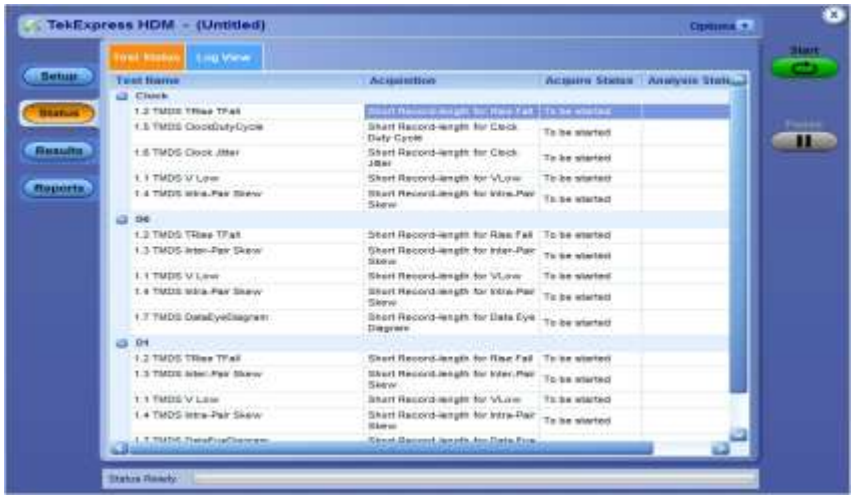
TP2 Source Eye for HDMI 2.0 6G signal



Single End Input eye rendered at Tek lab

HDMI 2.0 Tx Compliance Software





HDMI 2.0 Sink testing Equipment needs

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 Sink testing for Jitter Verification/Calibration/Controller.
- P7313SMA probes > 3
- Option HDM and HDM-DS
- HDMI 2.0 Fixture set
- 2# AWG7122C with Opt 01,02 or 06, 08 for **HDMI 2.0 Compliance only setup**.

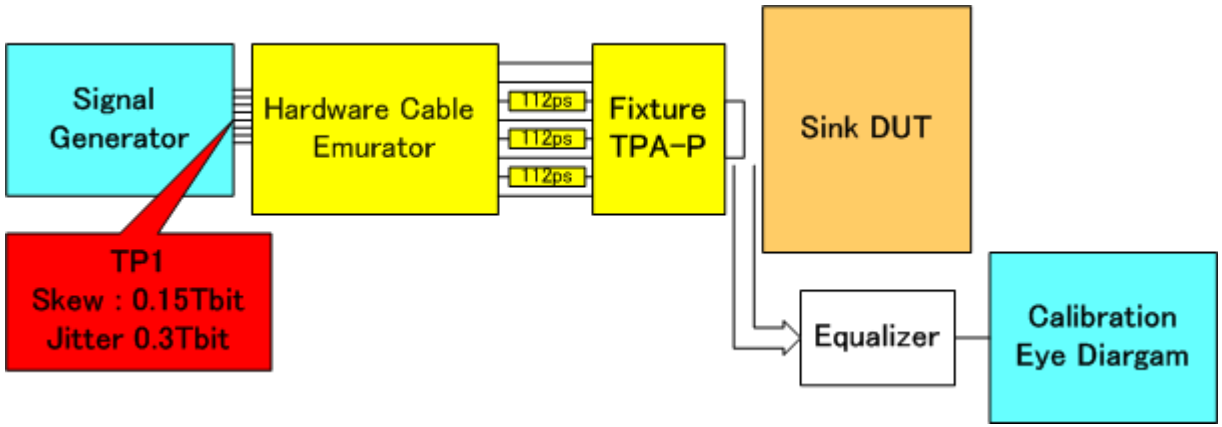
OR

2# AWG70002A with Opt 01,03 and 225 for **HDMI 2.0 Compliance and Margin Test setup.(Margin test feature will be available later and is part of roadmap**)

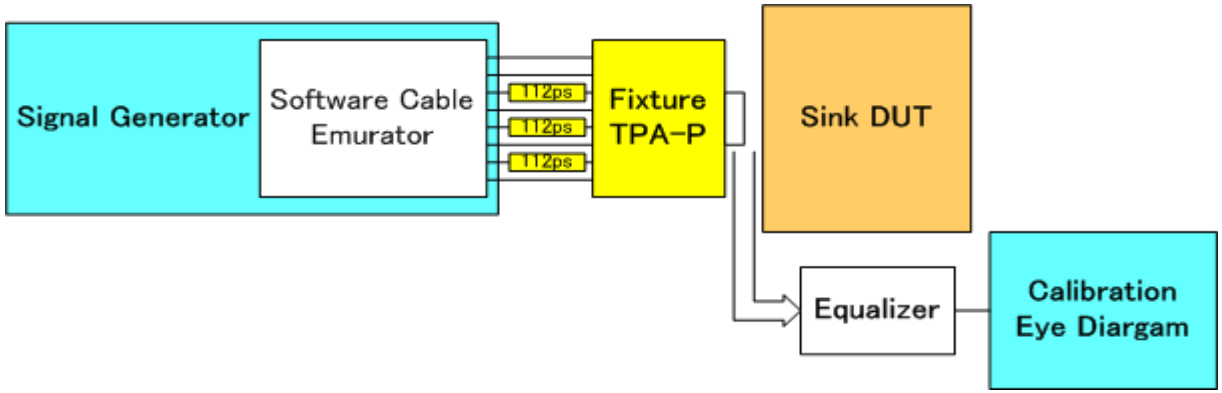
Note- We shall also support a 12.5GHz BW scope which would result in appx. 10% inaccuracy in RT/FT results .

Requirement for Signal generation

Cable Emulation and Skew by Hardware



Hardware Skew and Software Cable Emulation



Sink Electrical tests

Test ID HF2-1: Sink TMDS Electrical – 340-600Mcsc – Min/Max Differential Swing Tolerance

Test ID HF2-2: Sink TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

Test ID HF2-3: Sink TMDS Electrical – 340-600Mcsc – Jitter Tolerance

Test ID HF2-4: Sink TMDS Electrical – 340-600Mcsc – Differential Impedance (performed using sampling scope)

HDMI 2.0 Rx solution positioning statement

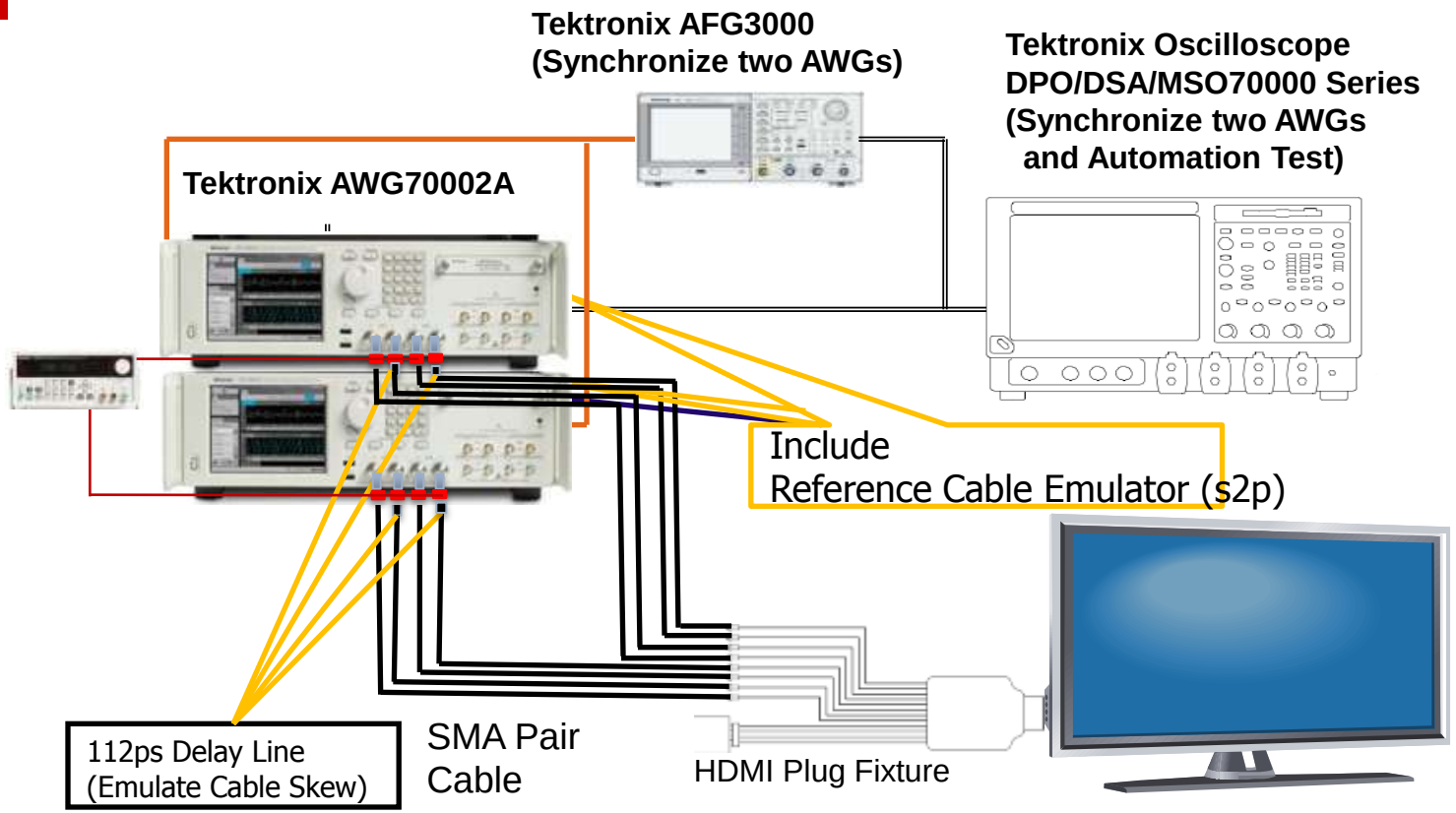
- Tektronix will support HDMI 2.0 Sink Electrical and protocol tests using either 2# AWG7122C (w/ Opt 01,02/06,08) OR 2# AWG70002A (W/ Opt 01,03 ,225)
- Solution Positioning:
  - **Compliance solution** for HDMI 2.0 Rx
    - 2# AWG7122C with opt 01, 02/06 and 08
    - 1# AFG3102/C

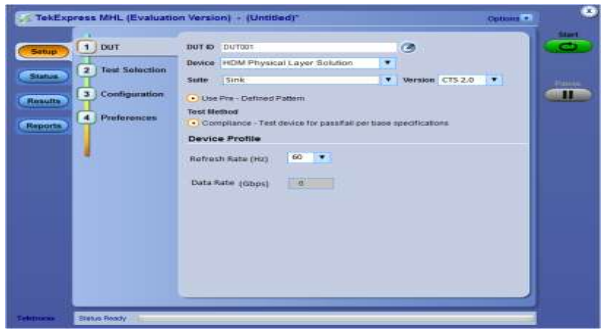
  Customers can use common test setup for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution.

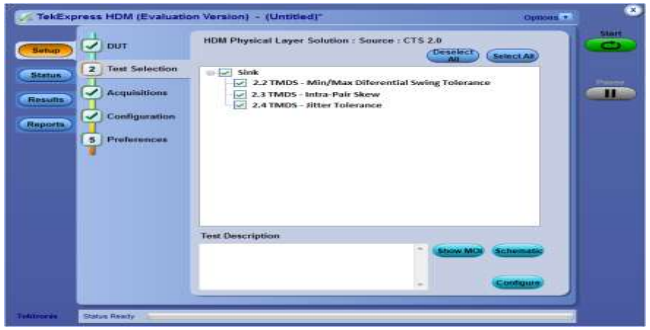
  - **Compliance and Margin solution** for HDMI 2.0 Rx
    - 2# AWG70002A with Opt 01,03 and 225.
    - 1# AFG3102/C

  Customers can use common test setup for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution

HDMI 2.0 Sink Test setup







Sink Testing 1.4b Vs 2.0

Jitter Tolerance test needs +ve and –ve lanes tested with 112ps delay line

Rest of the tests is similar to HDMI 1.4b tests

1.4b CTS test is a pre-requsite for HDMI 2.0

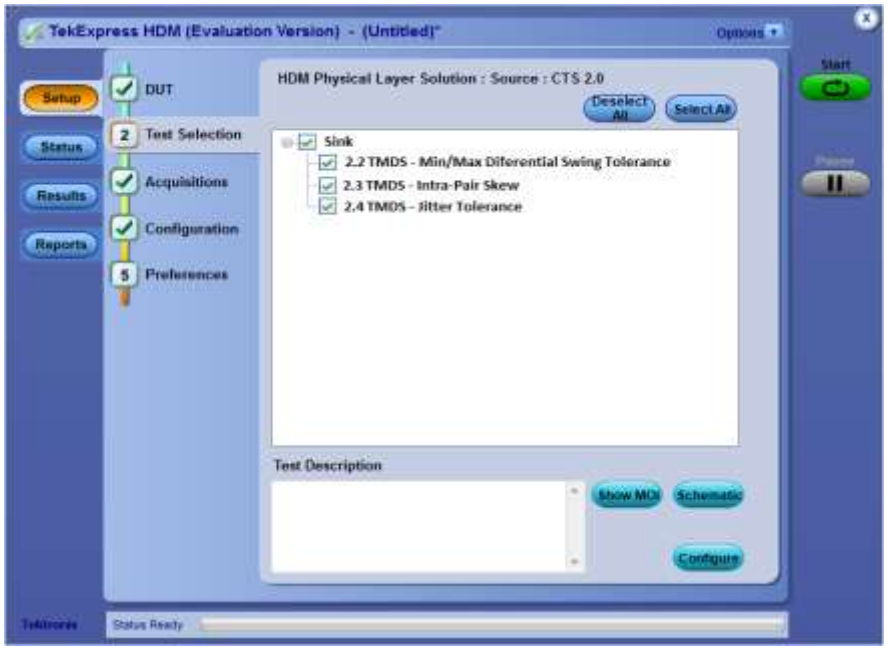
Need AWG 70002A for HDMI 2.0 Compliance and Margin needs while AWG7122C is suitable for HDMI 2.0 Compliance testing only..

Min 8GHz scope to 16GHz scope

Fixtures and Probes

HDM and HDM-DS Software

HDMI 2.0 Rx Compliance Software



HDMI 2.0 Equipment List

- DPO/DSA /MSO 70004C/B/D/DX with 10XL-Minimum 16GHz BW(we also support 12.5GHz BW scope)- needs Opt DJA, Opt SR-EMBD and SR-CUST.
  - Option HDM
  - Option HDM-DS

- AWG70002A With Option 01, 03 and 225
  - Rack Mount Kit
  - AFG3102/C

  OR

  AWG7122C with Option 01,02/06 and 08
  - AFG3102/C

- HDMI 2.0 Fixture set

- Termination Fixture (TF-HDMI-TPA-T)

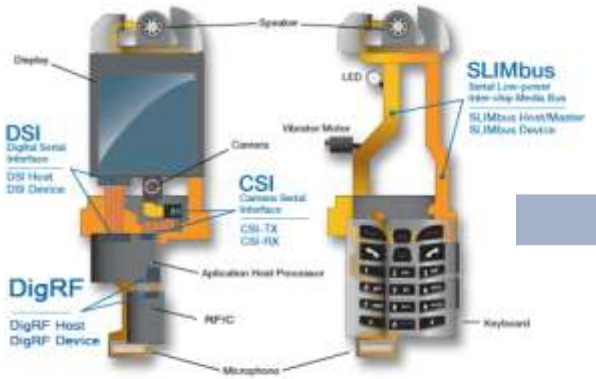
- P7313SMA probes –Quantity 4

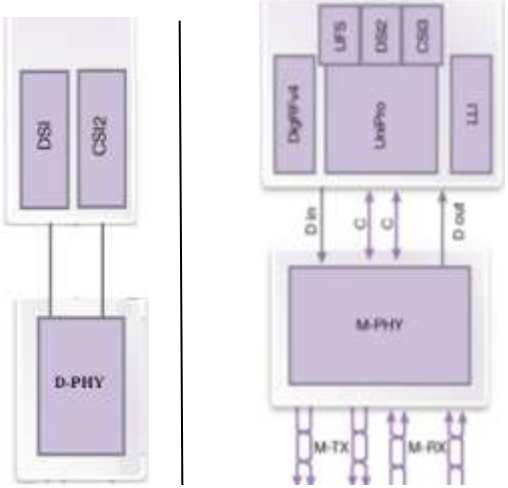
- HDMI DS accessory kit (Same 1.4b DS accessory kit is good enough)

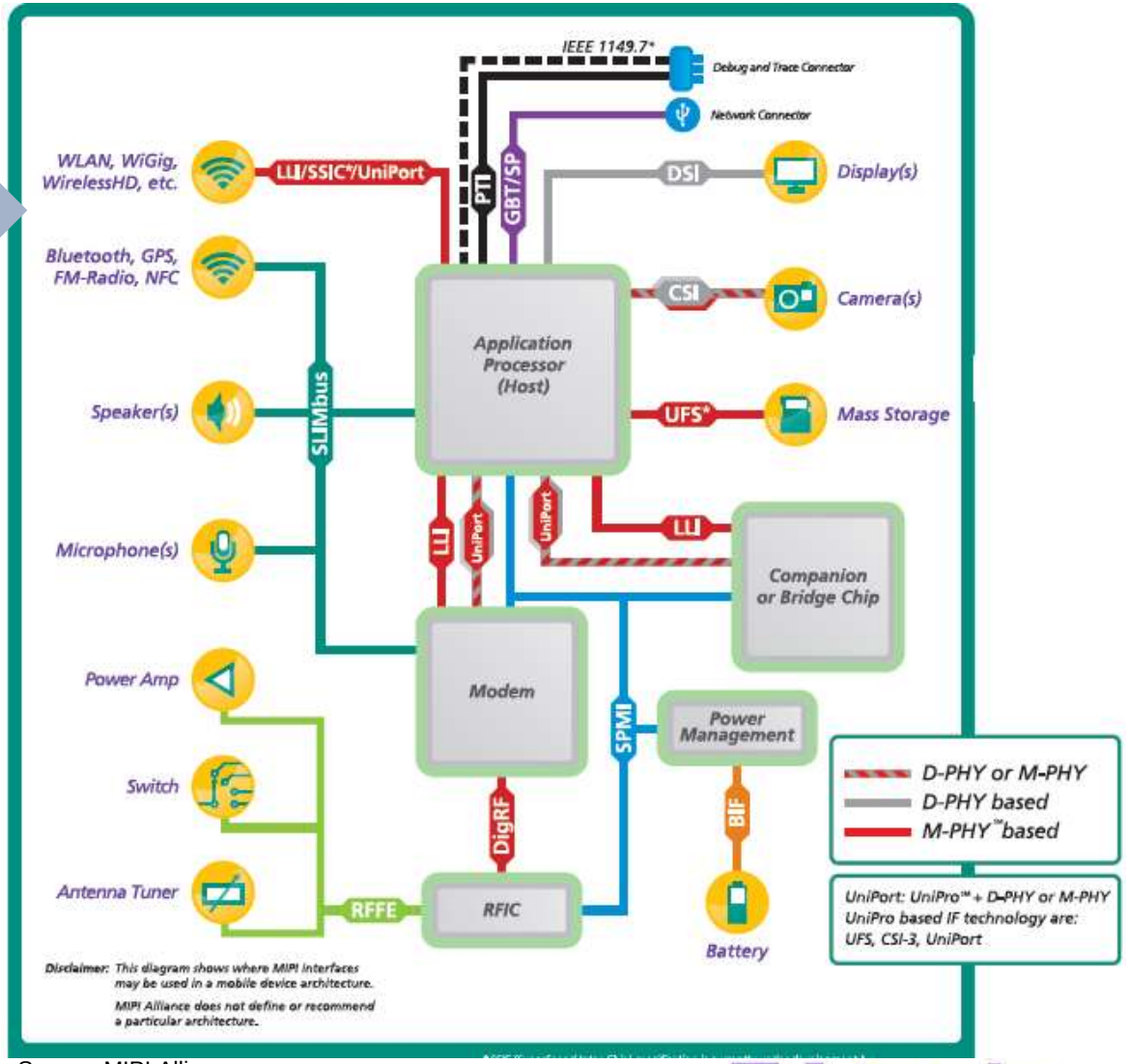
- Programmable Dual Channel Power supply

MIPI – D-Phy to M-Phy, C-Phy is coming soon

MIPI Technologies Overview
Example of a Mobile Platform







Source: MIPI Alliance

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Tek Strategic Involvement

With MIPI Alliance &UNH-IOL

- Tektronix is a ***Contributor Member*** of the MIPI Alliance
- M-PHY Tx/Rx CTS Test Document ***"Co-Authored"*** by Tektronix
- Tektronix has a close working relationship with UNH-IOL.
- ***Joint Press-Announcements*** of Tek with MIPI Alliance and UNH.
  - http://www2.tek.com/cmswpt/prdetails.lotr?ct=PR&cs=News+Release&ci=19076&lc=EN
  - "As an active MIPI contributor, Tektronix products speed the assessment of D-PHY and M-PHY performance and signal integrity. Tektronix is helping to simplify physical-layer test and validation."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2011*
  - http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6
  - "…Tektronix spurring the adoption of D-PHY and M-PHY specifications.."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2010*
  - "Tektronix has been supportive of UNH-IOL's collaborative efforts of physical layer measurement methodologies"
    - *Andy Baldman, MIPI Interop - R&D Technical Staff, UNH-IOL, Sept'2010*

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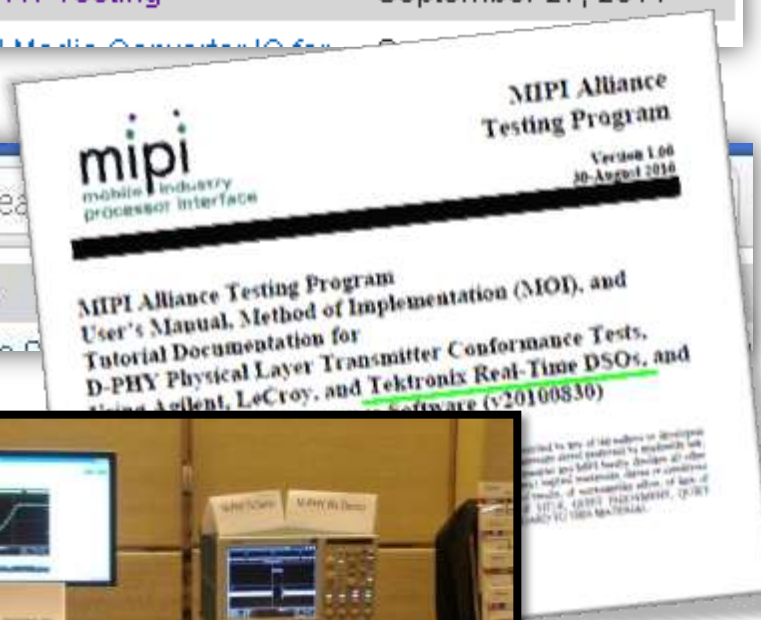
Tek Strategic Involvement

Tek Tools listed on MIPI Official Webpage, UNH Webpage &CTS Spec



UNH (University of New Hampshire)
is a 3rd party test house Using Tektronix setup

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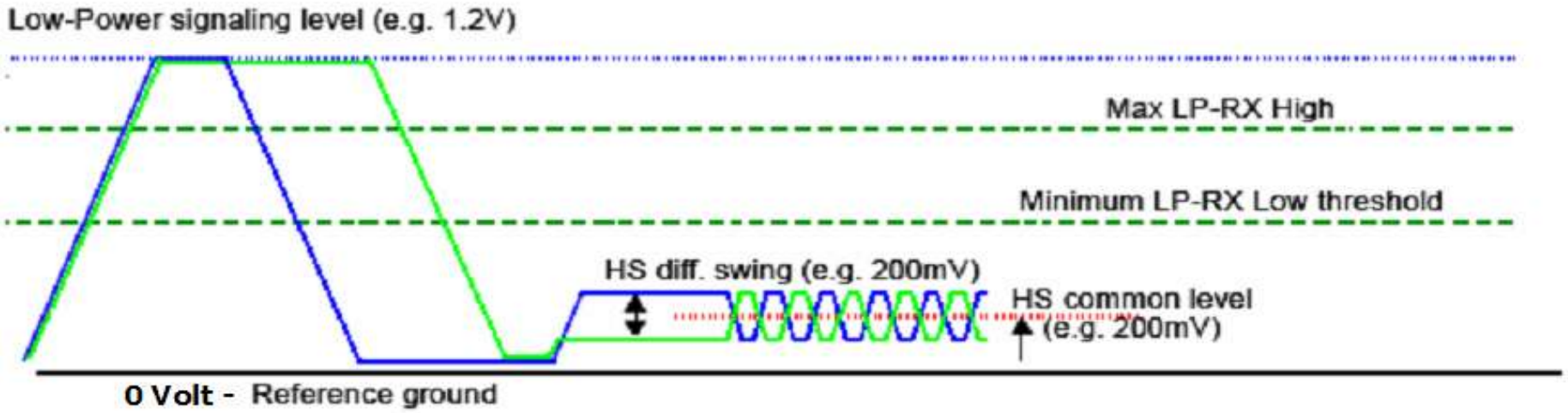
iol mipi alliance ektronix

What is D-PHY ?

- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP



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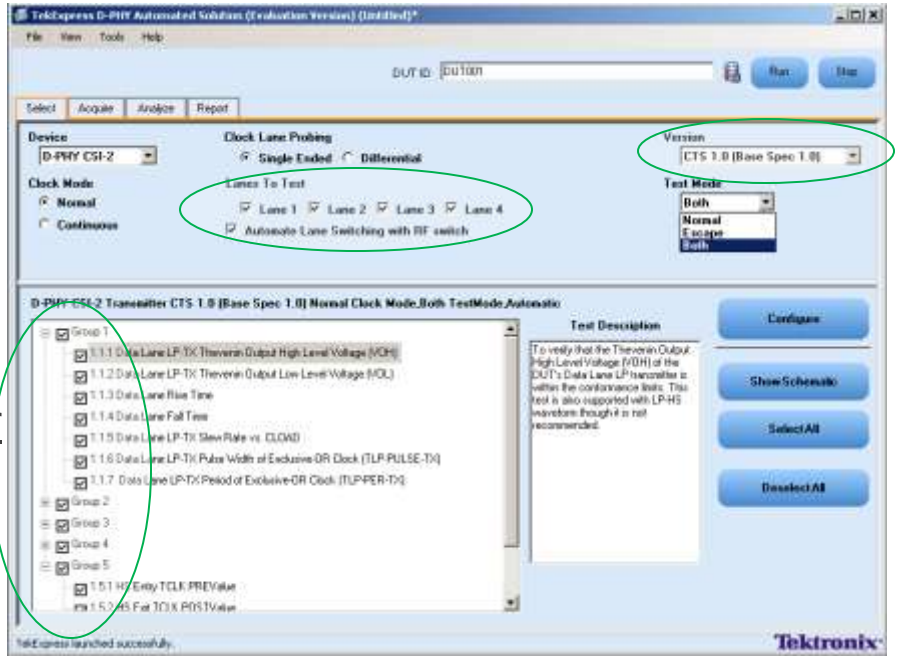
D-PHY Testing Challenges

- Logo testing is not required, but Optional.
  - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, similar to a DDR bus.
  - Mobile Phones do not need compliance logo, unlike USB/SATA devices
- No two MIPI devices are the same
  - Variable Data Rates
  - Up to 4 lanes of Data traffic,
  - Multiple different data formats
  - Specification enables custom limits.
- Characterization is significantly important
  - Mobile OEMs select the suppliers based on characterization reports.
- Several measurements (Total 49) to be performed.
  - Clock Lane
  - Data Lane
  - Clock-Data Timing

D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Runs on 7K/C and 70K/B/C/D scopes
  - Opt.TEKEXP is Pre-Requisite



- Differentiation
  - **Un-parallel** Automation (Auto-Cursors)
  - **100%** Widest Test Coverage
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.0)
- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & ”Zoom-in” Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready

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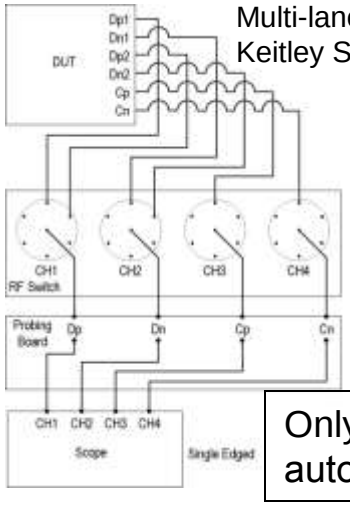
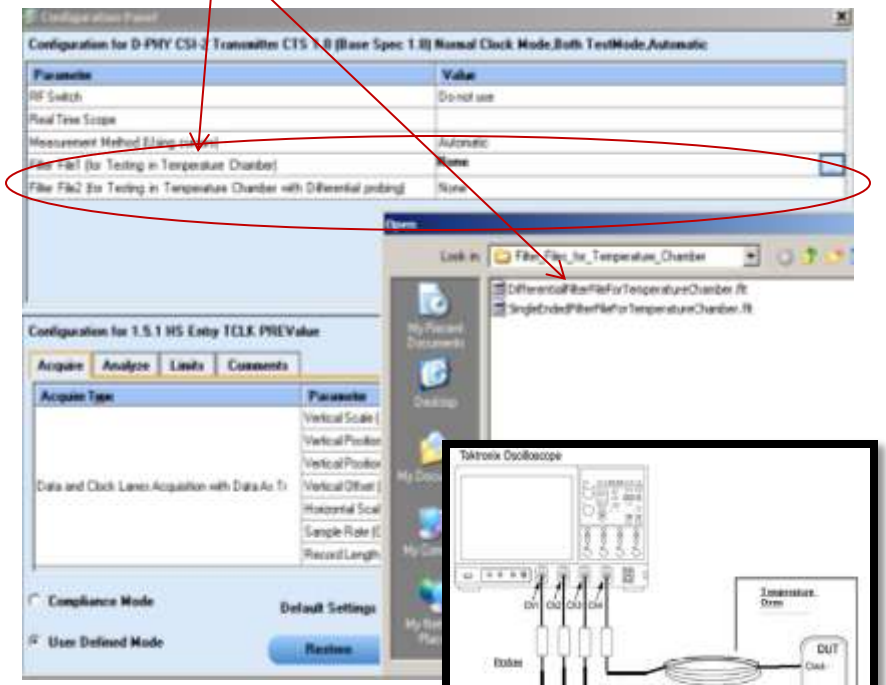
D-PHY Tx : Opt.D-PHYTX Features

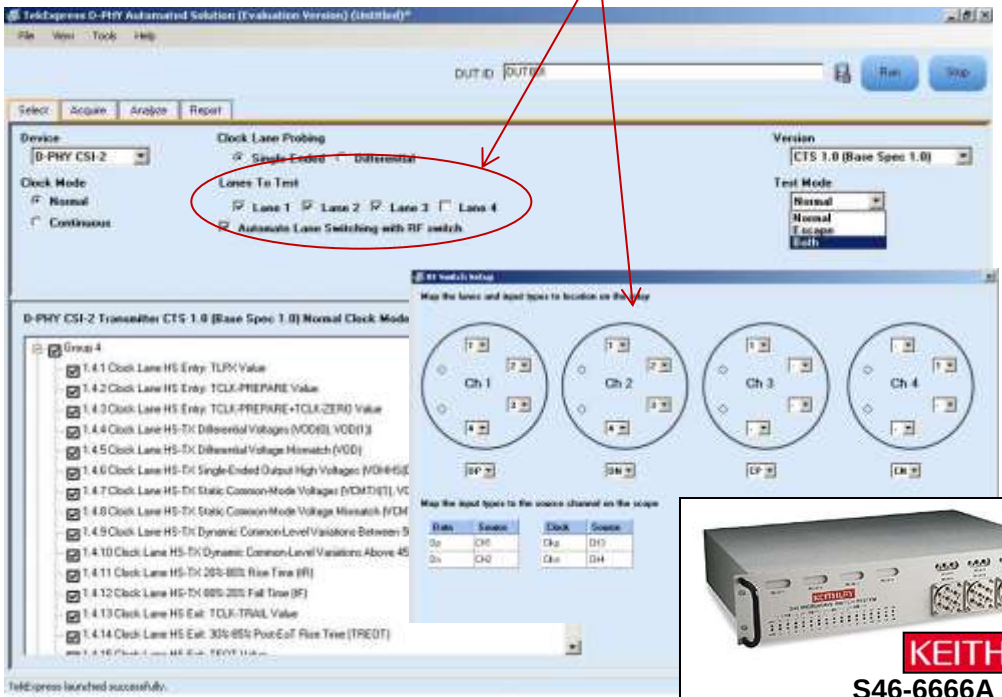
Provision to Load Filter-files for Temperature Chamber or Channel De-embedding



Multi-lane Automation Setup using Keitley S46-6666A/ any RF Switch



Only solution for Single-button automation of “multi-lane” DUTs.



S46-6666A Switch

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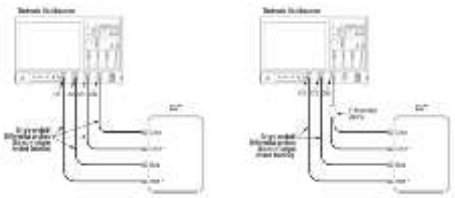
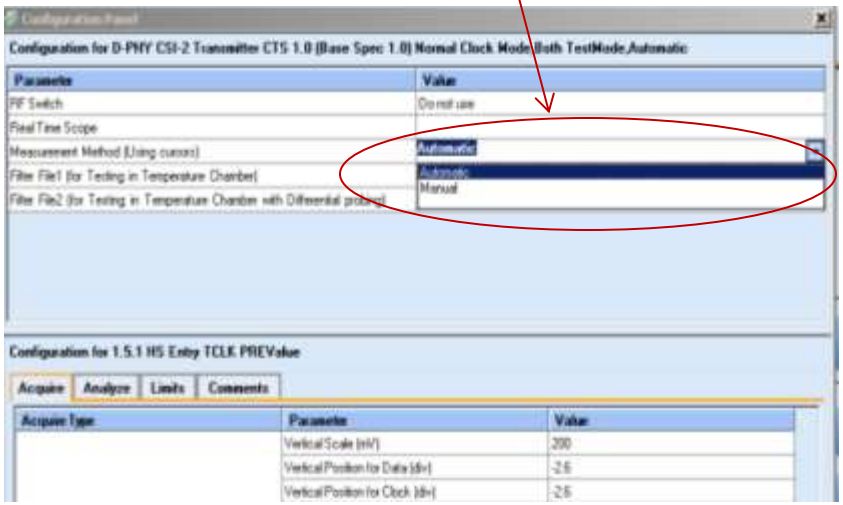
D-PHY Tx : Opt.D-PHYTX Features



Single-Lane Automation Setup using SE/Diff probes

Test Reports with “ZOOM-IN” screenshots of the cursors placement for each test.

Switch between Automatic and Manual cursor palcement. In Automatic mode, software can find the LP/HS regions automatically. Switch to Manual for debug or if your signal is too noisy.



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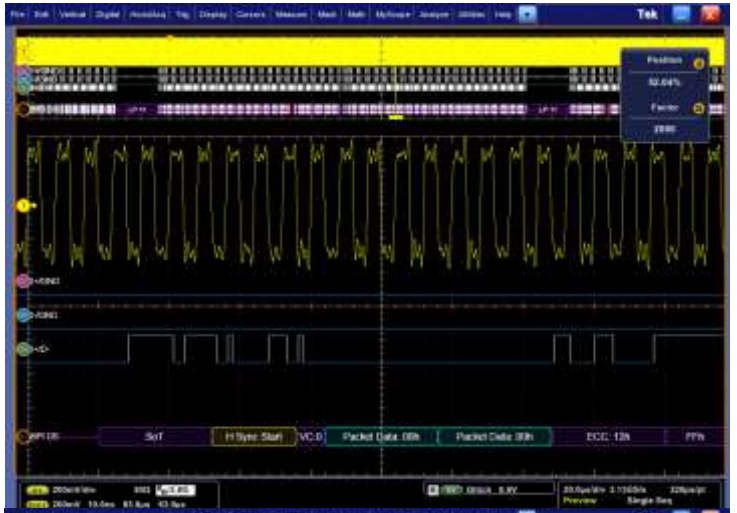
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI &CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial-- > Select MIPI DSI or CSI from the drop down list.

Probe using Mixed Channels

Analog Clock, Digital Data



Digital Clock, Analog Data

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D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

Errors/ Warnings indicated in Decode waveform &Event Table

Missing Sync

Checksum Error

ECC error

Errors and Warnings indicated in event table

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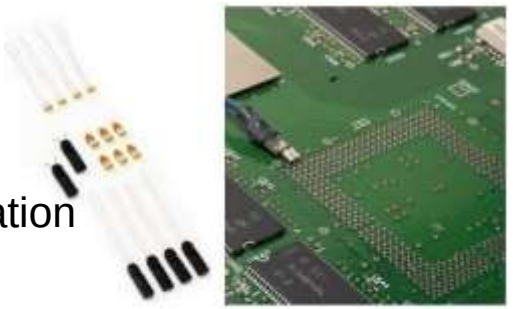
D-PHY Tx &Decode: Recommended Test Setup

www.Tek.com/MIPI

- Scope
  - DPO7354/C or DPO/DSA/MSO70404/B/C/D or higher for rise time accuracies
- Probes
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500/P73xx (clock is non-continuous), or 3x TDP3500/P73xx (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- Scope Software
  - Opt.D-PHYTX on TEKEXP for Conformance Test
  - Opt.D-PHY on DPOJET for Debug, Analysis &Characterization
  - Opt.SR-DPHY for Decoding CSI-2 and DSI traffic



P7380 probe used with a probe-tip

- Fixtures
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups: We recommend following UNH-IOL Termination board
    - http://www.iol.unh.edu/services/testing/mipi/fixtures.php
    - www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc

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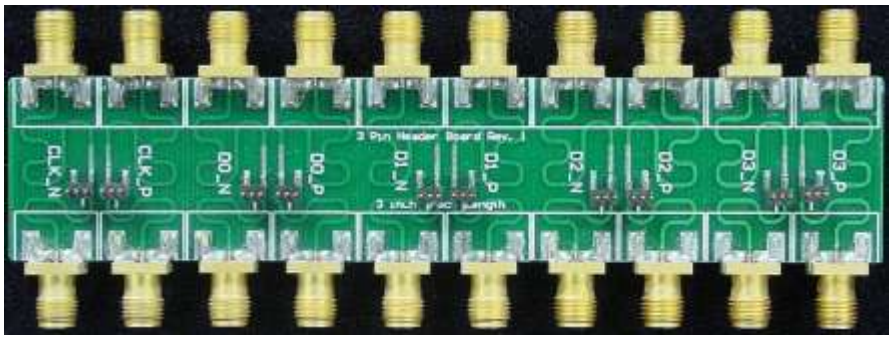
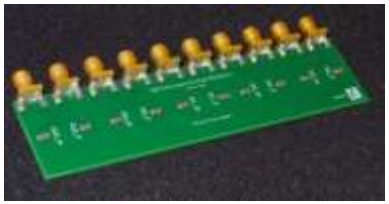
D-PHY Tx: Optional Accessories

Optional Based on DUT Scenarios (i.e. SMA/ Non-live setup/ Multi-lane)

- UNH-IOL RTB Reference Termination Board (list price: $2,895.), UNH-IOL Probing Board (list price: $450.), and Capacitive Load Board for Clock and Data Lane LP-TX Signaling tests (list price: $295.).
  - http://www.iol.unh.edu/services/testing/mipi/fixtures.php
  - www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc





- RF Switch,
  - Keithley S46-6666A, for multi-lane automation:
  - http://www.keithley.com/products/switch/rfmicrowave/?mn=S46

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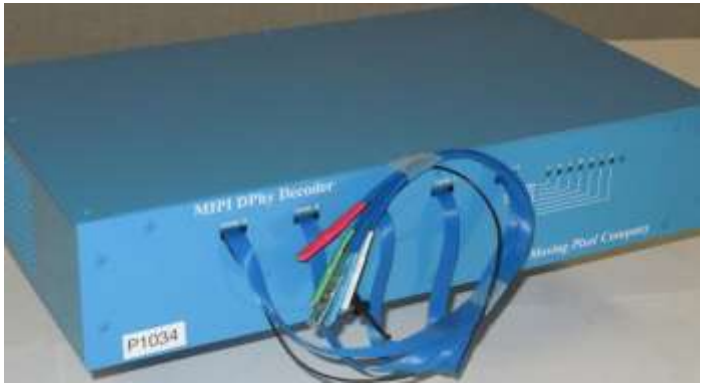
D-PHY Decoder Features Highlights

- Up to 4 data lanes and 1 clock lane. Data rate operation up to 1.5 Gb/s
- Connection to the DUT is via 5 active solder-down probes (supplied), one per lane
- Sophisticated real-time triggering
- real-time record filtering
- status monitoring
- activity statistics
- status LED indicators



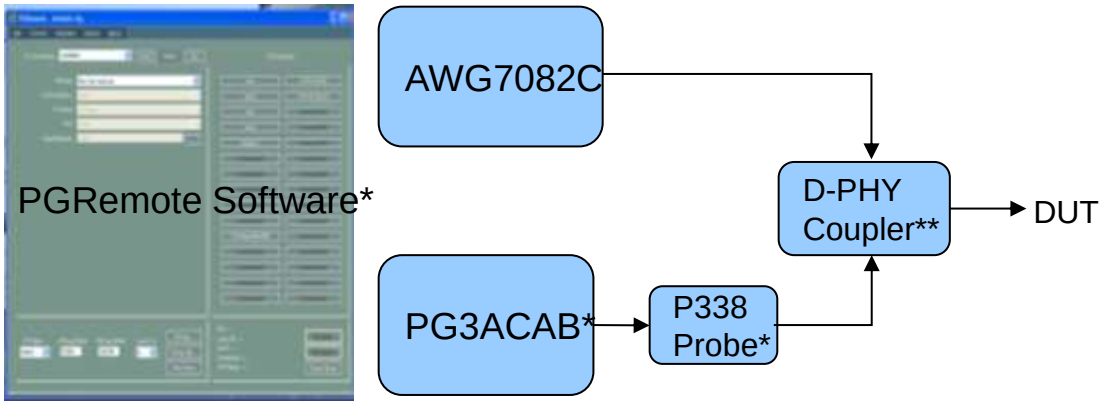
- active probes, solder-down, for minimal loading of the device under test
- Configuration control
- Disassembly of the captured information in a logic analyzer- like format
- Reassembly and display of any video information captured
- Storage of captured video frame(s) to a file(s)

D-PHY Rx : Test Solution Overview

Manual Setup based on PG with PGRemote Software

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals

Recommended Manual Setup



*These Moving Pixel products are available as Tektronix part number
**Tektronix part number not available yet. Expected Soon.

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D-PHY Rx : Test Solution Overview

100% Test Coverage to CTS v0.98

Group 1 LP - RX voltage and timing requirements			
Test	**Title**	**Page**	**Equipment**
2.1.1	LP - RX Logic 1 Input Voltage (V_{IH})	108	PG
2.1.2	LP - RX Logic 0 Input Voltage, non-ULP State (V_{IL})	110	PG
2.1.3	LP - RX Logic 0 Input Voltage, ULP State ($V_{IL-ULPS}$)	112	PG
2.1.4	LP - RX Minimum Pulse Width Response (T_{MIN-RX})	113	PG
2.1.5	LP - RX Input Hysteresis (T_{HYST})	114	PG
2.1.6	LP - RX Input Pulse Rejection (e_{SPIKE})	116	PG + AWG + DC Power Supply
2.1.7	LP - RX Interference Tolerance (V_{INT} and f_{INT})	120	PG + AWG
2.1.8	LP - CD Logic Contention Thresholds (V_{ILCD} ans V_{IHCD})	122	PG + AWG
Group 2 LP - RX Behavioral Requirements			
Test	**Title**	**Page**	**Equip**
2.2.1	LP - RX Initialization Period (T_{INIT})	125	PG
2.2.2	ULPS Exit: LP - RX $T_{CLKULPS}$ Timer Value	126	PG
2.2.3	Clock Lane LP - RX Invalid/Aborted ULPS Entry	127	PG
2.2.4	Data Lane LP - RX Invalid/Aborted Escape Mode Entry	128	PG
2.2.5	Data Lane LP - RX Invalid/Aborted Escape Mode Command	130	PG
2.2.6	Data Lane LP - RX Escape Mode Invalid Exit (Informative)	132	PG
2.2.7	Data Lane LP - RX Escape Mode, Ignoring Post Trigger-Command Extra Bits	134	PG
2.2.8	Data Lane LP - RX Escape Mode Unsupported/Unassigned Commands	136	PG

Group 3: HS - RX Voltage and Setup/Hold Requirements			
Test	**Title**	**Page**	**Equipment**
2.3.1	HS - RX Common Mode Voltage Tolerance ($V_{CMRX(DC)}$)	139	PG
2.3.2	HS-DX Differential Input High Threshold (V_{DIFFH})	141	PG
2.3.3	HS-DX Differential Input Low Threshold (V_{DIFFL})	143	PG
2.3.4	HS - RX Single-Ended Input High Voltage (V_{SSHRX})	144	PG
2.3.5	HS - RX Single-Ended Input Low Voltage (V_{SSLRX})	146	PG
2.3.6	HS - RX Common Mode Interference 50MHz - 450MHz (delta VCMRX(LF))	148	PG + AWG
2.3.7	HS - RX Common Mode Interference Beyond 450MHz (delta VCMRX(HF))	150	PG + AWG
2.3.8	HS - RX Setup/Hold and Jitter Tolerance	151	PG + AWG
Group 4: HS - RX Timer Requirements			
Test No.	**Title**	**Page**	**Equipment**
2.4.1	Data Lane HS - RX $T_{D-TERM-EN}$ Value	156	PG
2.4.2	Data Lane HS - RX $T_{HS-SETTLE}$ + $T_{HS-SETTLE}$ Tolerance	158	PG
2.4.3	Data Lane HS - RX $T_{HS-SKIP}$ Value	160	PG
2.4.4	Data Lane HS - RX $T_{HS-EXIT}$ Tolerance	162	PG
2.4.5	Data Lane HS - RX $T_{HS-TRAIL}$ Value	164	PG
2.4.6	Clock Lane HS - RX $T_{CLK-TERM-EN}$ Value	166	PG
2.4.7	Clock Lane HS - RX $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ Tolerance	167	PG
2.4.8	Clock Lane HS - RX $T_{CLK-SETTLE}$ Value	169	PG
2.4.9	Clock Lane HS - RX $T_{CLK-TRAIL}$ Tolerance	171	PG
2.4.10	Clock Lane HS - RX $T_{CLK-MISS}$ Value	173	PG
2.4.11	Clock Lane HS - RX $T_{CLK-PRE}$ + $T_{CLK-POST}$ Tolerance	175	PG

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PG3A and P338 MIPI D-PHY Rx Solution

Key Features

- MIPI D-PHY Probe for use with PG3AMOD and PG3ACAB
- Generate CSI2 and DSI data over D-PHY
- 4-Data Lanes and 1-Clock lane
- 1.5Gbps @ 4Lane and 800Mbps @ 8 lanes
- 1.5Gbps @ 8Lanes if using two PG3A
- SMA outputs for each lane
- LP and HS Voltage and Timing adjustable on a each lane separately

PG3A

P338

Preserve your investment with the ONLY >4 lane, 1.5Gbps stimulus solution in the market.

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Practice Connection

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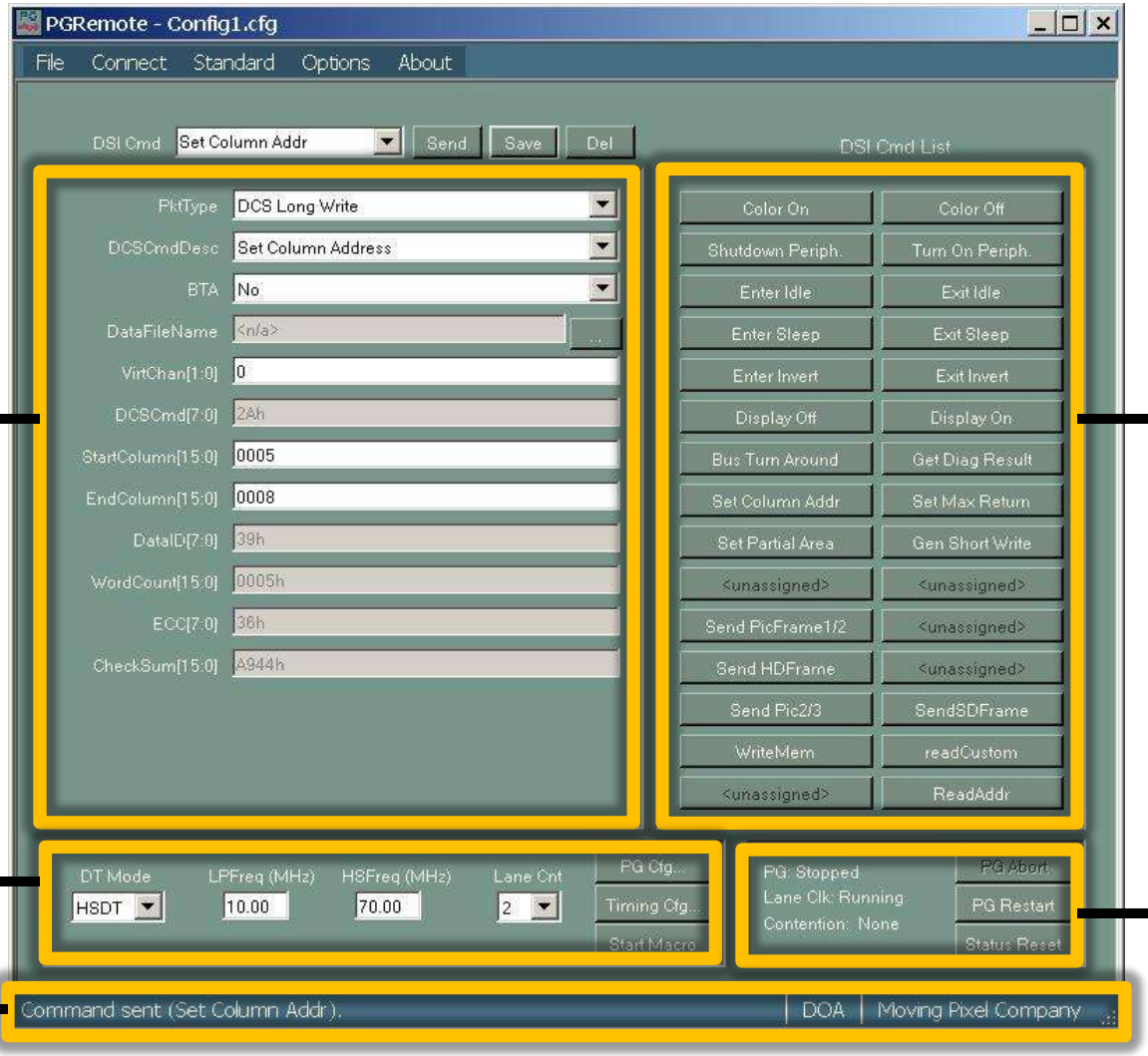
PGRemote

Push Button Interface to generate CSI2 / DSI Vectors



Define CSI/DSI commands and arguments

Configuration Parameters for PG playback, and D-PHY

Status Bar

Command Buttons

PG, probe status and operational controls

PGRemote Main Window

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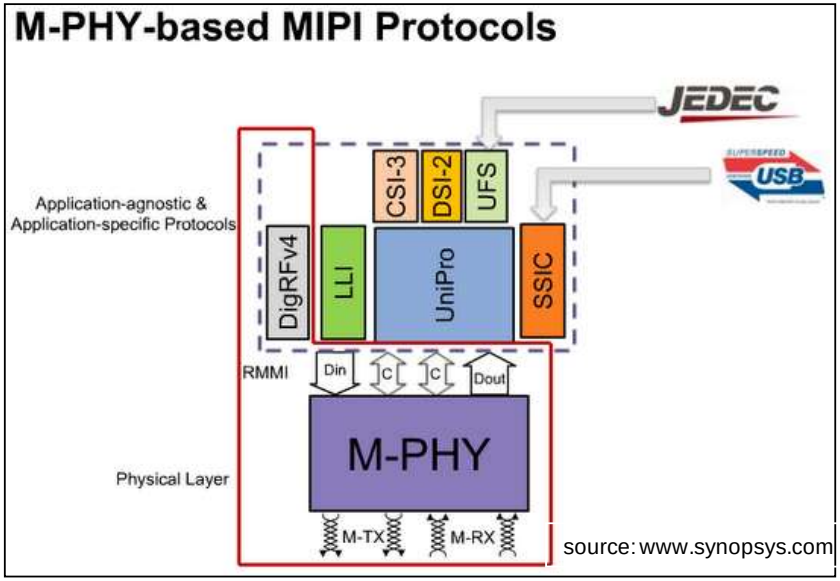
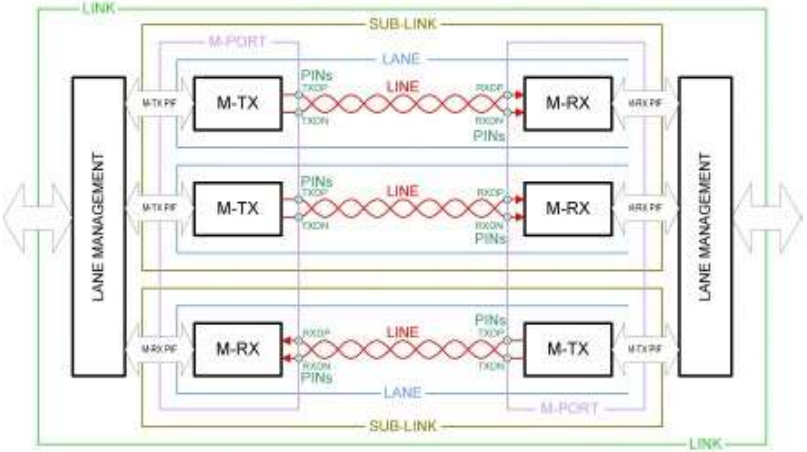
What is M-PHY ?

- M-PHY is a high-speed serial interface to the DigRFv4, UniPro, LLI, CSI-3 and DSI-2 interconnect standards of the MIPI Alliance, and the UFS and SSIC protocol standards of JEDEC and USB-IF respectively.
- M-PHY is a flexible architecture that allows the implementer to support high data rates at minimal power, cost & I/O redesign, for applications such as High Definition Video
- A Fast, Scalable, Serial Communications Architecture
  - Link – Connects M-PHY Transmitter to an M-PHY Receiver
  - Sub-link – Manage one or more lanes
  - Lane – Operation defined in the protocol (DSI, CSI, UniPro, DigRF)





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M-PHY Transmitter Testing Challenges

M-PHY Signal Characteristics							
Signaling mode	**Datarates**			**Amplitudes**		**Impedance**	
	Gears	A (Gbps)	B (Gbps)	Large	Small	Resistive Terminated	Non Terminated
High Speed (HS)	G1	1.25	1.45	Terminated: 160-240mV, Non-Terminated: 320-480mV	Terminated: 100-130mV, Non-Terminated: 200-260mV	50 ohms	-
	G2	2.5	2.91				
	G3	5	5.83				
PWM (ie. TYPE-I)	Gears	Min (Mb/s)	Max (Mb/s)			50 ohms	10k ohms
	G0	0.01	3				
	G1	3	9				
	G2	6	18				
	G3	12	36				
	G4	24	72				
	G5	48	144				
	G6	96	288				
	G7	192	576				
SYS (ie. TYPE-II)			576 (Mb/s)			50 ohms	10k ohms

- Higher data rate will increase importance of Signal Integrity of links
  - More emphasis on timing/jitter and noise (signal integrity)
  - Receiver testing will be needed to stress-test resulting BER
- 1000+ tests per lane, covering multiple Gears, Terminations, Amplitudes.
- Termination – Restive or not Terminated.
  - LS mode can operate either of them
  - HS mode it is always terminated, so swings are halved.
- Type-I and Type-II are Low speed modes, and are NOT interoperable
  - Type-I operates on independent local clocks. Type-II requires a shared Ref-clock.
  - DUTs may support both

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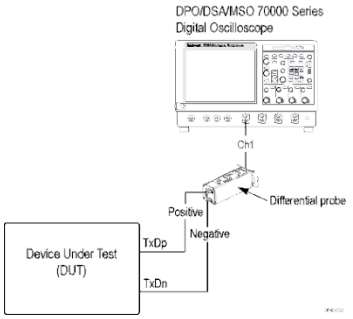
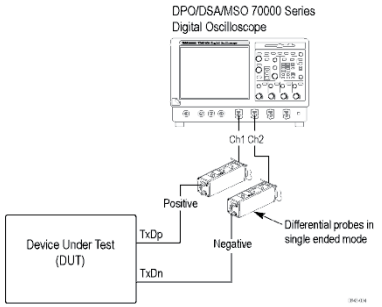
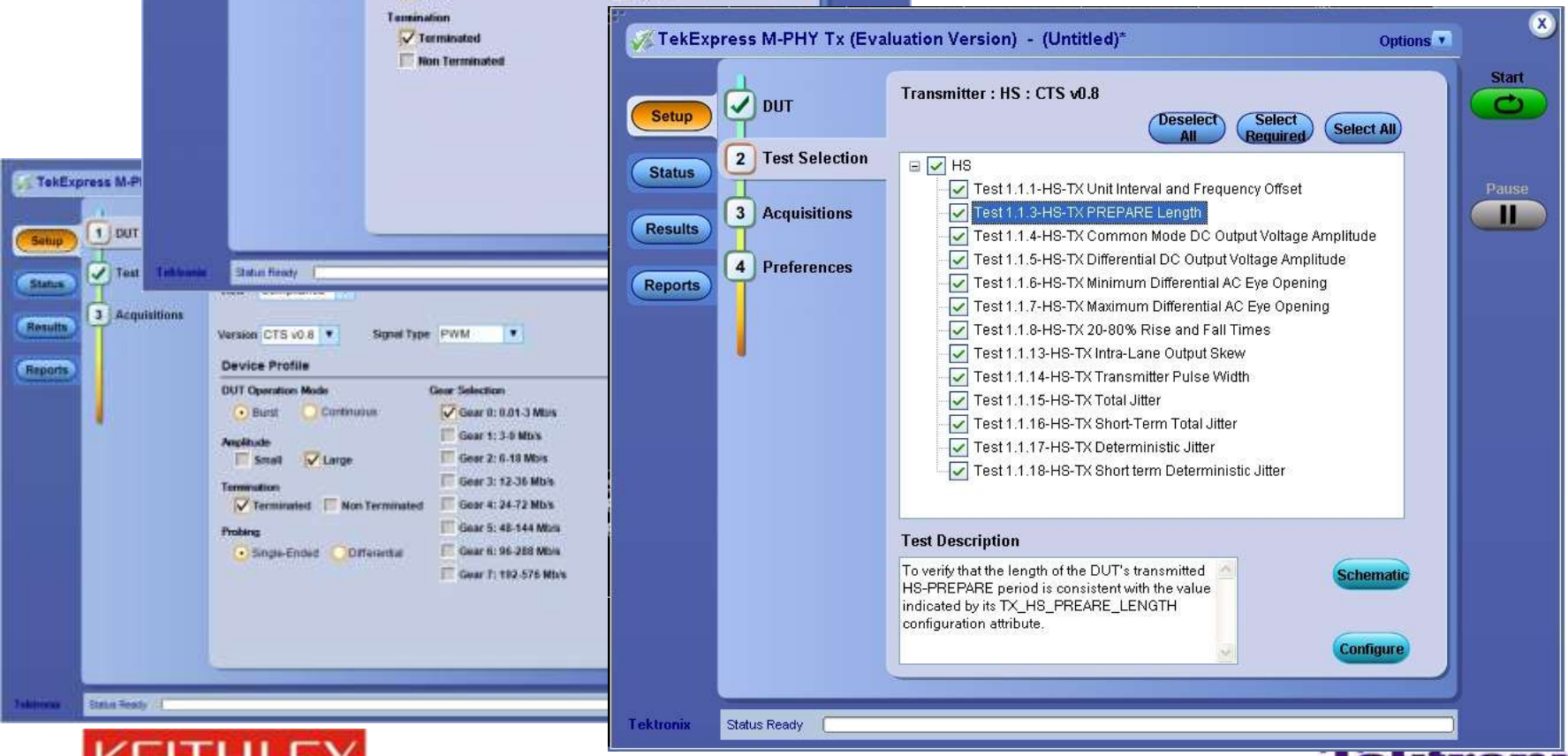
M-PHY Tx : Opt.M-PHYTX Automation Features

M-PHYTX – HS Test Configurations







M-PHYTX – HS Tests Coverage

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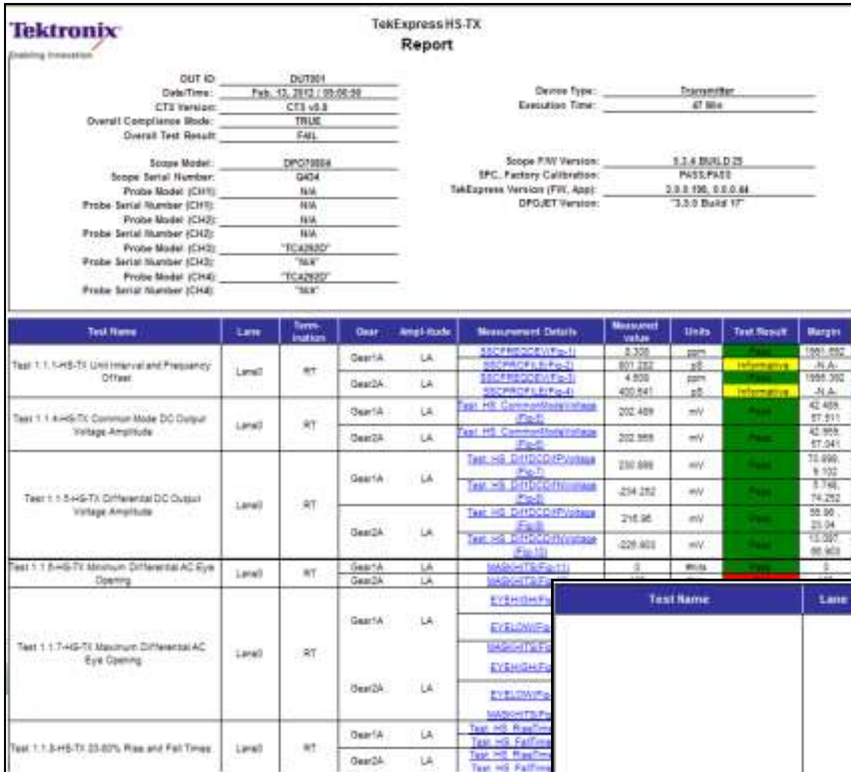
M-PHY Tx : Opt.M-PHYTX Automation Features

Comprehensive Test Reports



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TekExpress HS-TX

Report

DUT ID:	DUT001	Device Type:	Transmitter
Date/Time:	Feb. 13, 2012 / 05:08:50	Execution Time:	47 Min
CTS Version:	CTS v0.8		
Overall Compliance Mode:	TRUE		
Overall Test Result:	FAIL		
Scope Model:	DPO70804	Scope F/W Version:	5.3.4 BUILD 25
Scope Serial Number:	Q404	SPC, Factory Calibration:	PASS,PASS
Probe Model (CH1):	N/A	TekExpress Version (FW, App):	2.0.0.196, 0.0.0.44
Probe Serial Number (CH1):	N/A	DPOJET Version:	"3.0.0 Build 17"
Probe Model (CH2):	N/A		
Probe Serial Number (CH2):	N/A		
Probe Model (CH3):	"TCA292D"		
Probe Serial Number (CH3):	"N/A"		
Probe Model (CH4):	"TCA292D"		
Probe Serial Number (CH4):	"N/A"		

Test Name	Lane	Termination	Gear	Amplitude	Measurement Details	Measured value	Units	Test Result	Margin
Test 1.1.1-HS-TX Unit Interval and Frequency Offset	Lane0	RT	Gear1A	LA	SSCFREQDEV(Fig-1)	8.330	ppm	Pass	1991.692
					SSCPROFILE(Fig-2)	601.282	pS	Informative	-N.A-
			Gear2A	LA	SSCFREQDEV(Fig-3)	4.600	ppm	Pass	1995.392
					SSCPROFILE(Fig-4)	400.541	pS	Informative	-N.A-
Test 1.1.4-HS-TX Common Mode DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_CommonModeVoltage (Fig-5)	202.489	mV	Pass	42.489, 57.511
			Gear2A	LA	Test_HS_CommonModeVoltage (Fig-6)	202.959	mV	Pass	42.959, 57.041
Test 1.1.5-HS-TX Differential DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_DIFDCDIFPVoltage (Fig-7)	230.898	mV	Pass	70.898, 9.102
				LA	Test_HS_DIFDCDIFNVoltage (Fig-8)	-234.252	mV	Pass	5.748, 74.252
			Gear2A	LA	Test_HS_DIFDCDIFPVoltage (Fig-9)	216.96	mV	Pass	55.96, 23.04
				LA	Test_HS_DIFDCDIFNVoltage (Fig-10)	-226.903	mV	Pass	13.097, 66.903
Test 1.1.6-HS-TX Minimum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	MASKHITS(Fig-11)	0	Hits	Pass	0
			Gear2A	LA	MASKHITS(Fig...	[illegible]	[illegible]	[illegible]	[illegible]
Test 1.1.7-HS-TX Maximum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	EYEHIGH(Fig...				
					EYELOW(Fig...				
					MASKHITS(Fig...				
			Gear2A	LA	EYEHIGH(Fig...				
					EYELOW(Fig...				
					MASKHITS(Fig...				
Test 1.1.8-HS-TX 20-80% Rise and Fall Times	Lane0	RT	Gear1A	LA	Test_HS_RiseTime...				
					Test_HS_FallTime...				
			Gear2A	LA	Test_HS_RiseTime...				
					Test_HS_FallTime...				

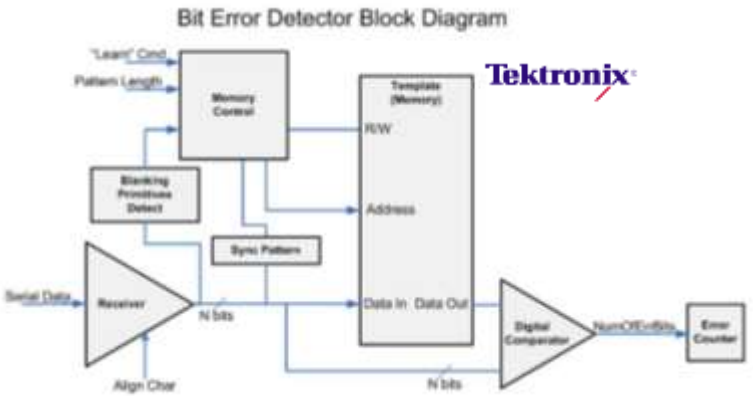
Single-printable report covering results from Multiple lane, Multiple Gears, Amplitudes, etc

Results from multiple test-configuration, of a single-test

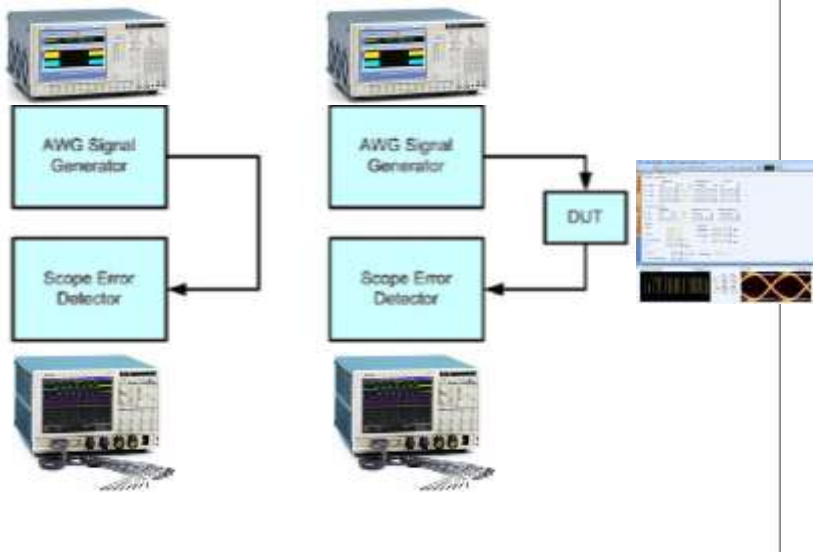
Test Name	Lane	Termination	Gear	Amplitude	Measurement Details	Measured value	Units	Test Result	Margin	Low Limit	High Limit	Compliance Mode
Test 1.2.1-PWM-TX Transmit Bit Duration	Lane0	RT	Gear0	SA	Transmit Bit Duration	1	Mbps	Pass	0.99, 2	>= 0.01	<= 3	Yes
				LA	Transmit Bit Duration	1	Mbps	Pass	0.99, 2	>= 0.01	<= 3	
			Gear1	SA	Transmit Bit Duration	5	Mbps	Pass	2, 4	>= 3	<= 9	
				LA	Transmit Bit Duration	5	Mbps	Pass	2, 4	>= 3	<= 9	
			Gear2	SA	Transmit Bit Duration	10	Mbps	Pass	4, 8	>= 6	<= 18	
				LA	Transmit Bit Duration	10	Mbps	Pass	4, 8	>= 6	<= 18	
			Gear3	SA	Transmit Bit Duration	36	Mbps	Pass	24, 0	>= 12	<= 36	
				LA	Transmit Bit Duration	36	Mbps	Pass	24, 0	>= 12	<= 36	
			Gear4	SA	Transmit Bit Duration	36	Mbps	Pass	12, 36	>= 24	<= 72	
				LA	Transmit Bit Duration	36	Mbps	Pass	12, 36	>= 24	<= 72	
			Gear5	SA	Transmit Bit Duration	60	Mbps	Pass	12, 84	>= 48	<= 144	
				LA	Transmit Bit Duration	60	Mbps	Pass	12, 84	>= 48	<= 144	
			Gear6	SA	Transmit Bit Duration	100	Mbps	Pass	4, 188	>= 96	<= 288	
				LA	Transmit Bit Duration	100	Mbps	Pass	4, 188	>= 96	<= 288	
			Gear7	SA	Transmit Bit Duration	200	Mbps	Pass	8, 378	>= 192	<= 576	
				LA	Transmit Bit Duration	200	Mbps	Pass	8, 378	>= 192	<= 576	

M-PHY Rx : Based on Scope built-in Error Detector

Scope-Integrated M-PHY BER using Opt.ERRDT Shipping Today



- 8B/10B Data:
  - Hardware Serial trigger: 1.25 Gb/s to 6.25 Gb/s
  - BER covers PRBS 312Mbs and above data rates.



MIPI® M-PHY Receiver
Methods of Implementation (MOI)

MIPI M-PHY Receiver - TEKTRONIX MOI

RX ERROR DETECTOR

Overview:
This section of tests verifies the M-PHY receiver error detection mechanism as defined in the M-PHY Specification.

GROUP 1: M-RX Error Detection Requirements

Overview:
This group of tests verifies various requirements of error detection on MIPI M-PHY receiver. Scope error detector is used for this purpose. For M-PHY error detector, ERRDT and STU option should be enabled in scope and Tekscope firmware v6.1.1.32 or later is required.

Status:
The test descriptions contained in this group are considered to be in initial draft form. Additional modifications to both the test descriptions and implementations are expected.

Pay Load:
Continuous PRBS 7/PRBS 9 Pattern with NRZ signaling (HS-Gear1, HS-Gear2 and DigRF data rates)
Custom burst pattern with 8b/10b encoded with NRZ/PWM/SYS signaling.

Note:
Please refer to the MPHY specification ver .90

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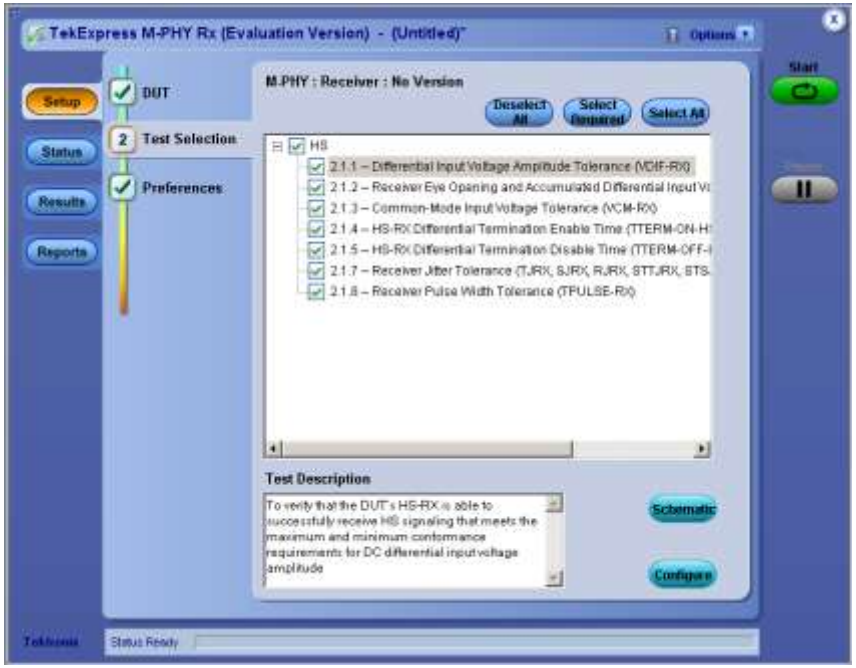
M-PHY Rx : Opt.M-PHYRX Automated Solution

- Opt.M-PHYRX
  - TekExpress (2.0) option for Fully-Automated receiver testing
  - Provides Conformance Testing
  - Based on Latest M-PHY Base Spec v1.0 &UNH's Conformance Test Suite
  - Runs on DPO/DSA70KB/C or MSO70K/C scopes
  - TekExpress framework is included.
- Differentiation
  - Simply 2-box setup.
  - Built upon Scope ErrorDetecror ERRDT.
  - Wide HS test coverage



- Value proposition
  - Test Reports with Pass/Fail summary, with Bit-Error counts

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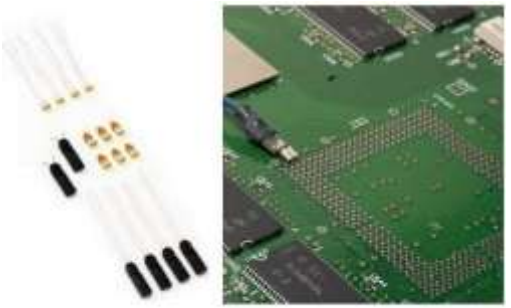
M-PHY Tx &Rx Recommended Test Setup (www.tek.com/MIPI)

- Scopes
  - DPO70604/B/C or above, for HS-Gear1 Only (Tx &Rx).
  - DPO70804/B/C or above, for HS-Gear1&2 Only (Tx &Rx)
  - DPO71254/B/C or above, for All HS-Gears (Rx Only)
  - DPO72004/B/C or above, for All HS-Gears (Tx &Rx).
- Probes
  - 2x P73xxSMA/P73xx, for Tx HS upto Gears2, or 2x P75xx with P75LRST for Tx HS upto Gear3.
  - 2x P73xxSMA/P73xx, for Tx PWM All Gears.
  - 1x P73xxSMA, for Rx.
- Signal Generators for Rx
  - AWG7082C, AWG7102 or above, for HS-Gear1 Only.
  - AWG7122C without Interleave, for HS-Gear1&2 Only.
  - AWG7122C with Interleave (option 06), for All HS-Gears.
- Software
  - New Opt.M-PHYTX Transmitter Automated Solution (Opt.DJA is pre-requisite).
  - New PGY-UPRO Protocol Decode (Opt.ST6G optionally required).
  - New PGY-LLI Protocol Decode (Opt.ST6G optionally required).
  - Opt.M-PHYRX Receiver Automation (Opt.ERRDT is pre-requisite).
  - Opt.SR-810B, for 8b-10b Decode
  - MPHYVIEW, for DigRFv4 Protocol Decode
  - Optional: Opt.M-PHY Essentials based on DPOJET
  - Optional: SerialXpress for custom-patterns using AWG



P7380 probe used with a probe-tip

- Fixtures
  - As MIPI is chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected. For live-setups: No Fixtures required. For non-live setups UNH-IOL Termination boards expected to be available soon

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M-PHY Rx Recommended Test Setup – Continued

- Recommended Accessories, for opt.M-PHYRX Receiver Automation setup
  - 2x Matched pair of SMA cables
  - 1x GPIB Cable
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors

- Optional: Accessories for Rx “custom-patterns” using SerialXpress (manual setup)
  - 2x Matched pair of SMA cables, , for AWG custom patterns creation
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors
  - 2x BiasTee (part number 5542 from Pico Second), for AWG Interleave Option (for HS-Gear3)
  - 2x TCA-SMA Connectors, for AWG custom patterns creation
  - Option 01 –Memory expansion to 64 M enabled on AWG
  - Option 08 – Fast Sequence Switching enabled on AWG
  - Option 09 – Subsequence and Dynamic Jump enabled on AWG.

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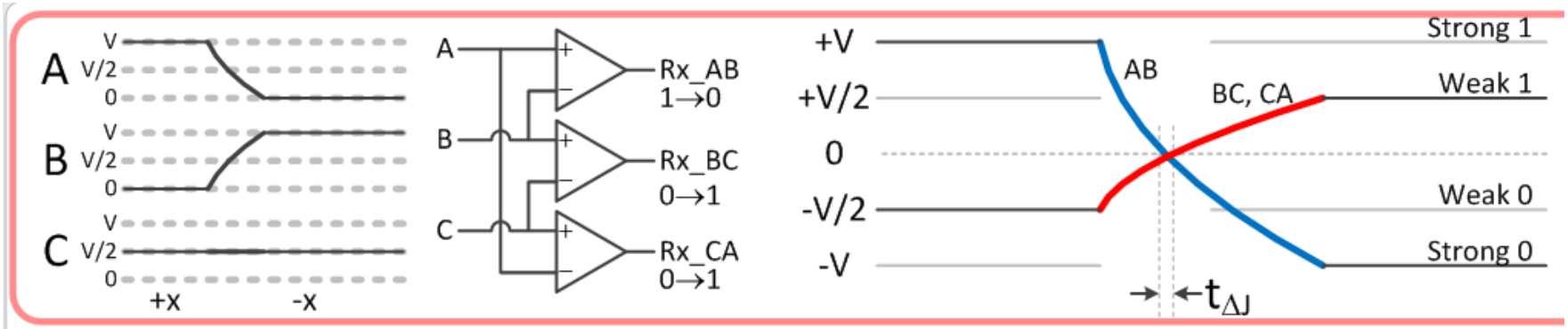
CPHY Solution Offering in 2014-15 - Details

- Scope analysis software
- 4-lane probing & termination board
- New solder-in scope probe tips
- AWG pattern and stress software – C-PHYXpress
- Python automation conformance software
  - Source TX
  - Sink RX
  - RF switch control
- 4-lane pattern generator
- 1-lane scope-based packet decoder
- 4-lane protocol analyzer

CPHY Signal Levels

- VA, VB, VC
  - HS Line Voltage { High, Low, Mid }
  - { V, 0, V/2 }

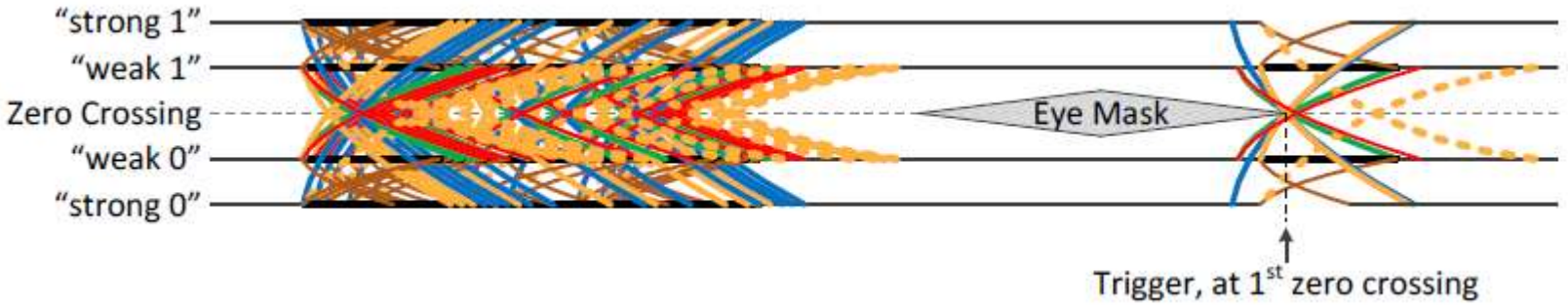
- VAB, VBC, VCA – Differential Signals



Source: MIPI Workgroup Proceedings

CPHY Eye Diagrams

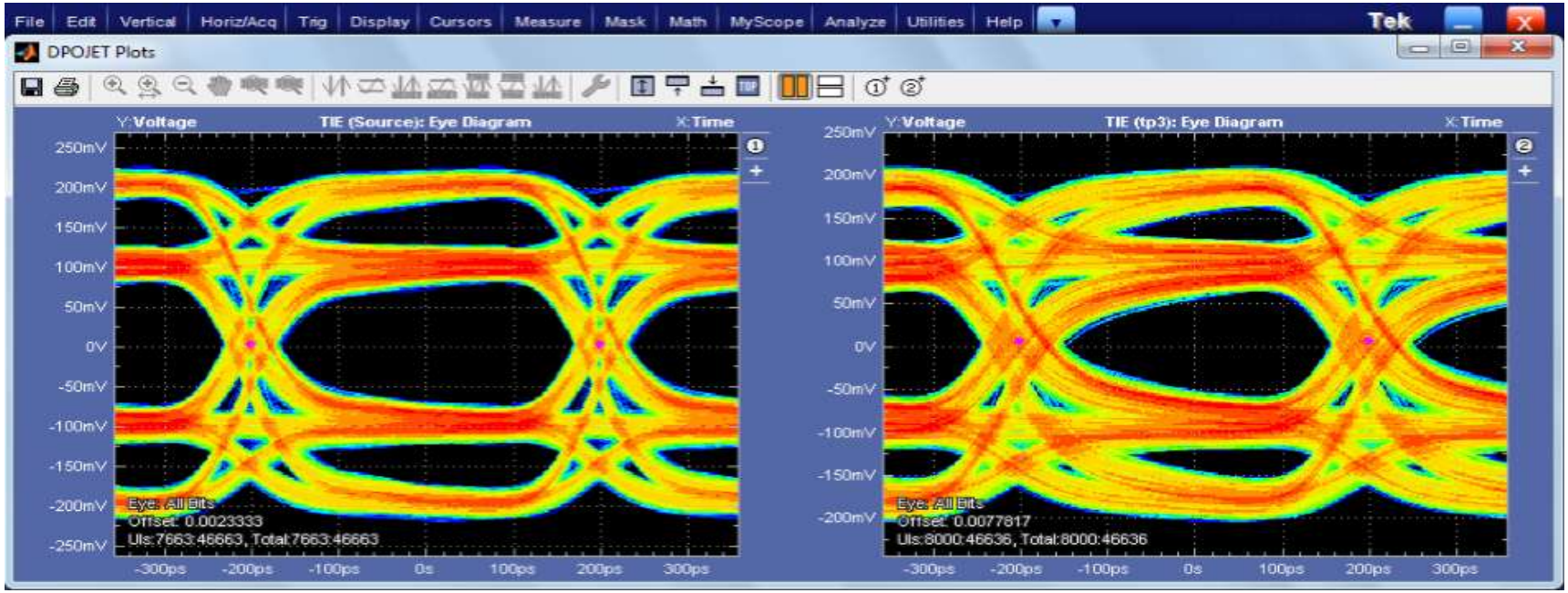
- CPHY uses a “triggered eye” method to render eye diagrams for analysis
  - Specified to model how three CPHY differential receivers work
- “Trigger” refers to the first crossing of Vab, Vbc, or Vca across the 0V threshold per UI
- This “trigger” is used as a reference point for plotting the eye diagram



Example:

Embed Results Verification

- Results can be quickly verified by using DPOJET jitter & eye diagram software
- CPHY analysis is then performed on these signals in accordance with spec requirements.



Before embed

After embed

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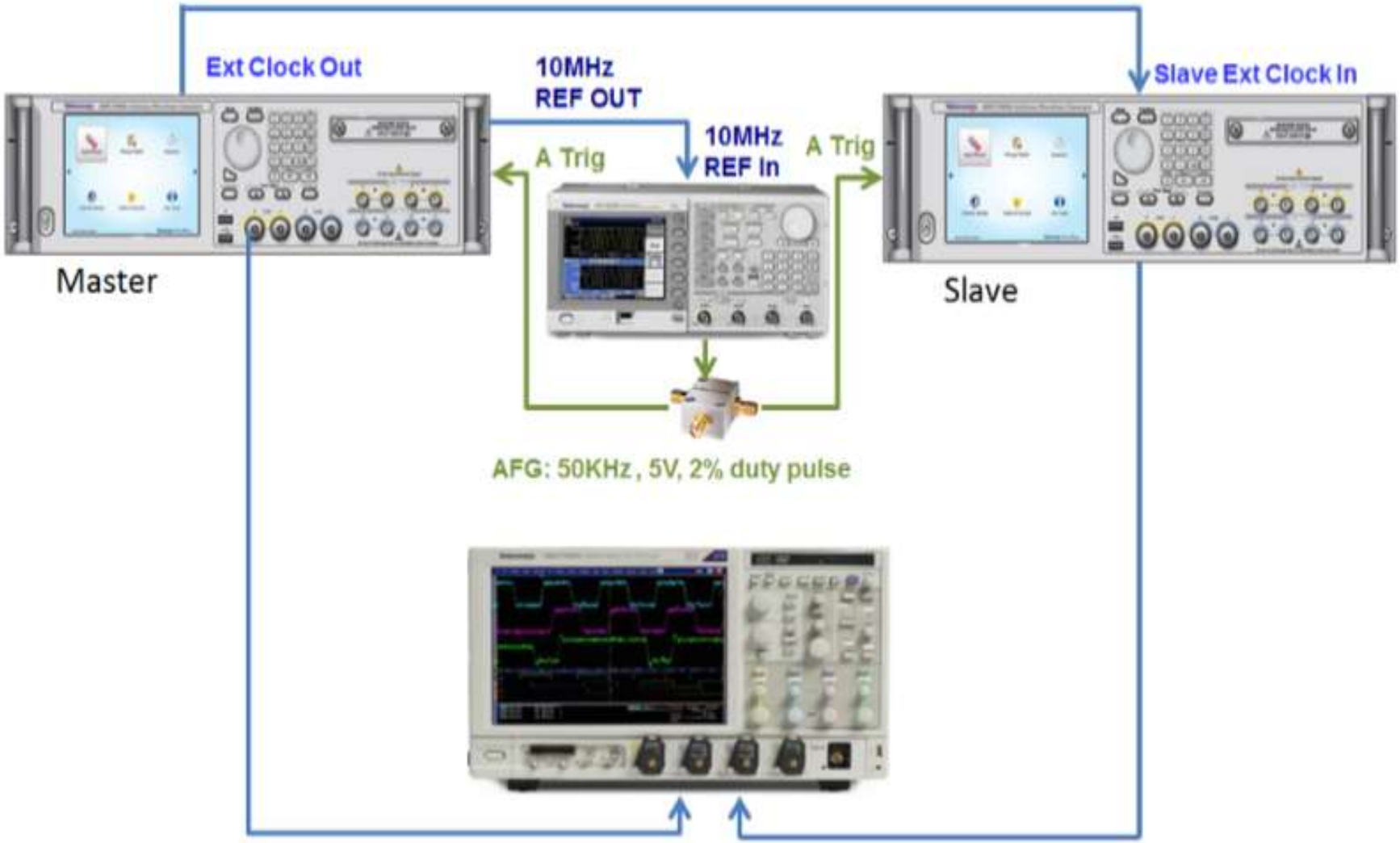
Example Setup Dual AWG70000



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Generate CPHY Traffic

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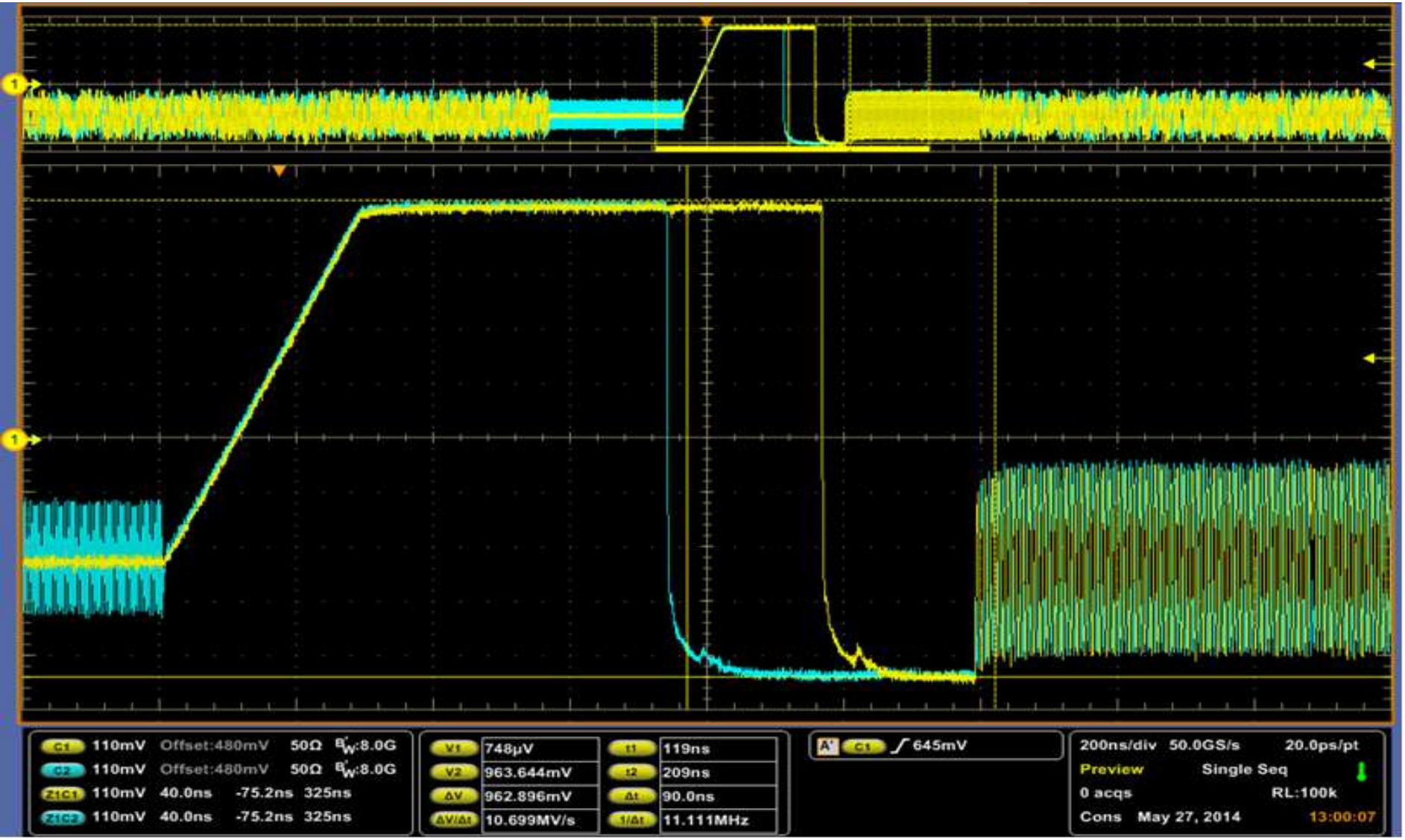
LP-HS Transition – (LP swing 0V up to 1V, HS swing 50mV up to 435mV)



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Thanks !

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