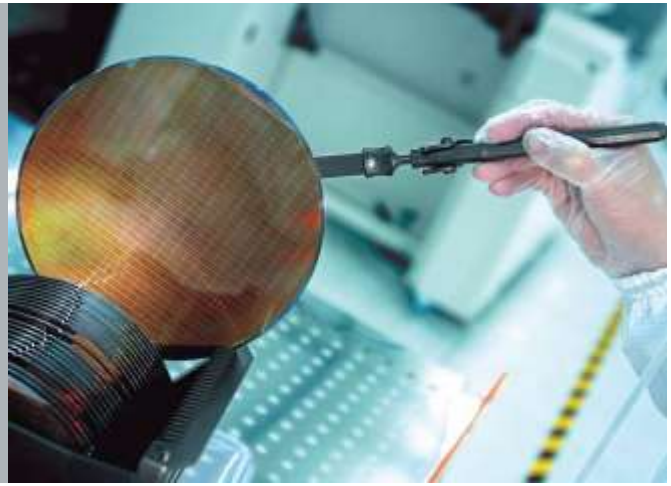
HDMI2.0 Solution



Tektronix®

Agenda

- HDMI Overview and updates
- Additional resources

Tektronix®

HDMI –High Definition Multimedia Interface

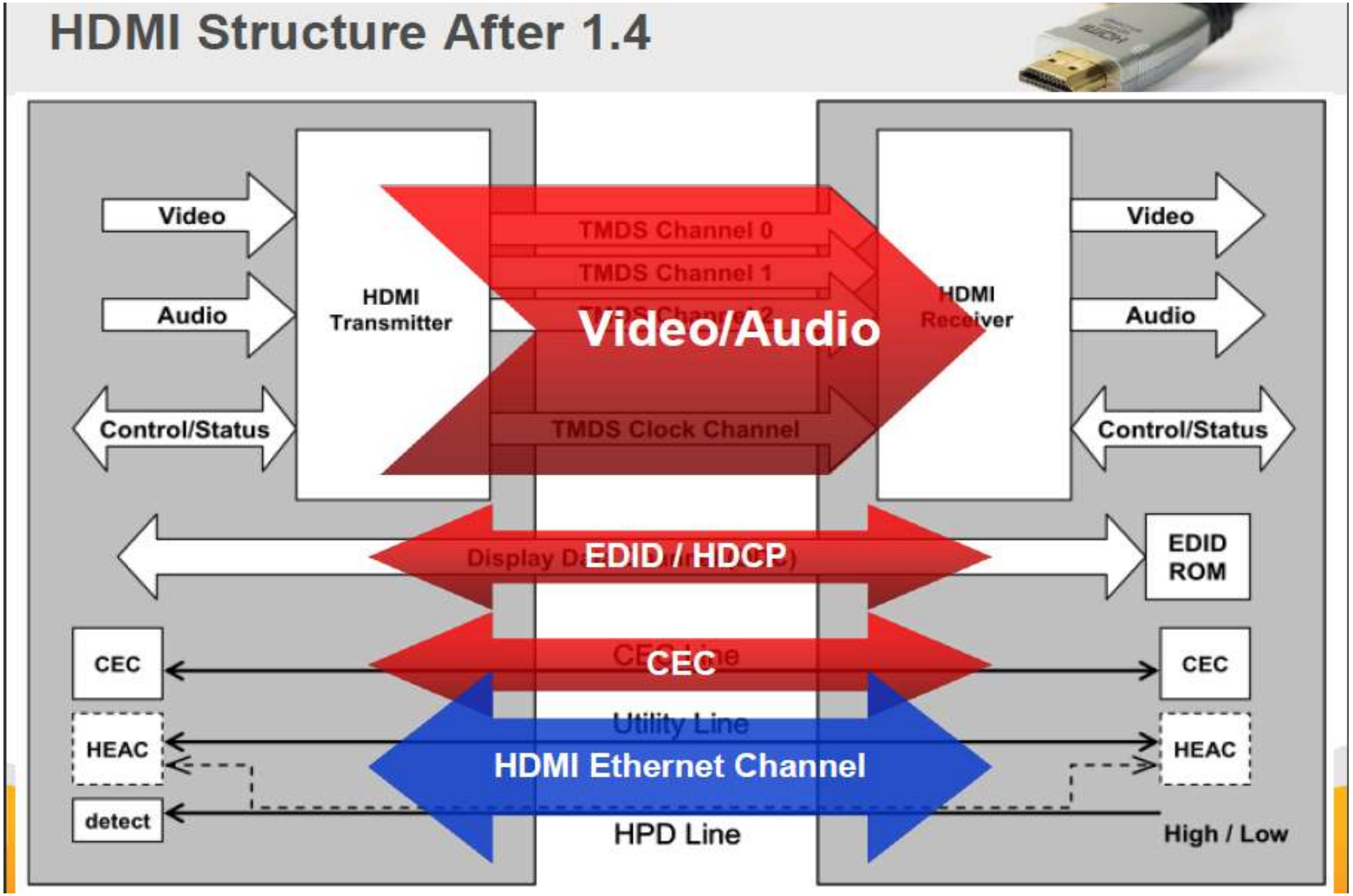
Overview of HDMI

- From 2003 till date and looking ahead…
  - Tek only solution provide for HDMI from 2003 to 2007
  - Contributor of SoftCRU method to the Specification
  - Innovative Sink solution leveraging Direct Synthesis method of AWG
- Hdmi 1.0 ---- 1.65GBps
- Hdmi 1.4—3.4GBps
- Hdmi 2.0….. 6GBps

HDMI™
HIGH-DEFINITION MULTIMEDIA INTERFACE

Tektronix®

HDMI Basics


HDMI Structure After 1.4
Video
Audio
Control/Status
HDMI Transmitter
TMDS Channel 0
TMDS Channel 1
Video/Audio
TMDS Clock Channel
HDMI Receiver
Video
Audio
Control/Status
EDID / HDCP
EDID ROM
CEC
CEC
CEC
Utility Line
HEAC
HDMI Ethernet Channel
HEAC
detect
HPD Line
High / Low

Tektronix HDMI 1.4b Solution- Approved in CTS 1.4b

DPO/DSA/MSO
Real Time Oscilloscopes

AWG5K/B or AWG7K/B
Arbitrary Waveform Generators

DSA8200 Sampling Scope
with i-connect software

Common Set of test equipment for HDMI and HEAC

HDMI Fixtures:

1. Type A(TF-HDMI-TPA-S/-STX)
2. Type C(TF-HDMIC-TPA-S/-STX)
3. Type D(TF-HDMID-TPA-P/-R)
4. Type E(TF-HDMIE-TPA-KIT)
5. HEAC Fixtures(TF-HEAC-TPA-KIT)

Probes and Accessories

HDMI Probes
HEAC Probes
HDMI Accessory Kit

GAME Changer - HDMI Protocol Analyzer

Tektronix®

Tektronix and HDMI Forum

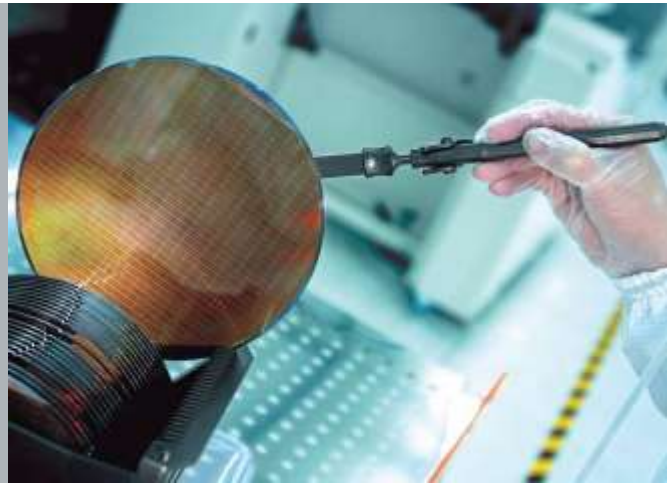
- 89 companies in the HDMI forum as of date. Source HDMI Forum
- Tektronix is member of this HDMI Forum. Actively participating in weekly/monthly calls and face-face meetings
- **Tektronix's U.N.Vasudev is Chairman of HDMI forum test subgroup**
- HDMI Forum has released the HDMI specifications 2.0 version 1.0 on 4th Sept 2013
  - Target
    - CTS 2013 Q4

Tektronix®

HDMI 2.0 features

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60/50 Hz – 594Mcsc**(Mega Characters per Second per Channel**
- Support 4K 2K 4:2:0 – 297Mcsc
- 3D; 21: 9 ; Audio
- Low level Bit error rate testing
- Scrambling is introduced and mandatory for rates >340Mcsc.

System Recommendation for HDMI 2.0 for Source Measurement



Tektronix®

HDMI 2.0 Source Testing Equipment Needs

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.
  - HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps
- P7313SMA probes (same used in HDMI 1.4b)
- Option HDM and HDM-DS
- HDMI 2.0 Fixture set

HDMI 2.0 Source Testing

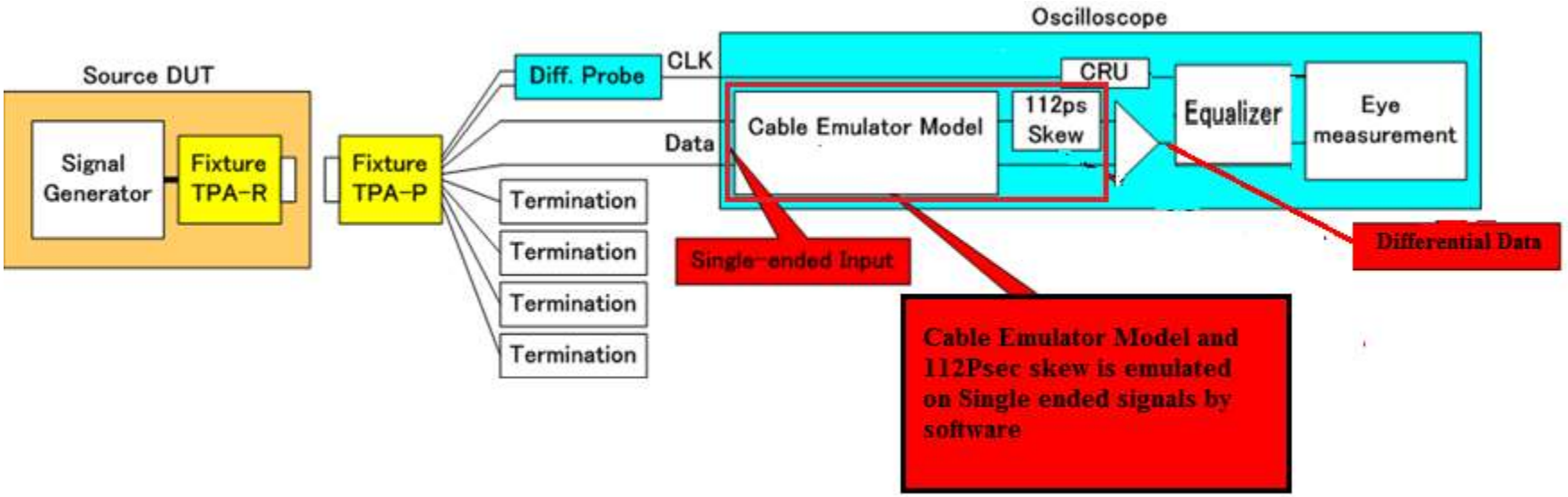
Tektronix®

Source Testing 1.4b Vs 2.0

- Eye Diagram test is now performed at TP2
- Rest of the tests is same as HDMI 1.4b
- 1.4b CTS test is a pre-requsite for HDMI 2.0
- Min 8GHz scope to 16GHz scope
- New Fixtures
- Same Probes
- HDM and HDM-DS Software

Source Testing

- Source Eye Diagram test is measured at TP2_EQ.
- TP2 is the signal after passing along a worst cable.
  - Worst cable has worst attenuation and skew of 112ps.



Tektronix®

Source Electrical Tests

Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – V_L

Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – T_{RISE}, T_{FALL}

Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew

Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage

Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle

Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter

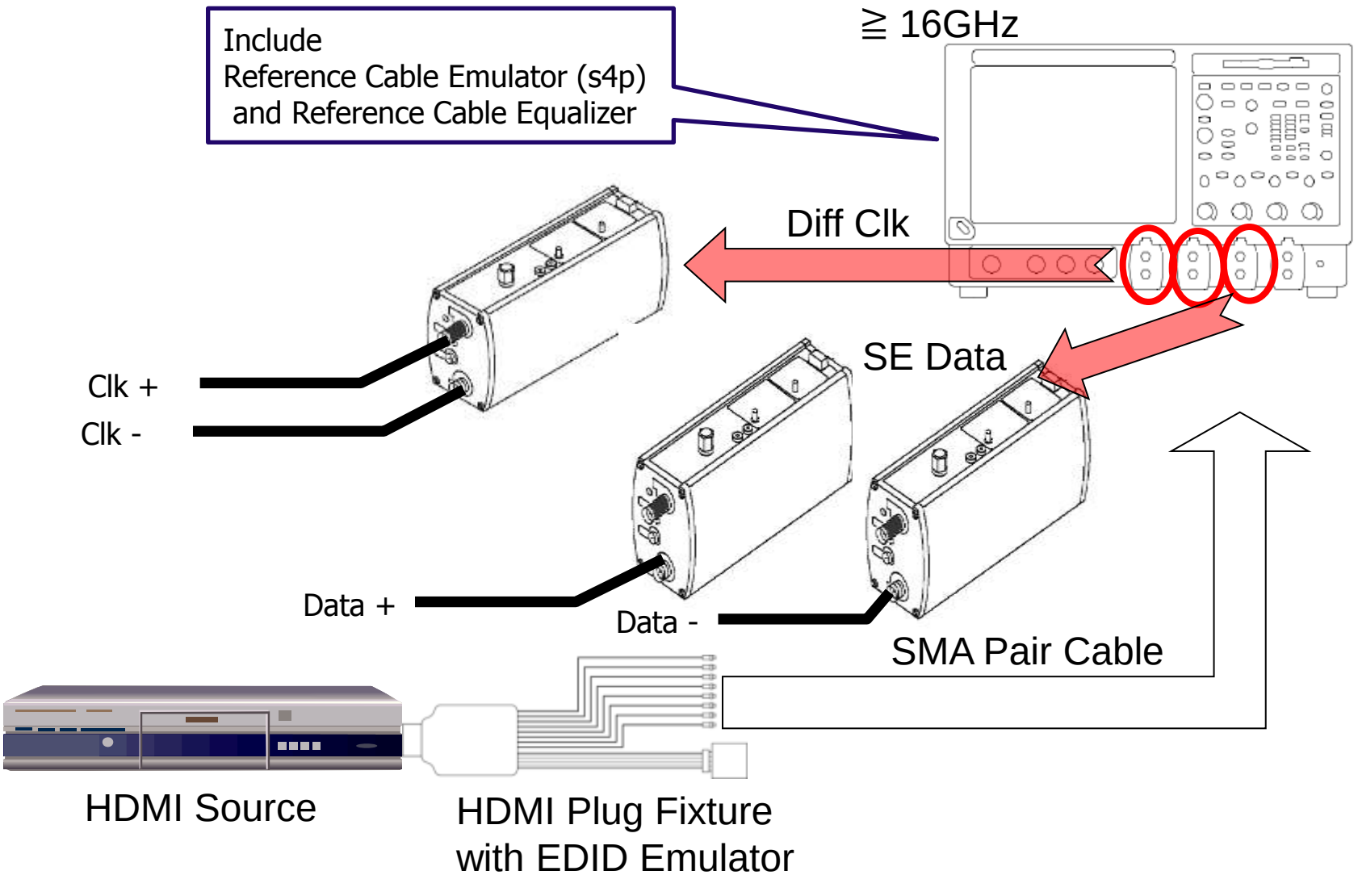
Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram

Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance (to be performed using sampling scope)

Tektronix®

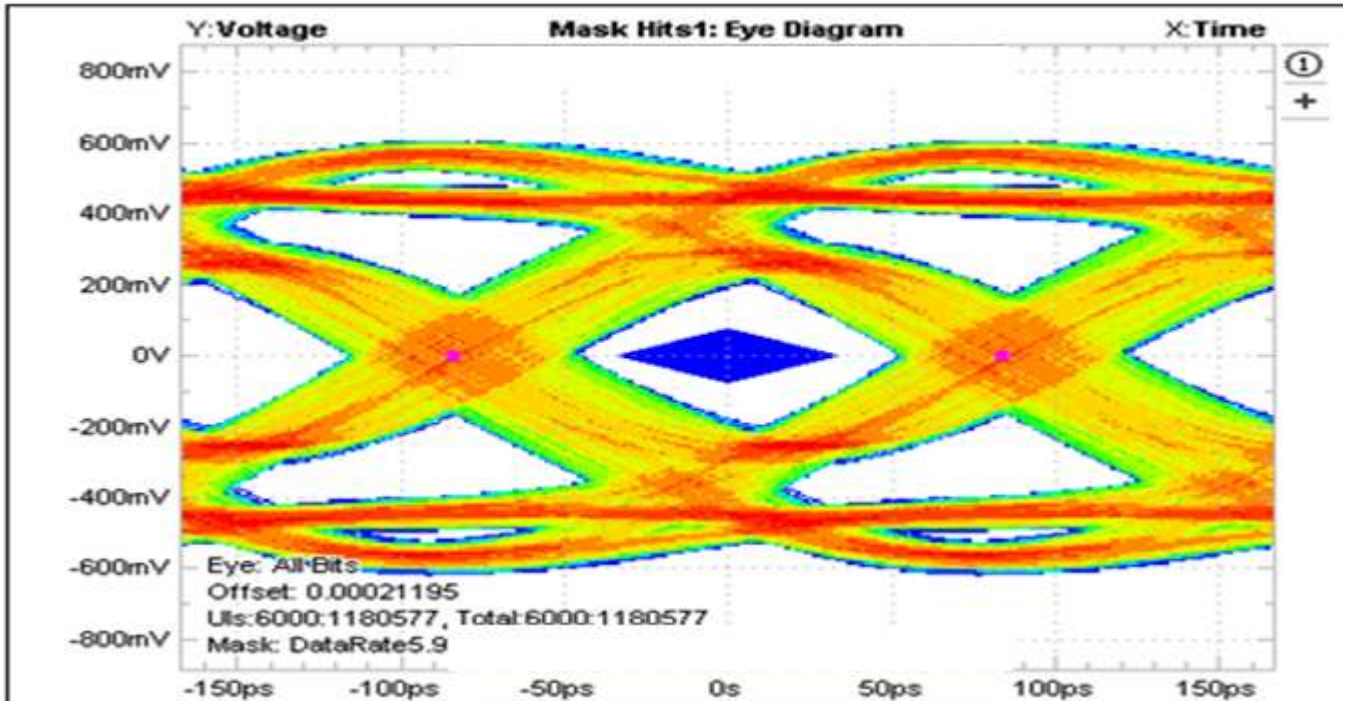
Source Eye Diagram Test

Tektronix Oscilloscope
DPO/DSA/MSO70000 Series
≧ 16GHz



Tektronix

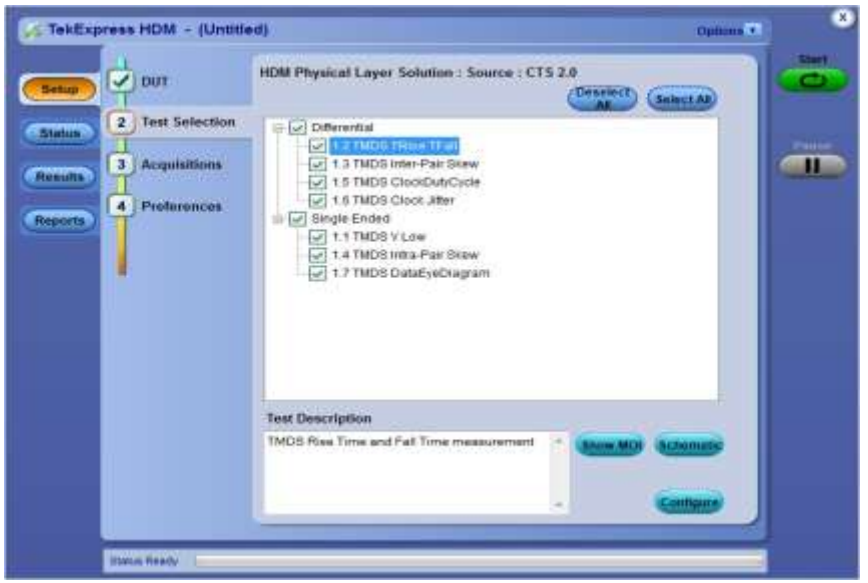
TP2 Source Eye for HDMI 2.0 6G Signal

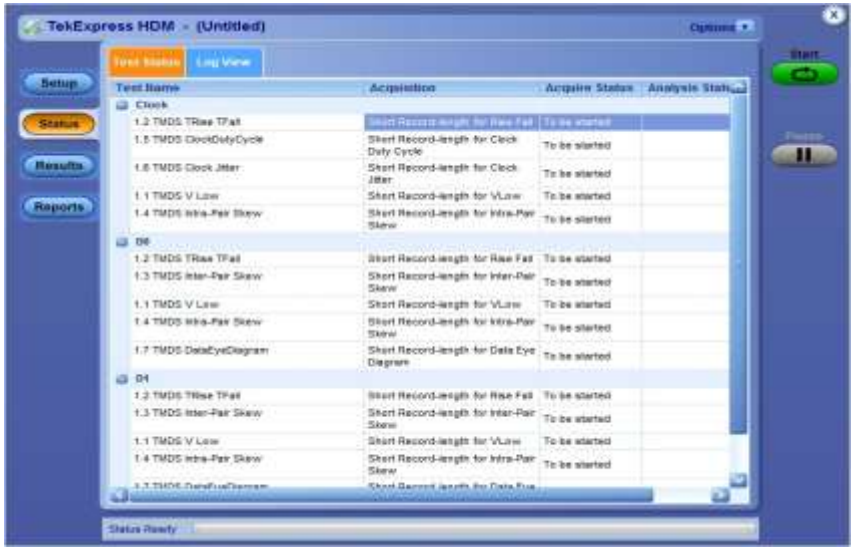


Single End Input eye rendered at Tek lab

Tektronix®

HDMI 2.0 Tx Compliance Software





Tektronix®

HDMI 2.0 Sink Testing

Tektronix®

HDMI 2.0 Sink testing Equipment needs

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 Sink testing for Jitter Verification/Calibration/Controller.
- P7313SMA probes
- Option HDM and HDM-DS
- HDMI 2.0 Fixture set
- 2# AWG7122C with Opt 01,02 or 06, 08 for **HDMI 2.0 Compliance only setup**.

OR

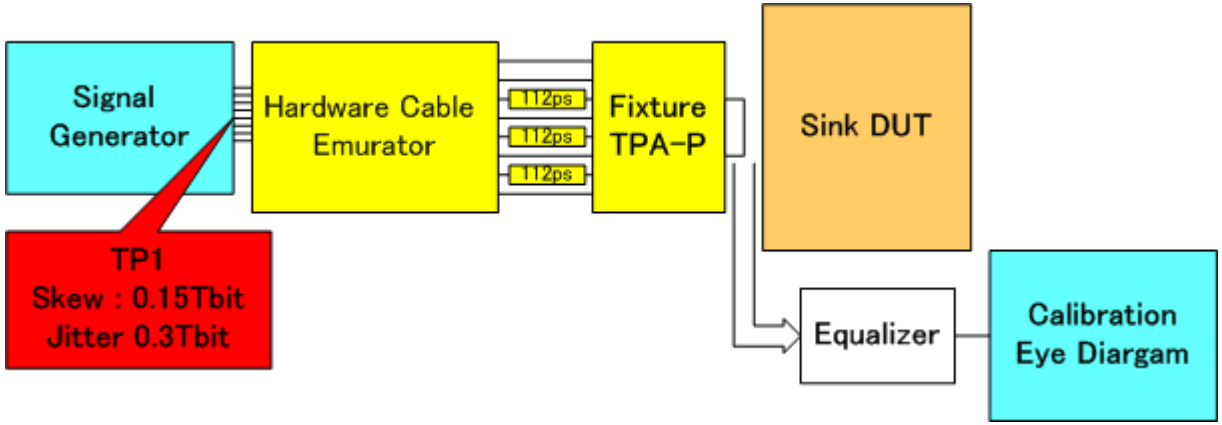
- 2# AWG70002A with Opt 01,03 and 225 for **HDMI 2.0 Compliance and Margin Test setup.(Margin test feature will be available later and is part of roadmap**)

Note- We shall also support a 12.5GHz BW scope which would result in appx. 10% inaccuracy in RT/FT results .

Tektronix®

Requirement for Signal Generation

Cable Emulation and Skew by Hardware



Hardware Skew and Software Cable Emulation

Sink Electrical tests

Test ID HF2-1: Sink TMDS Electrical – 340-600Mcsc – Min/Max Differential Swing Tolerance

Test ID HF2-2: Sink TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

Test ID HF2-3: Sink TMDS Electrical – 340-600Mcsc – Jitter Tolerance

Test ID HF2-4: Sink TMDS Electrical – 340-600Mcsc – Differential Impedance (performed using sampling scope)

HDMI 2.0 Rx solution positioning statement

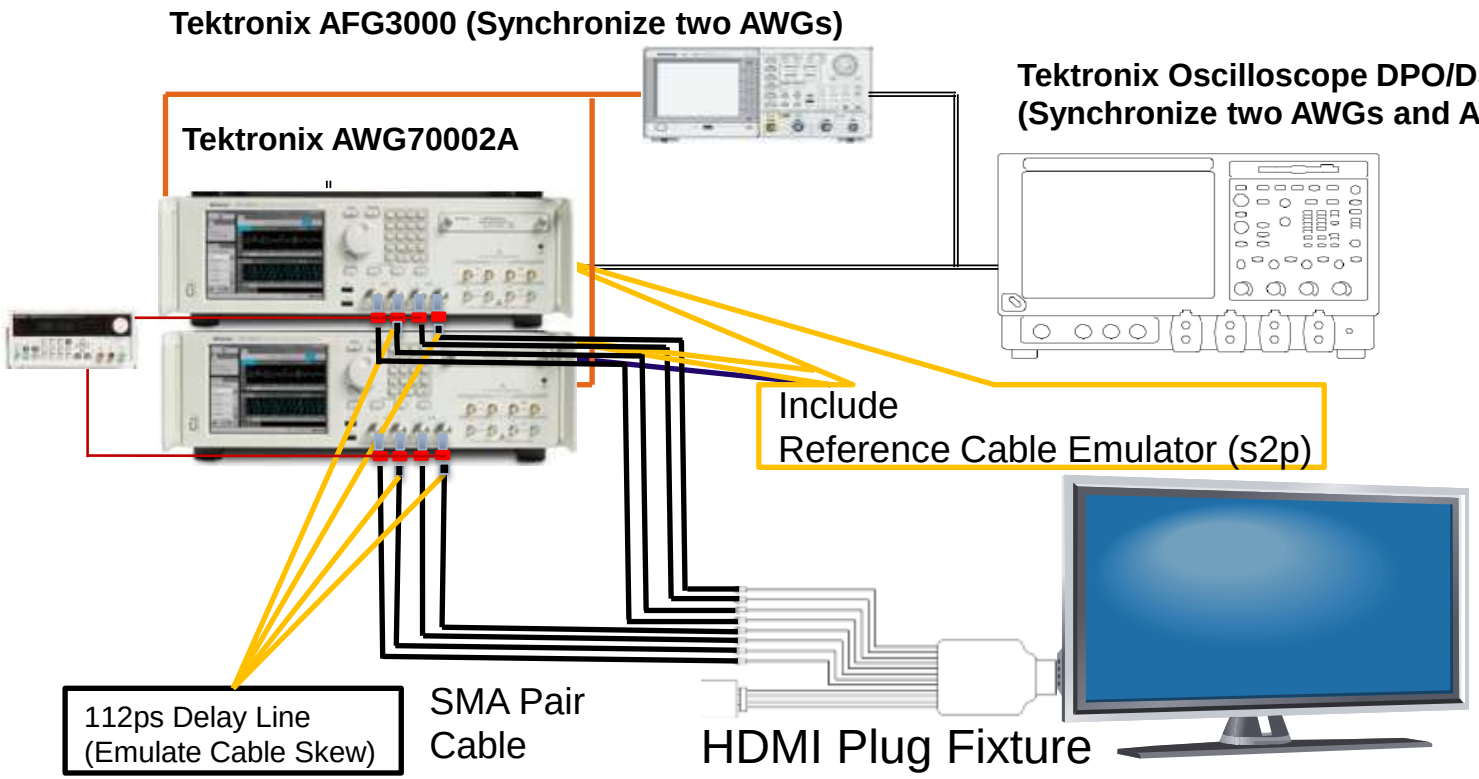
- Tektronix will support HDMI 2.0 Sink Electrical and protocol tests using either AWG7122C (w/ Opt 01,02/06,08) AND AWG70002A (W/ Opt 01,03 ,225)
- Solution Positioning:
  - **Compliance solution** for HDMI 2.0 Rx
    - 2# AWG7122C with opt 01, 02/06 and 08
    - 1# AFG3102/C

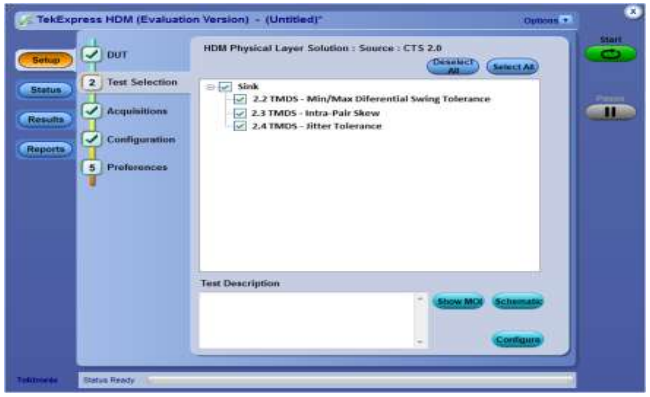
  Customers can use common test setup for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution.

  - **Compliance and Margin solution** for HDMI 2.0 Rx
    - 2# AWG70002A with Opt 01,03 and 225.
    - 1# AFG3102/C

  Customers can use common test setup for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution

HDMI 2.0 Sink Test Setup

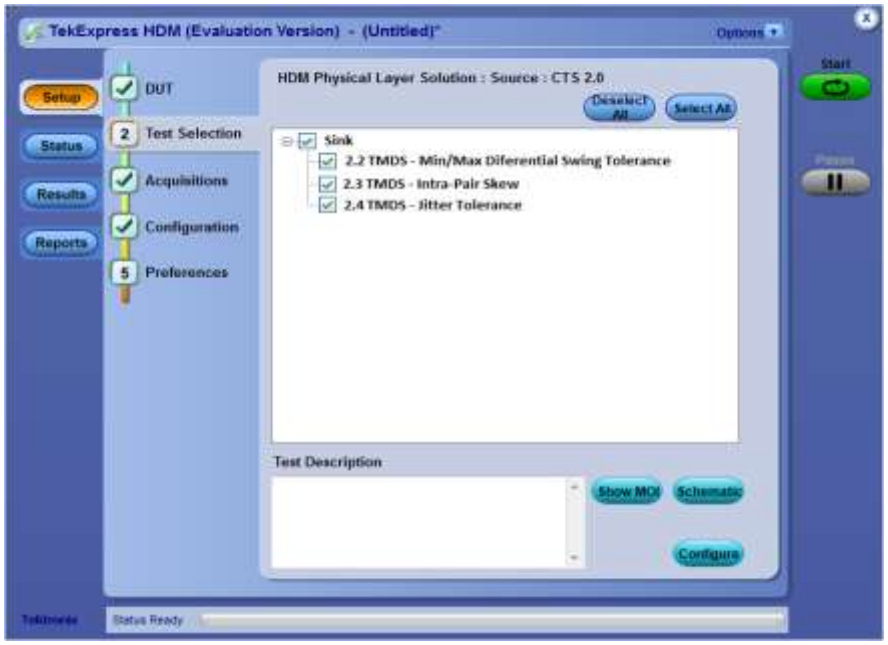




Sink Testing 1.4b Vs 2.0

- Jitter Tolerance test needs +ve and –ve lanes tested with 112ps delay line
- Rest of the tests is similar to HDMI 1.4b tests
- 1.4b CTS test is a pre-requsite for HDMI 2.0
- Need AWG 70002A for HDMI 2.0 Compliance and Margin needs while AWG7122C is suitable for HDMI 2.0 Compliance testing only..
- Min 8GHz scope to 16GHz scope
- Fixtures and Probes
- HDM and HDM-DS Software

HDMI 2.0 Rx Compliance Software



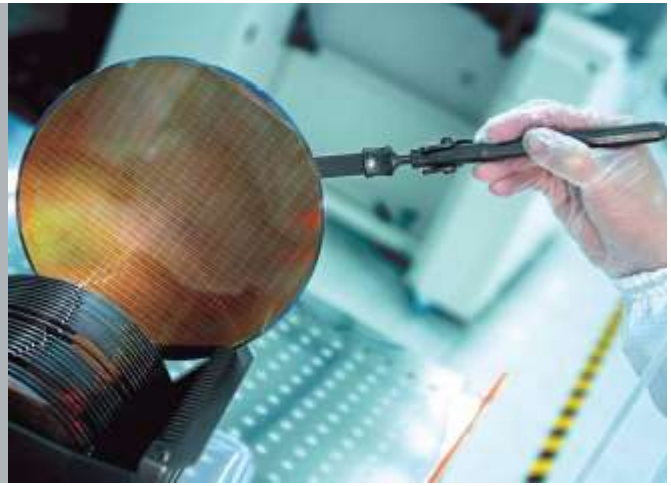
Tektronix®

Tektronix HDMI 2.0 Solution

- Tektronix HDMI 2.0 Solution will be available aligned to the CTS announcement from the new HDMI Forum.
- Full Source Test Solution including probes, Fixtures.
- Phased Rx Electrical solution- ensuring regular engagement with customers with pattern support added to solution.(between Dec 2013 to June 2014)
  - Release 1 HDMI 2.0 Sink Electrical tests HF2-1; HF2-2 and HF2-3 with the following VIC supported: (Dec MOI)
    - VIC 96,VIC97, VIC 101, VIC 102 ,VIC 106, VIC 107
  - Release 1 Sink Protocol test HF2-23 supported (Dec MOI)
  - Release 2 – 1H CY14 – remaining VICs for electrical tests- Target for next MOI approval event (Q1 CY14)
  - Final Release - Phased Rx Protocol solution- ensuring regular engagement with customers with pattern support added to solution.(starting by Q1 CY14 and complete by end 2014)
- Support for HDMI 1.4b CTS is a pre-requiste for HDMI 2.0 testing.
- Contact local Tektronix sales team for early interaction on our HDMI 2.0 solution.

Tektronix®

Introduction to USB 3.0 SuperSpeedPlus

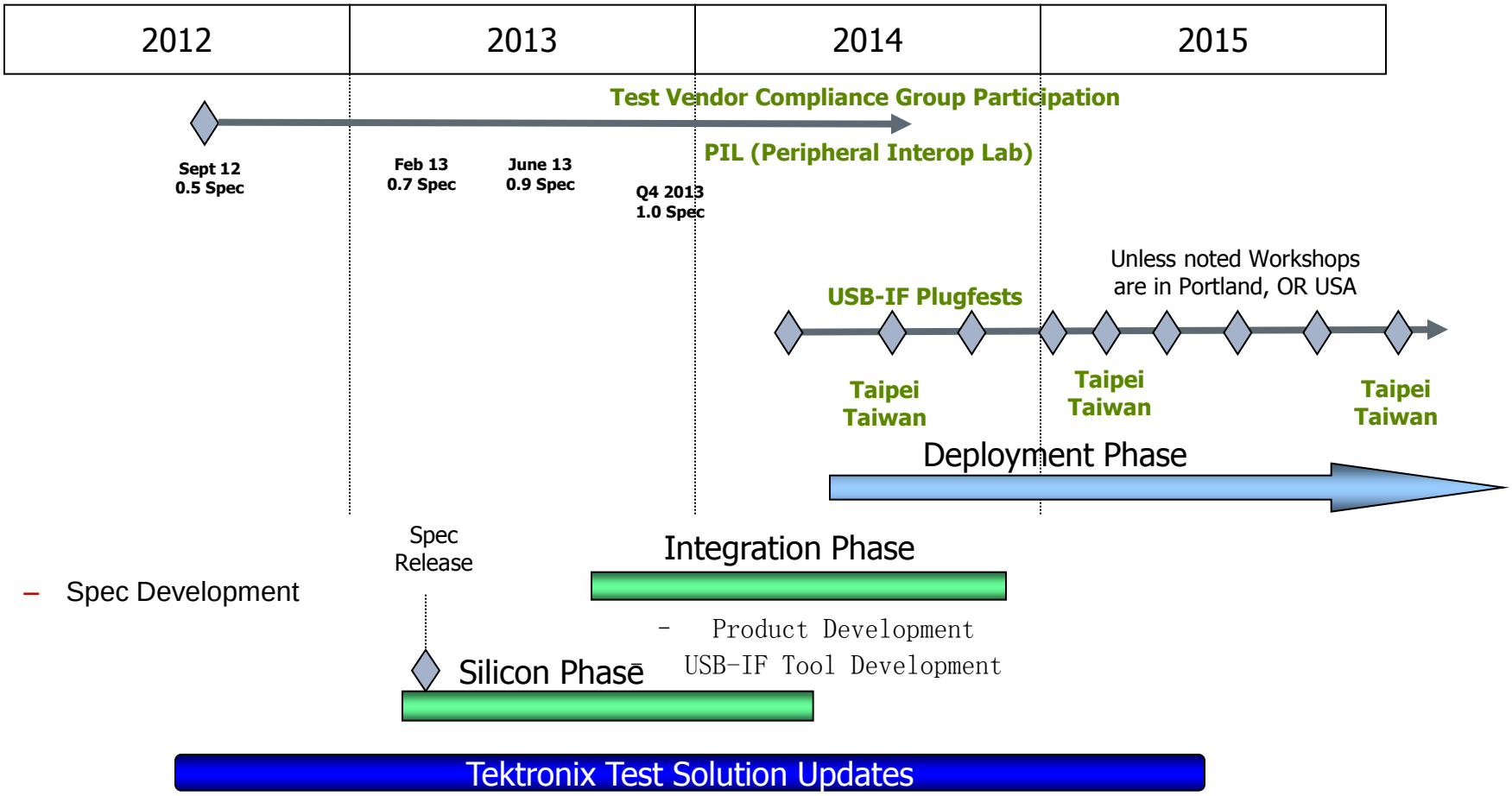


Tektronix®

Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging
- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture
- **USB 3.0, 10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation

USB 3.0 SuperSpeedPlus Technology Timeline



Transmitter, Receiver, Channel

Tektronix®

Why 10 Gb/s?

Video

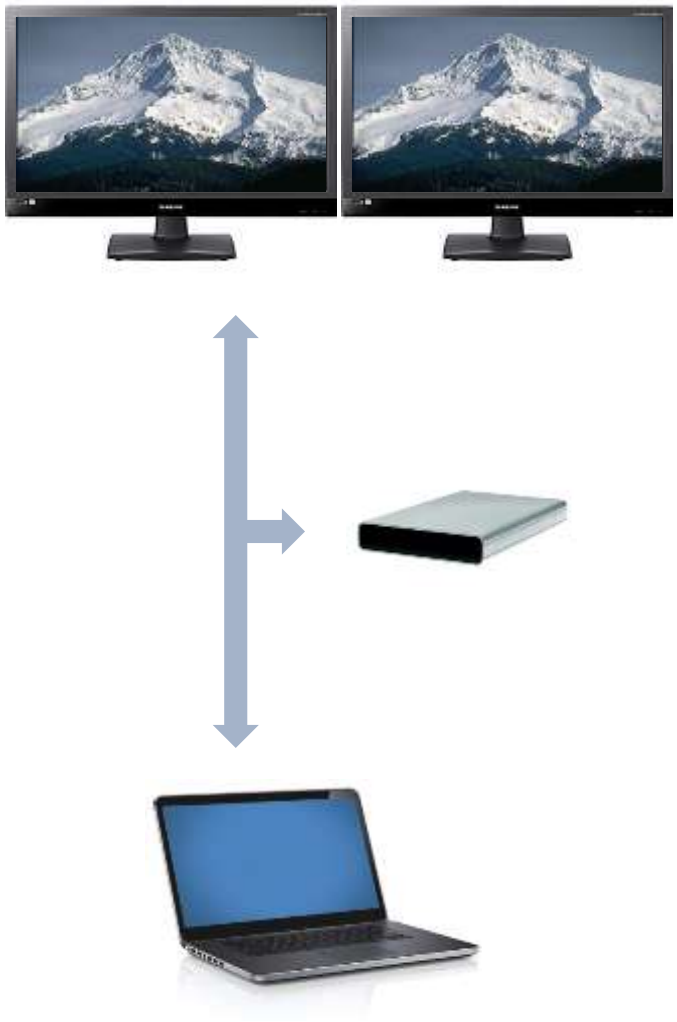
- HD video adapters with multi display outputs
- Dual HDMI/DVI with simultaneous 1080p displays

Storage

- 5 Gb/s with 8b/10b -> 400 MB/s
- High performance SSD saturation-> ~600 MB/s

Hub/Dock

- Multi-function, ‘All in One’ docking
- Faster backups, multiple monitors, etc.



Tektronix®

5 Gb/s Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

6 Physical Layer

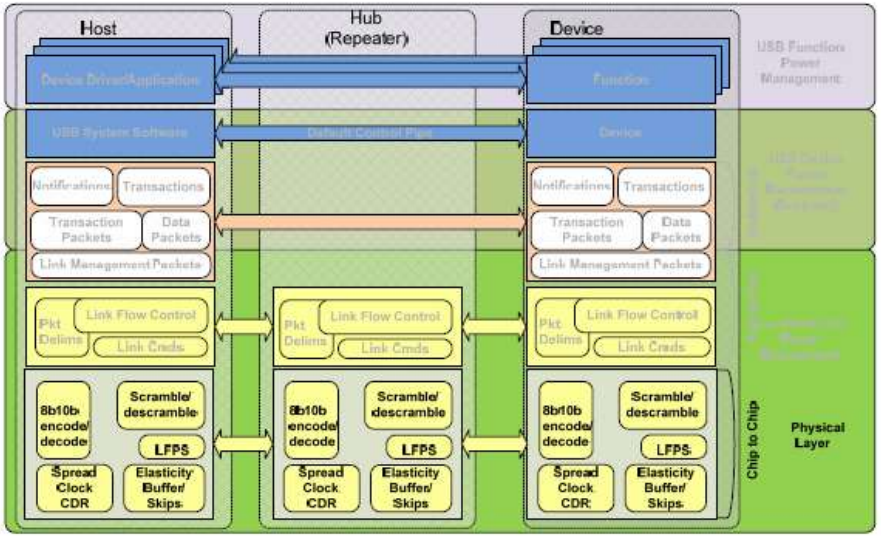


Figure 6-1. Super Speed Block Diagram: Physical

Source: USB 3.0 Rev 1.0 Specification

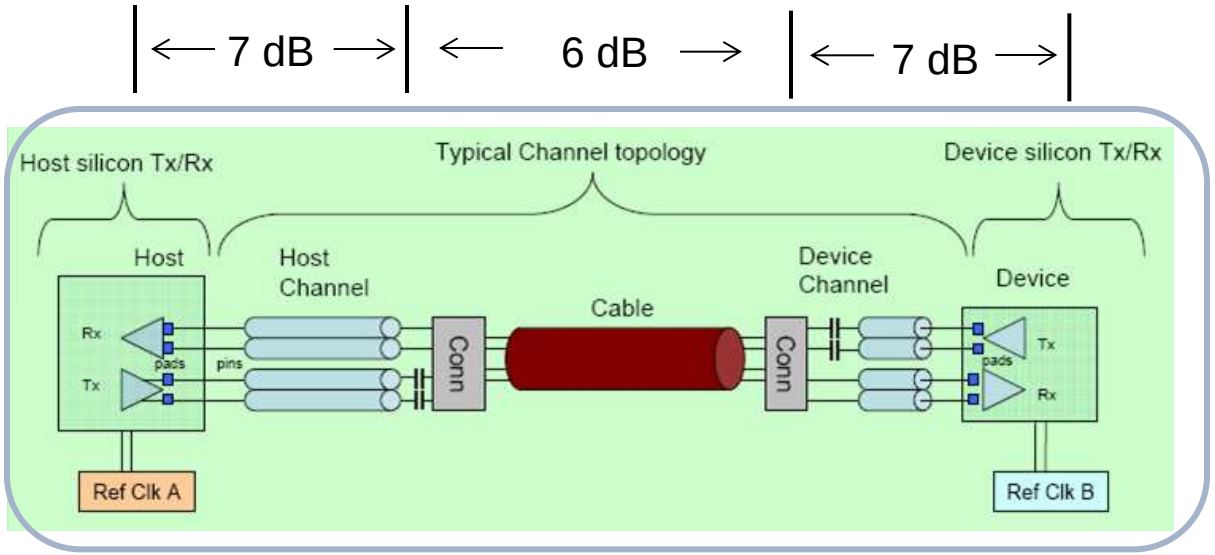
Tektronix®

10 Gb/s Comparison

	SuperSpeed	SuperSpeedPlus
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-20dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

Channel Budget

- Target 20 dB (5 GHz) end-to-end loss budget
- Transmitter Equalization
  - < 3.5 dB (short channel), minimal loss profile
  - ≥ 3.5 dB (long channel), need Tx optimization
- Repeater may be required if host/device loss > 7 dB
- Tx/Rx compliance at TP1 (far end)



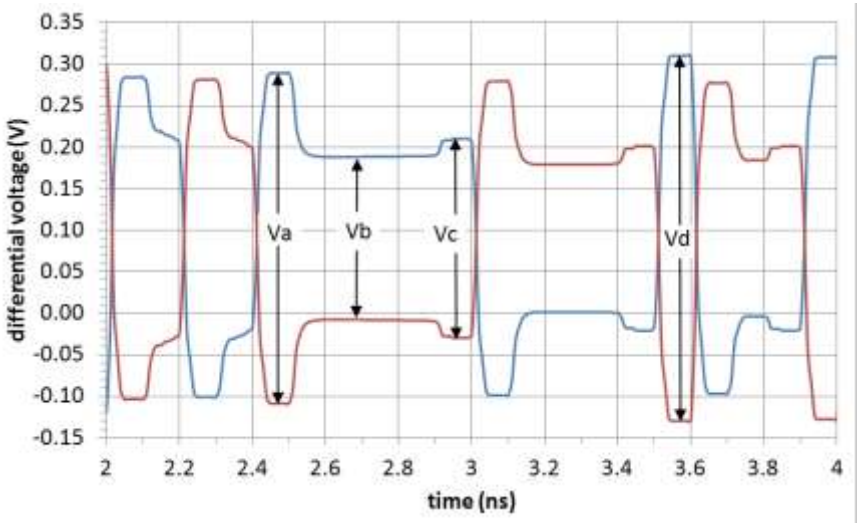
Source: USB 3.0 Rev 1.0 Specification

Tektronix®

Reference Transmitter Equalization

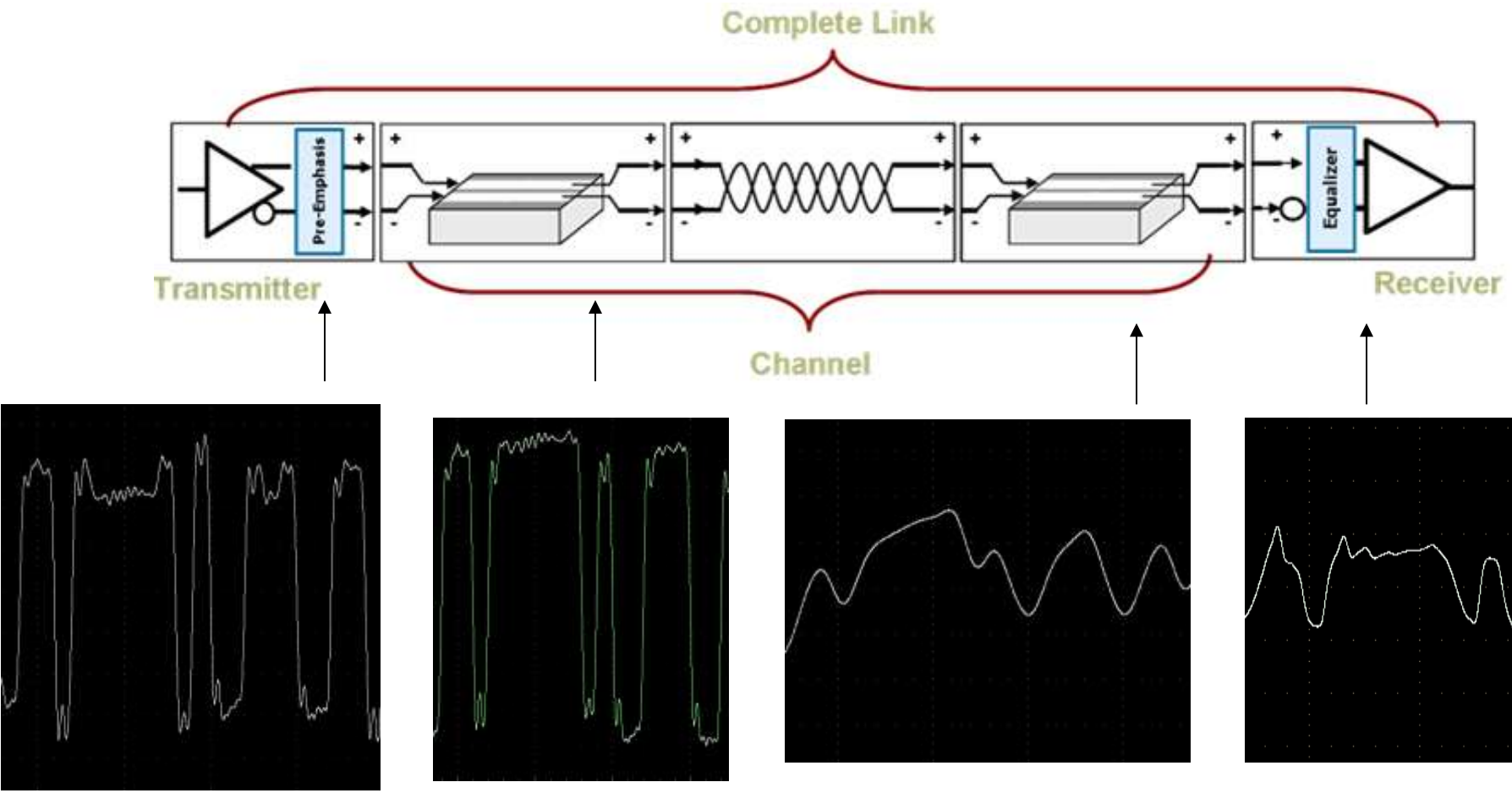
- USB channel profiles are dynamic (consumer)
- Need flexible solution space for link optimization
- Below are recommended Tx settings for good margin with target reference channels

Host/Device Loss	<3.5dB	≥3.5dB
C_{-1}	0.000	-0.125
C_1	-0.100	-0.125
Va/Vd	1.00	0.80
Vb/Vd	0.75	0.55
Vd/Vd	0.75	0.75



Tektronix®

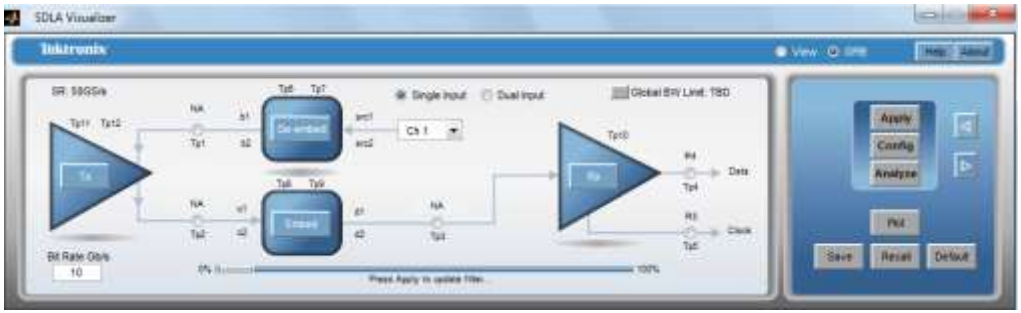
End-to-end PHY Validation

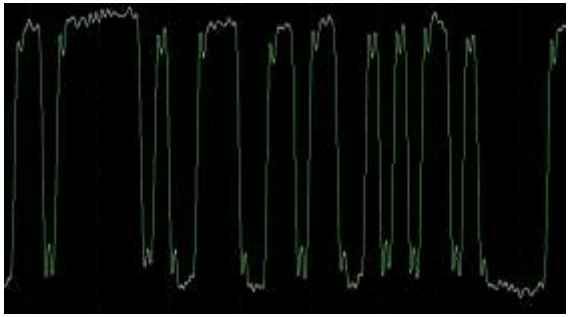


Tektronix®

Transmitter Validation Example - SDLA

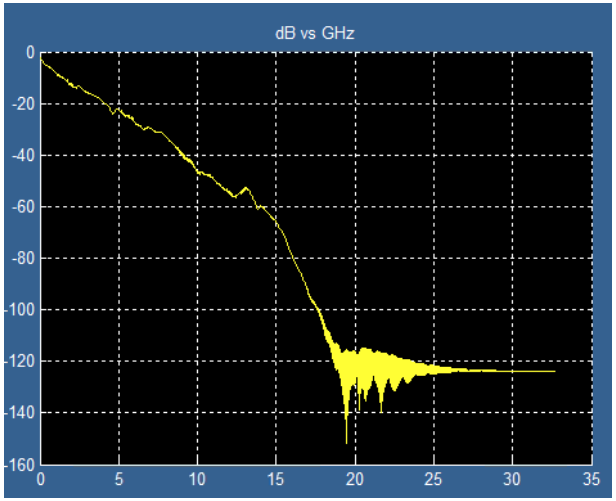
- Capture CP9 (Scr0) and CP10 (Ah)
- Input reference channel models

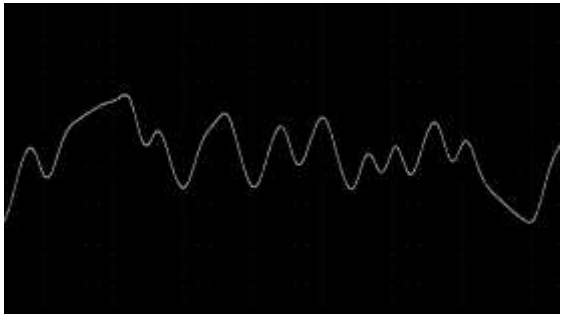




CP9 Scrambled Pattern (TP0)

USB3 Reference Channel



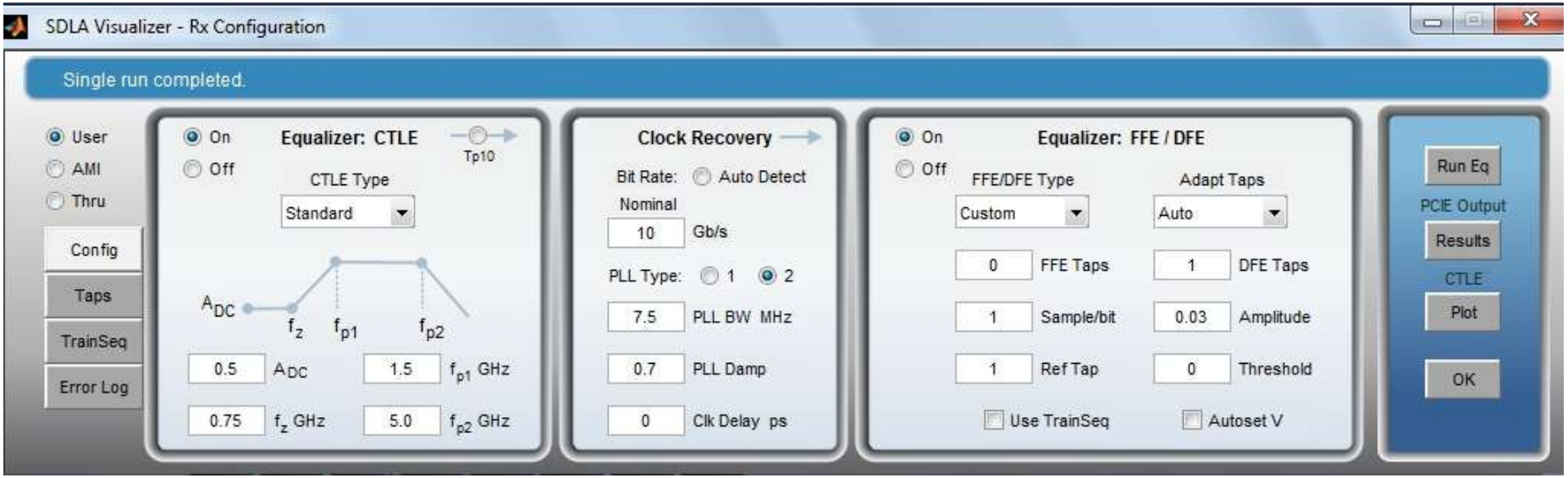


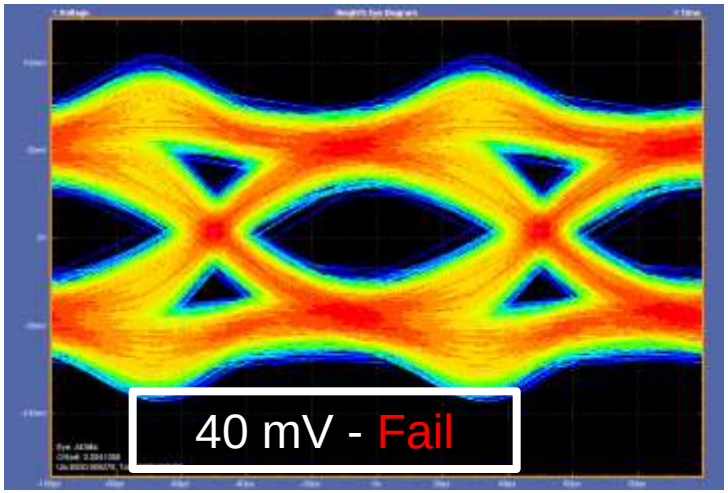
CP9 Scrambled Pattern (TP1)

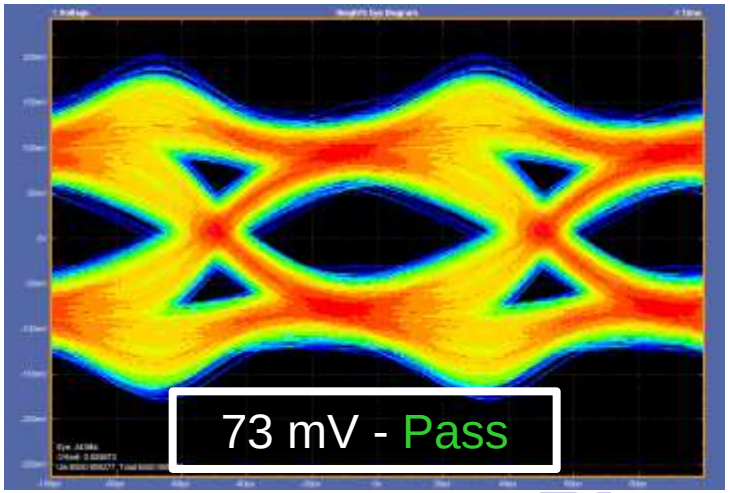
Tektronix®

Transmitter Validation Example - SDLA

- Find optimum Eye height vs. Rx EQ



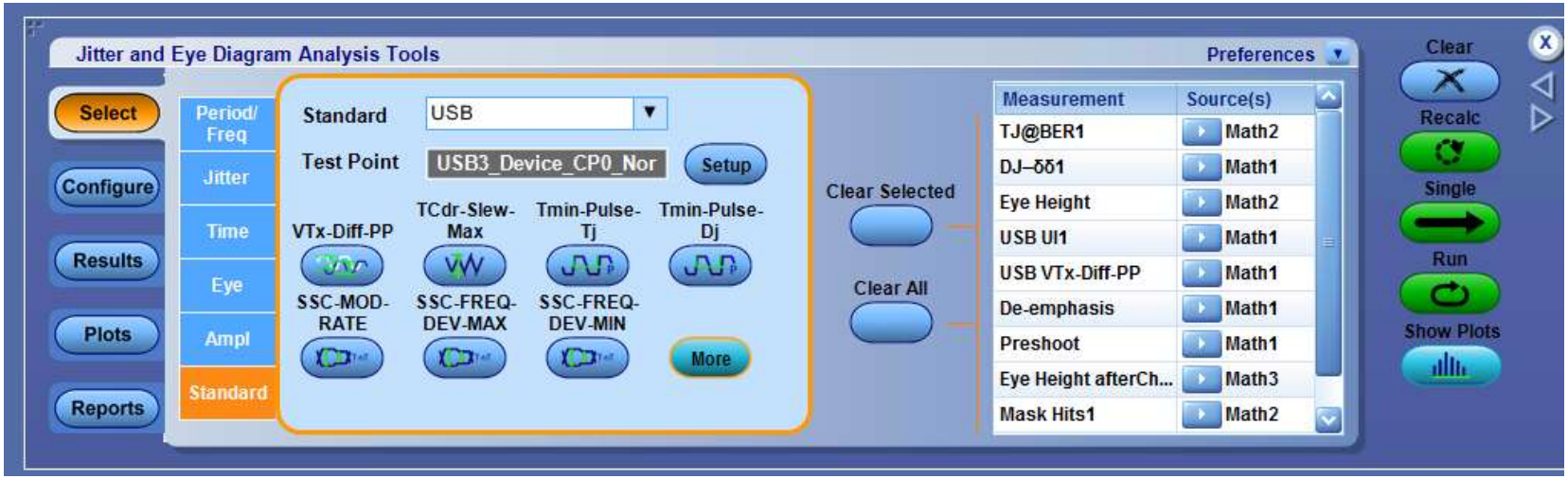




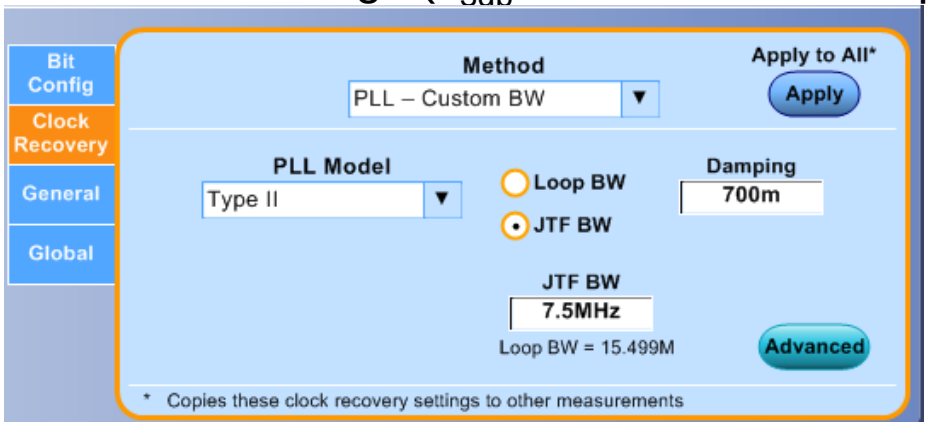
Tektronix®

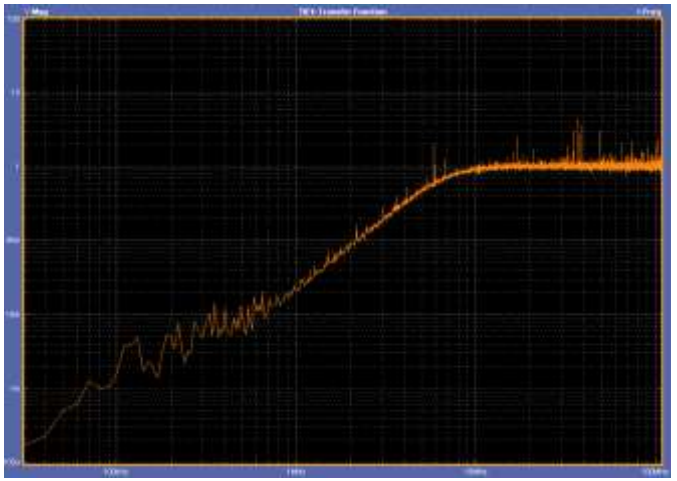
Transmitter Validation Example - DPOJET

- Recall DPOJET SSP setups



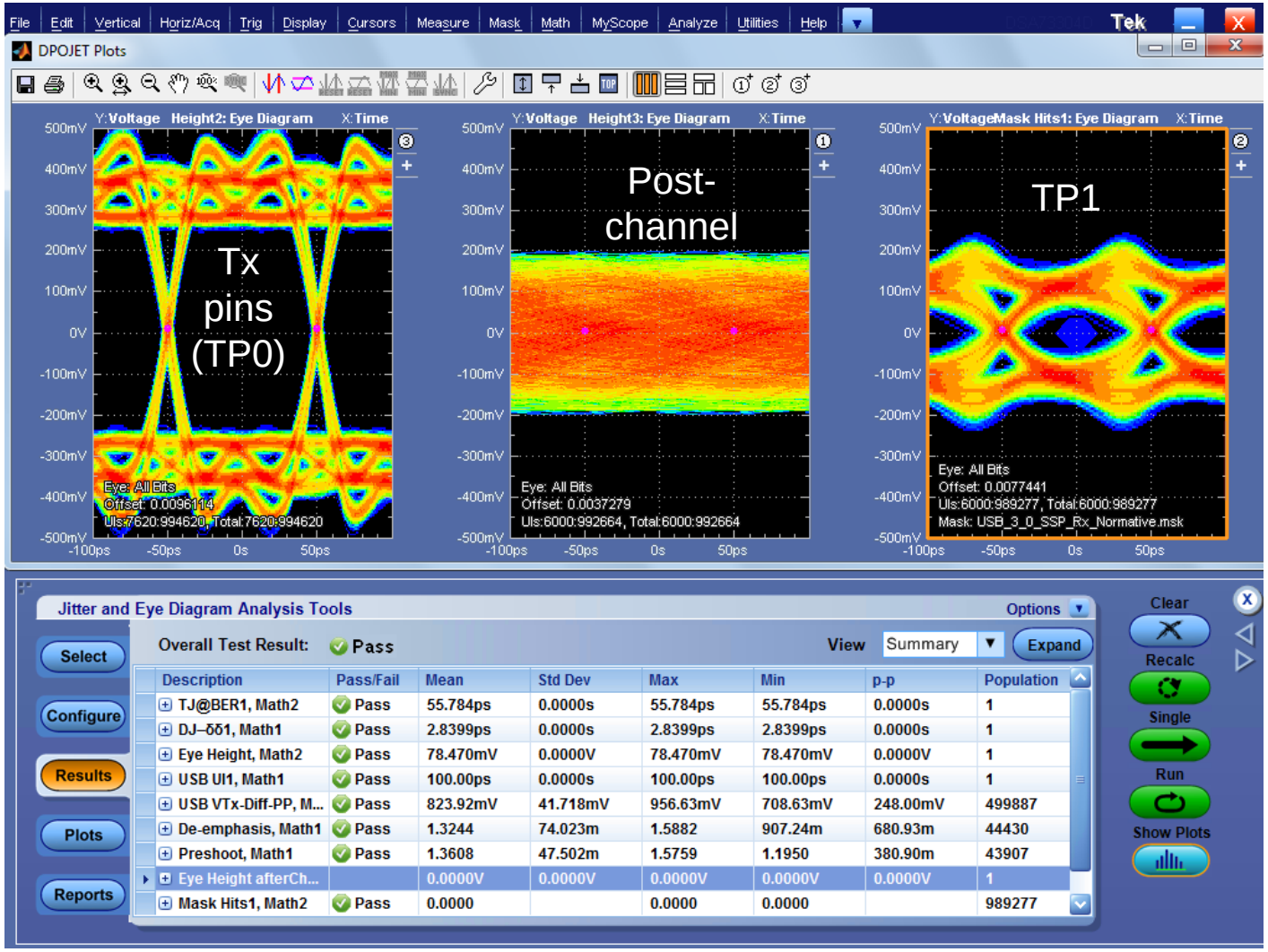
- Check JTF settings (f_{-3db} 7.5 MHz, 40dB slope)





Transmitter Validation Example - DPOJET

- Measure Eye height and jitter at TP1



Tektronix®

Recommended Transmitter Solution

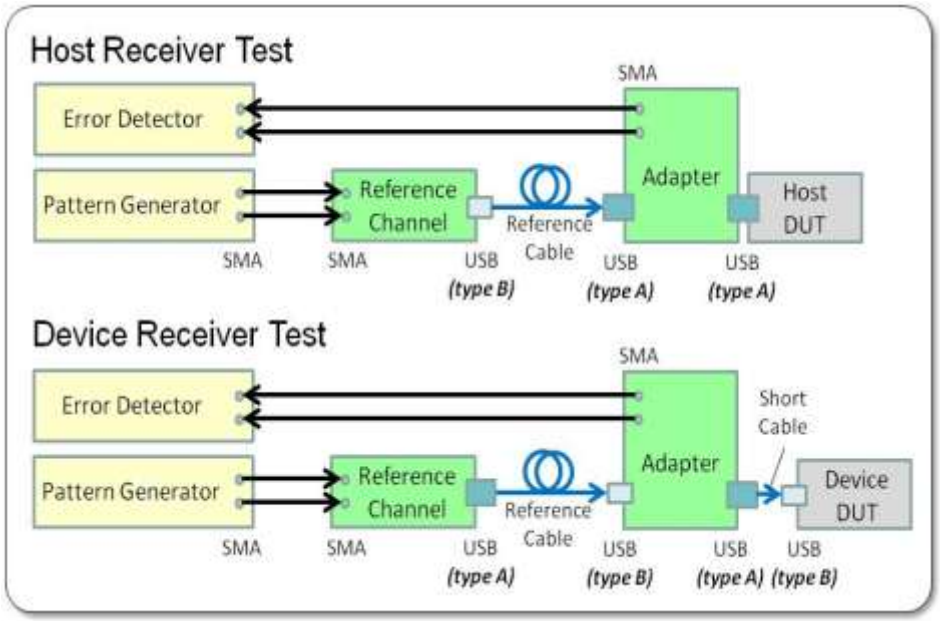
- ≥20 GHz BW, 100 GS/sec preferred
  - DSA72004C minimum required, DSA72504D or greater preferred
- >10M minimum record length allows capture of 1M UI at 100Gs/sec, no interpolation. Increase memory depth if interpolation will be enabled, or if >1MUI captures are desired.
- Option DJA Advanced DPOJET required, signal analysis
- Option SLA Advanced SDLA required, cycle through 7 CTLE/1 DFE settings
- Option USB3 recommended, provides USB3 TX specific measurements

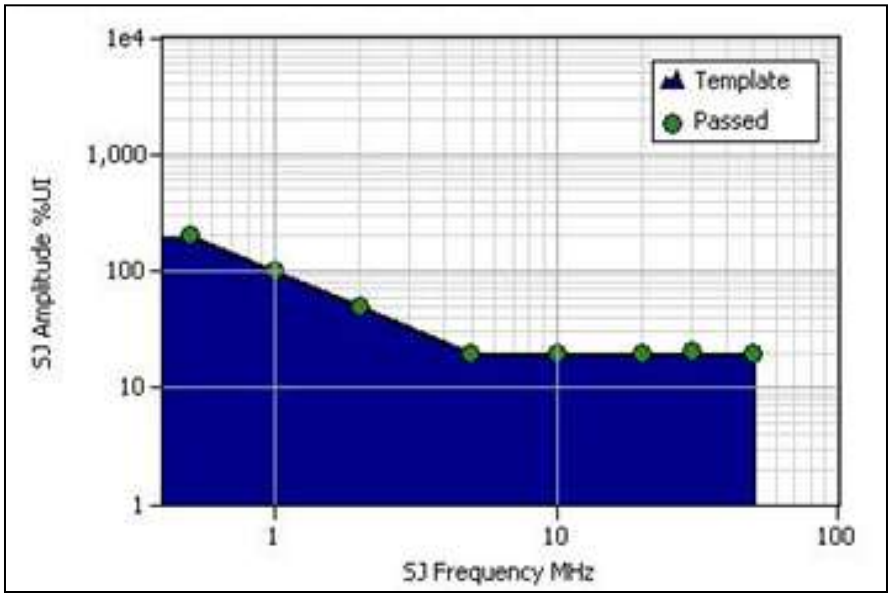
For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.

Tektronix®

Receiver Testing

- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions





Tektronix®

JTOL Template Comparison (TBD)

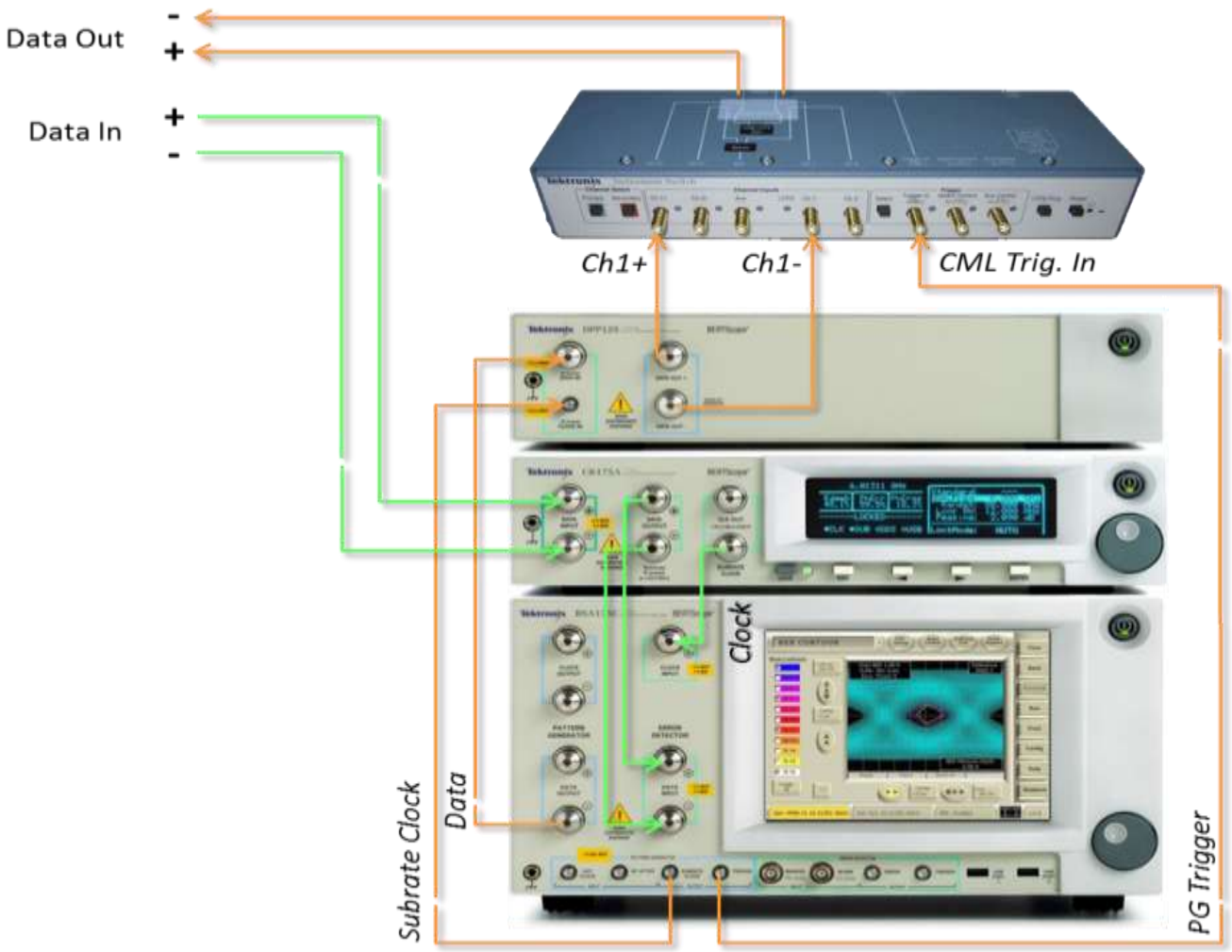
Symbol	Parameter	Gen 1	Gen 2	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	.184	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	2.56	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	1.28	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.64	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.32	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	TBD	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.7 Post= -3.3	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-1

Tektronix®

BERTScope USB 3.0 RX Test Configuration



USB Switch
creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

DPP125C
De-emphasis Processor

CR125A
Clock Recovery

BSA125C
BERTScope

Tektronix

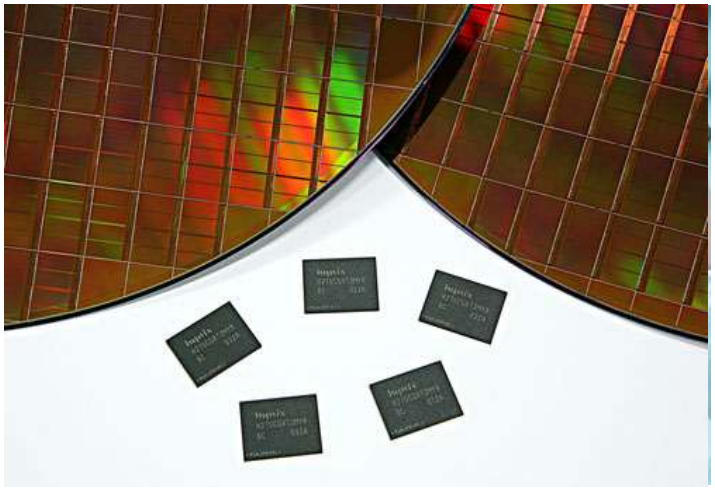
Summary

- New opportunity for growth with USB 10 Gb/s
- Adds additional challenges beyond legacy requirements (backwards compatibility)
- Higher performance, more complex design but feasible within current infrastructure
- Extensive PHY validation tools for early designs
  - New USB SSP DPOJET setups for Tx validation
  - BERTScope USB library with JTOL templates
  - DSA8300 Sampling oscilloscope for channel characterization
  - Test procedures documented in Methods of Implementation (MOI)

Tektronix®

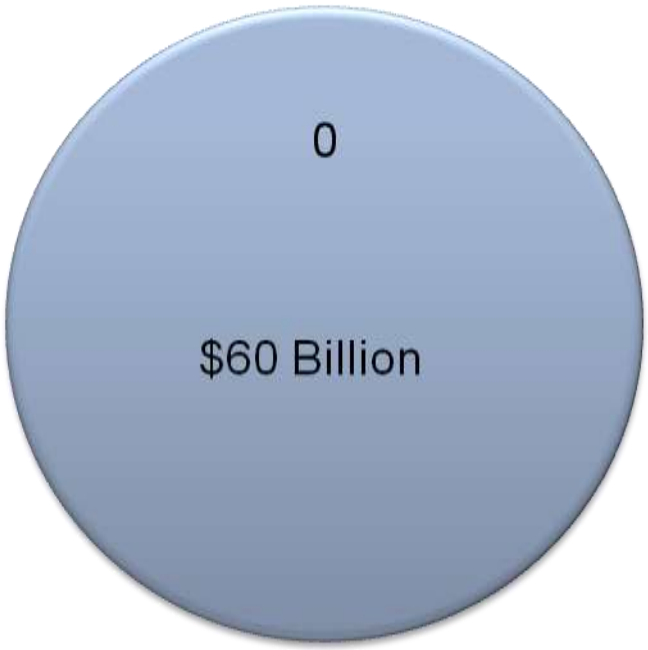
Debug and Validation of Flash Memory Interface

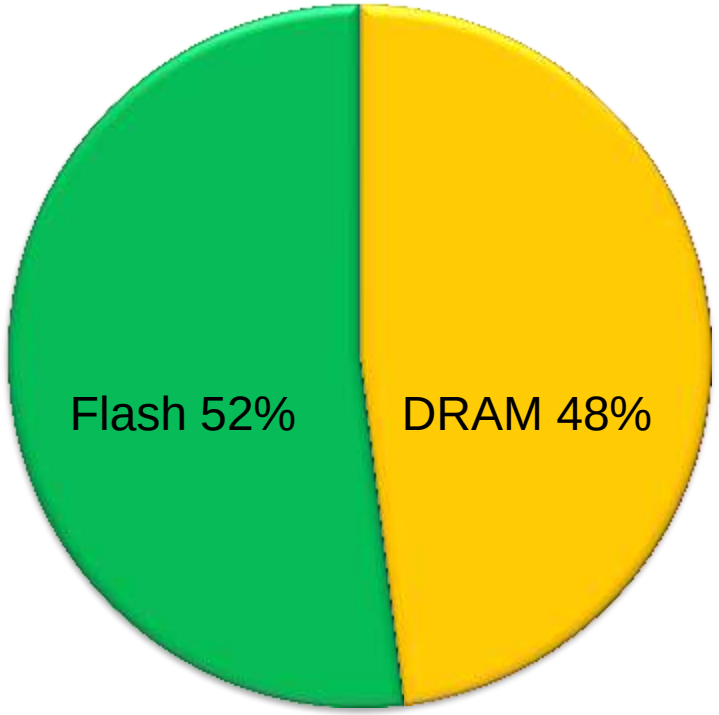
Measure the Analog signal characteristics and Protocol Level Details on the flash Memory Interface



Tektronix®

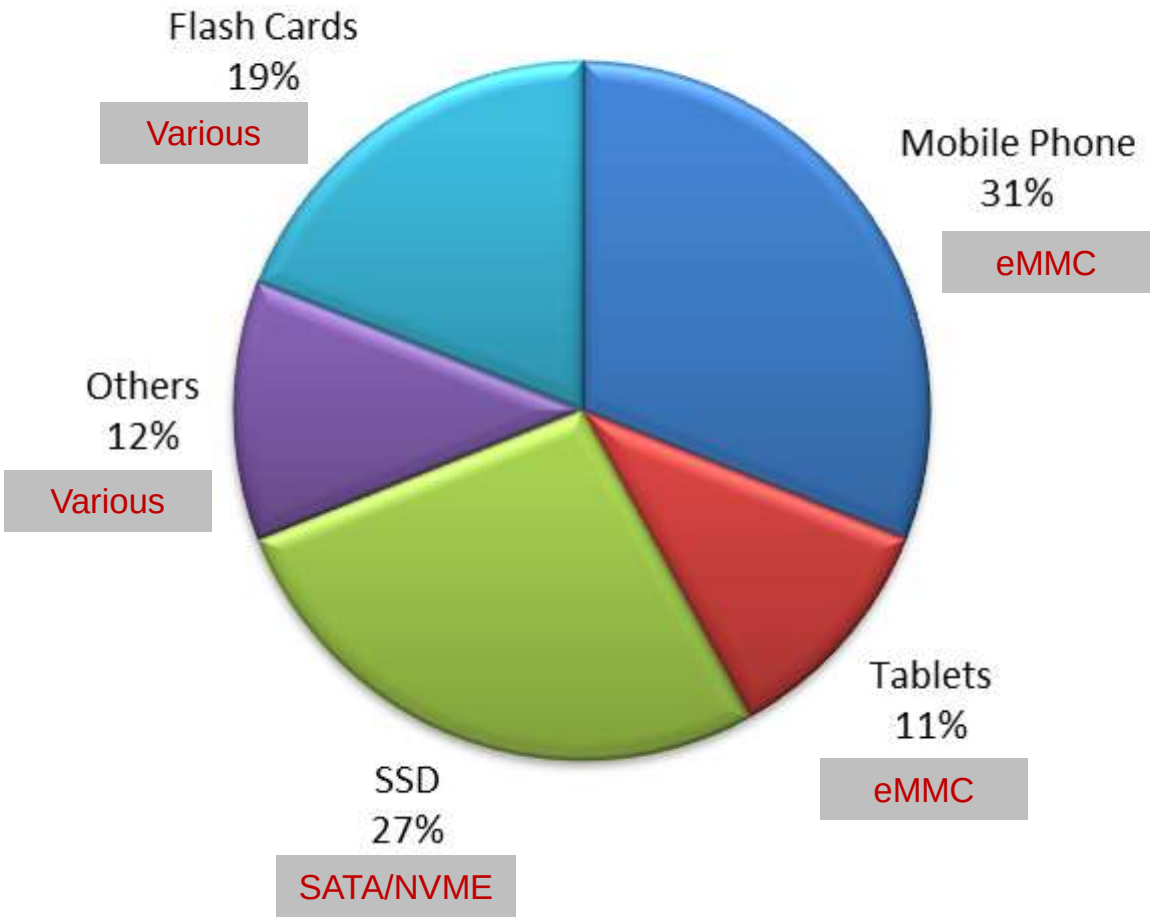
Memory Market Segmentation





Tektronix®

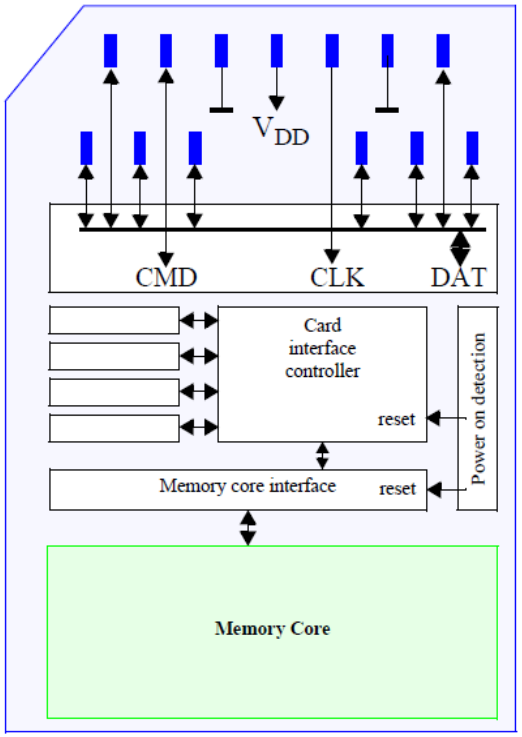
Flash Market Segmentation



Tektronix®

eMMC Card Concept

- Multimedia card transfers data via configurable data bus signals
- Communication Signals
  - **CLK:** Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
  - **CMD:** This signal is a bidirectional command channel used for card initialization and transfer of commands.
  - **DAT0-DAT7:** These are bidirectional data channels (1 bit/4 bit/8bit)



Tektronix

eMMC Electrical measurements as eMMC4.41- SDR

eMMC HighspeedSDR measurement for eMMC4.41 Specification			
Parameter	**Min**	**Max**	**Unit**
Clock Frequency Data Transfer Node	0	52	MHz
Clock frequency Indentifiction Mode	0	400	KHz
Clock High Time	6.5		ns
Clock low Time	6.5		ns
Clock rise time		3	ns
Clock fall time		3	ns
Inputs CMD, data (referenced to CLK)			
Input setup time CLK-CMD	3		ns
Input hold time CLK-Data	3		ns
Input set up time CLK-Data	3		ns
Input hold time CLK-Data	3		ns
Outputs CMD, Data (referenced to CLK)			
Output delay time during data transfer CLK-CMD		13.7	ns
Output hold time CLK-CMD	2.5		ns
Output delay time during data transfer CLK-Data		13.7	ns
Output hold time CLK-Data	2.5		ns
Signal Rise time		3	ns
Signal fall time		3ns	

eMMC Electrical Measurements for Backward Compatibility

eMMC Highspeed SDR measurement for eMMC4.41 Specification			
Parameter	**Min**	**Max**	**Unit**
Clock Frequency Data Transfer Node	0	26	MHz
Clock frequency Indentifiction Mode	0	400	KHz
Clock High Time	10		ns
Clock low Time	10		ns
Clock rise time		10	ns
Clock fall time		10	ns
Inputs CMD, data (referenced to CLK)			
Input setup time CLK-CMD	3		ns
Input hold time CLK-Data	3		ns
Input set up time CLK-Data	3		ns
Input hold time CLK-Data	3		ns
Outputs CMD, Data (referenced to CLK)			
Output setup time CLK-CMD	11.7		ns
Output hold time CLK-CMD	8.3		ns
Output setuptime CLK-Data	11.7		ns
Output hold time CLK-Data	8.3		ns

eMMC Electrical Measurements for DDR Mode-4.41

eMMC High speed DDR measurement for eMMC4.41 Specification			
Parameter	**Min**	**Max**	**Unit**
Clock Duty Cycle	45	55	%
Inputs CMD, data (referenced to CLK)			
Input setuptime CLK-CMD	2.5		ns
Input holdtime CLK-Data	2.5		ns
Input set up time CLK-Data	2.5		ns
Input hold time CLK-Data	2.5		ns
Outputs CMD, Data (referenced to CLK)			
Output delay time during data transfer CLK-CMD	1.5	7	ns
Output delay time during data transfer CLK-Data	1.5	7	ns
Signal Rise time		2	ns
Signal fall time		2	ns

Ultra High Speed cards

- UHS-1 provides 104 Mb/s performance with single ended performance
- UHS-I operation modes
  - DS- default signaling mode supports up to 25MHz up to 3.3V
  - HS- High speed up to 50MHz 3.3V
  - SDR12- SDR up to 25MHz at 1.8V
  - SDR25- SDR up to 50Mz at 1.8
  - SDR104- SDR upto 208MHz
  - DDR- DDR up to 50MHz 1.8V signalling

SD Electrical Measurements SDR12

Electrical Specification of SD SDR12		
Parameter	**Min**	**Max**
Clock frequency		025Mhz
Clock low time	10ns	
Clock high Time	10ns	
Clock Rise Time		10ns
Clock fall time		10ns
CLK-CMD Input Setup time	5ns	
CLk_CMD Input Hold time	5ns	
CLK-Data Inut Setup time	5ns	
CLK-CMD Input Hold time	5ns	
CLK-CMD Output delay ime during Data Transfer		14ns
CLK-data Output Delay time during Data Transfer		14ns
CLK-CMD Output delay time during Identification		50ns
CLK-Data Output Delay time during Identification		50ns

SD Electrical Measurements SDR25

Electrical Specification of SD SDR25		
Parameter	Min	Max
Clock Frequency	0	50MHz
Clock low time	7ns	
Clock high Time	7ns	
Clock Rise Time		3ns
Clock fall time		3ns
CLK-CMD Input Setup time	6ns	
CLk_CMD Input Hold time	2ns	
CLK-Data Inut Setup time	6ns	
CLK-CMD Input Hold time	2ns	
CLK-CMD Output delay ime during Data Transfer		14ns
CLK-data Output Delay time during Data Transfer		14ns
CLK-CMD output Hold Time	2.5ns	
CLK-DAT output delay time	2.5ns	

SD Electrical measurements- SD50

Electrical Specification of SD SDR50		
Parameter	Min	Max
Clock frequency	0	102MHz
Clock Period	9.6ns	
Clock Rise Time		0.2tCLK
Clock fall time		0.2tCLK
Clock Duty Cycle	30%	70%
CLK-CMD Input Setup time	3ns	
CLk_CMD Input Hold time	0.8ns	
CLK-Data Inut Setup time	3ns	
CLK-CMD Input Hold time	0.8ns	
CLK-CMD Output delay ime		2UI
CLK-data Output Delay time		2UI
CLK-CMD output vaid window	0.6UI	
CLK-CMD output Valid Window	0.6UI	

SD Electrical Measurements SDR104

Electrical Specification of SD SDR104		
Parameter	Min	Max
Clock frequency	0	208MHz
Clock Period	4.8ns	
Clock Rise Time		0.2tCLK
Clock fall time		0.2tCLK
Clock Duty Cycle	30%	70%
CLK-CMD Input Setup time	1.4ns	
CLk_CMD Input Hold time	0.8ns	
CLK-Data Inut Setup time	1.4ns	
CLK-CMD Input Hold time	0.8ns	
CLK-CMD Output delay ime		2UI
CLK-data Output Delay time		2UI
CLK-CMD output vaid window	0.6UI	
CLK-CMD output Valid Window	0.6UI	

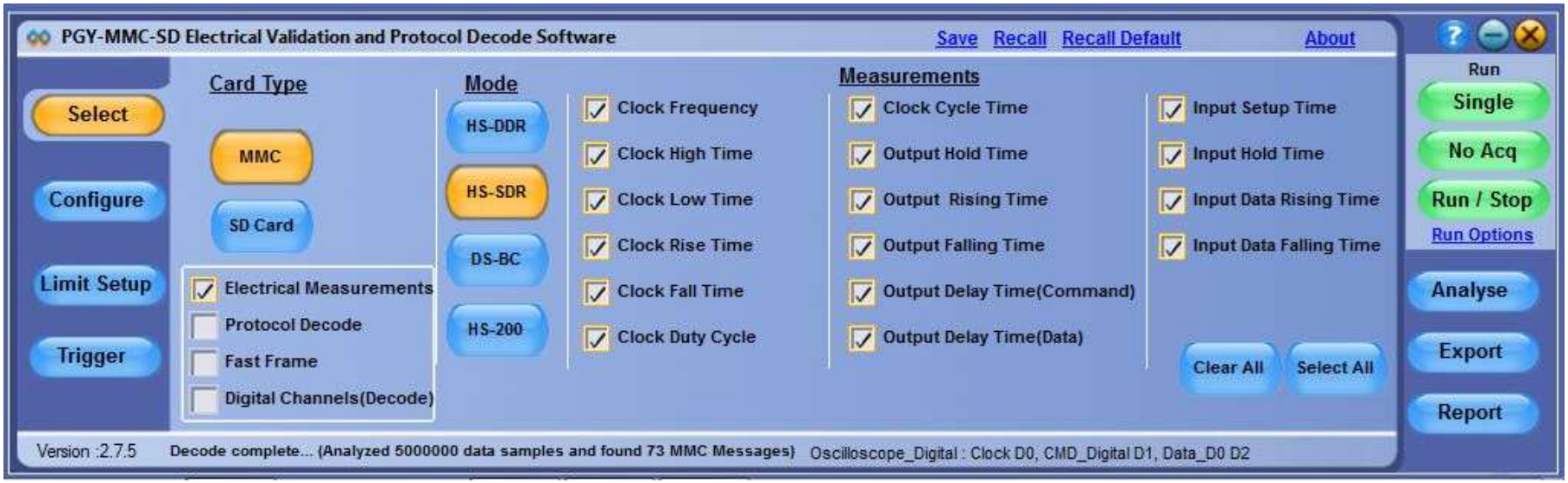
SD Electrical Measurements DDR50

Electrical Specification of SD DDR50		
DDR50	Min	Max
Clock frequency	0	50MHz
Clock Period	20ns	
Clock Rise Time		0.2tCLK
Clock fall time		0.2tCLK
Clock Duty Cycle	45%	55%
CLK-CMD Input Setup time	6ns	
CLk_CMD Input Hold time	0.8ns	
CLK-Data Inut Setup time	3ns	
CLK-CMD Input Hold time	0.8ns	
CLK-CMD Output delay ime		13.7ns
CLK-CMD output hold time	1.5ns	
CLK-data Output Delay time		7ns
CLK-DAT output hold time	1.5ns	

Market Needs

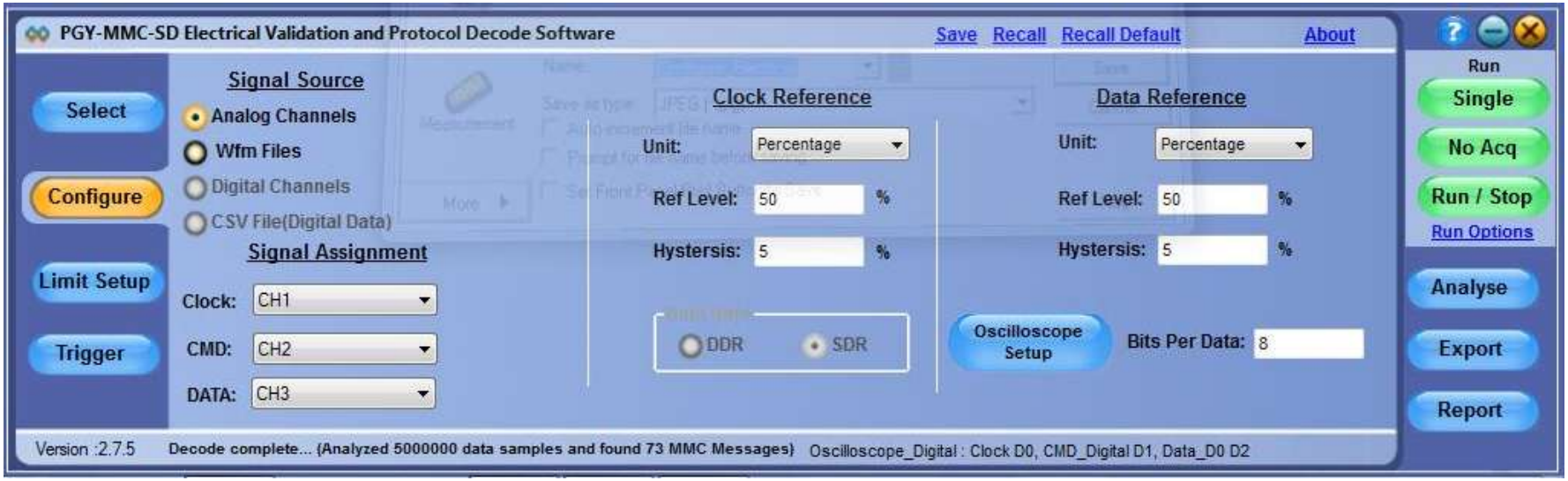
- Electrical validation of eMMC as per 4.41, 4.51 and 5.0 Specification
- Protocol Decode of command line
- Protocol Analysis (tests)
- Protocol Timing measurements
- Protocol Aware Trigger
- Protocol Decode for long duration
- Protocol decode of command and Data bus

PGY-eMMC/SD Electrical Validation and Protocol Decode Software- Select



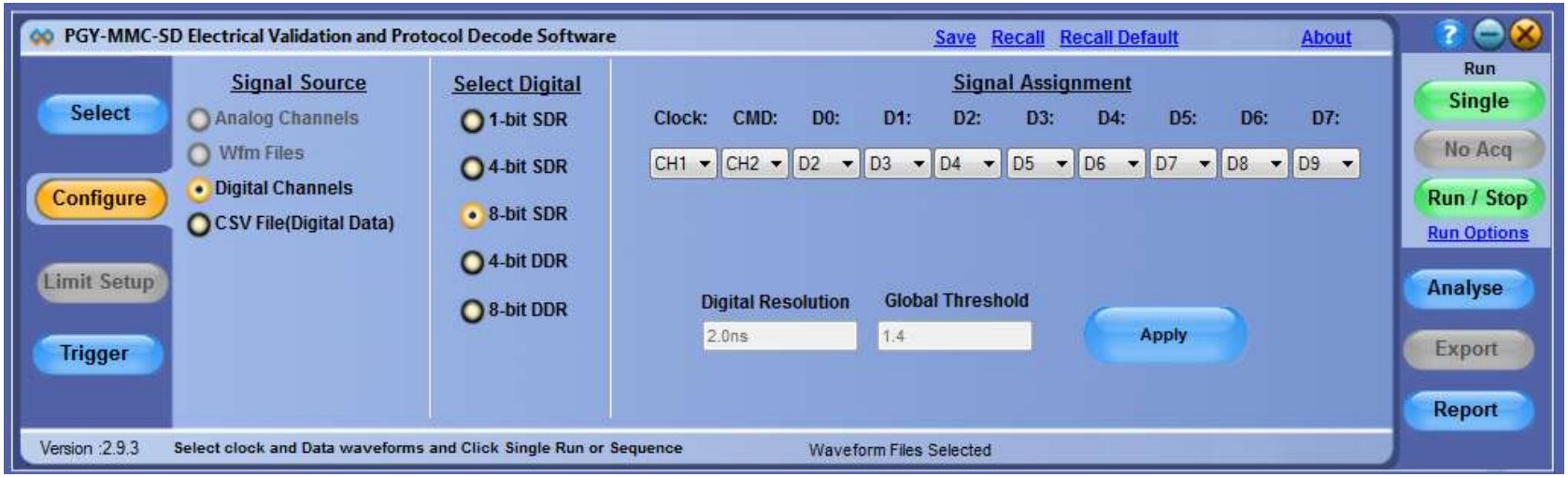
- User can select eMMC type and data mode
- eMMC electrical measurements as specified in eMMC Standard document are listed
- Supports electrical measurement for eMMC4.41 and 4.51 (HS200)
- Protocol aware measurements to support host and device measurements
- Flexibility to select Electrical Validation or Protocol Analysis or both or fast frame based decode and Protocol code using Digital Channel

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Configure- Electrical and Protocol Analysis



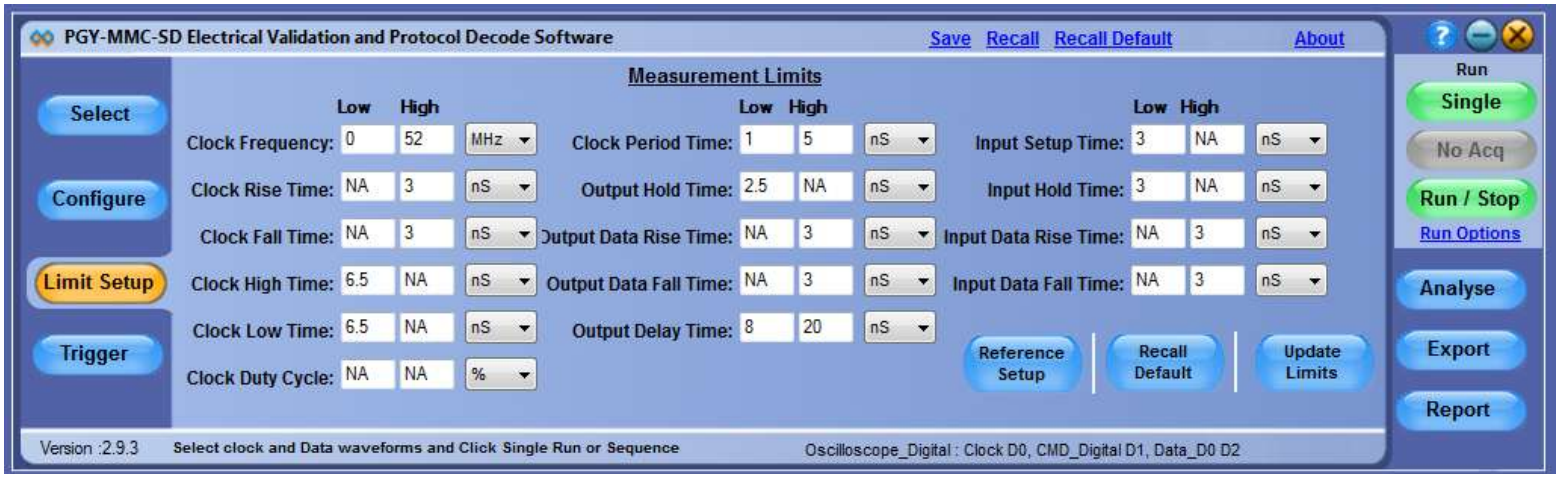
- Select the source of the signal from oscilloscope or saved files
- Flexibility to select Electrical validation or Protocol Analysis or both
- Clock and data reference identifies signal transitions
- Oscilloscope setup helps is automatic oscilloscope setup or recall saved oscilloscope setup

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Configure- Digital Decode



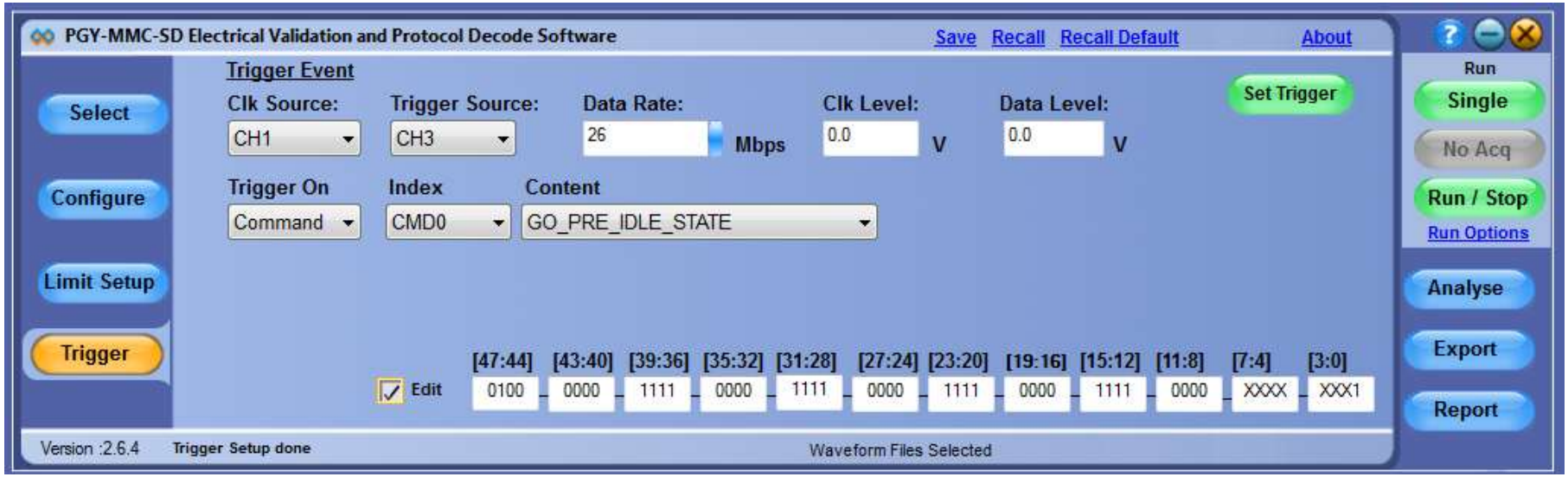
- Select the source of the signal from oscilloscope digital channel or saved CSV digital data file
- Combination of Analog and Digital Channels to reduce probe loading on CLK and CMD
- Select different data modes such as 1-bit SDR, 4-bit SDR, 8 bit SDR, 4 bit DDR and 8 bit DDR
- Set Global threshold and Digital Sampling Resolution

PGY-eMMC-SD Electrical Validation and Protocol Decode Software- Limit Setup



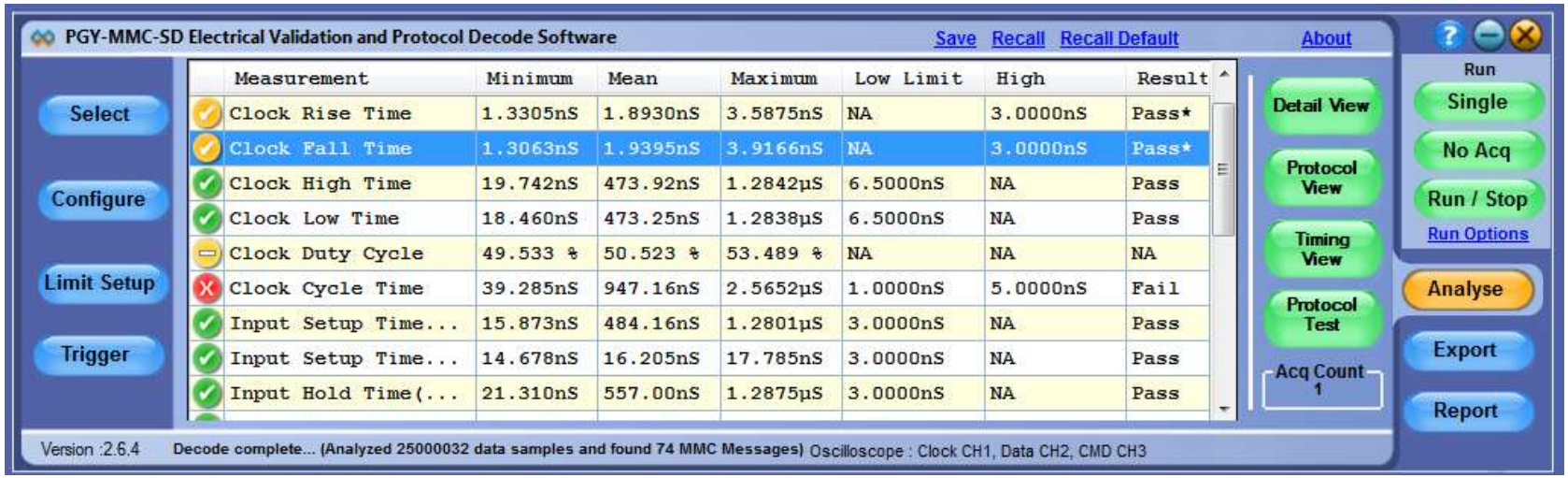
- Limits can be set to default limits as specified in standard document
- User has flexibility to edit the limits and apply
- Save and Recall the limits

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Protocol Aware Trigger



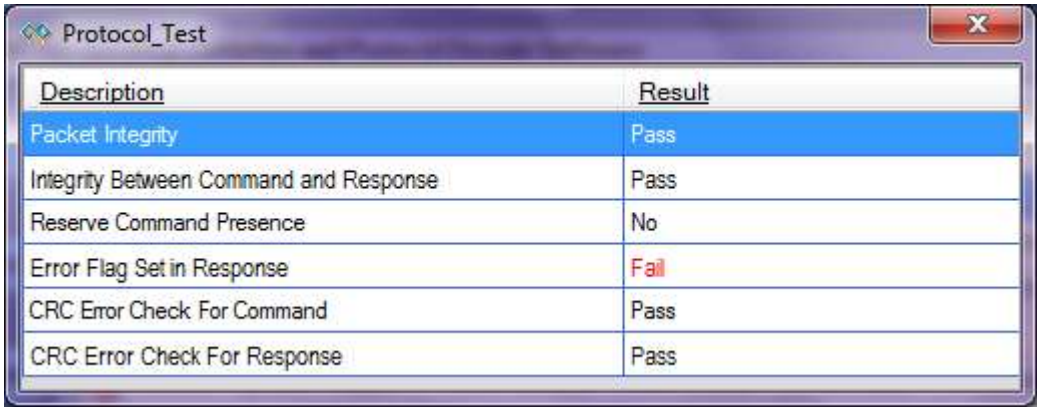
- eMMC Protocol Aware trigger capabilities
- Trigger on command or Response
- Flexibility to edit the trigger conditions
- Prerequisite is Serial pattern setup feature in oscilloscope

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Analyze



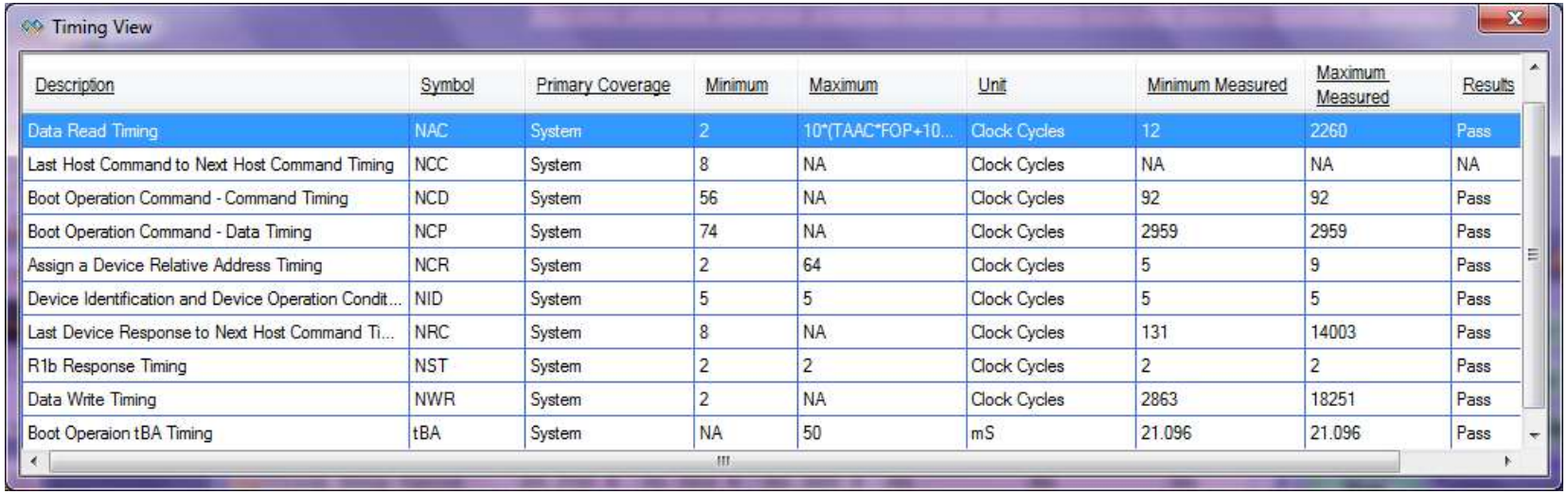
- Displays measurement limits and annotation to indicate pass or fail
- Provides min, max and mean measurement values
- Measurements are made using the complete acquisition data, min, mean and max value for the complete acquired data (max Record length support is 125MB)
- List the measurements for Clock, command , response, data write and data read to cover all the electrical tests as per eMMC specs
- Green annotation indicates test pass, orange color indicates, test may be failed for either min or max value and Red color indicates test is fail

Protocol test



- PGY-MMC analyses whether Protocol packets complies to specs
  - Packet Integrity checks for number of bits per packet in command or response.
  - Integrity between command and response checks for whether each command is receiving the expected response as per spec
  - Reserve command presence– Checks for any reserved command by host
  - Error Flags set Response- Indicates some error flags are set in response
  - CRC Checks in Command – verifies transmitted CRC value with computed CRC by taking row packet data
  - CRC Checks for Response- verifies transmitted CRC value with computed CRC by taking row packet data
- Enables Protocol checks without going through all the data

Timing View



Description	Symbol	Primary Coverage	Minimum	Maximum	Unit	Minimum Measured	Maximum Measured	Results
Data Read Timing	NAC	System	2	10*(TAAC*FOP+10...	Clock Cycles	12	2260	Pass
Last Host Command to Next Host Command Timing	NCC	System	8	NA	Clock Cycles	NA	NA	NA
Boot Operation Command - Command Timing	NCD	System	56	NA	Clock Cycles	92	92	Pass
Boot Operation Command - Data Timing	NCP	System	74	NA	Clock Cycles	2959	2959	Pass
Assign a Device Relative Address Timing	NCR	System	2	64	Clock Cycles	5	9	Pass
Device Identification and Device Operation Condit...	NID	System	5	5	Clock Cycles	5	5	Pass
Last Device Response to Next Host Command Ti...	NRC	System	8	NA	Clock Cycles	131	14003	Pass
R1b Response Timing	NST	System	2	2	Clock Cycles	2	2	Pass
Data Write Timing	NWR	System	2	NA	Clock Cycles	2863	18251	Pass
Boot Operaion tBA Timing	tBA	System	NA	50	mS	21.096	21.096	Pass

- PGY-MMC-SD software checks for all timing measurements between command, Response and data
- Checks for number of cycles between command-Response, Response-data and so forth
- Gives Pass/fail results

Tektronix®

Protocol Decode using Digital Channels (MSO)

- Recommended use cases

  Case#1

  – Connect Digital Channel to eMMC CLK, CMD and Data lines
  – Connect CLK and CMD to Analog Channel
  – Set eMMC Protocol Trigger to trigger on read and write operation
  – Run the application

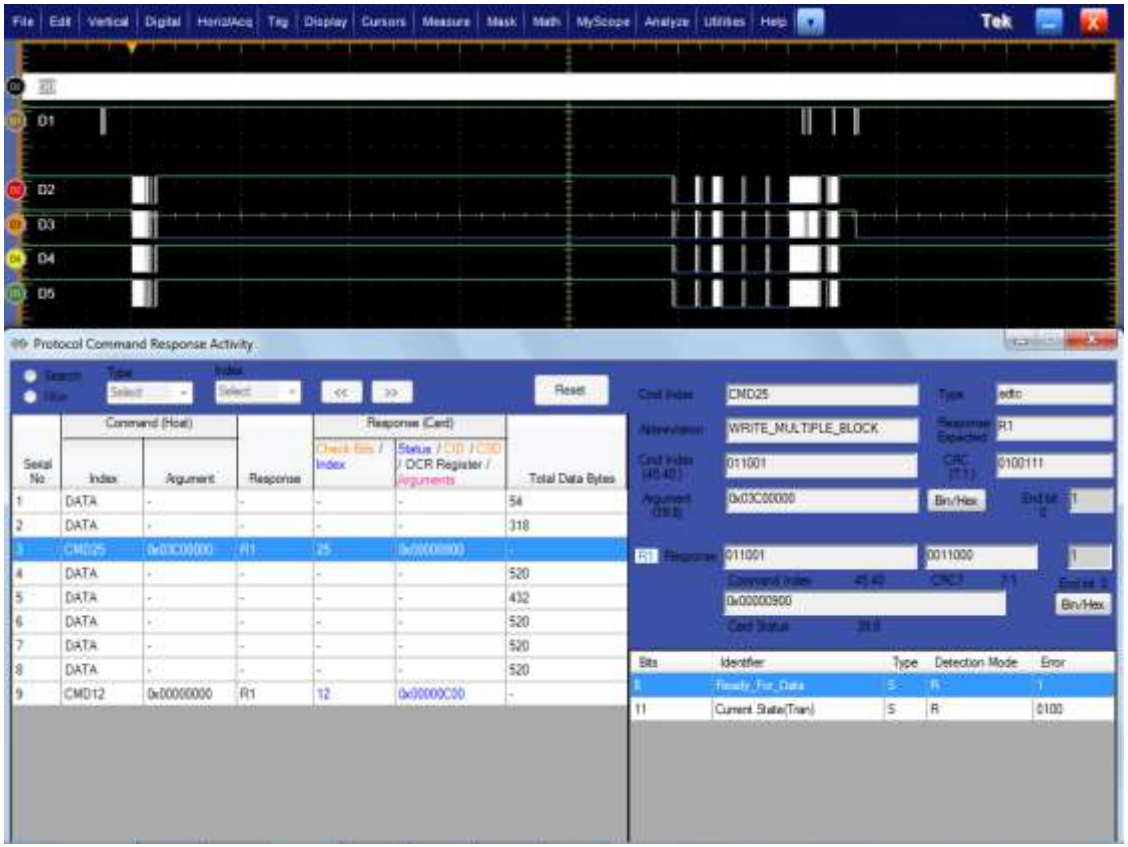
  Case #2

  – Connect Digital Channel to eMMC CLK, CMD and Data lines
  – Set Data line falling edge as trigger condition
  – Run the application

- Above cases allows you focus on decoding the datelines

Protocol Decode using Digital Channels

- Protocol View list decoded data
- Each row will have CMD, response and number data bytes
- Selected row details including all data bytes is displayed on right bottom
- Only oscilloscope based solution

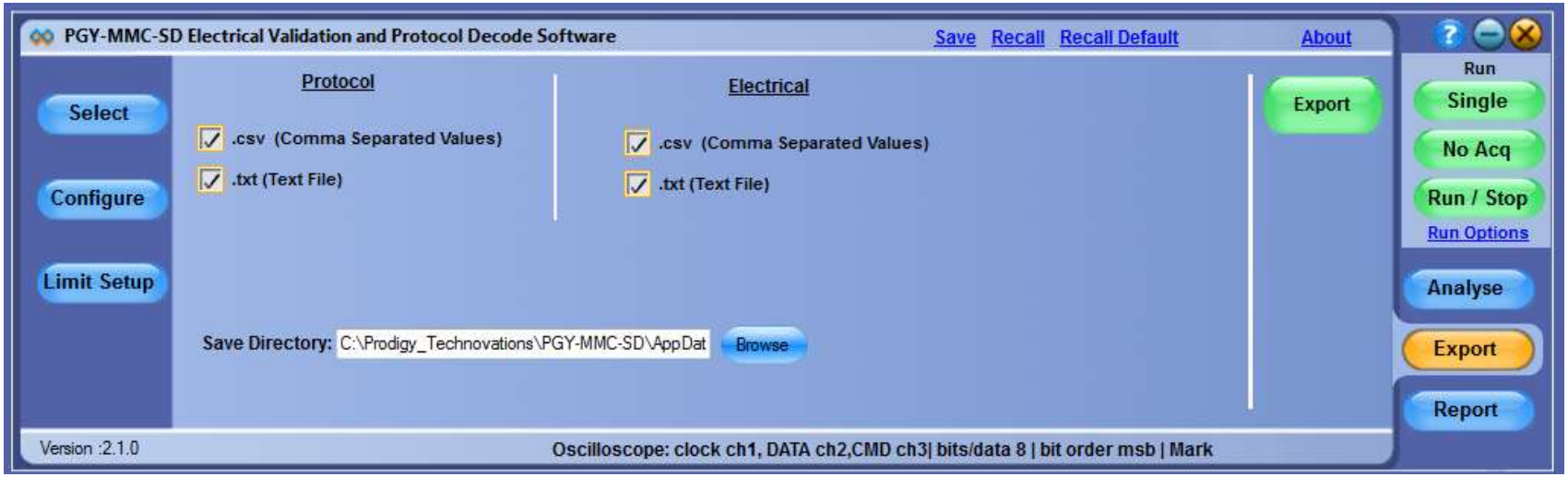


Tektronix®

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Detail View

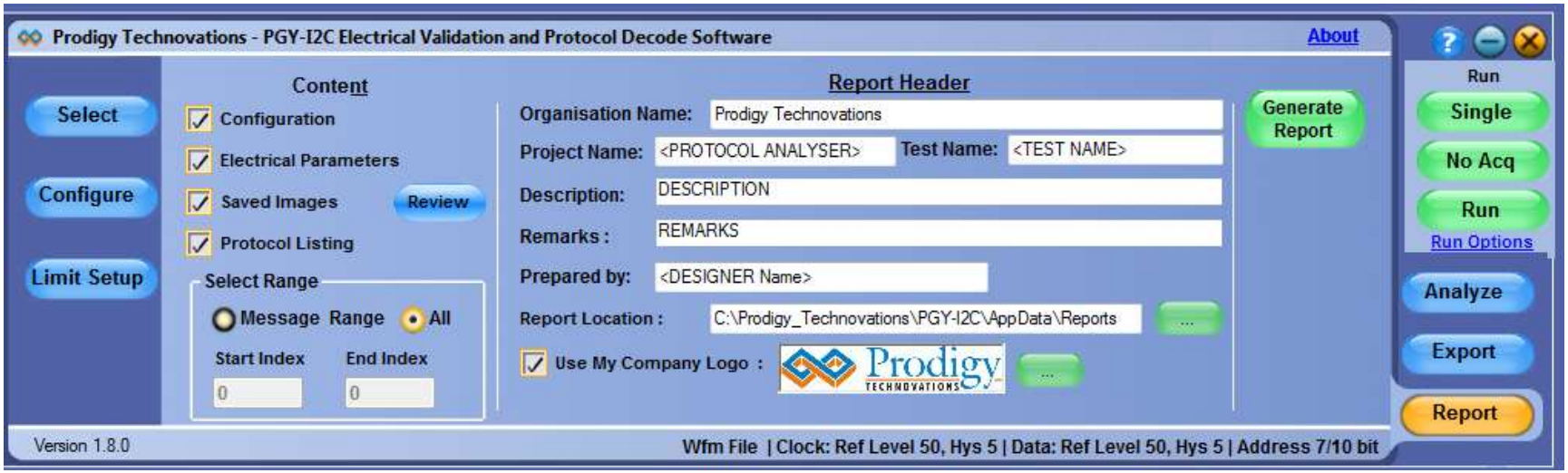
- Provides powerful debug environment co-relating physical layer waveform, protocol decode data and electrical measurements
- If any protocol packet is failed in Protocol test is highlighted in red color
- Selected protocol decode message waveform is plotted in selected waveform window
- Reference cursor will be placed in acquired waveform window to indicate the position of the waveform in Acquired data
- Failed Electrical measurements selected in red color
- Cursor measurements for manual analysis
- Markers to indicate reference level for measurement
- Take snapshot of selected waveform image from detail view for report
- Decode tables list the Commands and responses from card
- Utility features for zooming the waveform, pan, cursors, reference set markers and image capture for report

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Export



- Export of Electrical measurements and Protocol Decode data to CSV and TXT file format
- Browser allows to place the data in desired location

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Report



- Supports customizable pdf format report generation
- Report can include electrical measurements, protocol decode, oscilloscope images, detail view images, and reference level setup
- Review of saved images allows the user to add title to image, description and delete the images

Market Needs

- Electrical validation of eMMC as per 4.41, 4.51 and 5.0 Specification (Supported; 5.0 spec by June 2014)
- Protocol Decode of command line (Supported)
- Protocol Analysis (tests) (Supported)
- Protocol Timing measurements (Supported)
- Hardware based realtime Protocol Aware Trigger (supported)
- Protocol Decode for long duration (Supported)
- Protocol decode of command and Data bus (Supported)

Competitive info

- Agilent Provide separate Electrical validation software for eMMC and SD
- Tektronix & Provides single integrated eMMC/SD/SDIO Electrical validation and protocol Analysis Software
- Agilent does not provide Protocol Analysis Software
- LeCroy has no solution in space

Details of UPIU

UPIU Data Structure	Description
NOP Out	The NOP Out transaction acts as a ping from an initiator to a target. It can be used to check for a connection path to a device and LUN.
NOP In	The NOP In transaction is a target response to an initiator when responding to a NOP In request.
Command	The Command transaction originates in the Initiator (host) and is sent to a logical unit within a Target device. A Command UPIU will contain a Command Descriptor Block as the command and the command parameters. When using the phase collapse feature the UPIU will also contain a data segment that would have been sent during the DATA OUT phase. This represents the COMMAND phase of the command.
Response	The Response transaction originates in the Target and is sent back to the Initiator (host). A Response UPIU will contain a command specific operation status and other response information. When using the phase collapse feature, the UPIU will also contain a data segment that would have been sent during the DATA IN phase. This represents the STATUS phase of the command.
Data Out	The Data Out transaction originates in the Initiator (host) and is used to send data from the Initiator to the Target (device). This represents the DATA OUT phase of a command.
Data In	The Data In transaction originates in the Target (device) and is used to send data from the Target to the Initiator (host). This represents the DATA IN phase of a command.
Task Management Request	This transaction type carries SCSI Architecture Model (SAM) task management function requests originating at the Initiator and terminating at the Target. The standard functions are defined by the SAM-5 specification. Addition functions might be defined by UFS.
Task Management Response	This transaction type carries SCSI Architecture Model (SAM) task management function responses originating in the Target and terminating at the Initiator.
Ready To Transfer	The Target device will send a Ready To Transfer transaction when it is ready to receive the next Data Out UPIU and has sufficient buffer space to receive the data. The Target can send multiple Ready To Transfer UPIU if it has buffer space to receive multiple Data Out UPIU packets. The maximum data buffer size is negotiated between the Initiator and Target during enumeration and configuration. The Ready To Transfer UPIU contains a DMA context and can be used to setup and trigger a DMA action within a host controller.
Query Request	This transaction originates in the Initiator and is used to request descriptor data from the Target. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.
Query Response	This transaction originates in the Target and provides requested descriptor information to the Initiator in response of the Query Request transaction. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.

Prodigy TECHNOVATIONS

Thank You

Tektronix®

Thank you!