USB3.0/3.1 Physical Layer Testing

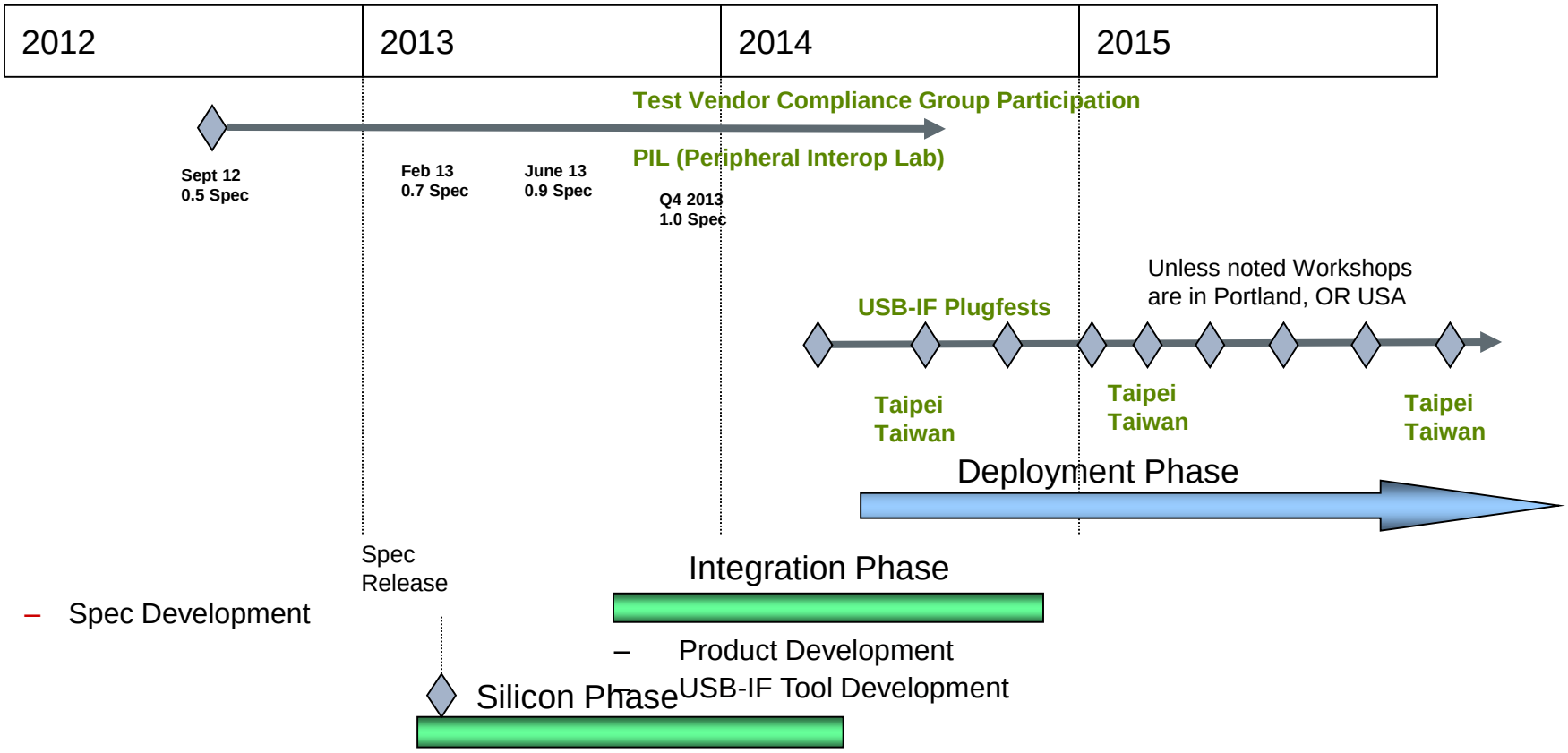
泰克科技（中国）有限公司 张晓
Tim.Zhang@tektronix.com

Tektronix®

Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging
- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture
- **USB 3.1, 10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation

USB 3.0/3.1 Technology Timeline

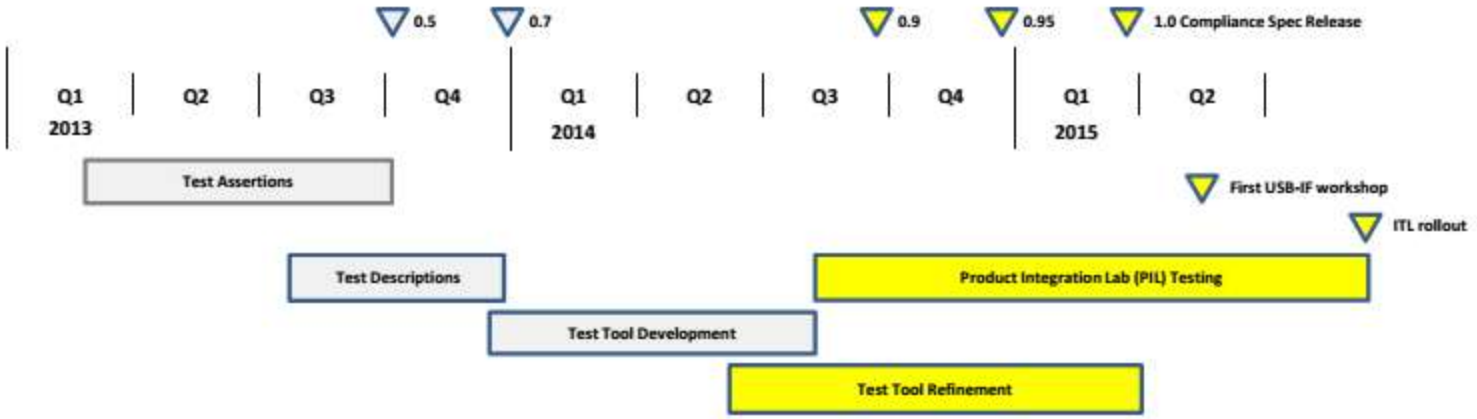


Tektronix

USB3.1 Compliance Timeline

USB 3.1 Compliance Timeline

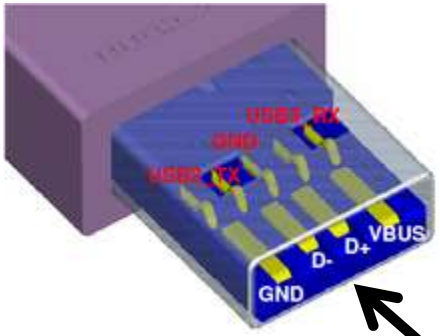
Version	Milestones	
0.5	Test Assertions	
0.7	Test Assertions + Test Descriptions	Draft Test Specification
0.9	Tests coded and Test Specification updated	Begin testing at PIL
0.95	Beta tool release	Ready to certify products
1.0	Final tool release	Release to ITLs



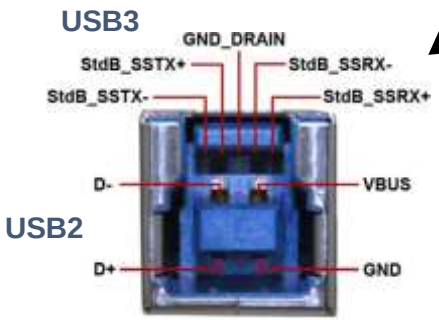
Tektronix

Overview: Cable Assembly

Std A Connector (host)

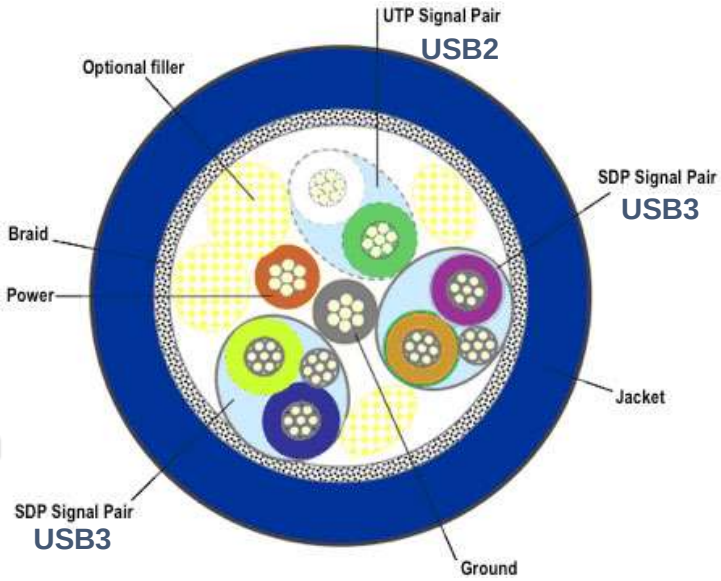


mB Connector (device)



Std B Connector (device)

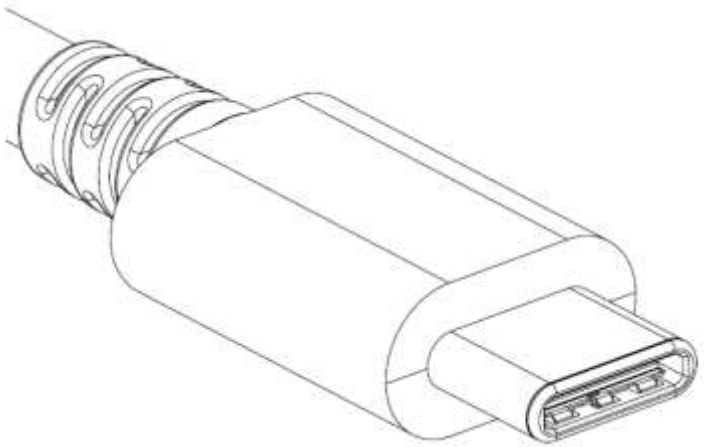
Cable Cross-section



Tektronix

NEW Type C connector

- Used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- Enhances ease of use by being plug-able in either upside-up or upside-down directions
- Enhances ease of use by being plug-able in either direction between host and devices
- New Configuration Control signal (low speed) for handshaking
- Two high speed diff pairs for mux'ing data



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	RFU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	RFU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Why 10 Gb/s?

Video

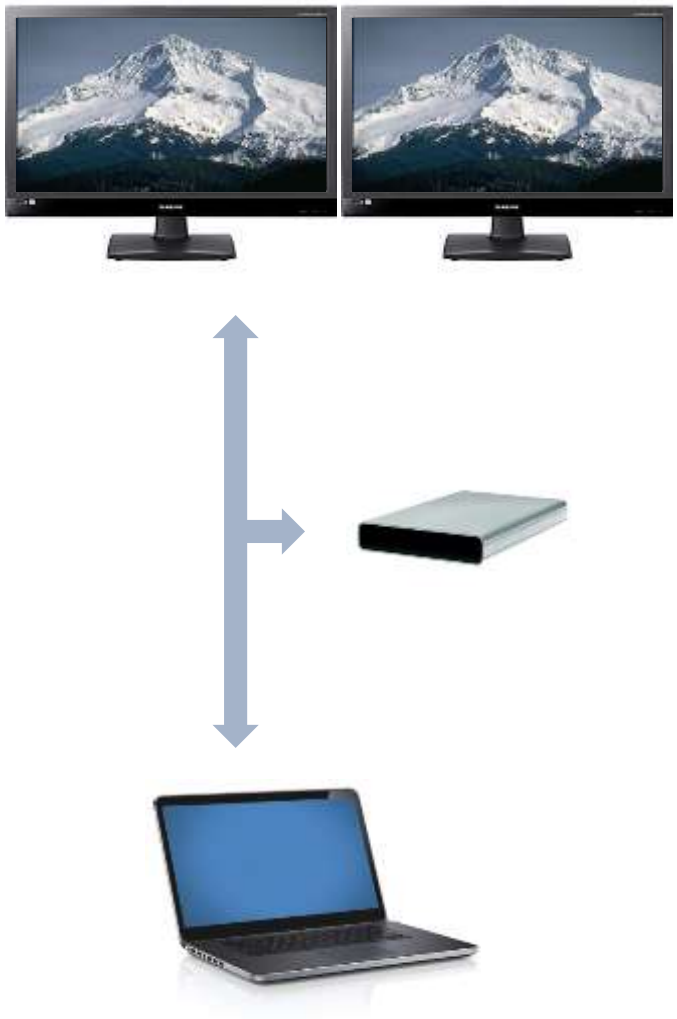
- HD video adapters with multi display outputs
- Dual HDMI/DVI with simultaneous 1080p displays

Storage

- 5 Gb/s with 8b/10b -> 400 MB/s
- High performance SSD saturation-> ~600 MB/s

Hub/Dock

- Multi-function, ‘All in One’ docking
- Faster backups, multiple monitors, etc.



Naming convention

- SuperSpeed (SS) = 5 Gb/s
- SuperSpeedPlus (SSP) = 10 Gb/s

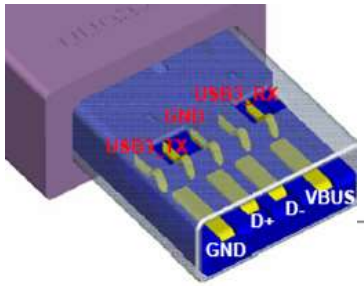
- Similar to other standards
  - Gen1 = 5G
  - Gen2 = 10G
  - GenX = 5G or 10G

- SS and SSP are qualifiers not names
  - E.g. SuperSpeedPlus device, host or hub

- Enhanced SuperSpeed = ≥ Gen1 speed
  - Reference for possible future higher data rate

USB 3.0 Key Considerations

- **Receiver Testing Now Required**
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- **Channel Considerations**
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- **New Challenges**
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- **Test Strategy**
  - Cost-effective tools
  - Flexible solutions



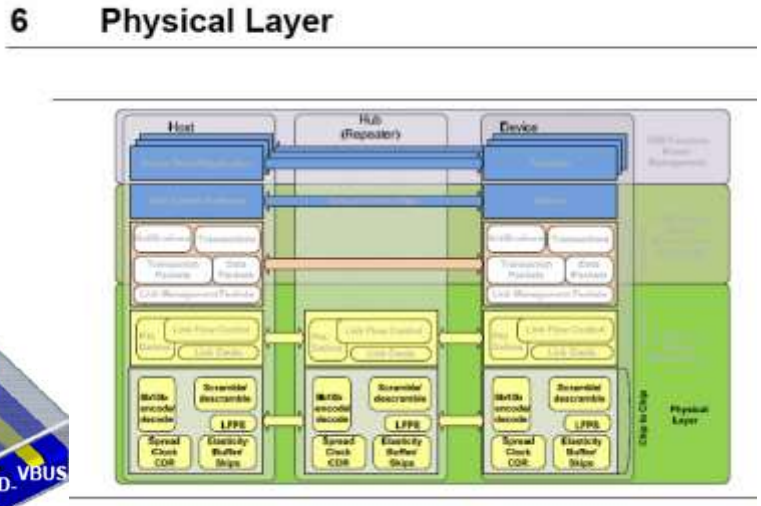
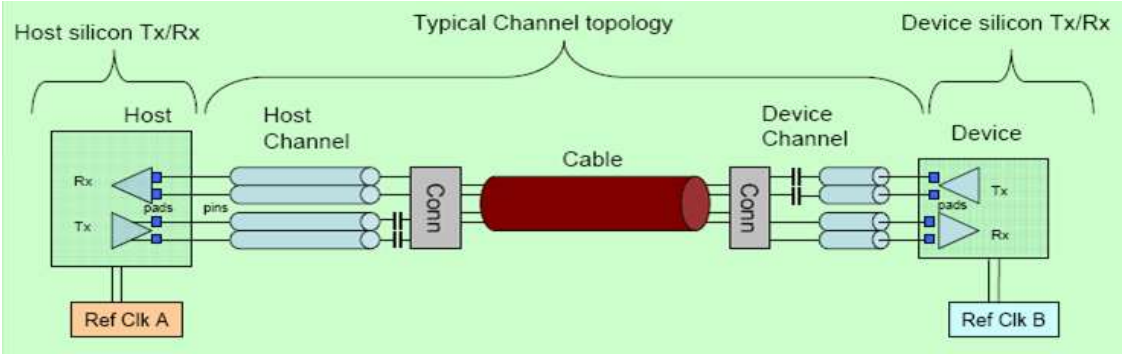


Figure 6-1. Super Speed Block Diagram: Physical

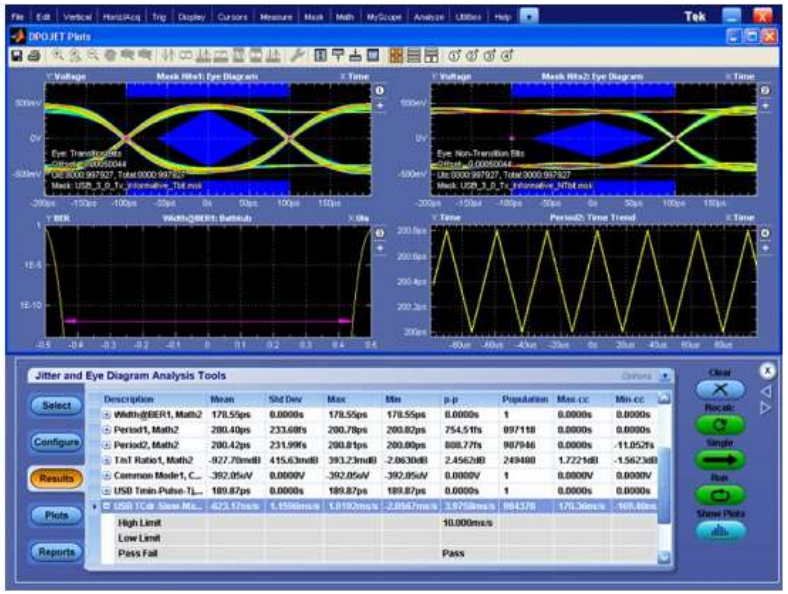


Source: USB 3.0 Rev 1.0 Specification

Tektronix

Transmitter Solutions

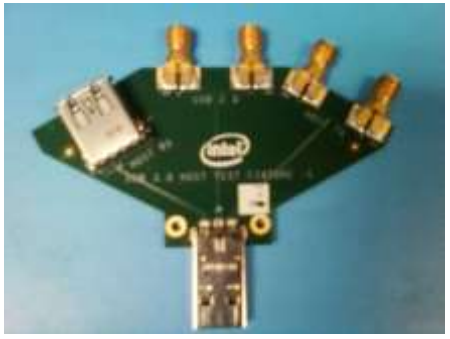
- **Comprehensive Solution Goes Beyond Compliance**
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results
- **Complete Toolset for Characterizing USB 3.0 Designs**
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG



Tektronix

USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing
    - Available from the USB-IF



USB 3.0 Compliance Test Configuration

- **USB 3.0 is a closed eye specification**
  - Reference channel is embedded and CTLE is applied
- **USB 3.0 Reference Channels**
  - Host Reference Channel
    - 11” back panel is applied for device testing
  - Device Reference Channel
    - 5” device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels
- **USB 3.0 Reference Equalizer**
  - Attenuates the low frequency content of the signal to open the eye

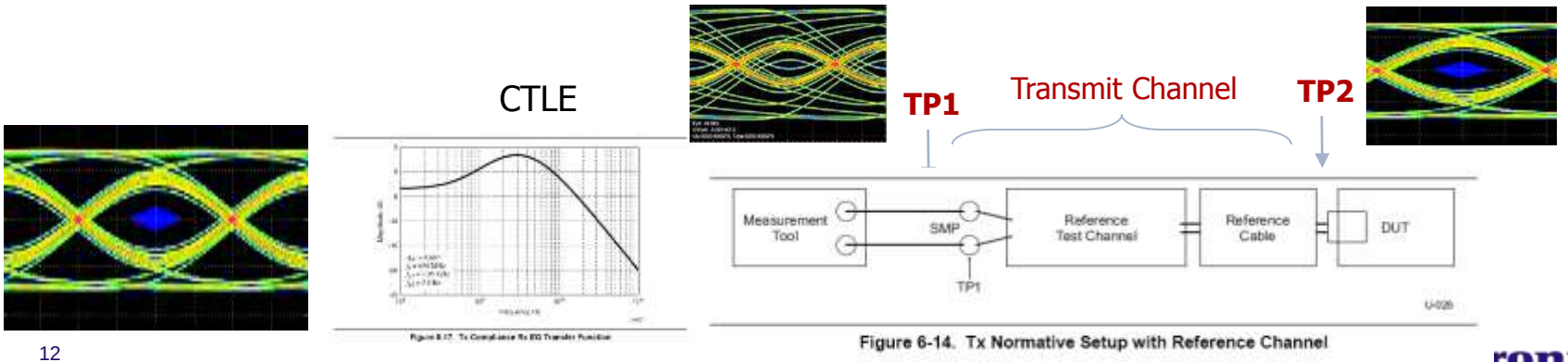
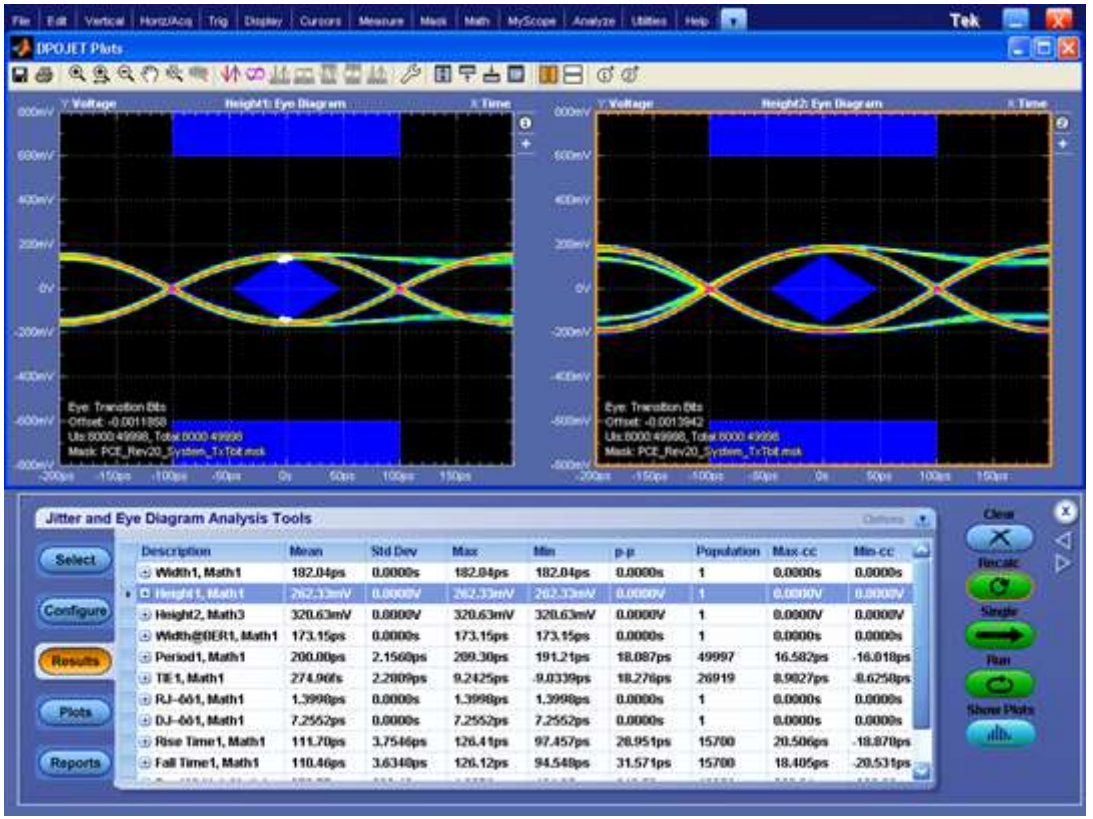


Figure 6-14. Tx Normative Setup with Reference Channel

Fixture and Channel De-Embedding

- Why de-embed – Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins
- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software

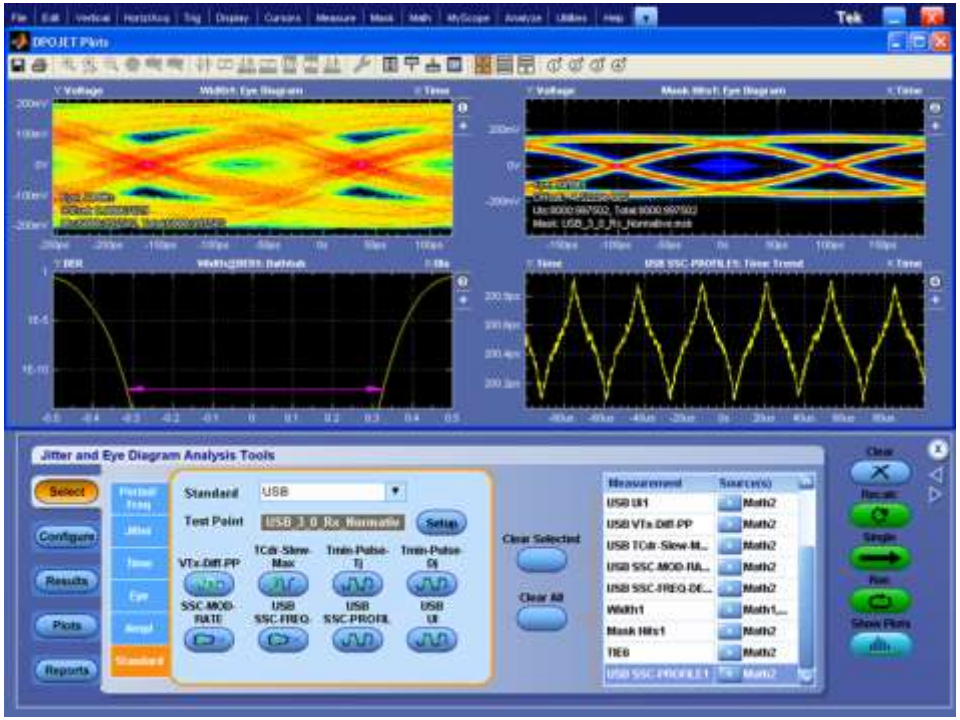
Before → **After**



Tektronix

USB 3.0 Transmitter Measurement Overview

- **Voltage and Timing**
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- **Low Frequency Periodic Signaling (LFPS)**
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- **SSC**
  - Modulation Rate
  - Deviation



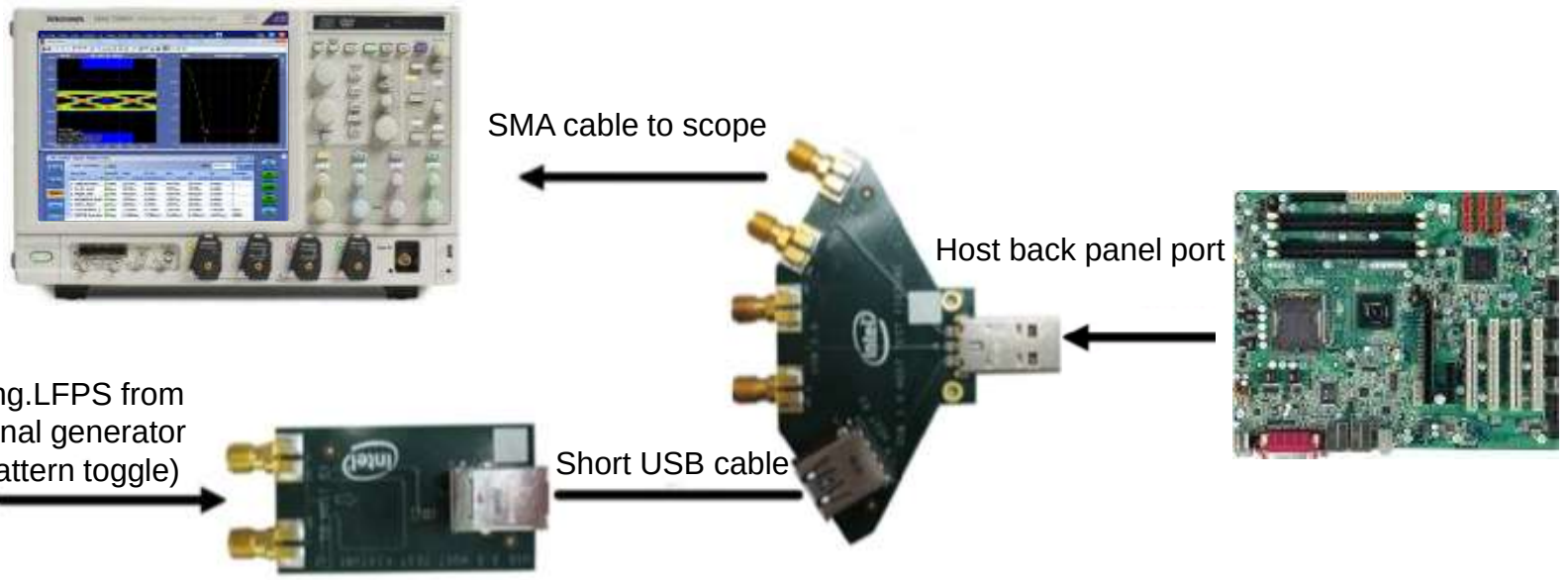
Tektronix

SuperSpeed Transmitter Compliance Testing

1. Connect DUT to scope via test fixture.
2. Transmit CP1 (toggle pattern) & measure 10^6 consecutive UI
   - This step used to measure RJ
3. Repeat with CP0 (scrambled D0.0)
   - Will combine RJ (step 2) with DJ to extrapolate TJ (step5)
4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   - Channels are S-Parameter-based and are embedded into captured waveform
5. Extrapolate jitter to 10^{-12} BER

Spec	Min	Max	Units
Eye Height	100	1200	mV
Rj @ 10^{-12} BER		0.23	UI
Tj @ 10^{-12} BER		0.66	UI

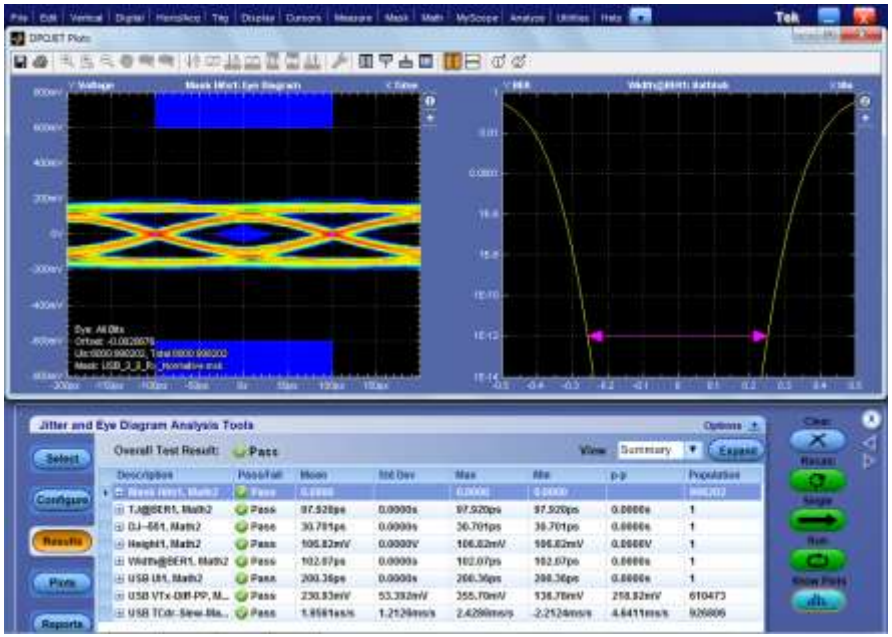
Example Host Test Setup



Tektronix

Voltage and Timing

- Tj – Dual Dirac at 10–12 BER
- Tx Deterministic Jitter – Dual Dirac
- Tx Random Jitter – Dual Dirac
- Differential p-p Tx Voltage Swing
- Transmitter Eye – Dual Dirac@BER
- Eye Width@BER
- Eye Mask Hits



Tektronix

LFPS TX Measurements

- LFPS signaling is critical for establishing link communication
- LFPS TX test verify common mode, voltage, tPeriod, tBurst, tRepeat
- Channel is not embedded for LFPS tests

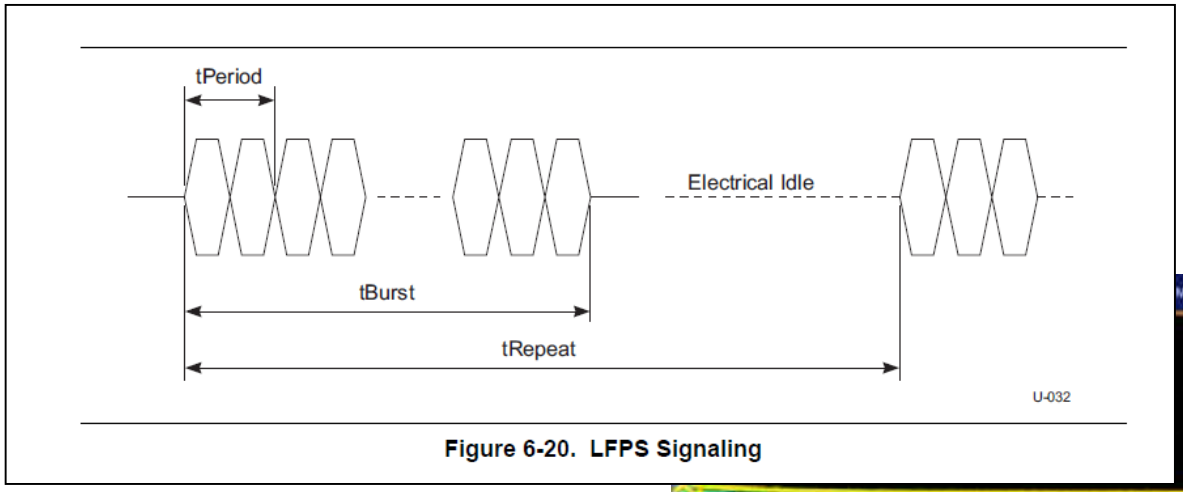
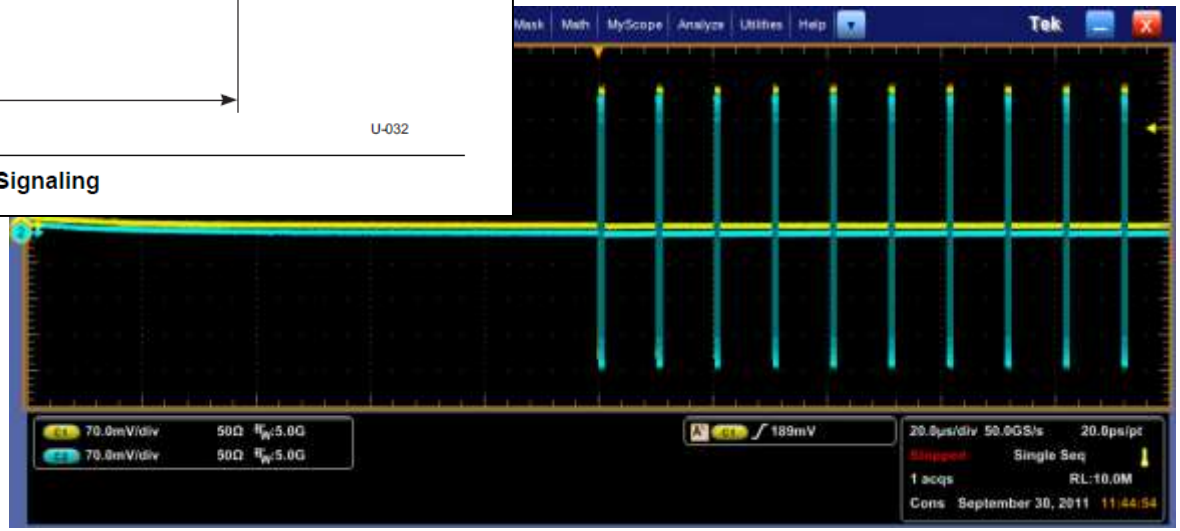


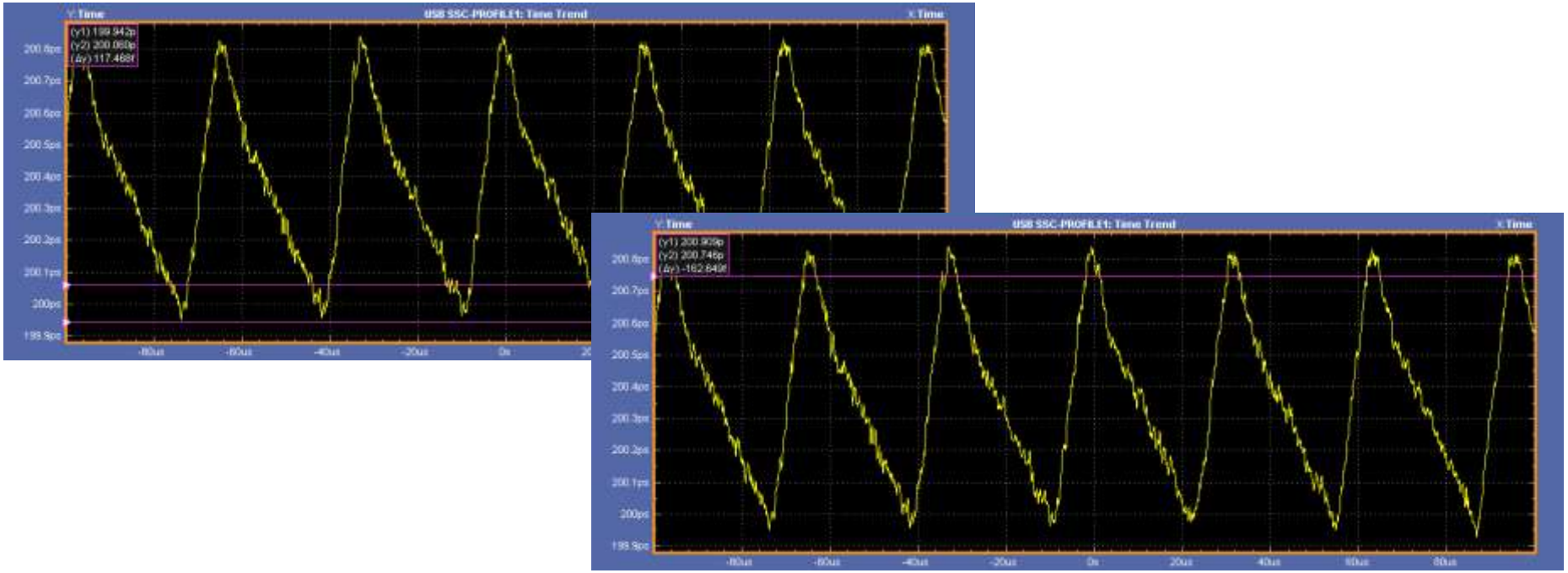
Figure 6-20. LFPS Signaling



Tektronix

SSC Measurements

- Both Maximum and Minimum Frequency Deviation must be considered
  - Assume nominal UI of 200ps
  - Limits are +0/-4000ppm and +0/-5000ppm, plus +/- 300ppm for ref clock accuracy
- Compliance Channel is not embedded for SSC measurements



Tektronix

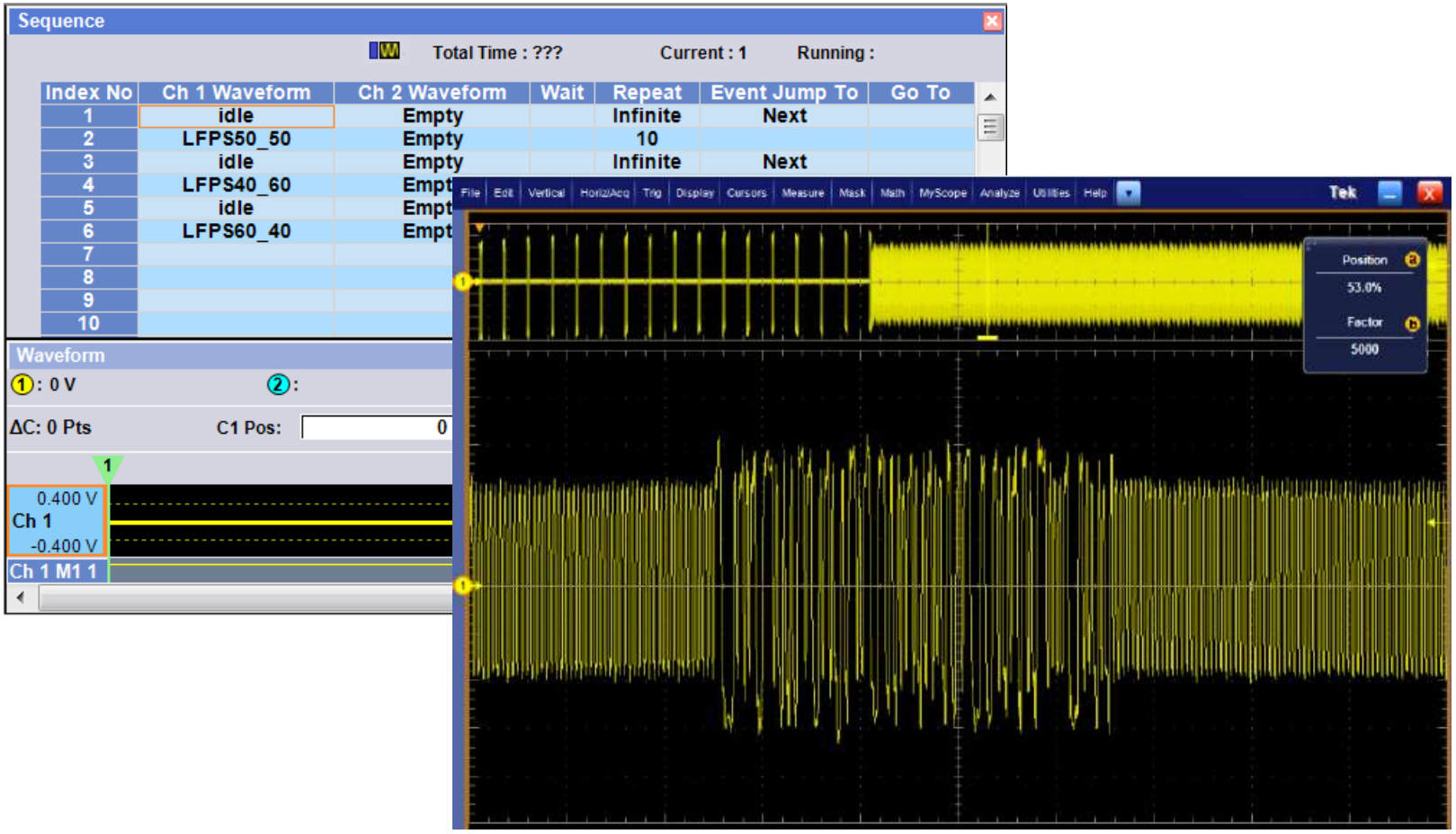
LFPS RX Test

- Required Compliance Test to verify that the DUT RX will respond to LFPS signaling
- Test is ran across four different settings

tPeriod	VTX-DIFF-PP-LFPS	Duty Cycle
50ns	800mV	50%
50ns	1000mV	40%
50ns	1000mV	60%
50ns	1200mV	50%

LFPS RX Test

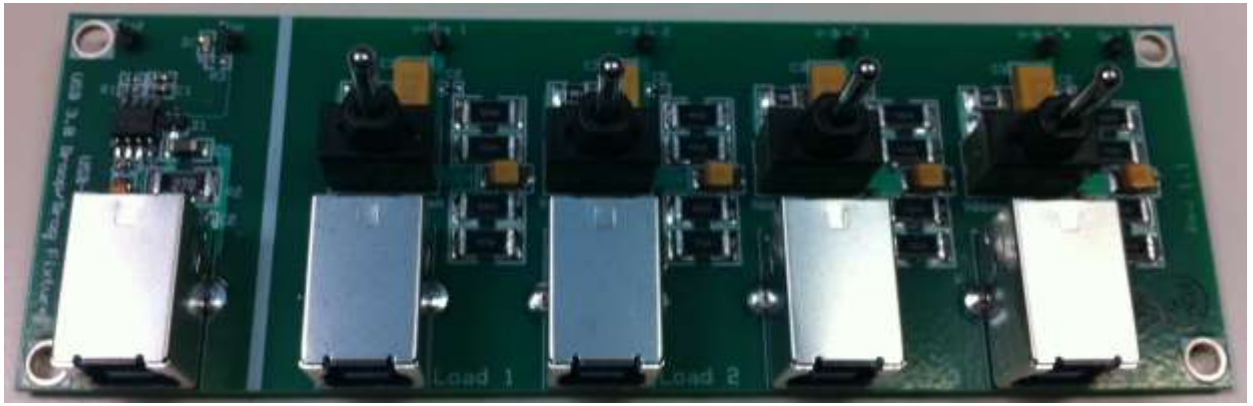
- AWG generates spec compliant LFPS signaling
- Validate LFPS response with RT Scope



Tektronix

USB 3.0 Droop / Drop Test

- New Test Fixture Available from USB-IF
  - Provides 150mA / 900mA load
  - Previous fixture provides 100mA / 500mA load
- Amount of power drawn is changed from 500mA to 900mA for high power devices
- Fixture is orderable at: http://www.usb.org/developers/estoreinfo/USB_product_order_form.pdf



Tektronix

NEW Debug and Analysis Tools

- USB3 Decode with Hierarchal Bus display
- Includes Digital, 8b10b, PHY, LINK, and Transaction layers
- Enables decode, search and trigger, available with option SR-USB

Tektronix

Decode and Trigger Examples

USB3 Link Training

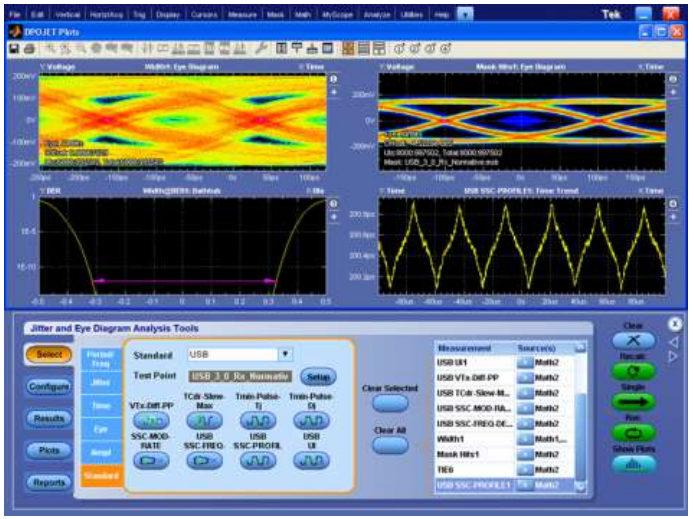
USB3 Trigger Setup

Tektronix

Complete USB 3.0 Transmitter Solution

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures
- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)
- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50 GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

Opt. USB3



Opt. USB-TX

TF-USB3-AB-KIT

Tektronix

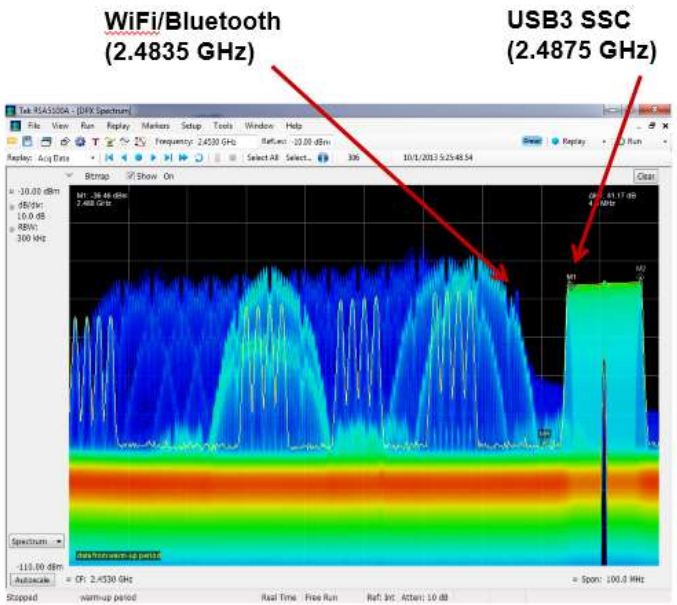
What's new—ECN#18 USB3.0 Radio Friendly Clock Unit Interval

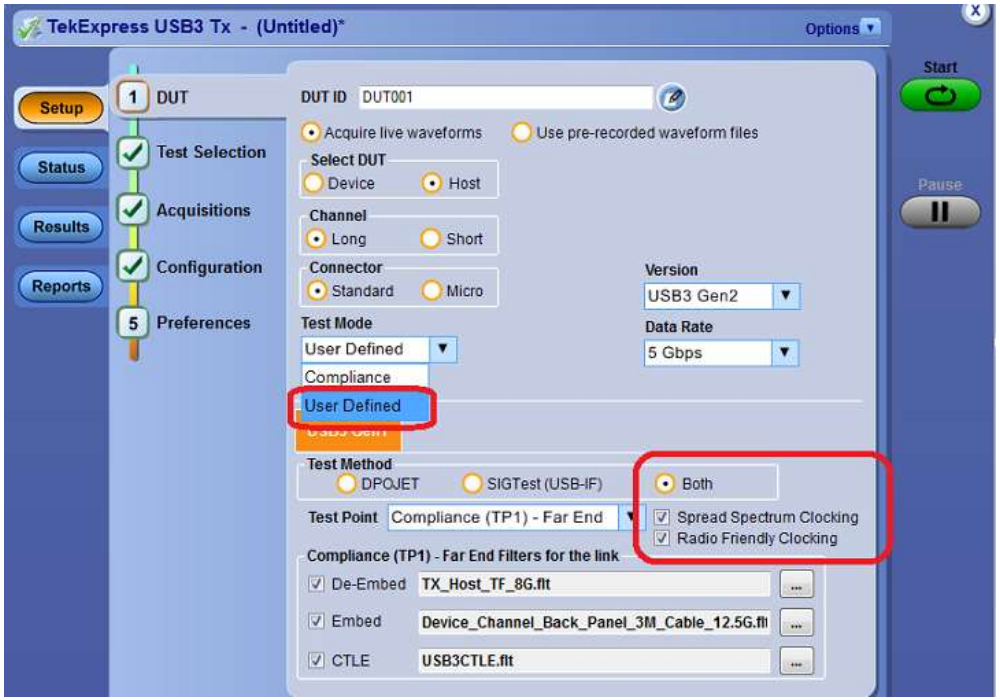
Table 6-9. SSC Parameters

Symbol	Description	Limits		Units	Note
		Min	Max		
$t_{SSC-MOD-RATE}$	Modulation Rate	30	33	kHz	
$t_{SSC-FREQ-DEVIATION}$	SSC deviation	+0/-4000 +0/-2000	+0/-5000 +0/-3000	ppm	1, 2, 3 4

Note:

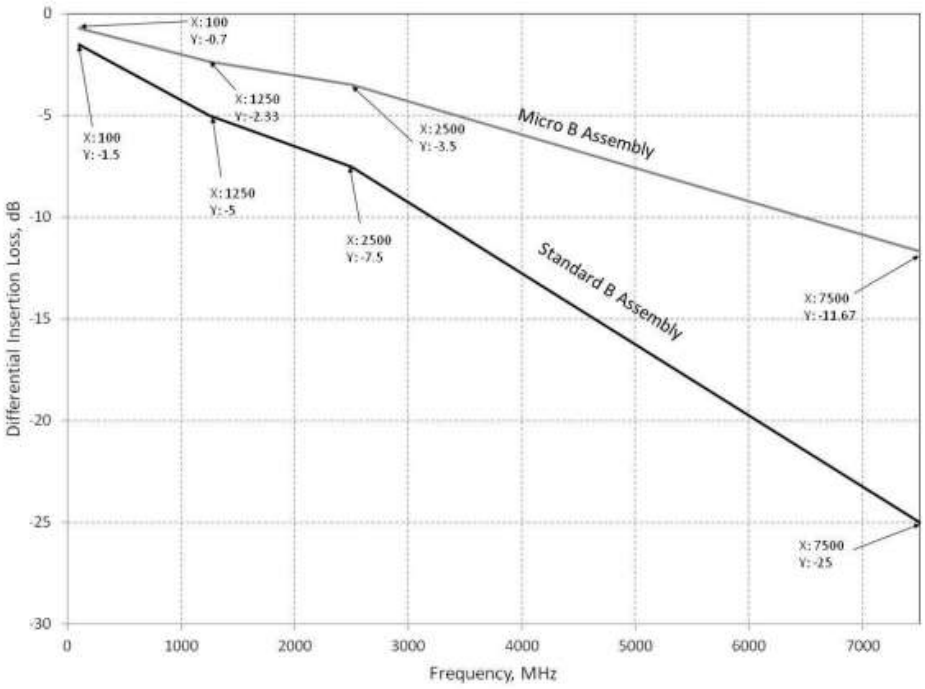
1. The data rate is modulated from 0 ppm to -5000 ppm of the nominal data rate frequency and scales with data rate.
2. This is measured below 2 MHz only.
3. Receiver compliance testing is done under the maximum spread condition.
4. Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000ppm.

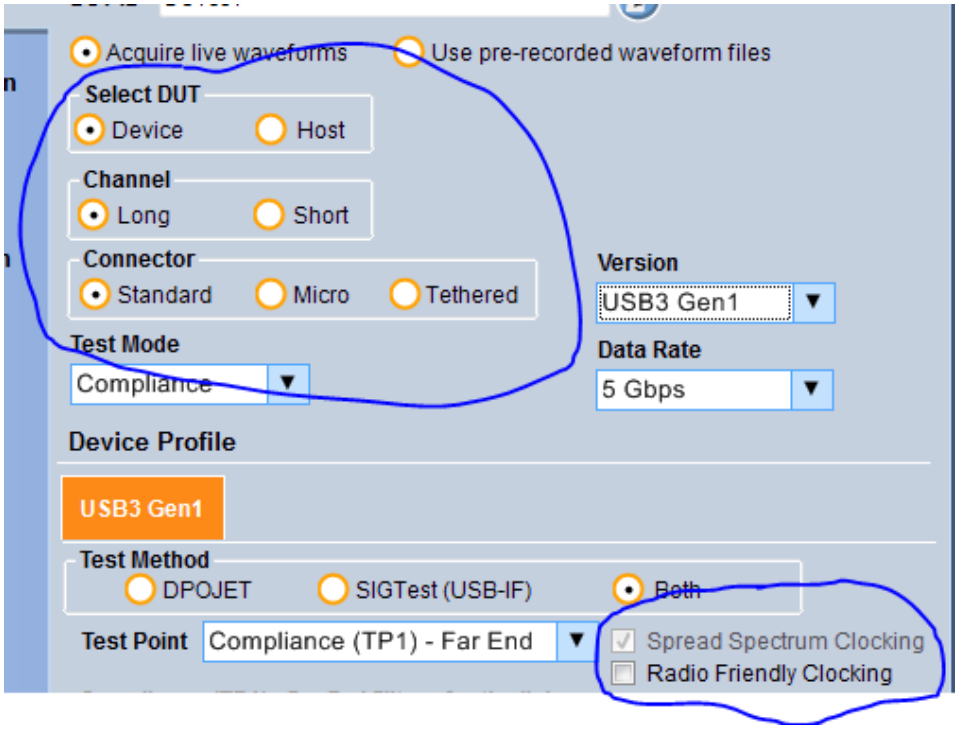




Tektronix

What's new---ECN#19 USB3.0 MicroB Cable Loss Specification





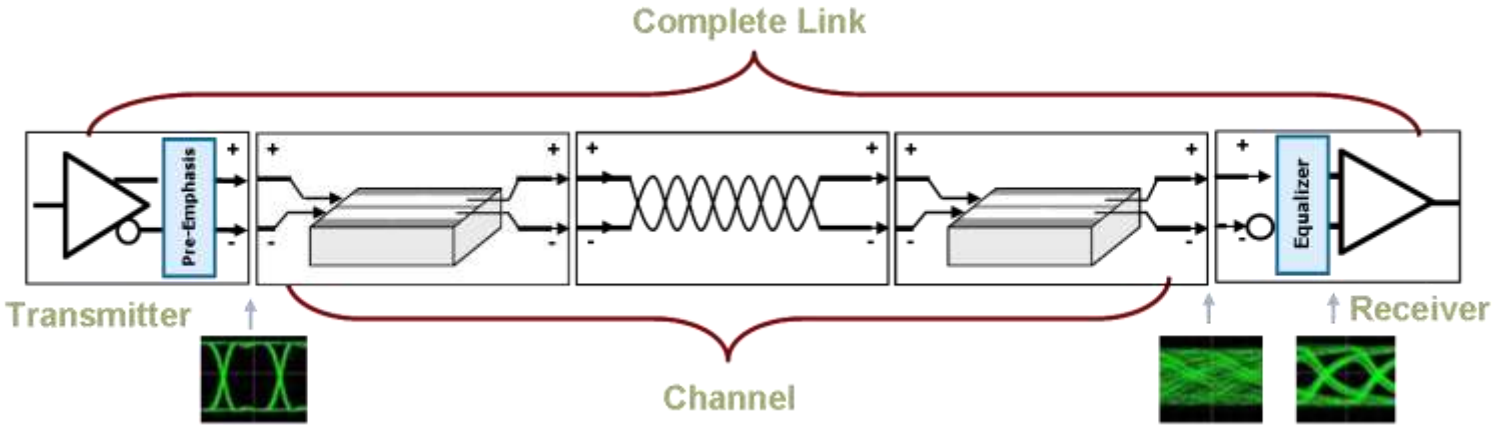
Tektronix

USB 3.0 Receiver Testing

Tektronix®

USB 3.0 Receiver Testing Overview

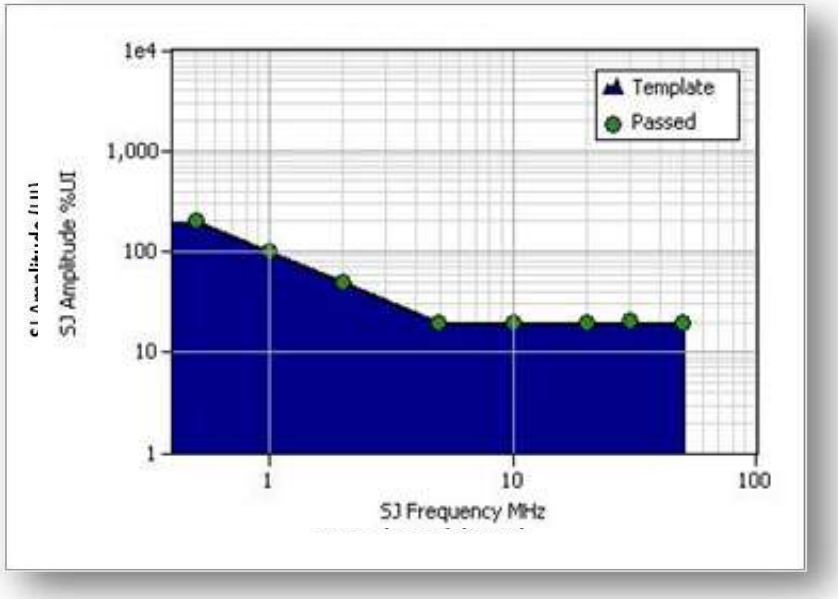
- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions



Tektronix

USB 3.0 Compliance Receiver Tolerance Test Overview

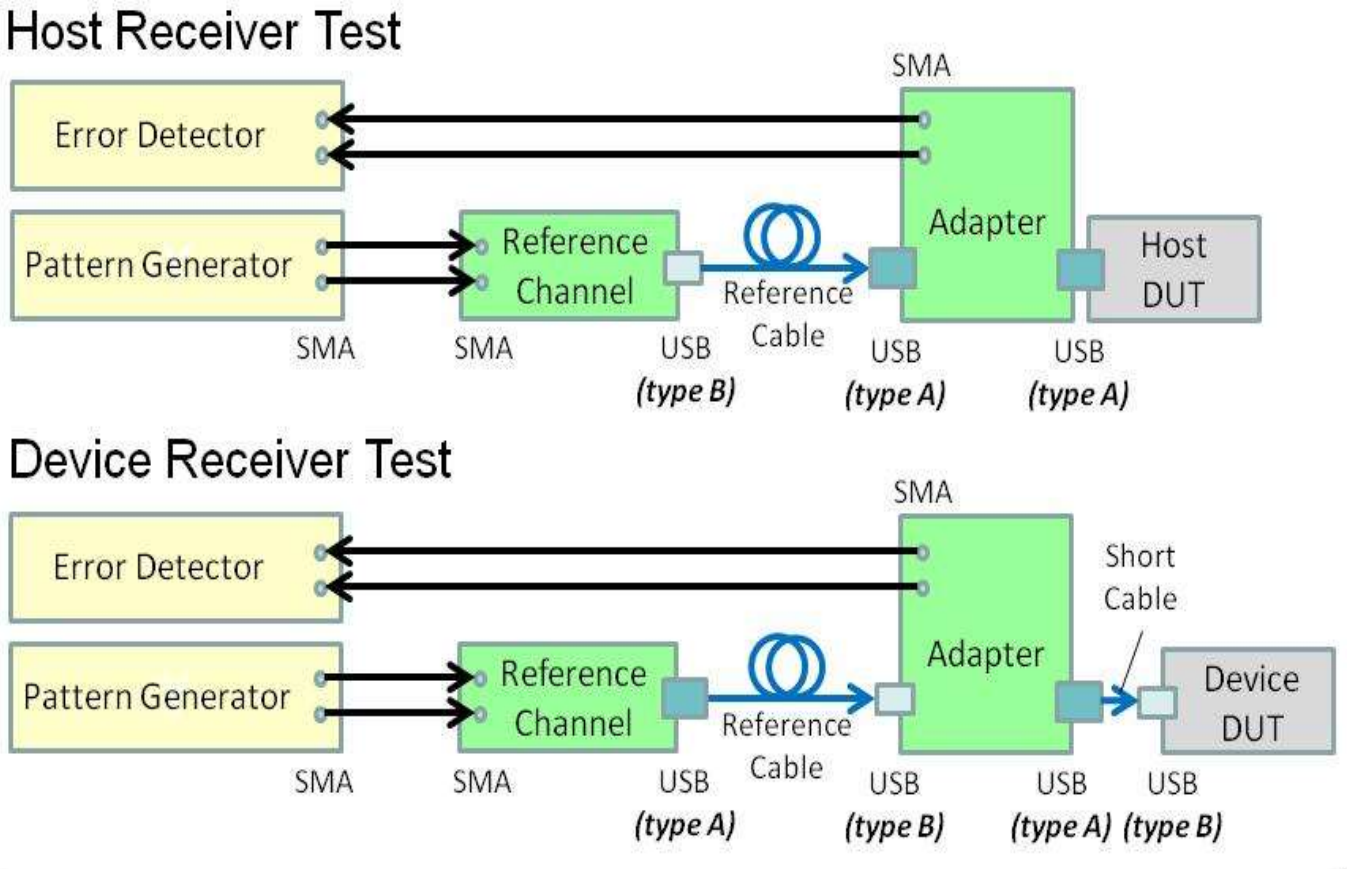
- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- De-Emphasis Level is set to -3dB
- Amplitude at the end of the compliance channel: 180mV Hosts and 145mV Devices
- Each SJ term in the table below is tested one at a time after the device is in loopback mode



Frequency	SJ	RJ
500kHz	400ps	2.42ps RMS
1MHz	200ps	2.42ps RMS
2MHz	100ps	2.42ps RMS
4.9MHz	40ps	2.42ps RMS
10MHz	40ps	2.42ps RMS
20MHz	40ps	2.42ps RMS
33MHz	40ps	2.42ps RMS
50MHz	40ps	2.42ps RMS

Tektronix

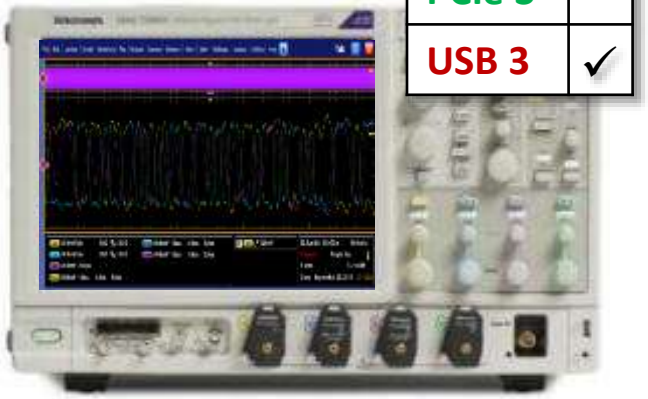
Generic USB 3.0 RX Test Configuration



Tektronix

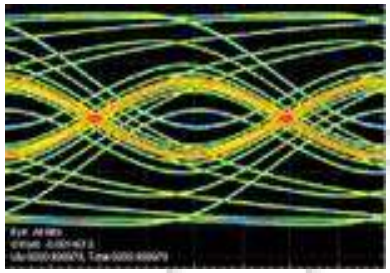
USB 3.0 Stress Recipe - Calibration

PCIe 3	
USB 3	✓



Long waveform **capture by Real Time Scope**

Tx Eq



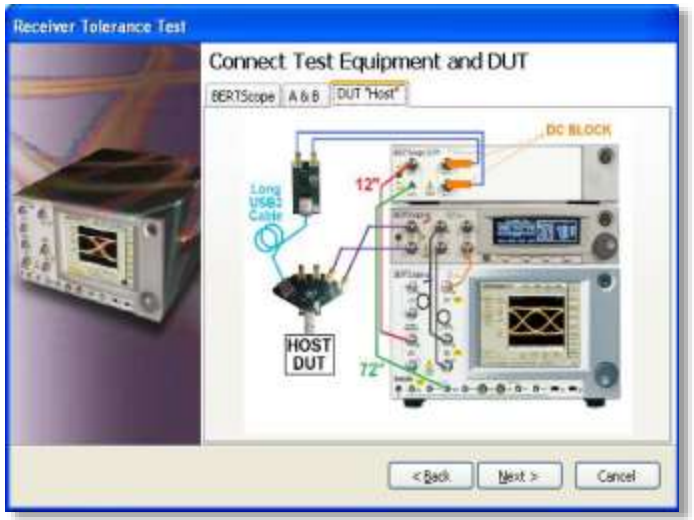
Channel

Test Equipment

SigTest Post-processing

RJ Source

SJ Source



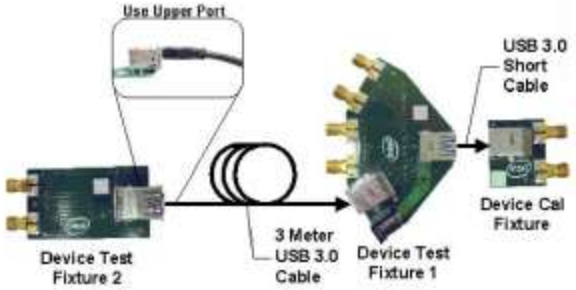
Mature standard with **fully automated** solutions for stress calibration and **good correlation**

Tektronix

USB 3.0 Calibration

- **Host Calibration Setup**

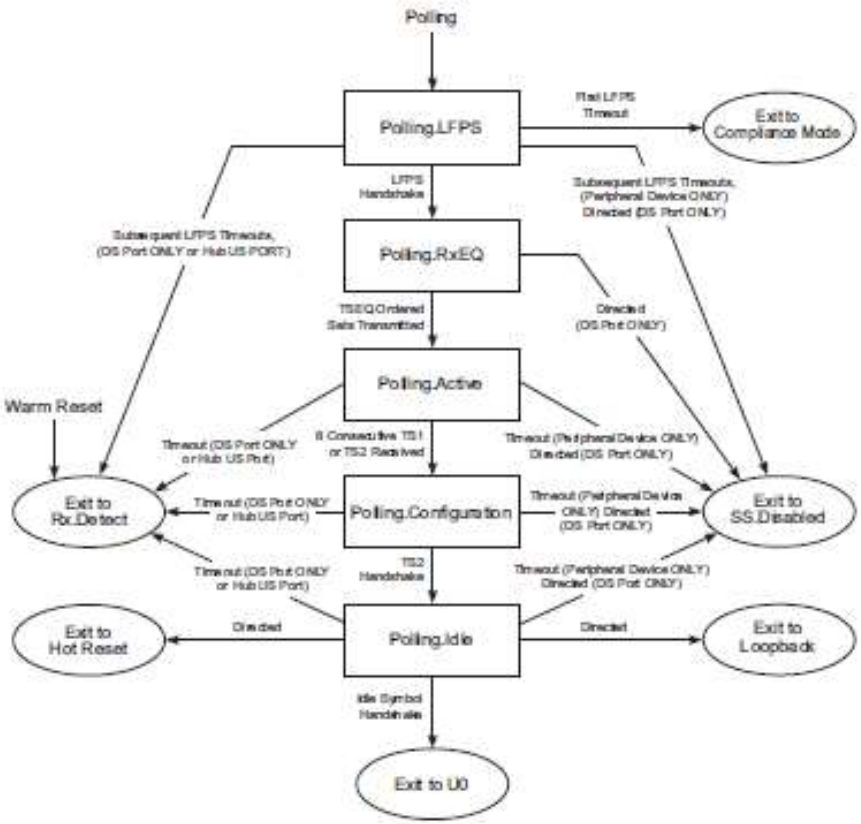
- **Device Calibration Setup**



- **Calibration Procedure**
  - ✓ Connect signal source directly to scope
  - ✓ Calibrate de-emphasis to 3.0 dB + 5/-0% dB using CP0 with SSC off and CTLE off
  - ✓ Connect signal source through the compliance channel
  - ✓ Measured peak to peak TJ
  - ✓ Calibrate RJ(2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10-10) with CP1 at the end of the channel applying CTLE and JTF
  - ✓ Calibrate SJ using CP0 until measured peak to peak TJ increases by that amount. Apply CTLE and set JTF at 50Khz.
  - ✓ Expected Tj with jitter off should be less than 100 ps. If this threshold is exceeded, replace the channel fixture(s) and/or cable(s).

USB 3 Loopback Negotiation

- **RX Detect**
  - SuperSpeed Link Partner is Availability is determined
- **Polling.LFPS**
  - DUT and Generator Send LFPS and establishes LFPS Handshake
- **Polling.RxEQ**
  - DUT and Generator send TSEQ in order to establish DUT RX Equalization Settings
- **Polling.Active**
  - DUT and Generator send 8 TS1
- **Polling.Configuration**
  - Generator instructs DUT to loopback by setting the loopback bit in the TS2 training sequence
- **Polling.Idle**
  - DUT directed to Loopback



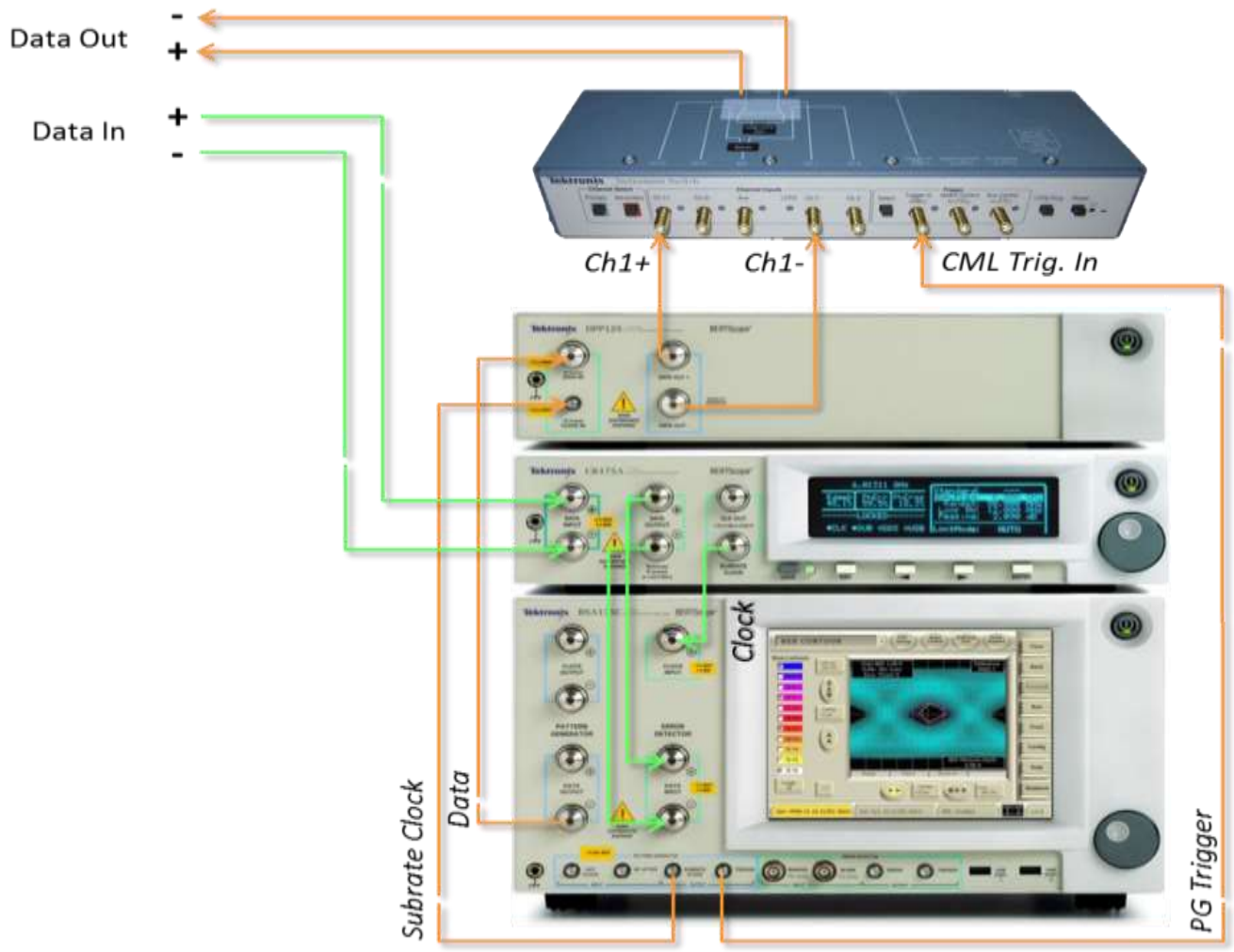
Tektronix

Two Solutions for USB 3.0 Receiver Testing

BERTScope BSA85C and AWG7122C

- **Tektronix has the right solution to meet your needs**
  - Both provide fully automated Receiver Compliance and Jitter Tolerance Testing
  - Both offer advanced impairments to debug problems caused by SSC or other anomalies
  - Both support a wide range of HSS Standards
  - Both support asynchronous clocking (SKP order set rejection)
- **BERTScope**
  - Performance that you need up to 26Gb/s for next generations standards including DisplayPort 1.2, SATA/SAS, 10G KR, PCI Express 3.0
  - Impairments can be changed on the fly to see the effect of increasing or reducing jitter
  - Debug and analysis tools enable quick identification of RX errors
  - True BER measurements
- **Arbitrary Waveform Generator**
  - Common platform for MIPI, HDMI, USB 3.0, and SATA
  - Only solution available that provides a common setup between transmitter and receiver testing without the need of RF switches and additional setup complexity
  - Easily apply sparameter models to verify designs under different channel conditions without the need of physical ISI channels
  - Generate SJ > 1Ghz to debug elusive problems caused by other system clocks

BERTScope USB 3.0 RX Test Configuration



USB Switch

creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

DPP125B
De-emphasis Processor

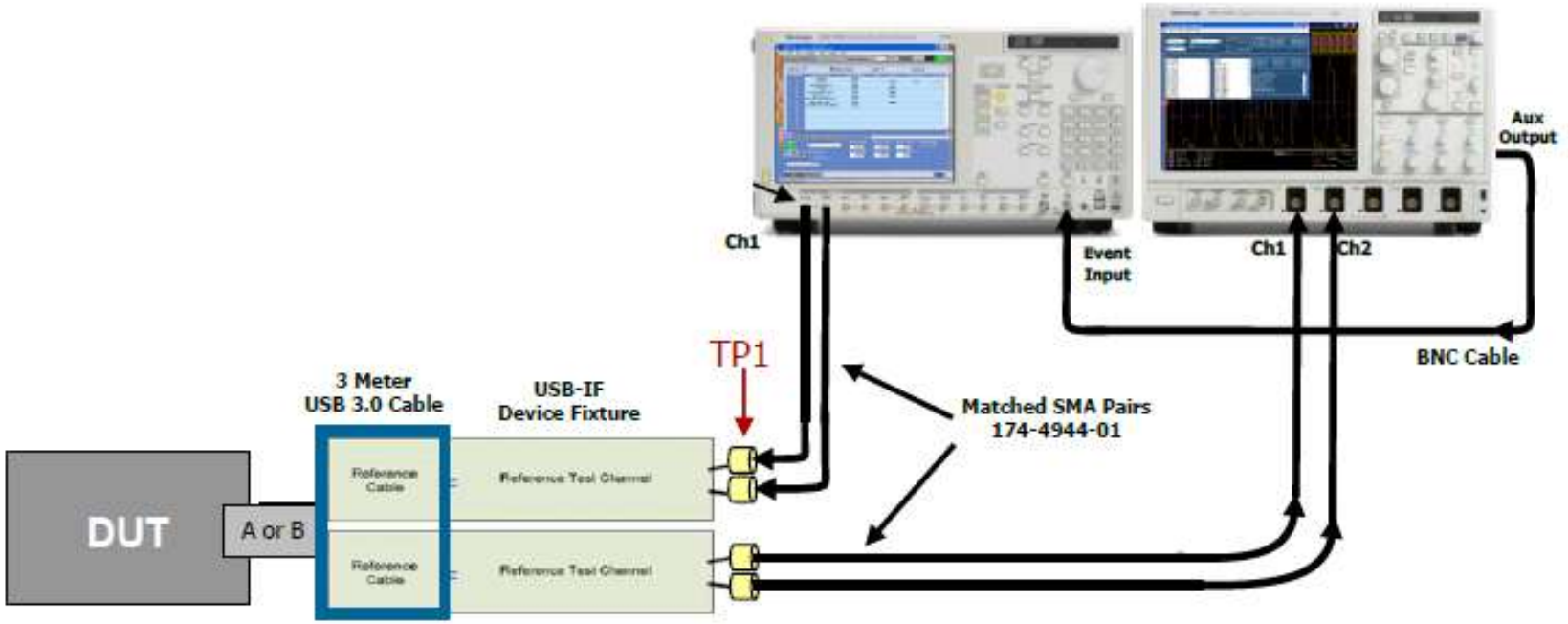
CR125A
Clock Recovery

BSA85C
BERTScope

Tektronix

AWG USB 3.0 RX/TX Test Configuration

- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)



Tektronix

Tektronix USB 3.0 Summary

- **Complete**
  - Solutions available today for USB3.0 Transmitter, Cable, Channel, and Receiver Testing
- **More than a Compliance Solution**
  - Solutions to meet debugging, characterization, and compliance needs
  - Receiver stresses that go beyond compliance
- **Increased Productivity**
  - Fully automated transmitter and receiver test solutions
  - Analysis tools integrated on the BERTScope enable the isolation and root cause determination of receiver errors
- **Performance**
  - 26Gb/s BERTScope provides coverage for next generation testing needs Low noise floor enables measurements of small data eyes for compliance testing and receiver calibration
  - Only 6.25Gb/s hardware serial trigger to capture protocol events that are causing failures or interoperability problems
- **Expertise**
  - Actively engaged in the USB Working Groups
  - Regional support by Tektronix Application Engineering Experts

Tektronix

Resources

Extensive application information at:

www.tek.com

USB: **USB-IF,** www.usb.org

Tektronix

Introduction to USB 3.0 SuperSpeedPlus

Tektronix®

Disclaimer

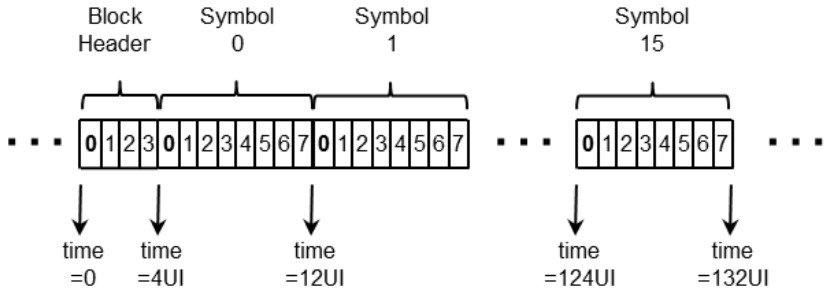
Presentation Disclaimer: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of USB-IF or other member companies.

USB 3.0 and 3.1 Comparison

	SuperSpeed	SuperSpeedPlus
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-20dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

128b/132b Encoding and Compliance Patterns

- 4-bit block header (0011 -> control, 1100 -> data)
- 128-bit (16 bytes) non-encoded payload
- Similar to PCI Express but with 4-bit header
  - 1 bit error (self correcting)
  - 2 bit error (detection)

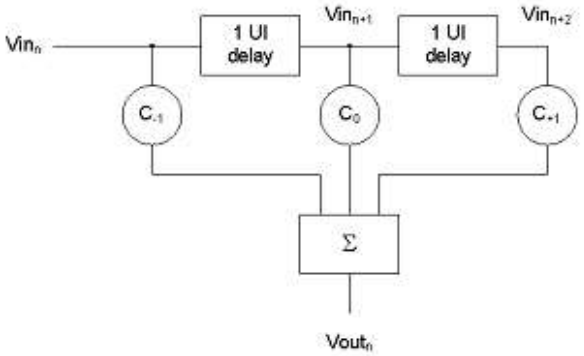


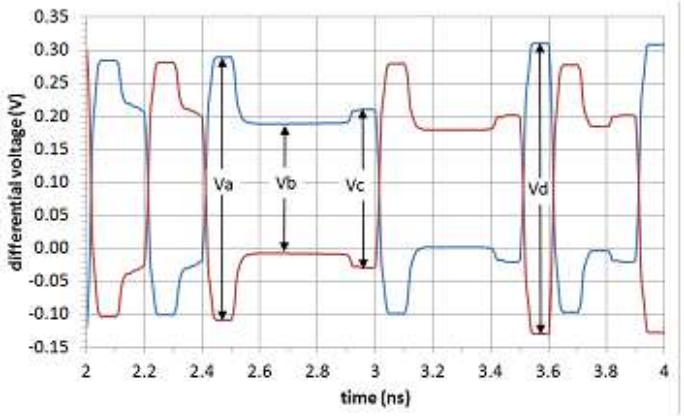
- Higher order scrambler (X^{23} vs. X^{16})
  - Improves EQ training with long, rich pattern
- Compliance with scrambled data (00h) and Nyquist (Ah)
- Pattern toggle between Gen1 and Gen2
  - Order TBD

Reference Transmitter Equalization

- USB channel profiles are dynamic (consumer)
- Need flexible solution space for link optimization
- Below are recommended Tx settings for good margin with target reference channels

Parameter	Value	Comments
Preshoot (dB)	2.2±1.0	***Normative requirement***
De-emphasis (dB)	-3.1±1.0	
C_{-1}	-0.083	Informative – for reference only
C_1	-0.125	
Nominal Boost (dB)	4.7	
Va/Vd	0.834	
Vb/Vd	0.584	
Vc/Vd	0.750	





$$preshoot = 20\log_{10}\left(\frac{V_{CP14}}{V_{CP15}}\right) = 20\log_{10}\left(\frac{Vc}{Vb}\right) = 20\log_{10}\left(\frac{-C_{-1}+C_0+C_1}{C_{-1}+C_0+C_1}\right)$$

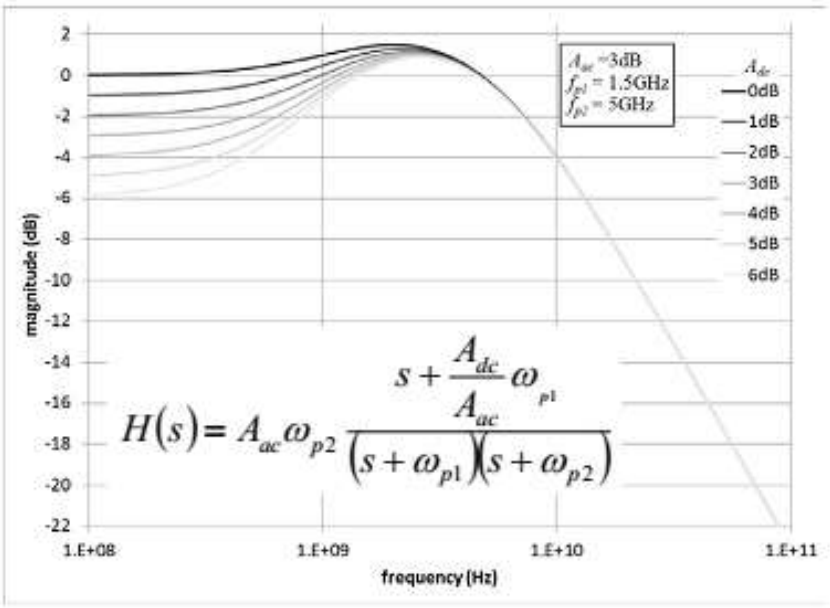
$$deemphasis = 20\log_{10}\left(\frac{V_{CP15}}{V_{CP13}}\right) = 20\log_{10}\left(\frac{Vb}{Va}\right) = 20\log_{10}\left(\frac{C_{-1}+C_0+C_1}{C_{-1}+C_0-C_1}\right)$$

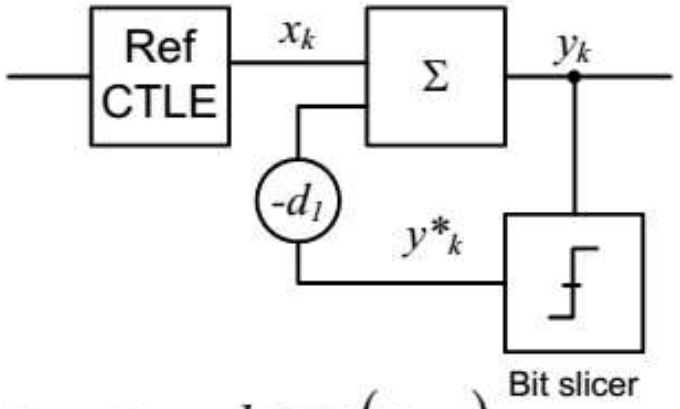
* TxEQ requirements defined by ECR.

Tektronix

Reference Receiver Equalizer

- seven pre-defined Rx EQ settings including CTLE gain and 1-tap DFE.
- Used for transmitter compliance testing
- Behavioral reference for receiver design



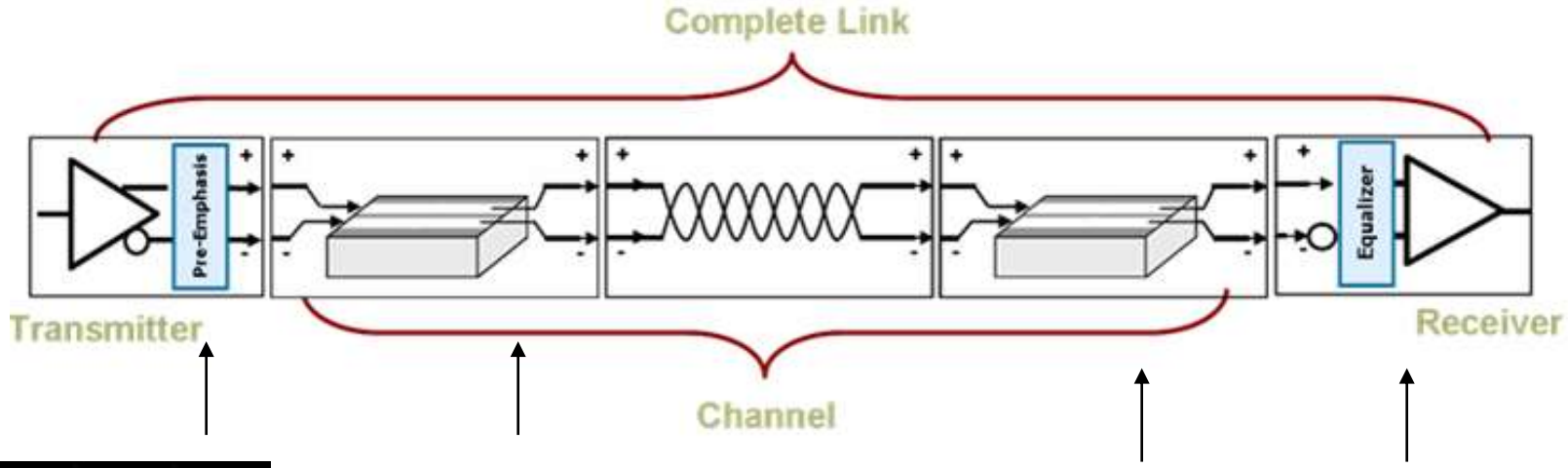


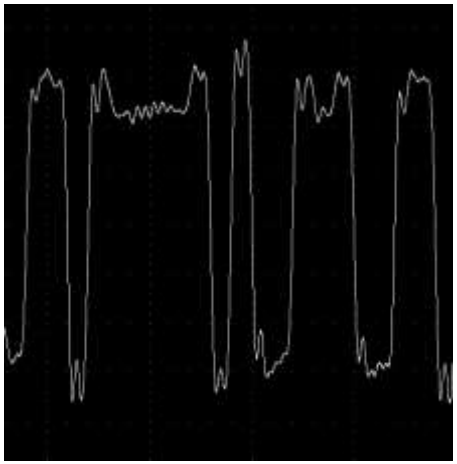
$$y_k = x_k - d_1 \operatorname{sgn}(y_{k-1})$$

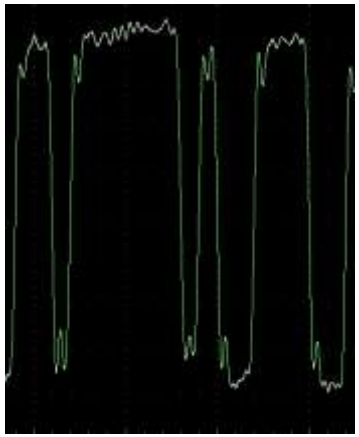
$$0 \le d_1 \operatorname{sgn}(y_{k-1}) \le 50mV$$

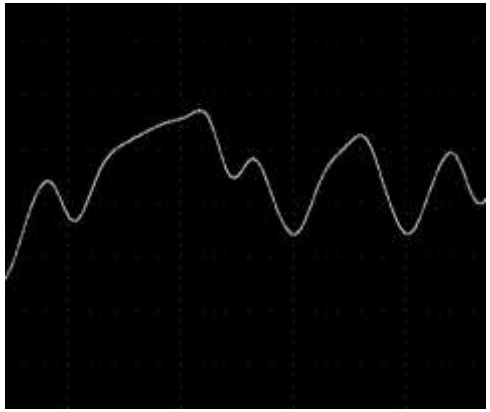
Tektronix

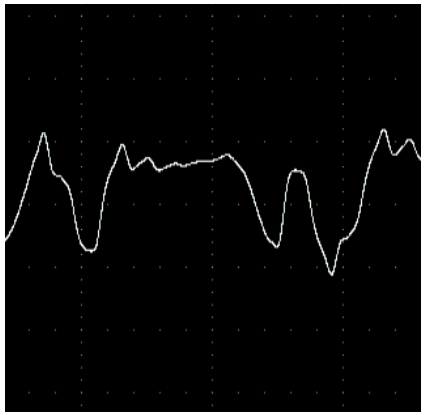
End-to-end PHY Validation











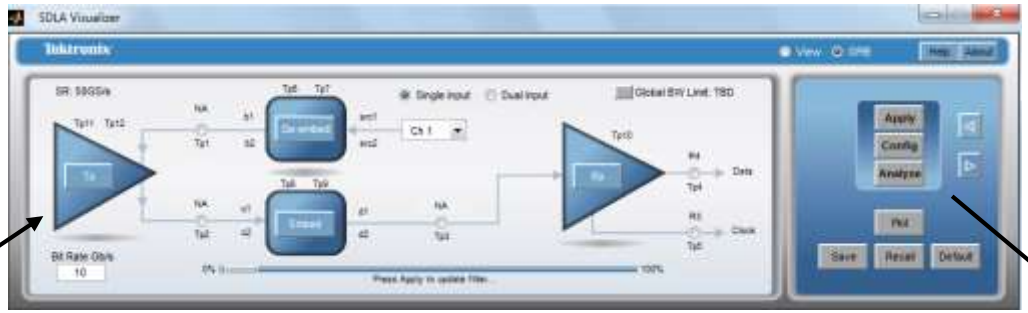
Tektronix

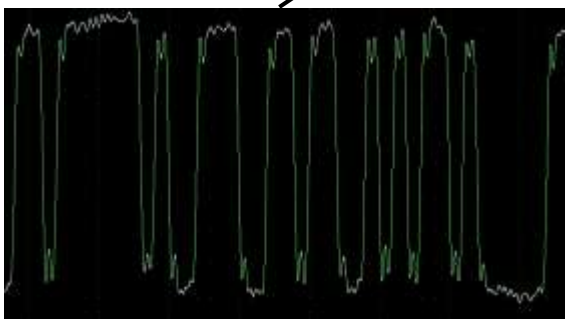
PHY Test Tools

- Similar process for USB 3.0 Gen1 Tx/Rx compliance testing
- Individual subsections (Tx, Rx, etc.) evaluated within system budget
  - ‘Far End’ Tx measurement including reference channels
- Next few slides outline current approach for electrical validation
- Let’s start with an example for Tx

Transmitter Validation Example - SDLA

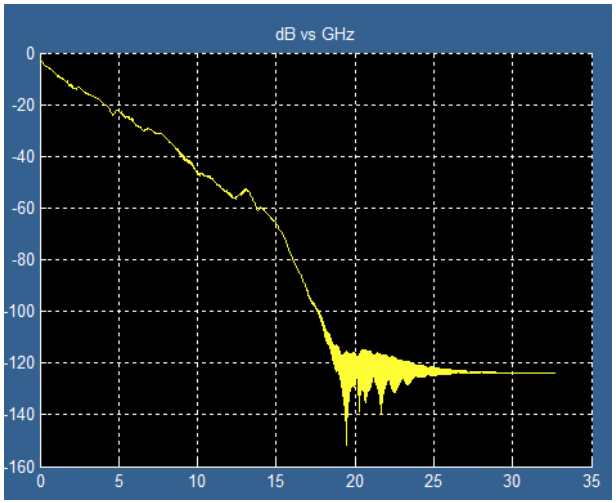
- Capture CP9 (Scr0) and CP10 (Ah)
- Input reference channel models

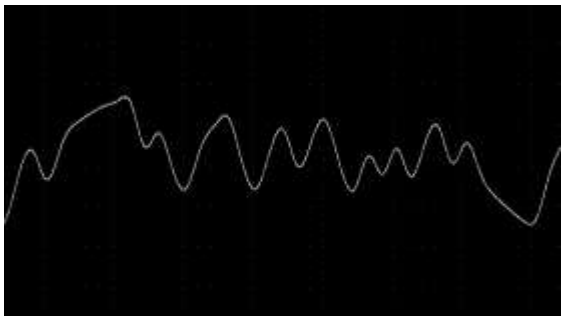




CP9 Scrambled Pattern (TP0)

USB3 Reference Channel



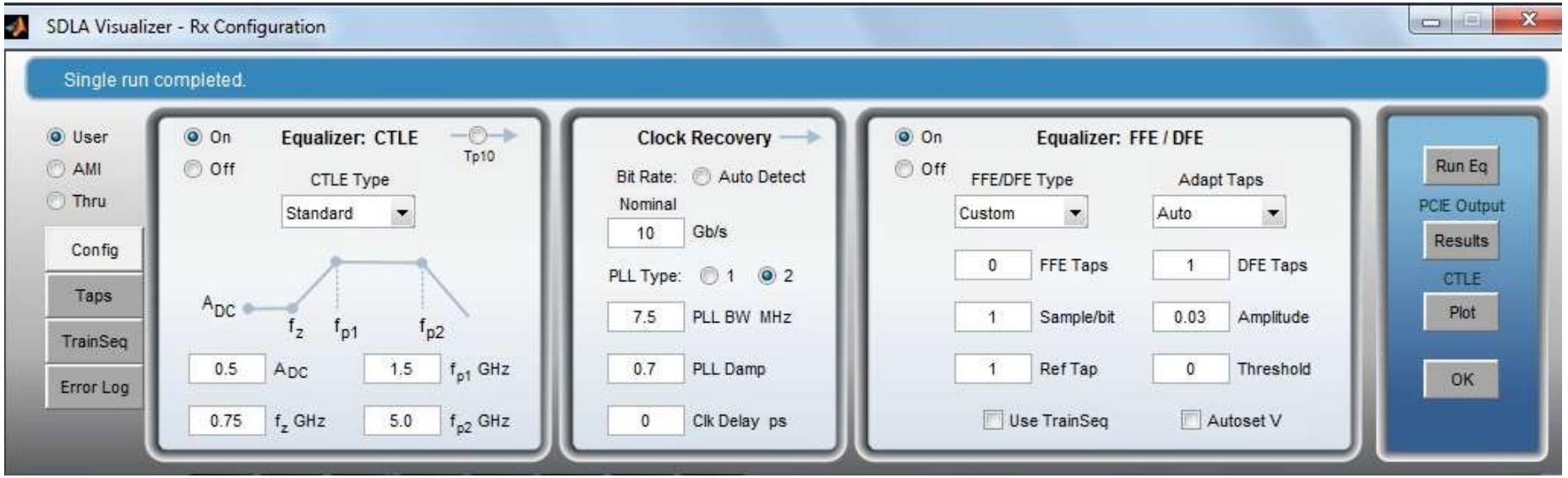


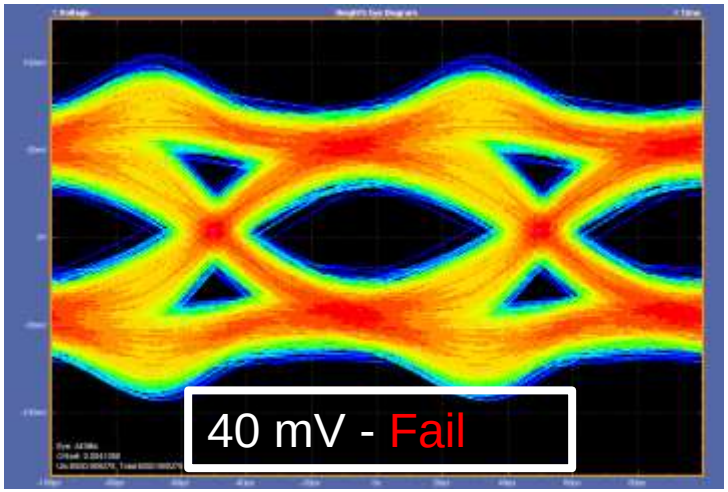
CP9 Scrambled Pattern (TP1)

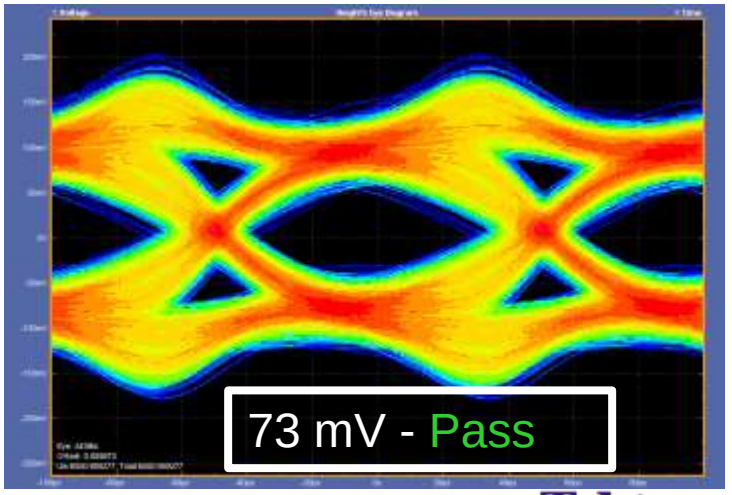
Tektronix

Transmitter Validation Example - SDLA

- Find optimum Eye height vs. Rx EQ



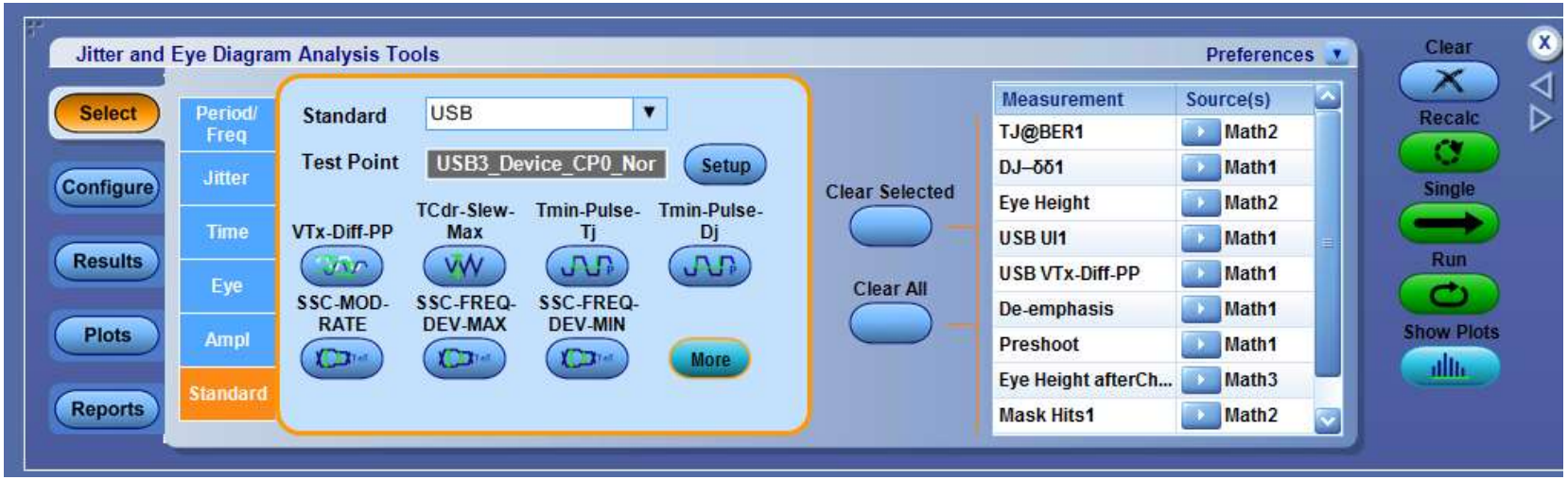




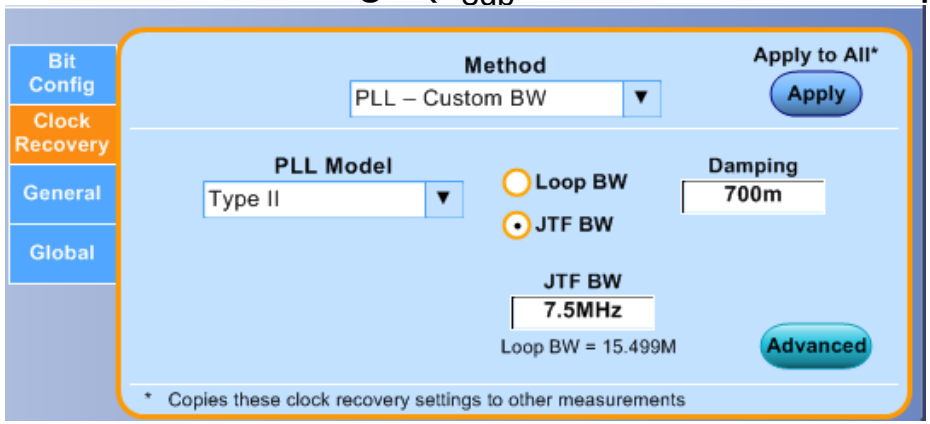
Tektronix

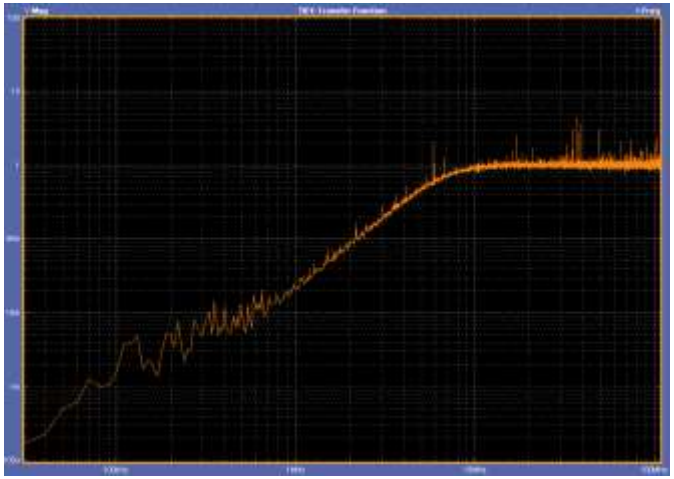
Transmitter Validation Example - DPOJET

- Recall DPOJET SSP setups



- Check JTF settings (f_{-3db} 7.5 MHz, 40dB slope)

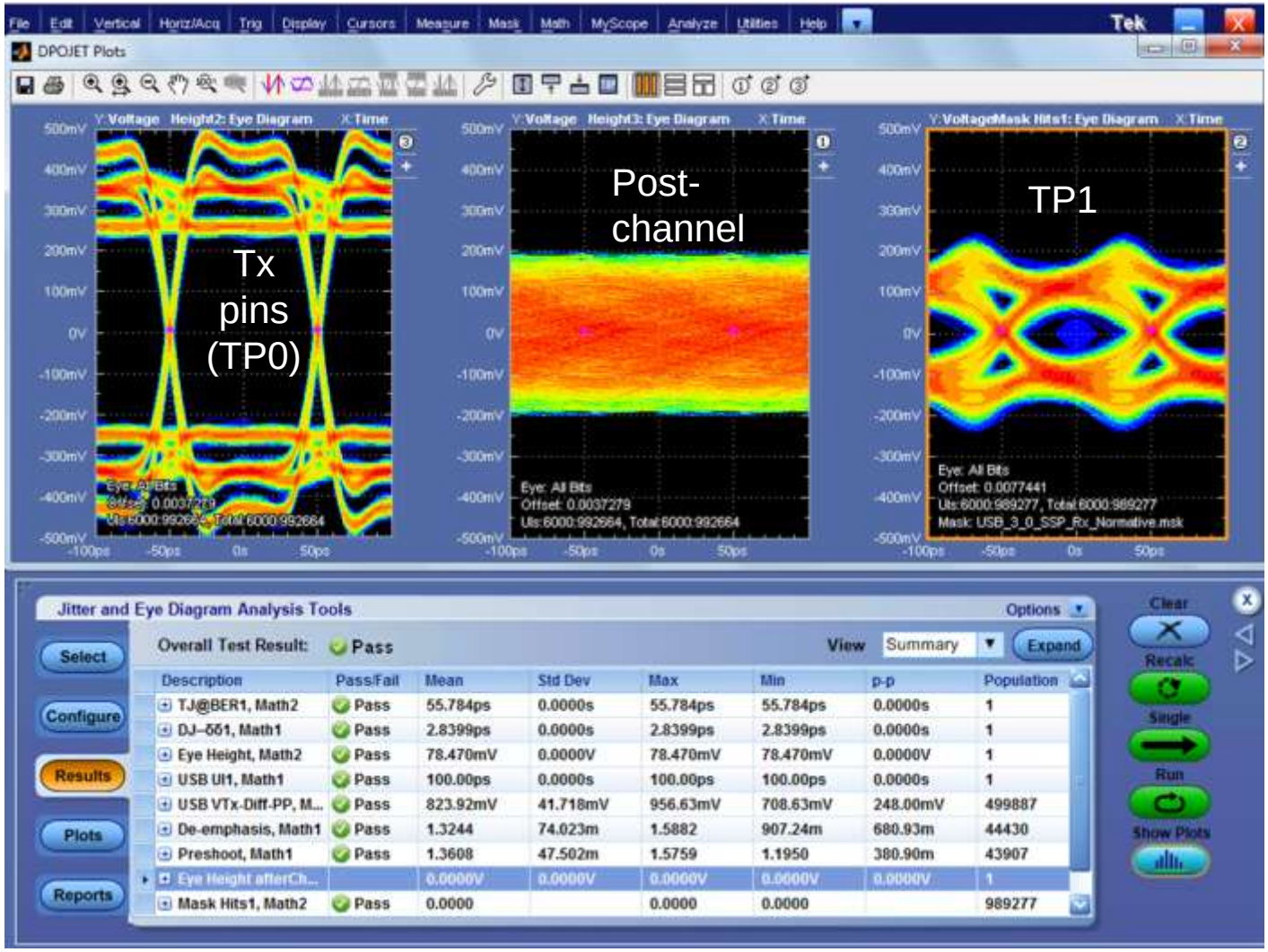




Tektronix®

Transmitter Validation Example - DPOJET

- Measure Eye height and jitter at TP1



Tektronix

Recommended Transmitter Solution

- ≥20 GHz BW, 100 GS/sec preferred
  - DSA72004C or higher recommended
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation. Increase memory depth if interpolation will be enabled, or if >1MUI captures are desired.
- Option DJA Advanced DPOJET required, signal analysis
- Option SLA Advanced SDLA required, cycle through 7 CTLE/1 DFE settings
- Option USBSSP-Tx recommended, provides USB3 TX specific measurements

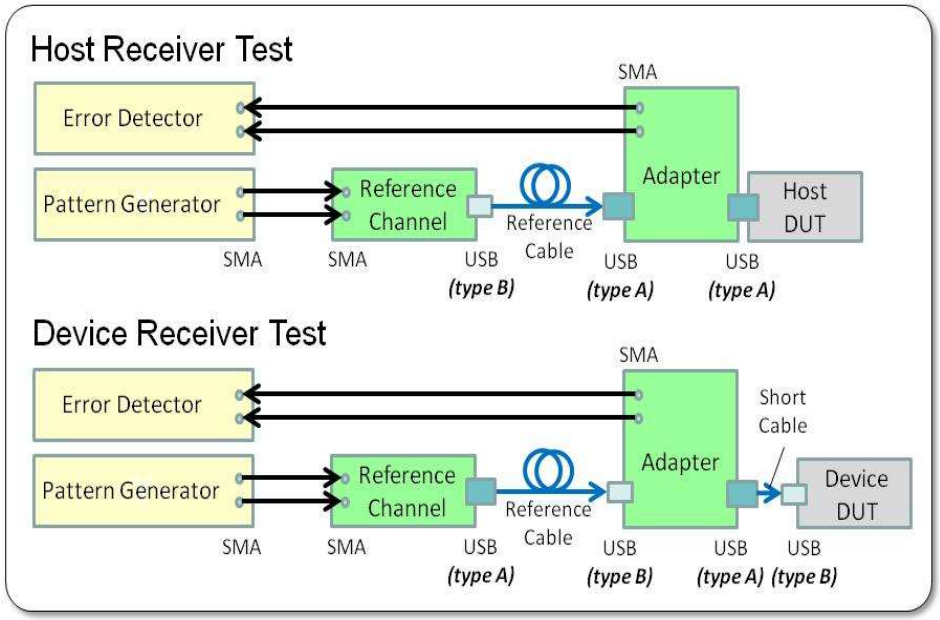
For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.

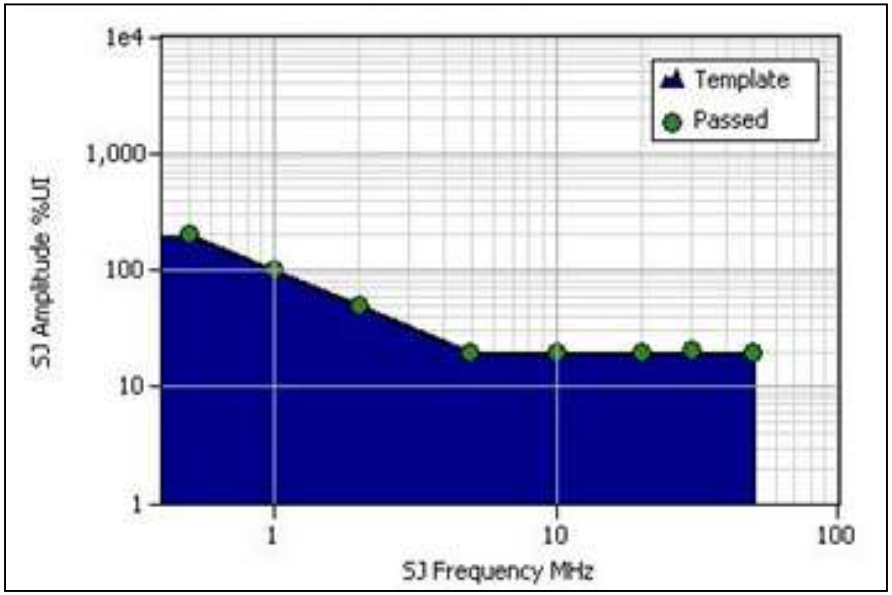
USB 3.1 Gen2 (Option SSP)

USB 3.1 Gen1/2 (Option USBSSP-TX)

Receiver Testing

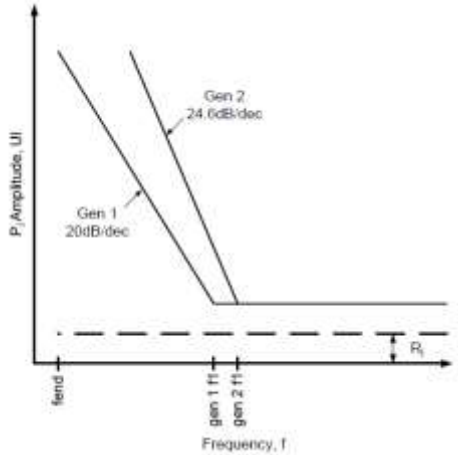
- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions





Tektronix

JTOL Template Comparison



Receiver Jitter Tolerance

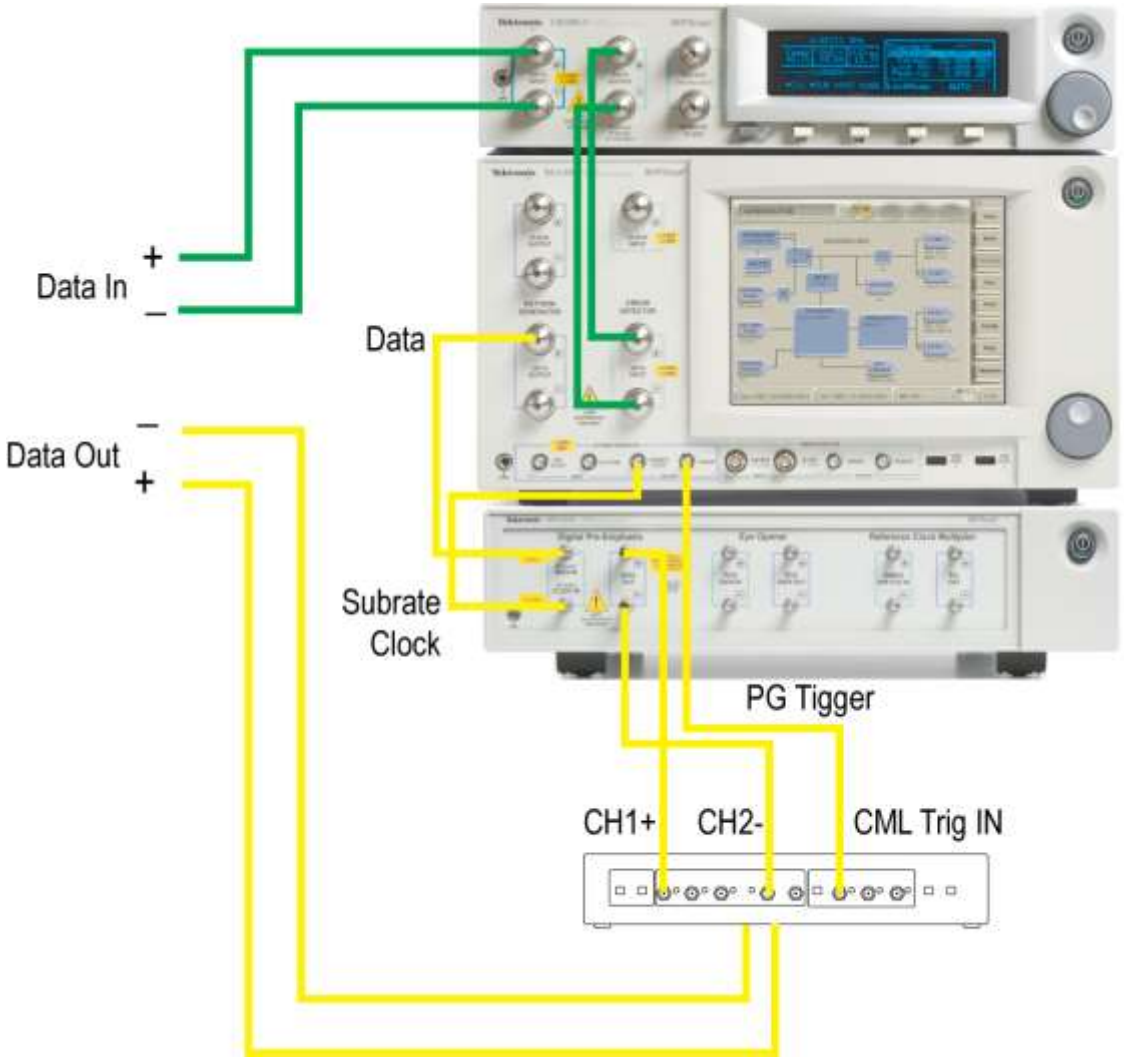
Symbol	Parameter	Gen 1	Gen 2	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.141	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	2.56	UI p-p	1,2,3
J_{Pj_1Mhz}		1	1.28	UI p-p	1,2,3
J_{Pj_2MHz}		0.5	0.64	UI p-p	1,2,3
J_{Pj_4MHz}		N/A	0.32	UI p-p	1,2,3
J_{Pj_f1}		0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}		0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}		N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	TBD	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.2 Post= -3.1	dB	1

Notes:
1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-19.

* Rx Jtol RJ & Tx EQ updated by ECR.

Tektronix

BERTScope USB 3.1 RX Test Configuration



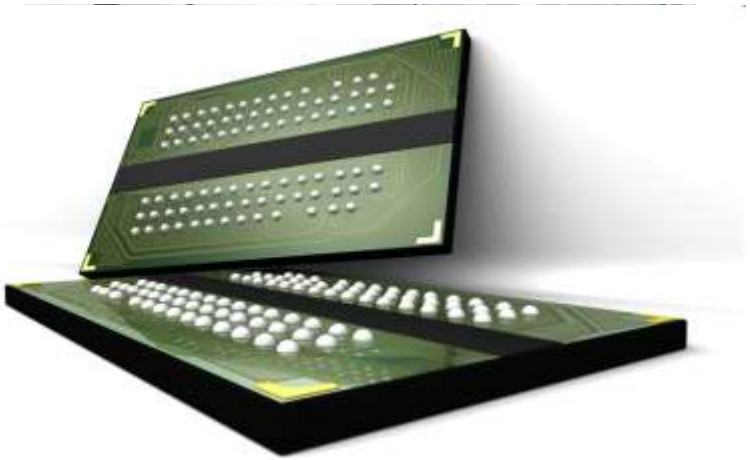
Tektronix

Summary

- New opportunity for growth with USB 10 Gb/s
- Adds additional challenges beyond legacy requirements (backwards compatibility)
- Higher performance, more complex design but feasible within current infrastructure
- Extensive PHY validation tools for early designs
  - New USB SSP DPOJET setups for Tx validation
  - BERTScope USB library with JTOL templates
  - DSA8300 Sampling oscilloscope for channel characterization
  - Test procedures documented in Methods of Implementation (MOI)

Tektronix®

Memory Interface Verification and Debug



Tektronix®

Memory Validation Challenges

Speed

Upward trend to meet the ever increasing application needs

Widely used High Speed Parallel Bus, resulting in more signal integrity issues

I/O Voltage

Downward Trend to improve Battery Life in portable devices

Reduce power consumption in Data Centers resulting in smaller data eyes

Capacity

Upward Trend, Multi-Core CPU's ability to handle large data sets

Multiple Channels, Slots per Channel, Ranks per Slot introduces probing complexity

Form Factors

DIMM, SODIMM, RDIMM, LRDIMM, PoP, BGA

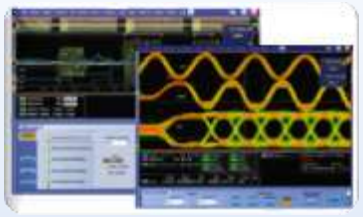
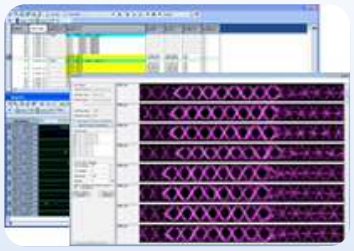
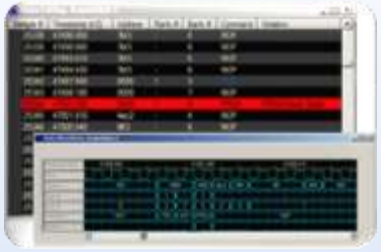
Multiple form factors for different applications needs introduces probing complexity

System level Visibility

Critical cross bus dependencies increase with speed

Signal Access and Time-correlated visibility across multiple buses

Memory Validation Continuum

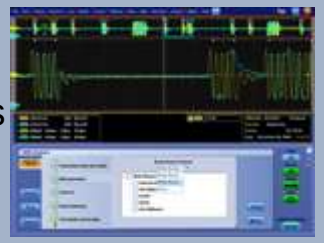
	Analog Validation	Digital Validation	Execution Validation
Instruments			
Probes			
Analysis SW			

Tektronix®

DDR Analog Verification and Debug

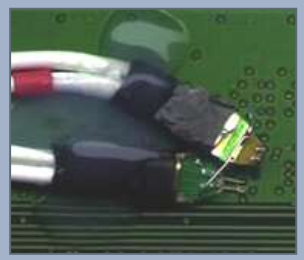
Signal Acquisition

- Automatically trigger and capture Memory Interface signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis



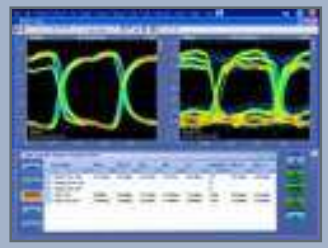
Signal Access - Probing

- Easy but reliable physical connectivity
  - access to various measurement points on DRAM device
- Maximum signal integrity
  - sufficient performance for signal speeds



Signal Analysis

- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator



Tektronix®

Signal Acquisition and Analysis

Triggering, ASM, DDRA and DPOJET

Tektronix®

DDRA Features and Benefits

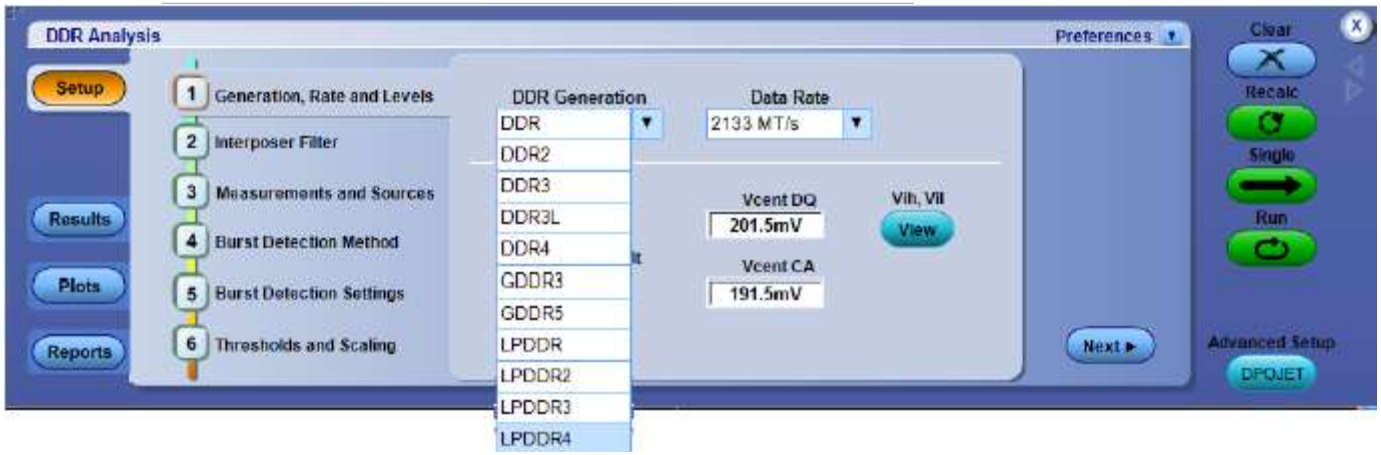
Complete Solution for Memory Interface Physical Layer Test

Feature	Benefits
Memory Validation and Debug	Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3 the newest standards targeted for Server/Computer and Mobile handsets.
Selectable Speed Grades	Support for various JEDEC specification defined speed grades as well as custom speeds
Auto Configuration Wizard	Easily set up the test configuration for performing the analysis.
Qualified Multi-Rank Measurements	Isolate measurements to a rank of interest by using the chip select signal in a multi rank configuration
Cycle Type Identification	Navigate and Timestamp all the READ and WRITE cycles in an acquired record using Search and Mark
Visual Trigger / Pin Point Triggering	Quickly trigger, isolate and capture events of interest with Pin-Point HW Triggering combined with Visual Trigger and Active Search and Mark capabilities in Tektronix Oscilloscopes, making them an indispensable tool for Memory Interface Validation.
De-embedding	De-embed the effects of the Interposers and Probes to provide more accurately representation of the signal.
Test Selection	Provides the ability to select the Memory specification and the Speed Grade against which the analysis needs to be done as well as individual tests or group of tests to perform targeted analysis.
Reporting	Automatically generate consolidated reports that include pass/fail results, statistical measurement information as well as details about the test setup
Conformance and Debug	Quickly switch into debug mode in case a system fails conformance tests and use the DPOJET jitter analysis package
Probing Solutions	P7500 Trimode Probe Family and Micro-Coax Tips combined with Nexus Technology Interposers for various memory standards and packaging types results in a complete probing system that provides easy access to memory interface signals and allows making differential, single-ended, and common mode measurements accurately and definitively
Digital Channels on MSO	Address/Command signals acquired on the digital channels of the Mixed Signal Oscilloscope can be used to precisely qualify bus cycles or events of interest as well as perform timing measurements
Analysis and Debug Tools	Tektronix provides a broad range of tools for Electrical Test, Logic Debug and Execution Validation.

Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
LPDDR4	JESD209-4
GDDR5	JESD212



Tektronix®

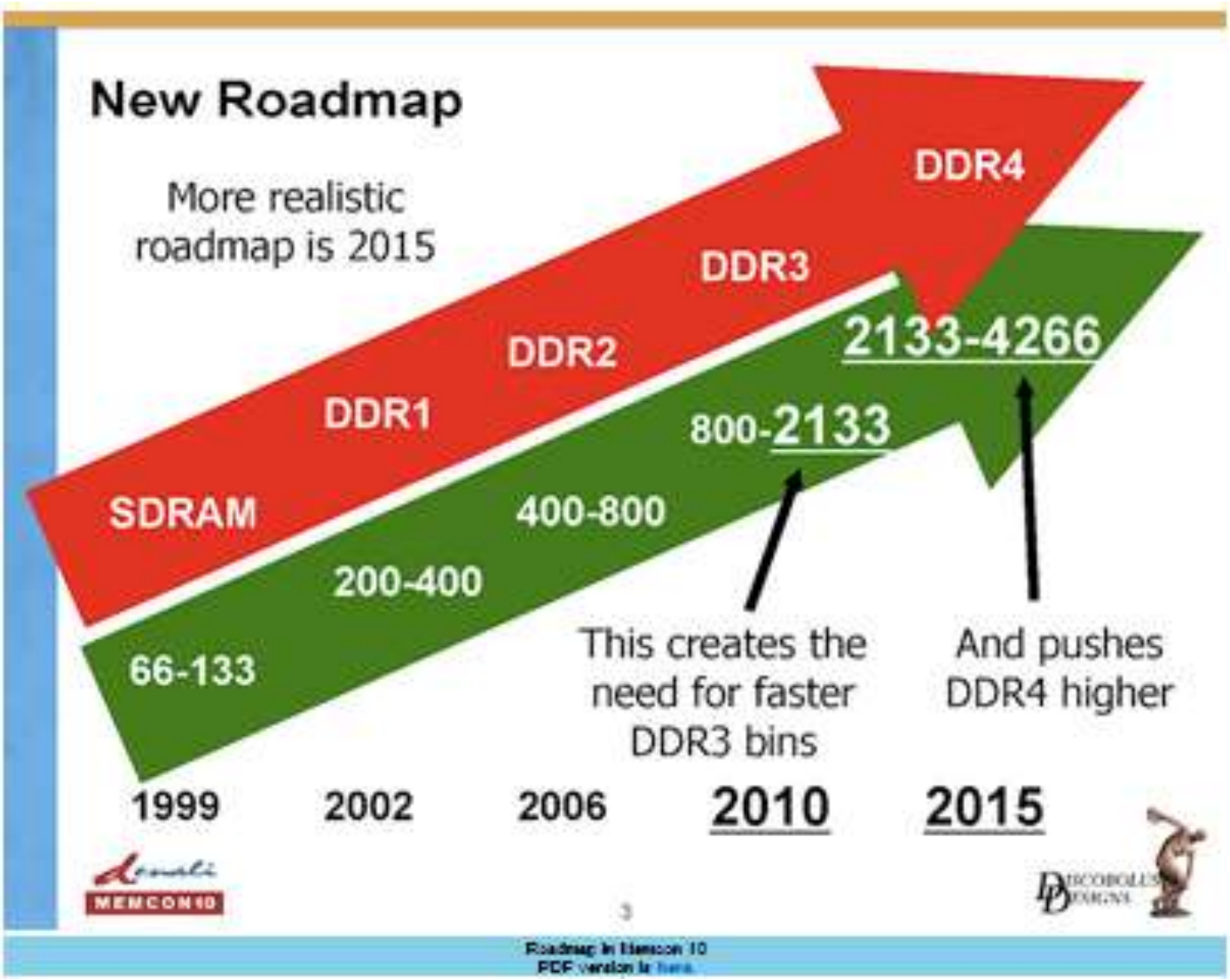
Memory Technology Overview

- DRAM - Dominant Memory Technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMM, SODIMM
  - Embedded systems
    - Cell phones, Ultra-Thin Notebooks, iPADs
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR4 release on 26th Sep 2012 Maximum 3200 MT/s data rates transfer
    - LPDDR3-E planned can go unto 2133MT/s
    - DDR3L* operates at 1.35V

  *The "L" in DDR3L stands for low-voltage 1.5V – DDR3

- DRAM variants
  - DIMM based - Speed and Performance
    - DDR, DDR2, DDR3 and DDR4
  - Low Power DDR
    - LPDDR, LPDDR2, LPDDR3, LPDDR3E, LPDDR4
  - Graphic DDR - Optimized for Speed - faster access
    - GDDR3, GDDR5 @ 5500 MT/s
  - Low Voltage DDR
    - DDR3L, DDR3U

Memory Market Trends – Main Stream



Tektronix®

Memory Market Trends - LPDDR

Mobile DRAM Technology Trend

- **Bring up right technology at right on time**
  - LP2-800 ('10) → LP3-1600('12) → LP4-3200('14)

	'10	'11	'12	'13	'14	'15
Interface VDD/VDDQ	LPDDR2 1.2V/1.2V		LPDDR3 1.2V/1.2V		LPDDR4	
				WIO and WIO2		
Speed	6.4GB/s	8.5GB/s	12.8GB/s		25.6GB/s+	
Density	2Gb	4Gb			8Gb	
PKG	Up to 4 die stacks : 1.0 mm → 0.9mm and below					

*Source : Samsung Presentation JEDEC Mobile Event Seoul

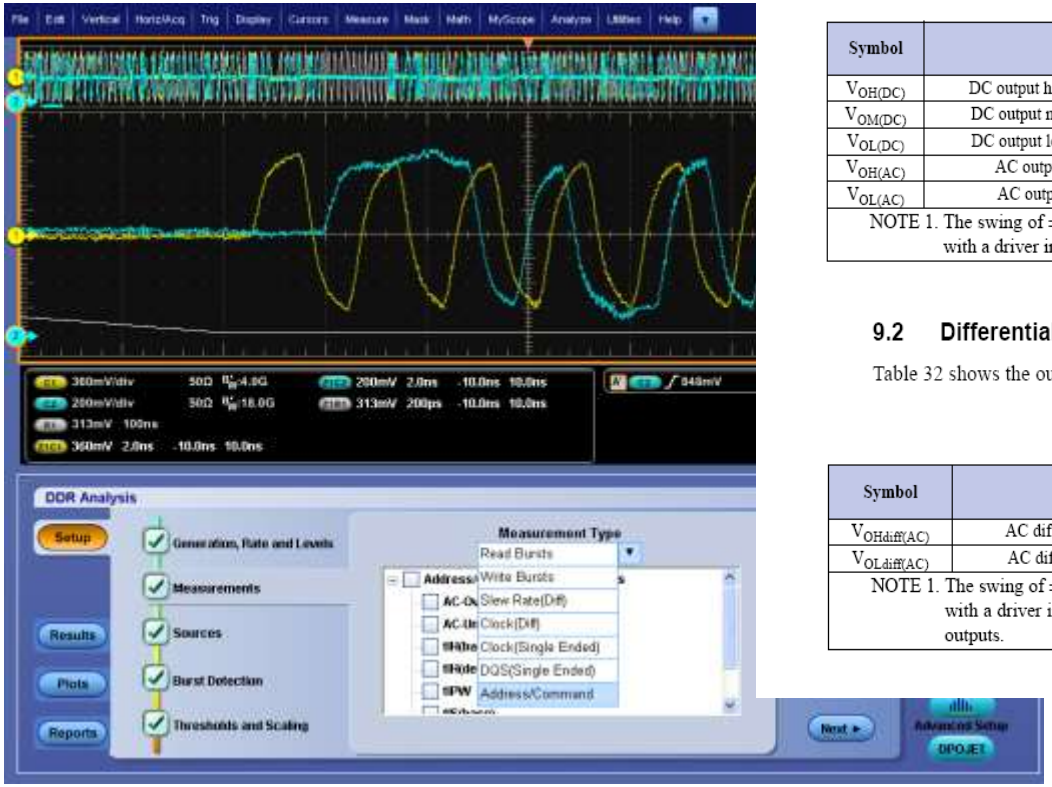
Oscilloscope Bandwidth Requirement

Memory Technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4	LPDDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s	to 4267MT/s
Max slew rate	5	5	5	10	12	12	8	18	18
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8	0.3
20-80 risetime (ps)	216	150	150	60	50	45	45	27	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0	15.0
Recommended Scope BW (Max Performance)	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16	16
Recommended Scope BW (Typ Performance)	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5	16

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 LPDDR3 and LPDDR4 is supported only on DSA/MSO/DPO70000C/D models only
- LPDDR4 is a separate license

Specialized Measurements for DDR

- JEDEC Standards specify measurements & methods



9 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

Table 31 — Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1
NOTE 1. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2.				

9.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of differential signals.

Table 32 — Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1
NOTE 1. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.				

Tektronix®

DDR4 DDRA Measurements

Broad range of JEDEC-specified measurements

- Example measurements list for DDR4

Write Burst
Data Eye Height
Data eye Width
tDQSH
tDQSL
tDSS-Diff
tDSH-Diff
tDVAC(DQS)
tDQSS-Diff
tWPRE
tWPST
TdIPW-High
TdIPW-Low
VIHL_AC
SRIN_dIVW_Rise
SRIN_dIVW_Fall

Clock Single Ended
Vix(ac)CK
VSEH(CK)
VSEH(CK#)
VSEL(CK)
VSEL(CK#)
AC-Overshoot(CK)
AC-Overshoot(CK#)
AC-Undershoot(CK)
AC-Undershoot(CK#)
AC-OvershootArea(CK)
AC-OvershootArea(CK#)
AC-UndershootArea(CK)
AC-UndershootArea(CK#)

Read Burst
Data Eye Height
Data eye Width
tRPRE
tRPST
tQSH
tQSL
tDQSCK-Diff
tDQSQ-Diff
tQH
tDVAC(DQS)
SRQdiff-Rise(DQS)
SRQdiff-Fall(DQS)
SRQse-Rise(DQ)
SRQse-Fall(DQ)
tLZ(DQ)
tHZ(DQ)
tLZ(DQS)
tHZ(DQS)

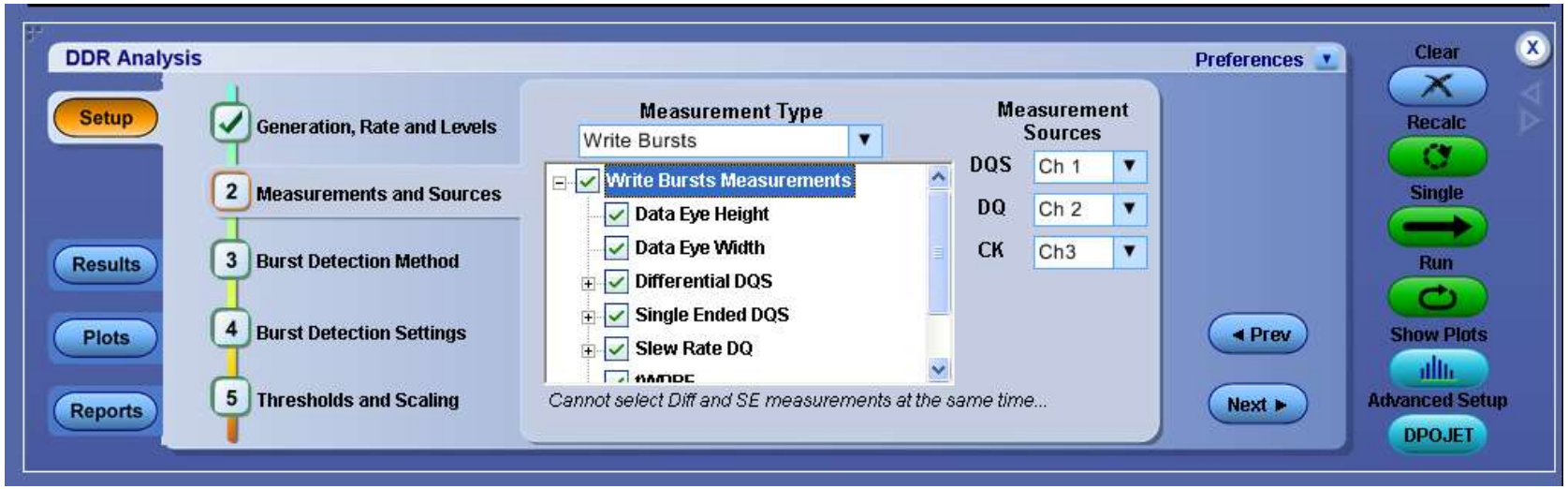
Address/Command
tIPW-High
tIPW-Low
AC-Overshoot
AC-Undershoot
AC-OvershootArea
AC-UndershootArea

Clock(Diff)
tDVAC(CK)
InputSlew-Diff-Rise(CK)
InputSlew-Diff-Fall(CK)
tCK(avg)
tCH(avg)
tCL(avg)
tCK(abs)
tCH(abs)
tCL(abs)
tJIT(duty)
tJIT(per)
tJIT(cc)
tERR(2per)
tERR(3per)
tERR(4per)
tERR(5per)
tERR(6per)
tERR(7per)
tERR(8per)
tERR(9per)
tERR(10per)
tERR(11per)
tERR(12per)
tERR(Nper) n - 13 TO 50

DQS(Single Ended)
AC-Overshoot(DQS)
AC-Overshoot(DQS#)
AC-Overshoot(DQ)
AC-Undershoot(DQS)
AC-Undershoot(DQS#)
AC-Undershoot(DQ)
AC-OvershootArea(DQS)
AC-OvershootArea(DQS#)
AC-OvershootArea(DQ)
AC-UndershootArea(DQS)
AC-UndershootArea(DQS#)
AC-UndershootArea(DQ)
Vix(ac)DQS
VSEH(DQS)
VSEH(DQS#)
VSEL(DQS)
VSEL(DQS#)

Test Setup and Configuration

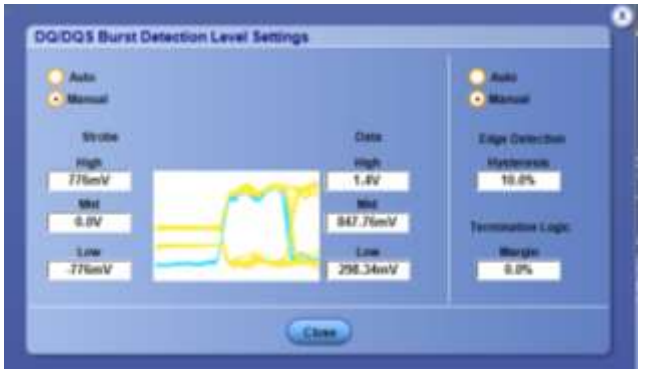
- All the tests are logically grouped based on the input source requirement
  - READ
  - WRITE
  - CLOCK
  - ADDR/CMD
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.
- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.

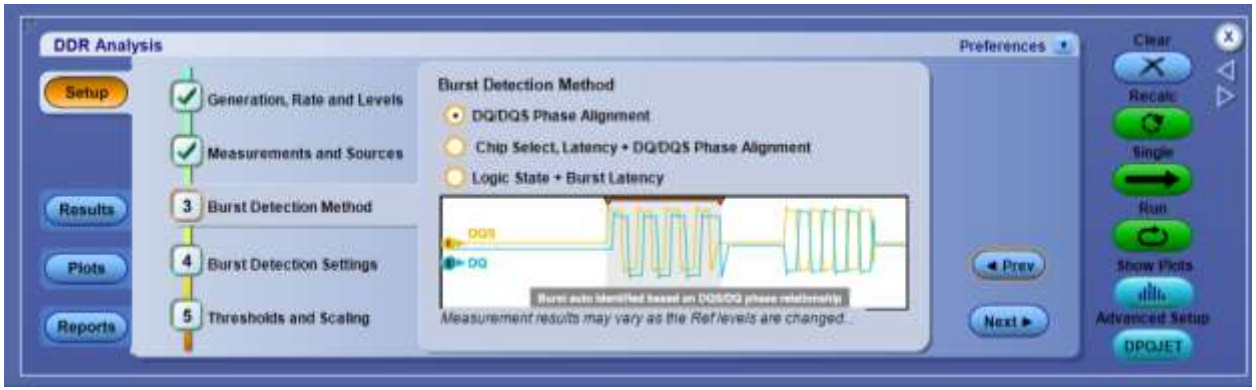


Tektronix

Burst Detection

- Read / Write bursts are automatically detected for analysis purposes
- Several different techniques are used for Read/Write Burst Separation
  - DQ/DQS phase alignment: DQ and DQS have different phase relationship in Read and Write bursts
  - CS, Latency + DQ/DQS Phase Alignment: CS is used to quality the occurrence of a burst, followed by DQ/DS phase relationship to distinguish between Read/Write
  - Logic State + Burst latency: The command bus probed using the digital channels on the MSO is used to identify Read/Write commands on the command bus are quality and distinguish Read and Write bursts
- Options are provided to adjust the levels to improve burst detection in systems with lower signal integrity



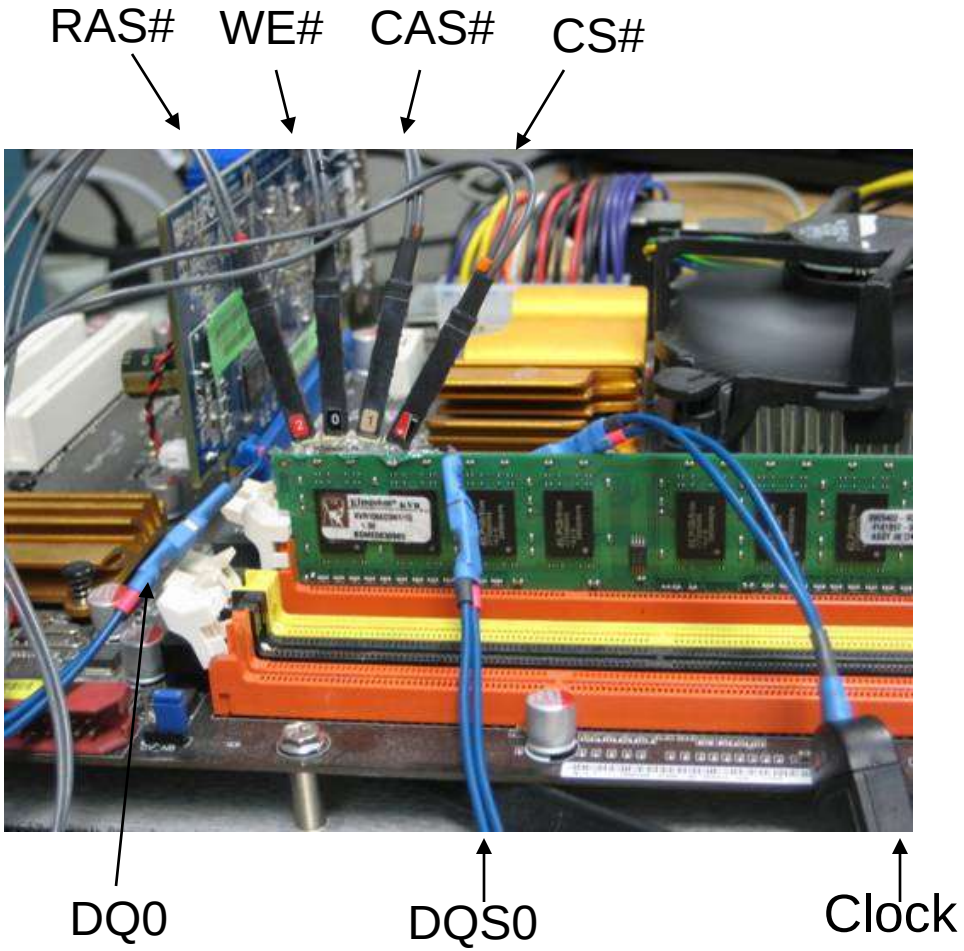


Tektronix

Digital + Analog Probing for MSO70K

- 16 Digital Channels in addition to 4 Analog Channels

#TSF Format	Type
#File Radix	
#+ Version 2.1.0 PATTERN	
#Command	Command
#Symbol Name	Pattern
#	CS RAS CAS WE (D3 D2 D1 D0)
#	
MODE_REG	0000
REFRESH	0001
PRECHARGE	0010
ACTIVATE	0011
WRITE	0100
READ	0101
NOP	0111
DESELECT	1XXX



Tektronix®

Uncompromised Analog/Digital Acquisition

Banner Specifications		
Analog		
Bandwidth 20 GHz on all 4 channels simultaneously	**Sample Rate** 50 GS/s on all 4 channels simultaneously	**Record Length** 250 M pt max. on all 4 channels simultaneously
Digital		
Bandwidth 2.5 GHz Analog BW with iCapture for 16 Logic channels	**Timing Resolution** 80 ps on 16 logic channels	**Record Length** 250 M pt max. on 16 logic channels

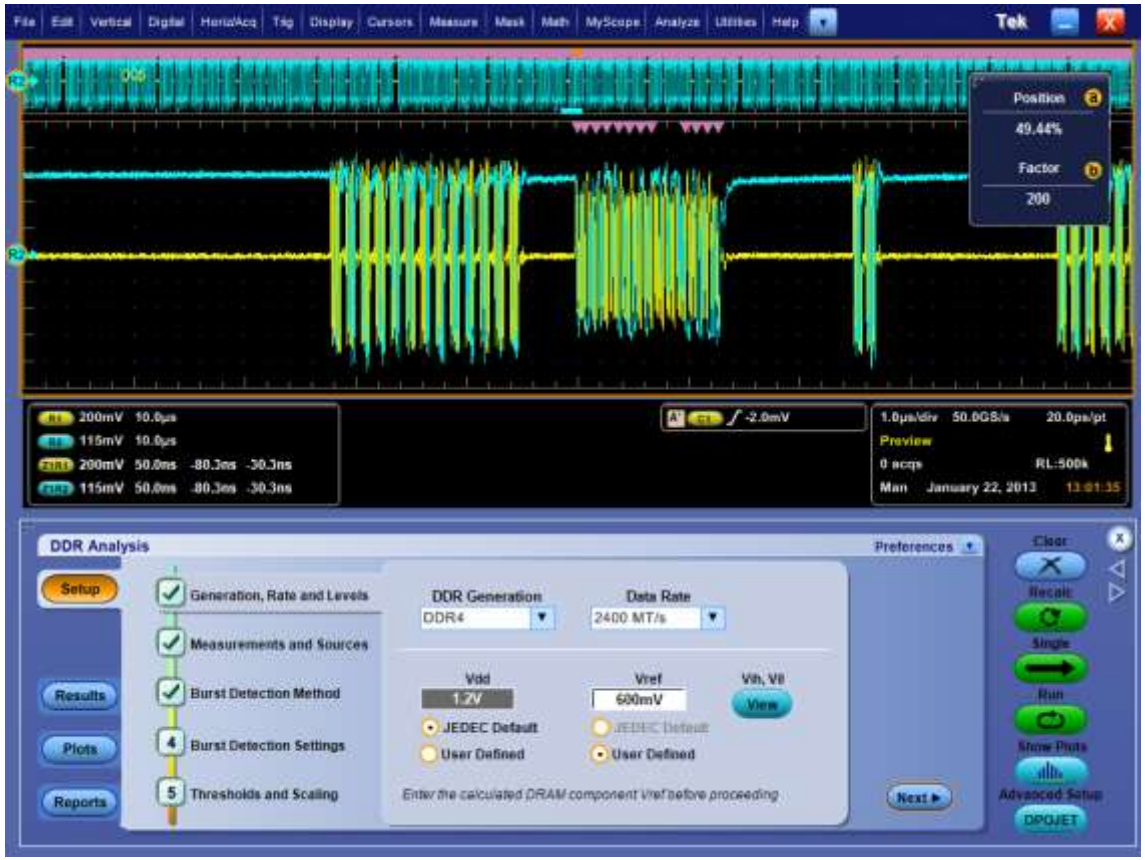
Tektronix®

MSO DDRA Integration – makes a powerful tool

- DDRA integrated with MSO 70k Digital channels
  - **Makes a perfect tool for DDR Analysis.**
- The following is a direct quote from an Agilent application note, evaluating different approaches to DDR PHY-layer testing:
  - "By connecting the control signals to the MSO's digital inputs, you can trigger on different operation modes (read, write, etc)… However, the MSO solution has low bandwidth… Otherwise, an MSO is a *perfect solution* for DDR signal debugging."

Burst Detection

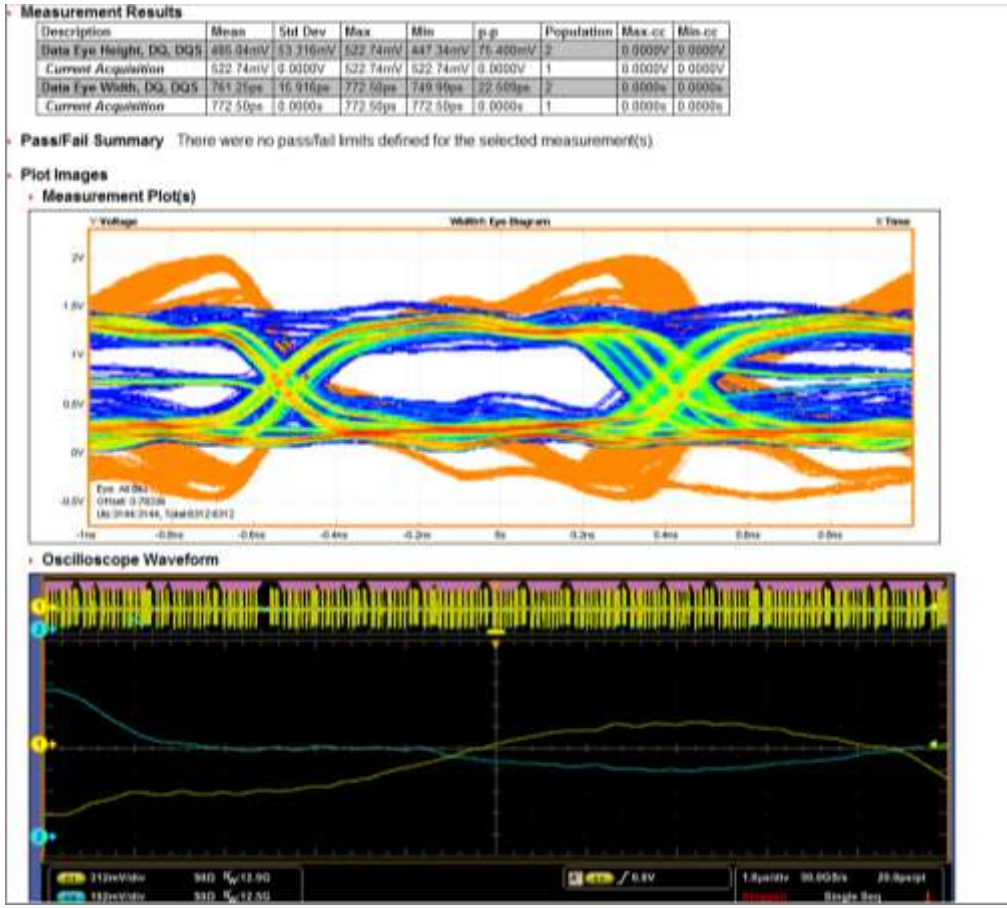
- Easily Identify, Mark & Measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL Reads/writes within an acquisition

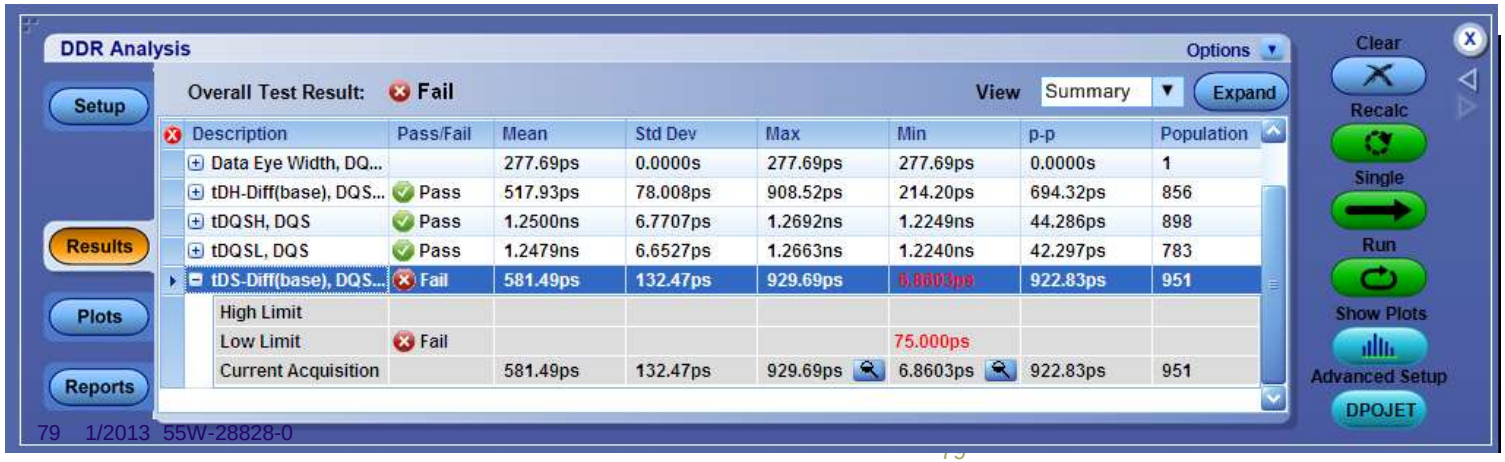


Tektronix®

Reports

- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes
  - Measurement results
  - Pass/Fail test results based on specification values
  - Summary and detail plots
  - Oscilloscope screenshots
  - Measurement and Instrument configuration summary
- Report contents are user definable content
- Provision to append more results later





Tektronix®

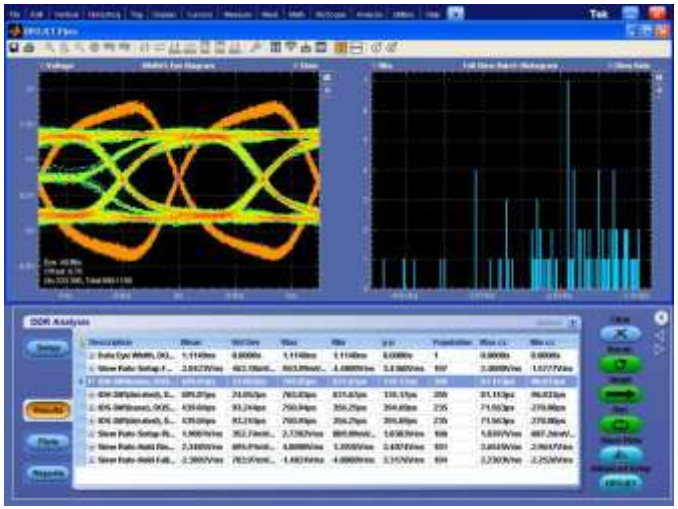
Beyond DDRA

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark

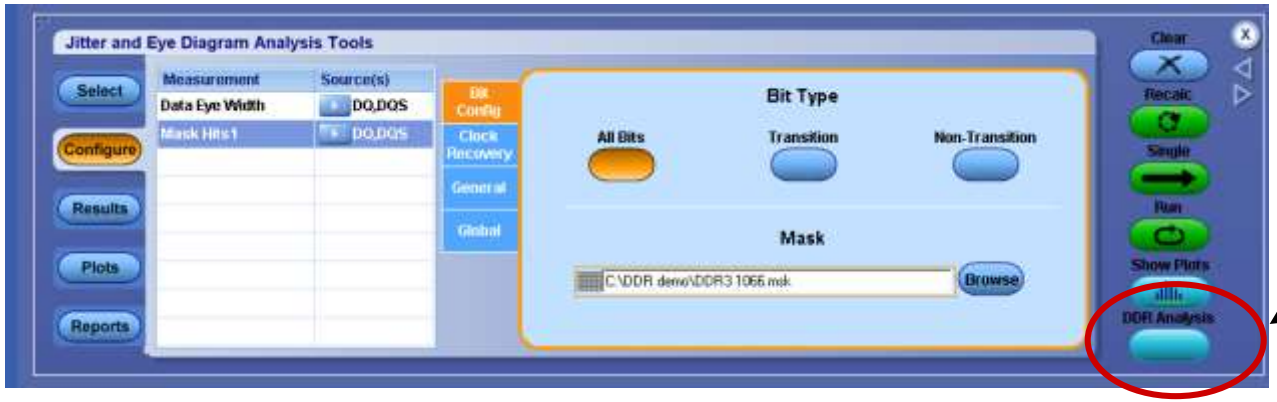
Signal Analysis & Debug

DDRA + DPOJET

- DDRA is not a closed tool – seamlessly links directly to DPOJET for measurement analysis
- Opportunity to change or fine-tune settings, add new measurements as needed



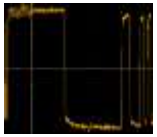
- DPOJET - powerful measurement engine for DDRA
- All settings are explicit – you can see them and change them.



"One Click" access to DPOJET & back

Tektronix®

DPOJET Analysis Overview

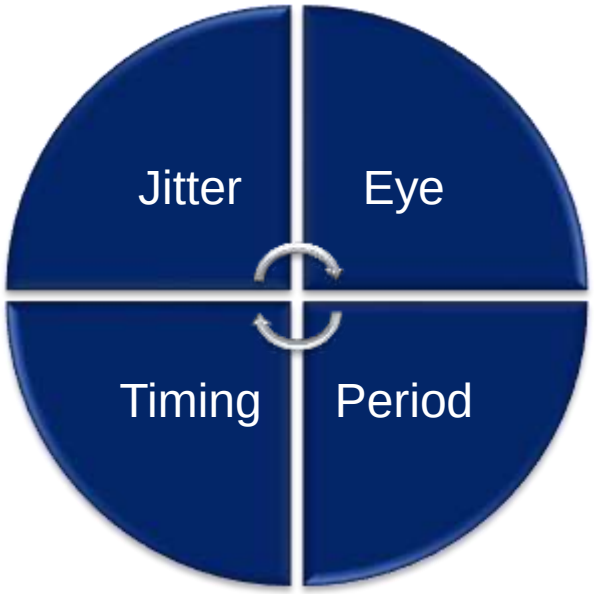


Live Analog
Live Digital
Reference Memory

Waveform

Link Analysis (SDLA)

Math



Results

Acquire

DPOJET works with the following data sources
- Analog
- Digital
- Math
- Reference

Transform

Data from a data source can be post processed to achieve visibility at multiple test points or after math transformations

Measure / Analyze

Measure simultaneously across multiple test points and measurement configurations

Plot and zoom on worst case to provide deeper levels of insight

Reporting

Get a test report with measurement results, pass fail limits, plots, user comments and instrument configurations.

Tektronix®

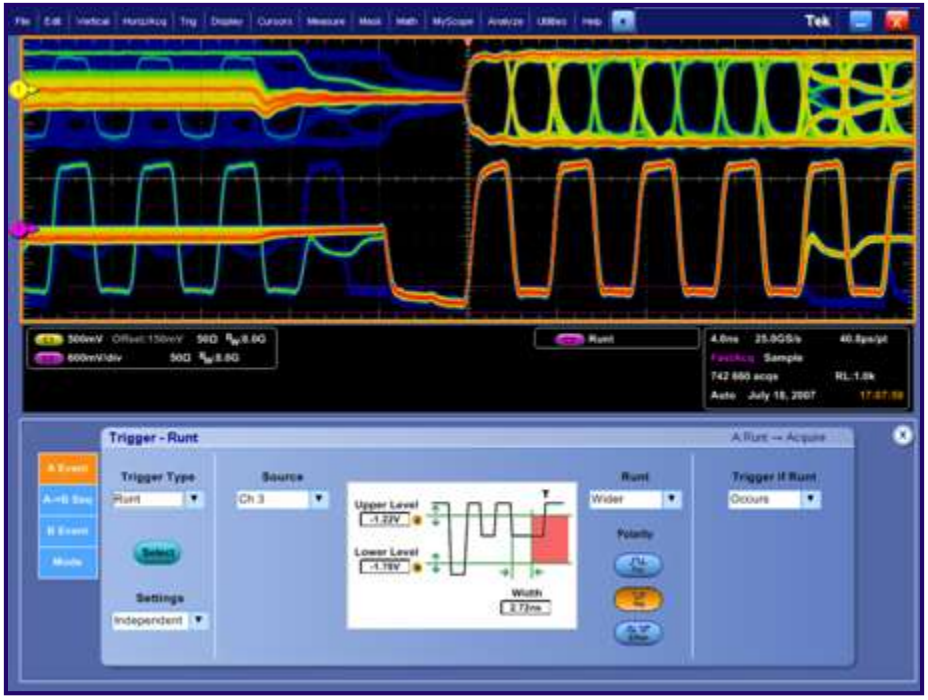
DPOJET Debug Tools

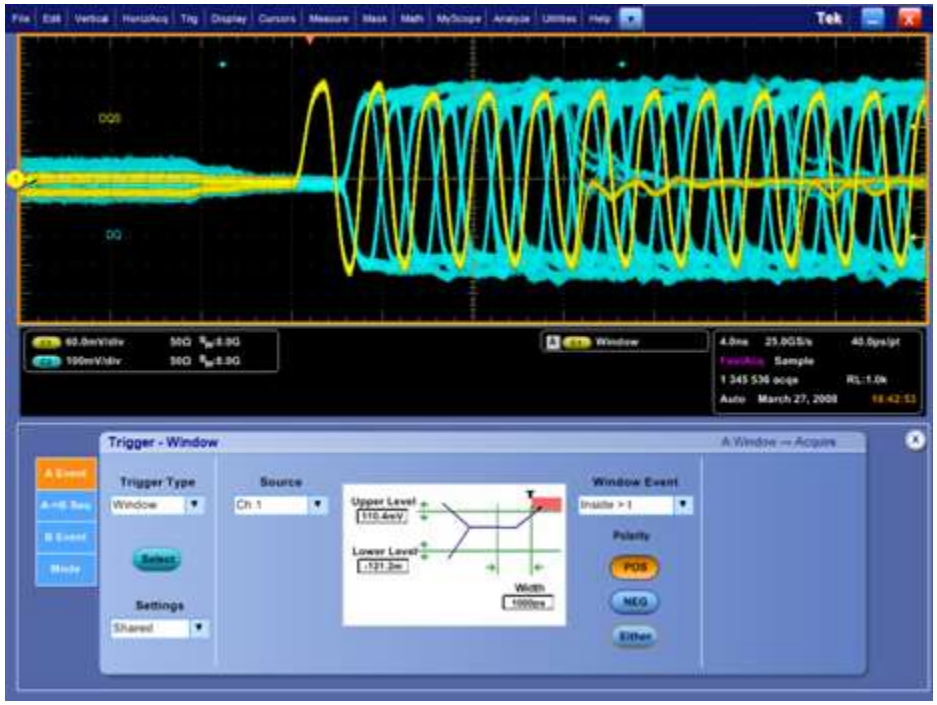
- "Find Worst Case Events" feature
  - Zoom to waveform from Min / Max for each measurement

Tektronix®

Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
  - FastAcq shows any disparities on signals, like infrequent glitch’s

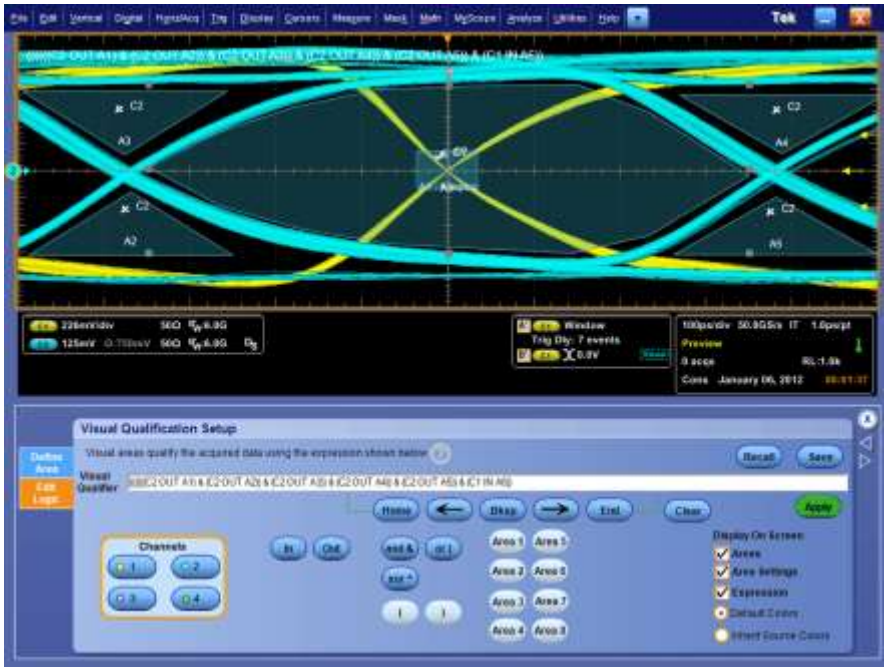




Tektronix®

Visual Trigger

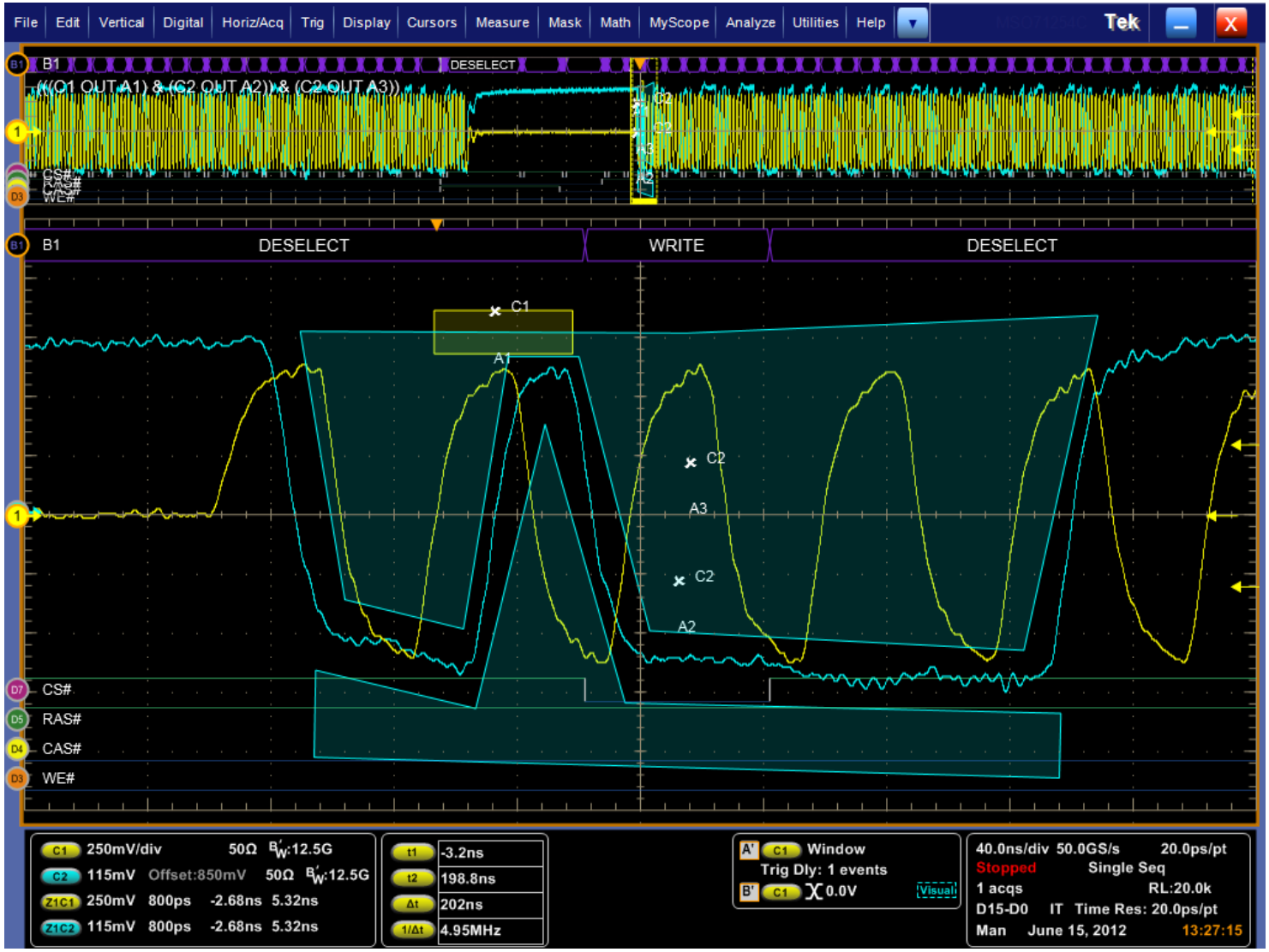
- 8 customizable zones to quality HW trigger setup
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 verticies
- Areas are “keep in” or “keep out” and can be applied to either trigA or trigB.
- Can be used to
  - Separate Read / Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams



Tektronix®

Visual Trigger Used For DQ Pattern Detection

010000X Pattern

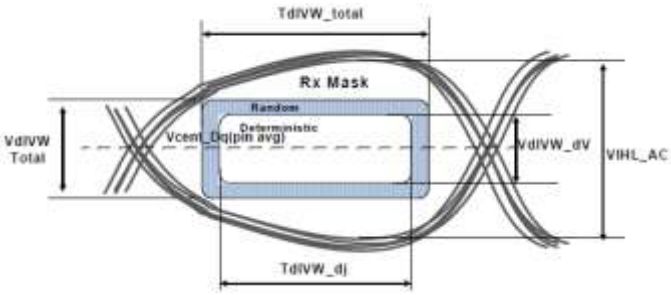


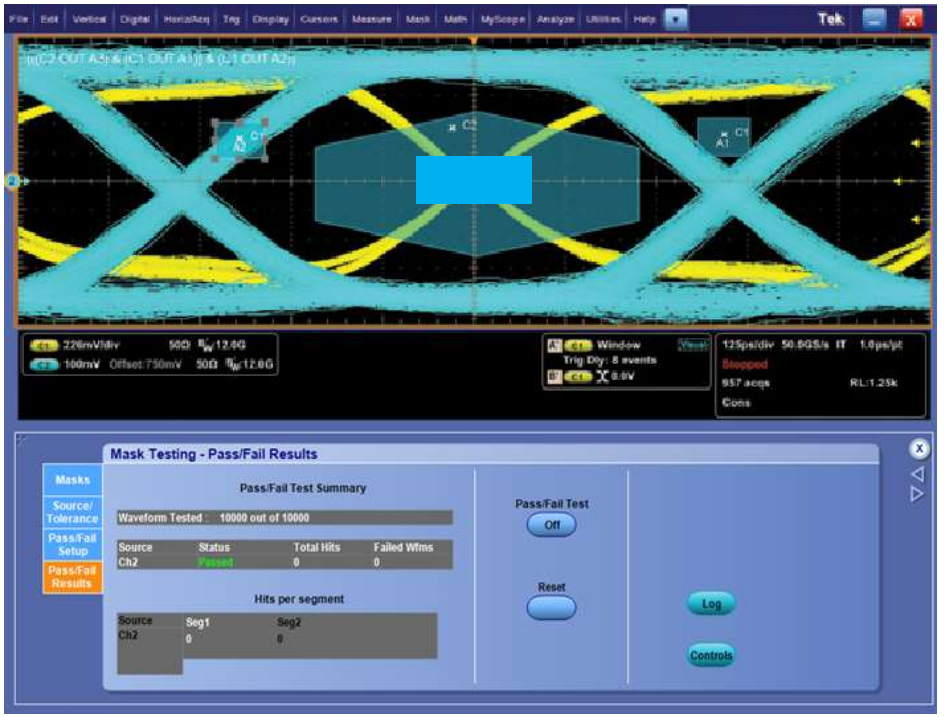
Tektronix®

Eye Mask testing

DRAM Input RX Mask

- For DDR4 JEDEC is moving to a mask based approach for DQ eye measurement at Rx input
- After the Eye is built using DDRA Using the built in Mask Measurement capability the Pass/Fail results can be obtained.



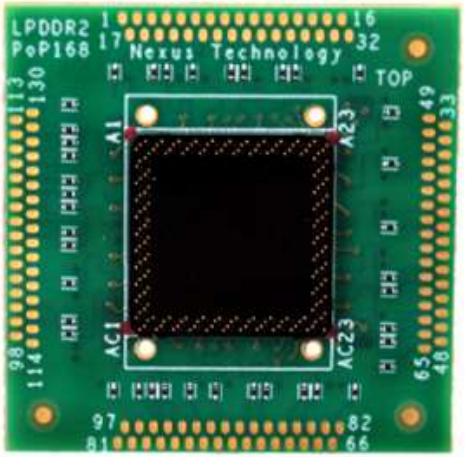


Mask = 136mV x 125ps (0.2UI)

Tektronix®

Signal Access

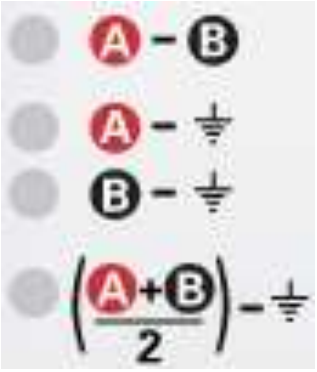
Probing

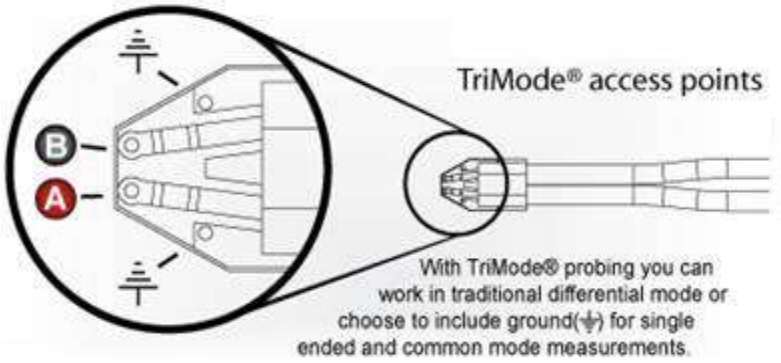


Tektronix®

TriMode Probing

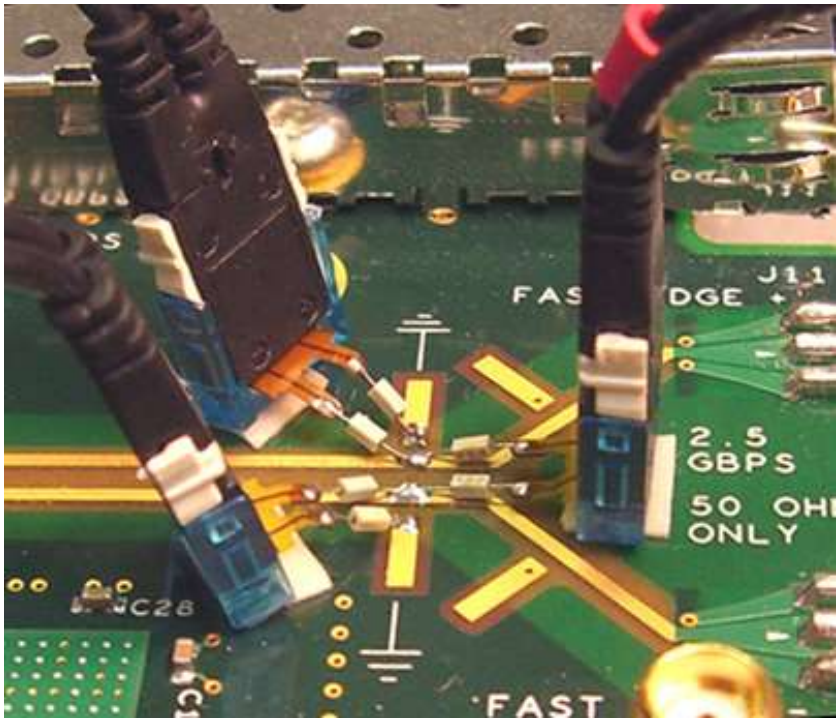
- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements: ((V+) + (V-))/2 with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!





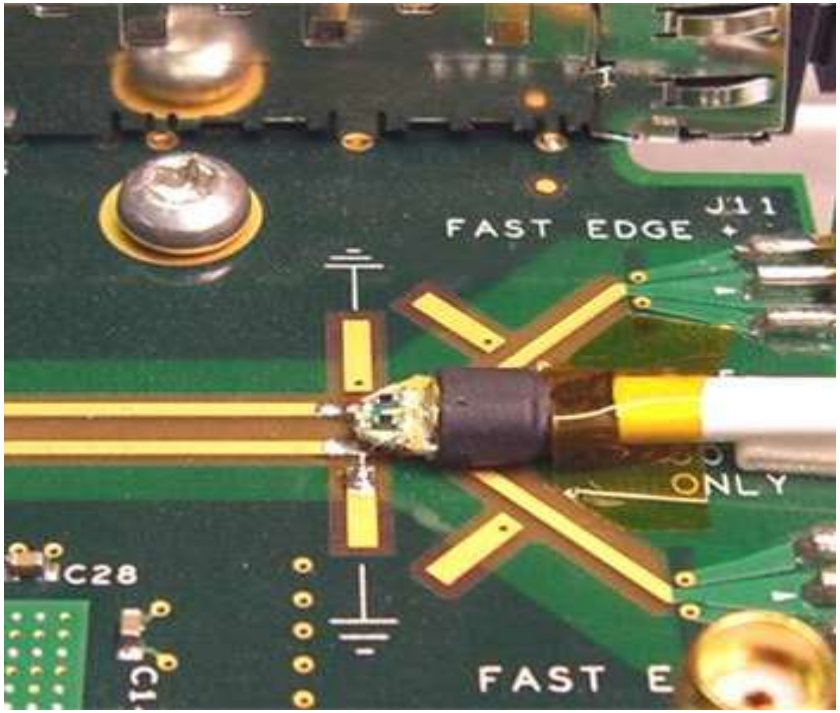
Tektronix®

Before and After



Before TriMode Probing

1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode

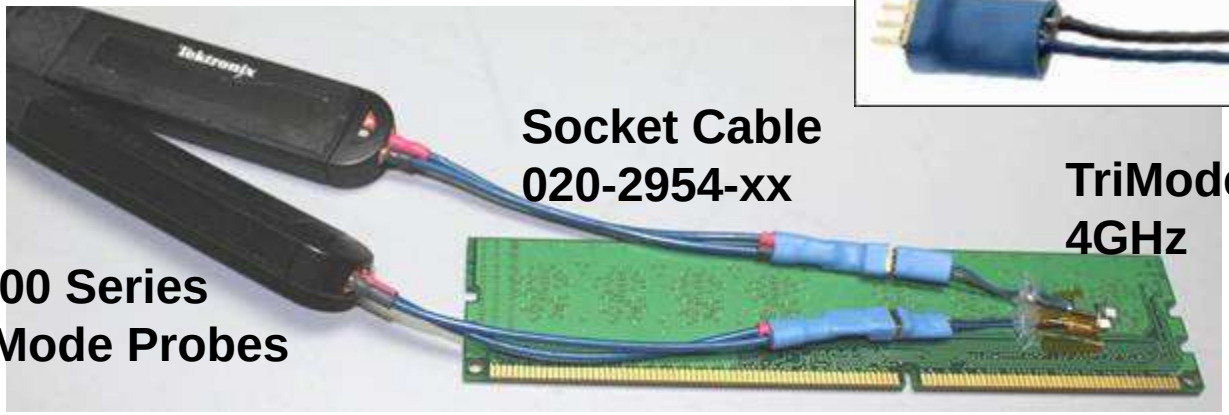


After TriMode Probing

1 Probe and 1 setup for
Differential, SE and Common Mode

Tektronix®

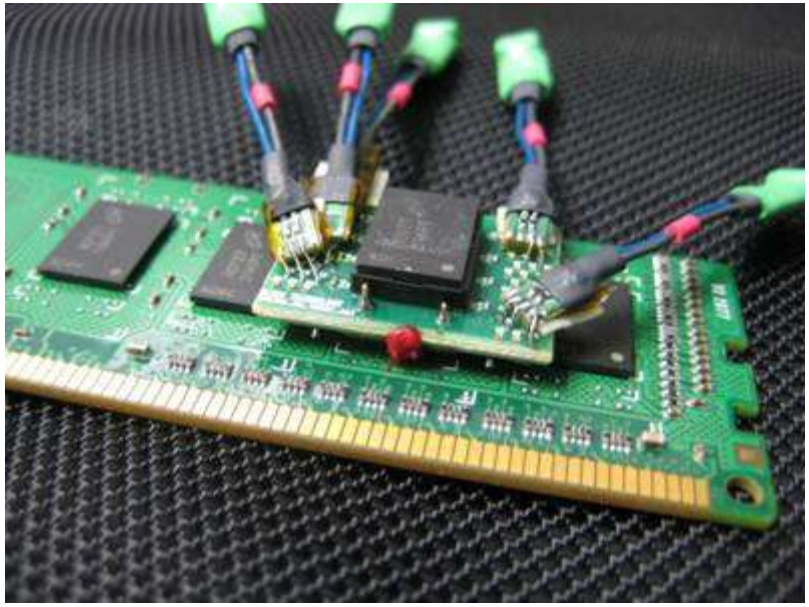
Analog Solder-In Probing Solutions

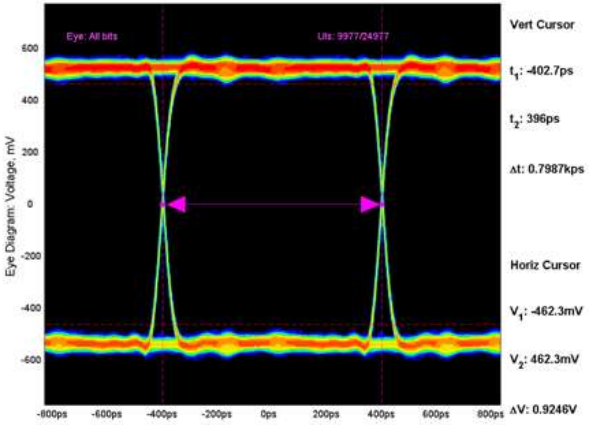


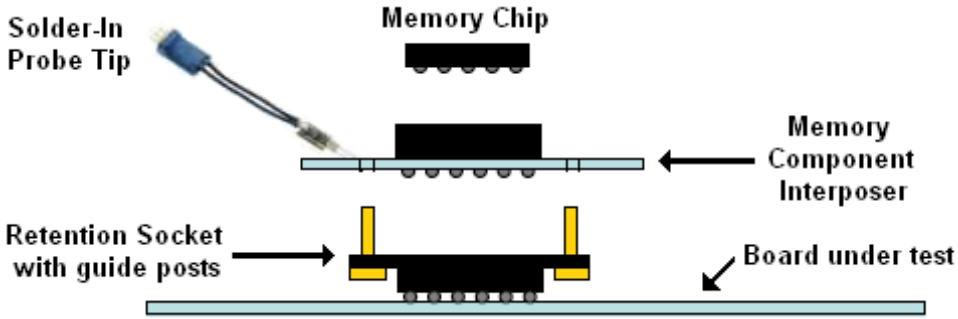
TriMode Micro-Coax Tip
4GHz

BGA Chip Access For DDR2, DDR3

- Unique, reusable socket design allows for multiple chip exchanges
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models

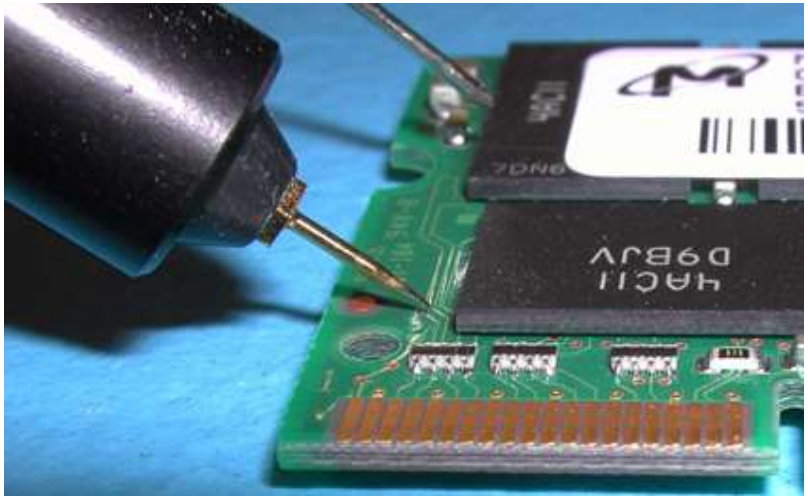






Memory Probing

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- Memory Components use BGA or PoP Packages
  - Reduces the parasitics, enabling performance at higher speeds
  - Mandate from JEDEC
- Probing a BGA or PoP package is Difficult
  - Unable to probe at the Balls of the Device
  - Probing at a connector, trace, or a via is not the same as probing at the device
  - Not a true representation of the signal



*Courtesy Micron Technologies

Memory Component Interposers

- Provide easy access to signals of Interest
- Controller Impedance path with embedded resistor for good signal Integrity
- De-embed filters to remove effects of interposer tap trace
- SPICE model available upon request for simulation and analysis

Memory Standard	Supported Form Factors	Interposer Types
DDR2	– BGA	– Socketed Interposer – Direct Attach Interposer
DDR3	– BGA	– Socketed Interposer – Direct Attach Interposer – MSO DIMM Interposer – Instrumented DIMM
DDR4	– BGA	– Socketed Interposer – Direct Attach Perimeter Interposer – MSO DIMM Interposer – Instrumented DIMM
LPDDR2	– BGA – PoP	– Socketed Interposer – PoP Interposer
LPDDR3	– BGA – PoP	– Socketed Interposer – PoP Interposer
GDDR5	– BGA	– Socketed Interposer – Direct Attach Interposer

Interposer Types

Socketed Interposers

- Comes with a Custom BGA Socket that needs to be soldered to Target
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

PoP Interposers

- Comes with a Custom BGA Socket that needs to be soldered to Application
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

Direct Attach Interposers

- Interposer is soldered to Target
- Memory Component is soldered to Interposer
- Full BGA visibility
- No Special design or routing requirements needed

Interposer Types

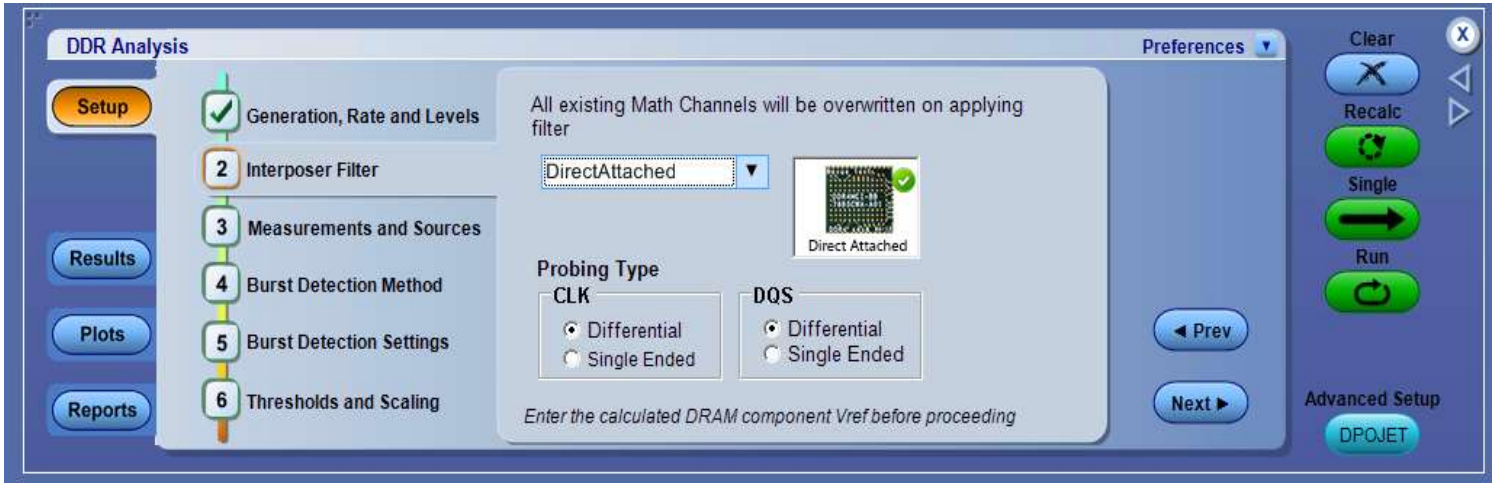
Direct Attach Perimeter Interposers

- Interposer is soldered to the Target
- Memory component is soldered to Interposer
- Signals are brought to pads on edge of the Interposer
- KoV of the interposer is the same size as the BGA component
- Because of limited space around the edge not all signals can be probed
- Choose between wide / narrow Address or data

MSO Interposers

- Provides a quick and easy access of the Addr/CMD signals to MSO digit
- Allows the Addr/cmd triggers to correlate Analog Inputs
- Combine with Component Interposers for high fidelity analog analysis

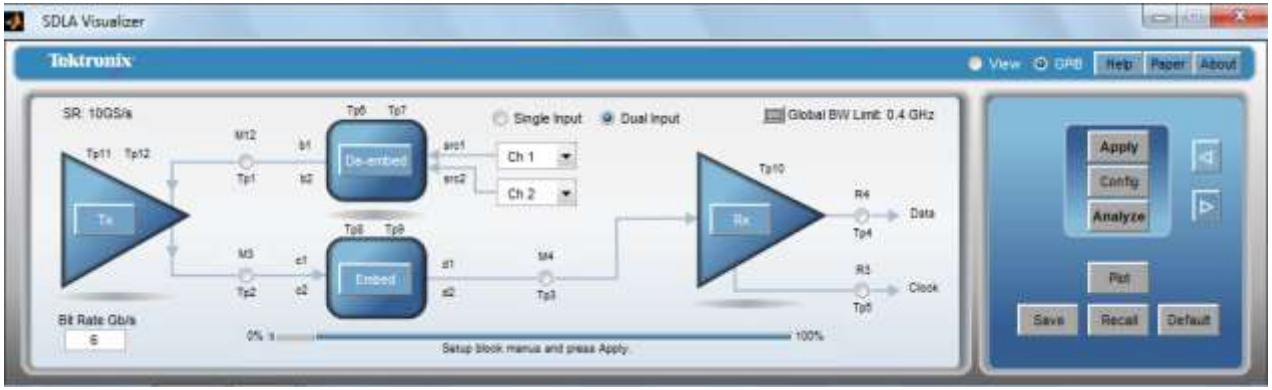
Interposer Filter File Integration



- Additional step in the setup process
- Integrates the application of the de-embed filter useful for characterization
- UI is XML driven new selections can be added to the menu's by editing XML
- Supports custom filter application

De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will available for the interposers upon request. These de-embedding filters are developed assuming nominal values
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used



Tektronix

Why use SDLA Visualizer

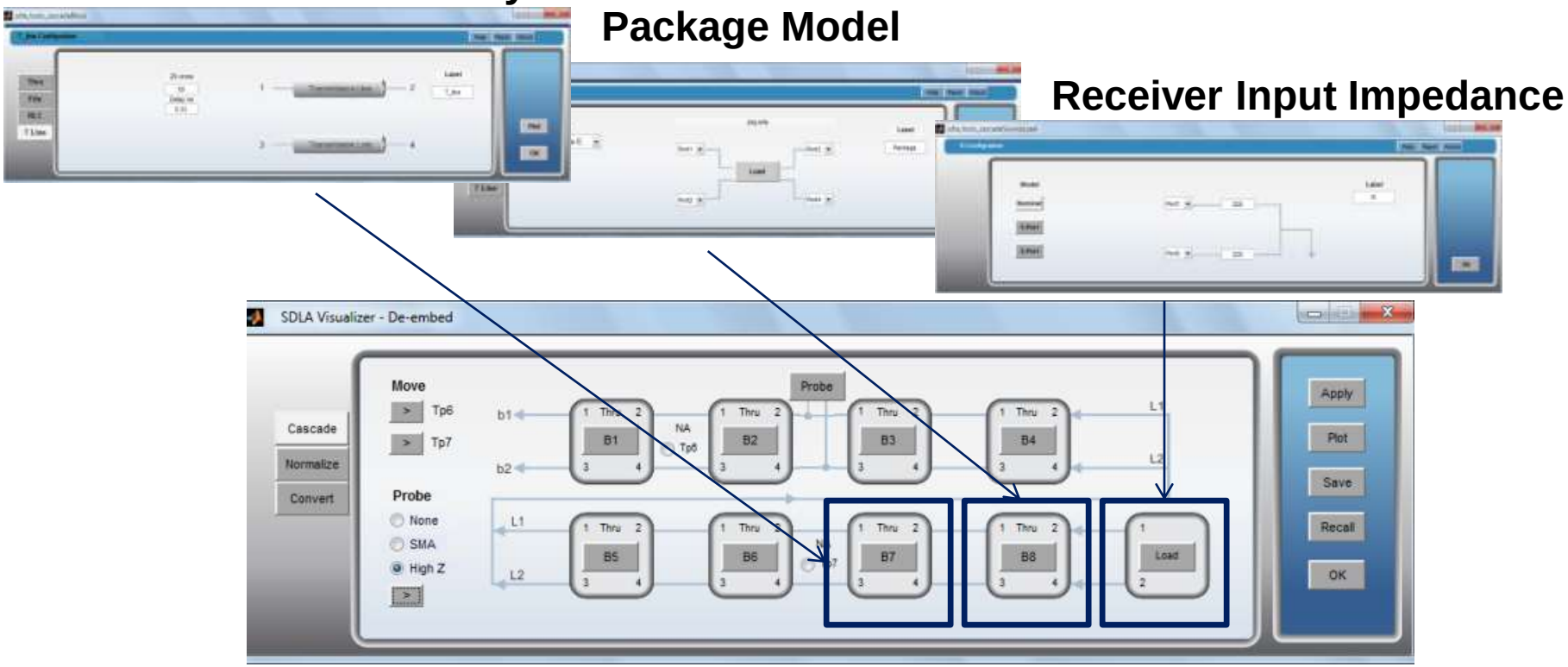
Remove Reflections

- Probing at non-ideal locations can cause reflections on the acquired signal, which are not present at the ideal probe location
- With SDLA visualizer, reflections from Memory interfaces can be compensated for with limited DUT knowledge

Transmission Line Delay

Package Model

Receiver Input Impedance



Tektronix®

Remove Reflections

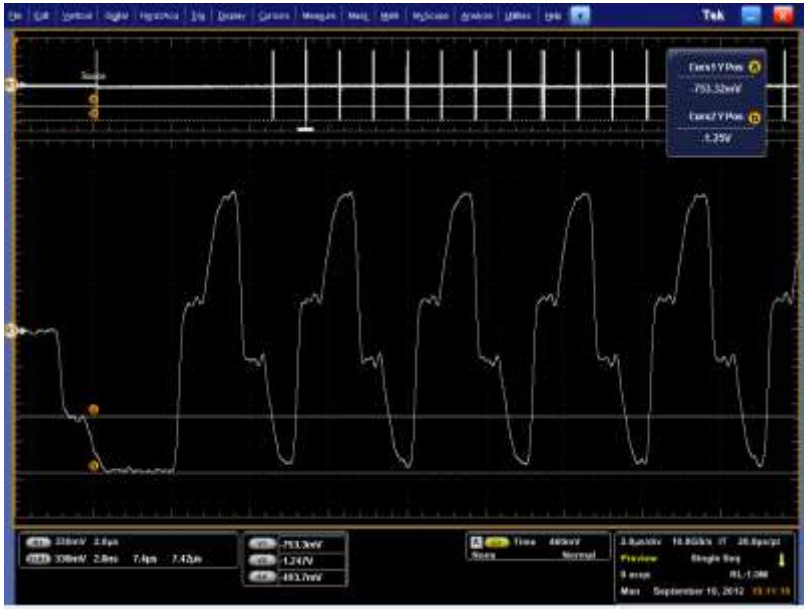
Estimate Load Resistance and Transmission Line Delay

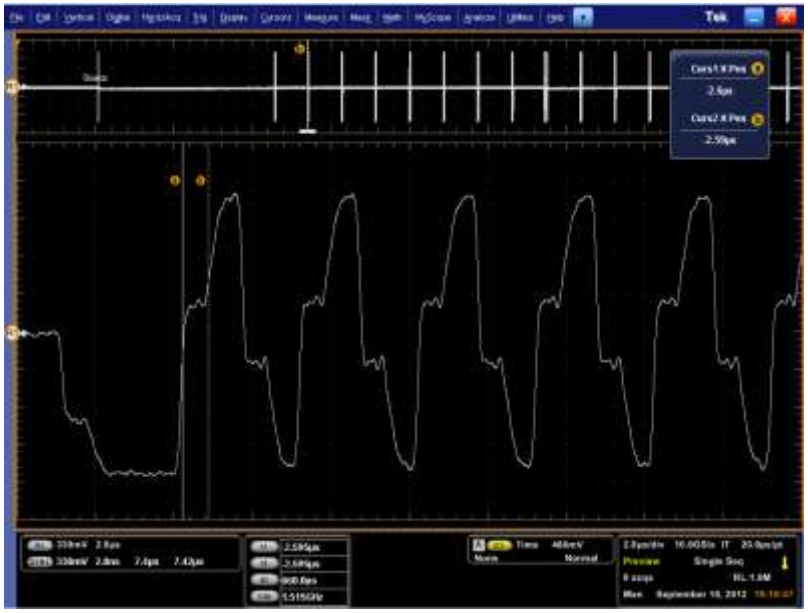
- Use cursors to get ratio of reflected to incident voltage.
- Compute resistance as :
  R = Z0 (1 + Γ) / (1 - Γ)
  Γ = (V2 – V1) / V1
  Γ = (1.25 – 0.75) / 0.75
  R = 200
- Tune R to get best results. 220 ohms was used

- Use cursor measurement to get delay for round trip reflection.
- Then divide by 2.

  Td = 660ps / 2

  Td = 330ps





Tektronix®

Remove Reflections

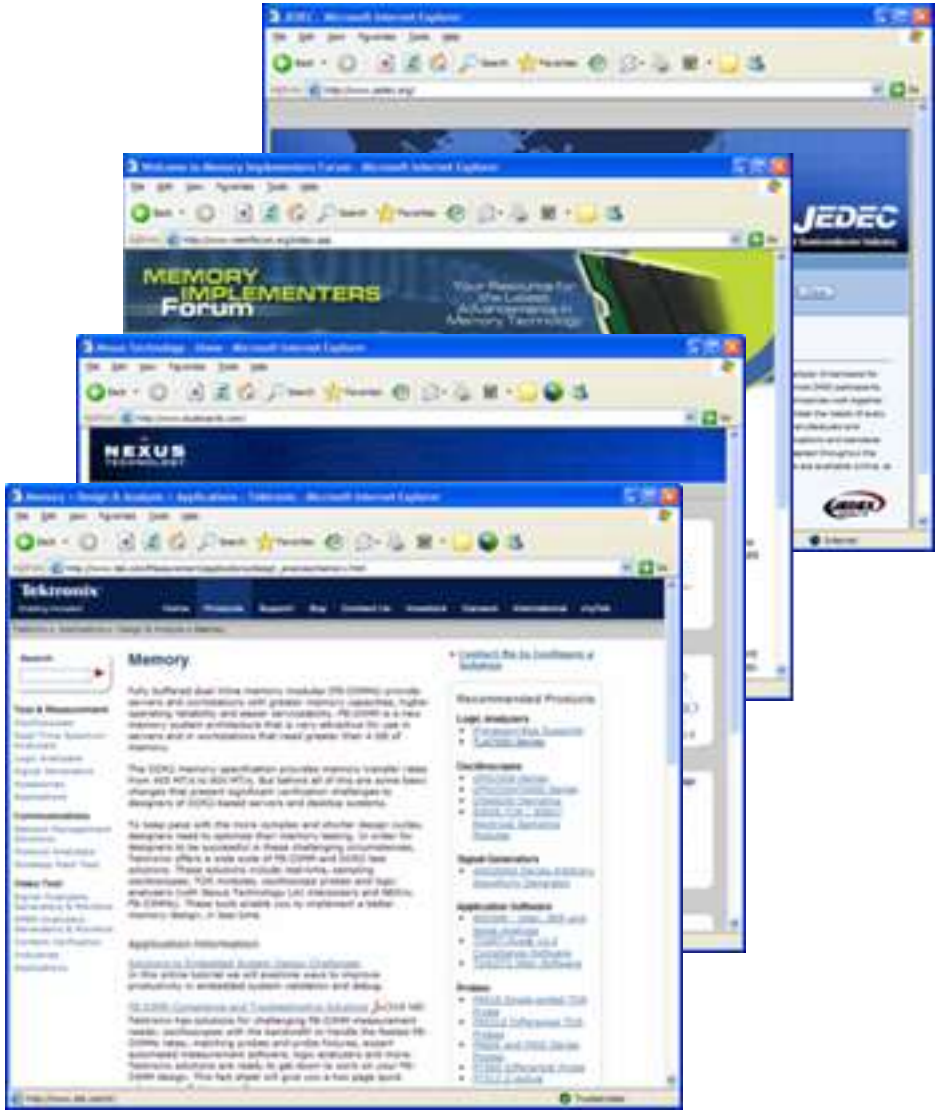
De-Embed Results…

- White is original acquired signal with the reflection.
- Purple is the de-embedded result showing reflection removal.

Tektronix®

Memory Information Resources

- Tektronix
  - www.tektronix.com/memory
- Nexus Technology
  - www.nexustechnology.com
- Memory Implementers Forum
  - www.memforum.org
- JEDEC
  - www.jedec.org



Tektronix®

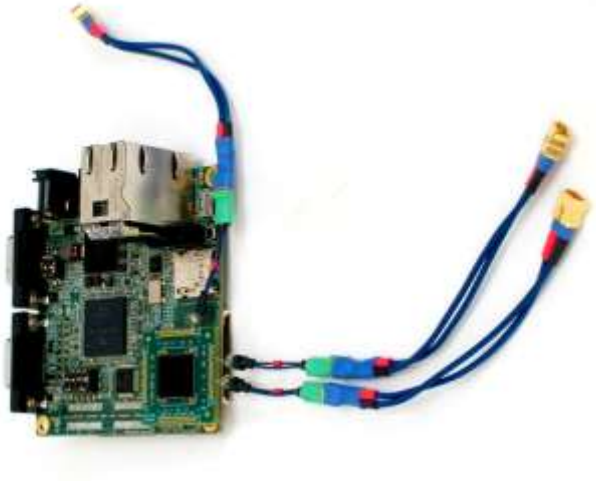
Summary – World's Best Memory Test Solution

Complete

- Provides JEDEC validation, characterization and full measurement support
- Comprehensive coverage of multiple memory standards in one single package

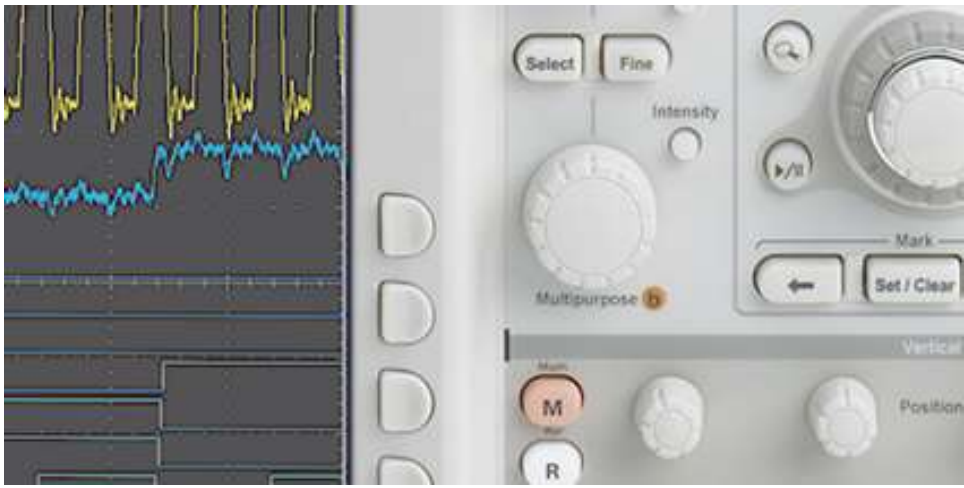
Performance

- Based upon high performing oscilloscopes and software analysis tools
- TriMode probing that enables three measurements with a single probe connection
- Read/Write burst identification on all bursts
- Automated setup with JEDEC pass/fail limits



Comprehensive Analog Verification and Debug Tools for Memory Interface

Thank You



Tektronix®