USB3.0/3.1 Physical Layer Testing
Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s (2000)**
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging

- **USB 3.0, 5 Gb/s (2008)**
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture

- **USB 3.1, 10 Gb/s (2013)**
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation
USB 3.0/3.1 Technology Timeline

<table>
<thead>
<tr>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spec Release</td>
<td>Spec Release</td>
<td>Test Vendor Compliance Group Participation</td>
<td>Test Vendor Compliance Group Participation</td>
</tr>
<tr>
<td>Sept 12 0.5 Spec</td>
<td>Feb 13 0.7 Spec</td>
<td>June 13 0.9 Spec</td>
<td>Q4 2013 1.0 Spec</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PIL (Peripheral Interop Lab)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Unless noted Workshops are in Portland, OR USA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Taipei Taiwan</td>
<td>Taipei Taiwan</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Taipei Taiwan</td>
<td>Taipei Taiwan</td>
</tr>
<tr>
<td></td>
<td></td>
<td>USB-IF Plugfests</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Deployment Phase</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Integration Phase</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Spec Development</td>
<td></td>
</tr>
<tr>
<td></td>
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<td>Product Development</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>USB-IF Tool Development</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tektronix Test Solution Updates</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmitter, Receiver, Channel</td>
<td></td>
</tr>
</tbody>
</table>
# USB 3.1 Compliance Timeline

## USB 3.1 Compliance Timeline

<table>
<thead>
<tr>
<th>Version</th>
<th>Milestones</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>Test Assertions</td>
<td></td>
</tr>
<tr>
<td>0.7</td>
<td>Test Assertions + Test Descriptions</td>
<td>Draft Test Specification</td>
</tr>
<tr>
<td>0.9</td>
<td>Tests coded and Test Specification updated</td>
<td>Begin testing at PIL</td>
</tr>
<tr>
<td>0.95</td>
<td>Beta tool release</td>
<td>Ready to certify products</td>
</tr>
<tr>
<td>1.0</td>
<td>Final tool release</td>
<td>Release to ITLs</td>
</tr>
</tbody>
</table>

[Diagram showing timeline with quarters and key milestones]
Overview: Cable Assembly

Std A Connector (host)

Std B Connector (device)

mB Connector (device)

Cable Cross-section

USB3

USB2

StdB_SSTX+

StdB_SSTX-

StdB_SSRX+

StdB_SSRX-

D–

D+

GND

VBUS

USB3

USB2

10 9 8 7 6

5 4 3 2 1

≈1.8mm

≈0.65mm

UTC Signal Pair

USB2

Optional filler

SDP Signal Pair

USB3

Braid

Power

Ground

Jacket

SDP Signal Pair

USB3
NEW Type C connector

- Used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- Enhances ease of use by being plug-able in either upside-up or upside-down directions
- Enhances ease of use by being plug-able in either direction between host and devices
- New Configuration Control signal (low speed) for handshaking
- Two high speed diff pairs for mux’ing data
Why 10 Gb/s?

**Video**
- HD video adapters with multi display outputs
- Dual HDMI/DVI with simultaneous 1080p displays

**Storage**
- 5 Gb/s with 8b/10b -> 400 MB/s
- High performance SSD saturation -> \(~600 \text{ MB/s}\)

**Hub/Dock**
- Multi-function, ‘All in One’ docking
- Faster backups, multiple monitors, etc.
Naming convention

- **SuperSpeed (SS) = 5 Gb/s**
- **SuperSpeedPlus (SSP) = 10 Gb/s**

- Similar to other standards
  - Gen1 = 5G
  - Gen2 = 10G
  - GenX = 5G or 10G

- SS and SSP are qualifiers not names
  - E.g. SuperSpeedPlus device, host or hub

- Enhanced SuperSpeed = ≥ Gen1 speed
  - Reference for possible future higher data rate
USB 3.0 Key Considerations

- **Receiver Testing Now Required**
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues

- **Channel Considerations**
  - Need to consider transmission line effects
  - Software channel emulation for early designs

- **New Challenges**
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

- **Test Strategy**
  - Cost-effective tools
  - Flexible solutions

Source: USB 3.0 Rev 1.0 Specification
Transmitter Solutions

- **Comprehensive Solution Goes Beyond Compliance**
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results

- **Complete Toolset for Characterizing USB 3.0 Designs**
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG
USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing
    - Available from the USB-IF
USB 3.0 Compliance Test Configuration

- **USB 3.0 is a closed eye specification**
  - Reference channel is embedded and CTLE is applied

- **USB 3.0 Reference Channels**
  - **Host Reference Channel**
    - 11” back panel is applied for device testing
  - **Device Reference Channel**
    - 5” device channel is applied for host testing
  - **3 Meter Reference Cable**
    - Used for host and device (except captive devices) testing in addition to reference channels

- **USB 3.0 Reference Equalizer**
  - Attenuates the low frequency content of the signal to open the eye
Fixture and Channel De-Embedding

- Why de-embed – Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins

- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software
USB 3.0 Transmitter Measurement Overview

- **Voltage and Timing**
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate

- **Low Frequency Periodic Signaling (LFPS)**
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod

- **SSC**
  - Modulation Rate
  - Deviation
SuperSpeed Transmitter Compliance Testing

1. Connect DUT to scope via test fixture.

2. Transmit CP1 (toggle pattern) & measure $10^6$ consecutive UI
   – This step used to measure RJ

3. Repeat with CP0 (scrambled D0.0)
   – Will combine RJ (step 2) with DJ to extrapolate TJ (step 5)

4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   – Channels are S-Parameter-based and are embedded into captured waveform

5. Extrapolate jitter to $10^{-12}$ BER

<table>
<thead>
<tr>
<th>Spec</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>100</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>Rj @ $10^{-12}$ BER</td>
<td>0.23</td>
<td></td>
<td>UI</td>
</tr>
<tr>
<td>Tj @ $10^{-12}$ BER</td>
<td>0.66</td>
<td></td>
<td>UI</td>
</tr>
</tbody>
</table>
Example Host Test Setup

- SMA cable to scope
- Short USB cable
- Ping.LFPS from signal generator (pattern toggle)
- Host back panel port
Voltage and Timing

- $T_j$ – Dual Dirac at 10–12 BER
- $T_x$ Deterministic Jitter – Dual Dirac
- $T_x$ Random Jitter – Dual Dirac
- Differential $p$-$p$ $T_x$ Voltage Swing
- Transmitter Eye – Dual Dirac@BER
- Eye Width@BER
- Eye Mask Hits
LFPS TX Measurements

- LFPS signaling is critical for establishing link communication
- LFPS TX test verify common mode, voltage, tPeriod, tBurst, tRepeat
- Channel is not embedded for LFPS tests
SSC Measurements

- Both Maximum and Minimum Frequency Deviation must be considered
  - Assume nominal UI of 200ps
  - Limits are +0/-4000ppm and +0/-5000ppm, plus +/- 300ppm for ref clock accuracy

- Compliance Channel is not embedded for SSC measurements
LFPS RX Test

- Required Compliance Test to verify that the DUT RX will respond to LFPS signaling
- Test is ran across four different settings

<table>
<thead>
<tr>
<th>tPeriod</th>
<th>VTX-DIFF-PP-LFPS</th>
<th>Duty Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>50ns</td>
<td>800mV</td>
<td>50%</td>
</tr>
<tr>
<td>50ns</td>
<td>1000mV</td>
<td>40%</td>
</tr>
<tr>
<td>50ns</td>
<td>1000mV</td>
<td>60%</td>
</tr>
<tr>
<td>50ns</td>
<td>1200mV</td>
<td>50%</td>
</tr>
</tbody>
</table>
LFPS RX Test

- AWG generates spec compliant LFPS signaling
- Validate LFPS response with RT Scope
USB 3.0 Droop / Drop Test

- New Test Fixture Available from USB-IF
  - Provides 150mA / 900mA load
  - Previous fixture provides 100mA / 500mA load

- Amount of power drawn is changed from 500mA to 900mA for high power devices

- Fixture is orderable at:
NEW Debug and Analysis Tools

- USB3 Decode with Hierarchal Bus display
- Includes Digital, 8b10b, PHY, LINK, and Transaction layers
- Enables decode, search and trigger, available with option SR-USB
Decode and Trigger Examples

USB3 Link Training

USB3 Trigger Setup
Complete USB 3.0 Transmitter Solution

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures

- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)

- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50 GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

TF-USB3-AB-KIT
What’s new—ECN#18 USB3.0 Radio Friendly Clock Unit Interval

Table 6-9. SSC Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Limits</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{SSC-MOD-RATE} )</td>
<td>Modulation Rate</td>
<td>30</td>
<td>33</td>
<td>kHz 1, 2, 3, 4</td>
</tr>
<tr>
<td>( t_{SSC-FREQ-DEV} )</td>
<td>SSC deviation</td>
<td>+0/-4000</td>
<td>+0/-5000</td>
<td>ppm 1, 2, 3, 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+0/-2000</td>
<td>+0/-3000</td>
<td></td>
</tr>
</tbody>
</table>

Note:
1. The data rate is modulated from 0 ppm to -5000 ppm of the nominal data rate frequency and scales with data rate.
2. This is measured below 2 MHz only.
3. Receiver compliance testing is done under the maximum spread condition.
4. Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000 ppm.
What’s new---ECN#19 USB3.0 MicroB Cable Loss Specification
USB 3.0 Receiver Testing
USB 3.0 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions
USB 3.0 Compliance Receiver Tolerance Test Overview

- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at $10^{-10}$
- De-Emphasis Level is set to -3dB
- Amplitude at the end of the compliance channel: 180mV Hosts and 145mV Devices
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SJ</th>
<th>RJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500kHz</td>
<td>400ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>1MHz</td>
<td>200ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>2MHz</td>
<td>100ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>4.9MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>10MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>20MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>33MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>50MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
</tbody>
</table>
Generic USB 3.0 RX Test Configuration

Host Receiver Test

- Error Detector
- Pattern Generator
- Reference Channel
- Adapter
- Host DUT

Device Receiver Test

- Error Detector
- Pattern Generator
- Reference Channel
- Adapter
- Device DUT

- Short Cable
USB 3.0 Stress Recipe - Calibration

Long waveform capture by Real Time Scope

Mature standard with fully automated solutions for stress calibration and good correlation
USB 3.0 Calibration

- **Host Calibration Setup**

- **Device Calibration Setup**

**Calibration Procedure**

- ✓ Connect signal source directly to scope
- ✓ Calibrate de-emphasis to 3.0 dB + 5/-0% dB using CP0 with SSC off and CTLE off
- ✓ Connect signal source through the compliance channel
- ✓ Measured peak to peak TJ
- ✓ Calibrate RJ(2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10-10) with CP1 at the end of the channel applying CTLE and JTF
- ✓ Calibrate SJ using CP0 until measured peak to peak TJ increases by that amount. Apply CTLE and set JTF at 50Khz.
- ✓ Expected Tj with jitter off should be less than 100 ps. If this threshold is exceeded, replace the channel fixture(s) and/or cable(s).
USB 3 Loopback Negotiation

- **RX Detect**
  - SuperSpeed Link Partner is Availability is determined

- **Polling.LFPS**
  - DUT and Generator Send LFPS and establishes LFPS Handshake

- **Polling.RxEQ**
  - DUT and Generator send TSEQ in order to establish DUT RX Equalization Settings

- **Polling.Active**
  - DUT and Generator send 8 TS1

- **Polling.Configuration**
  - Generator instructs DUT to loopback by setting the loopback bit in the TS2 training sequence

- **Polling.Idle**
  - DUT directed to Loopback
Two Solutions for USB 3.0 Receiver Testing

**BERTScope BSA85C and AWG7122C**

- **Tektronix has the right solution to meet your needs**
  - Both provide fully automated Receiver Compliance and Jitter Tolerance Testing
  - Both offer advanced impairments to debug problems caused by SSC or other anomalies
  - Both support a wide range of HSS Standards
  - Both support asynchronous clocking (SKP order set rejection)

- **BERTScope**
  - Performance that you need up to 26Gb/s for next generations standards including DisplayPort 1.2, SATA/SAS, 10G KR, PCI Express 3.0
  - Impairments can be changed on the fly to see the effect of increasing or reducing jitter
  - Debug and analysis tools enable quick identification of RX errors
  - True BER measurements

- **Arbitrary Waveform Generator**
  - Common platform for MIPI, HDMI, USB 3.0, and SATA
  - Only solution available that provides a common setup between transmitter and receiver testing without the need of RF switches and additional setup complexity
  - Easily apply sparameter models to verify designs under different channel conditions without the need of physical ISI channels
  - Generate SJ > 1Ghz to debug elusive problems caused by other system clocks
BERTScope USB 3.0 RX Test Configuration

USB Switch creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

DPP125B
De-emphasis Processor

CR125A
Clock Recovery

BSA85C
BERTScope
AWG USB 3.0 RX/TX Test Configuration

- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)
Tektronix USB 3.0 Summary

- Complete
  - Solutions available today for USB3.0 Transmitter, Cable, Channel, and Receiver Testing

- More than a Compliance Solution
  - Solutions to meet debugging, characterization, and compliance needs
  - Receiver stresses that go beyond compliance

- Increased Productivity
  - Fully automated transmitter and receiver test solutions
  - Analysis tools integrated on the BERTScope enable the isolation and root cause determination of receiver errors

- Performance
  - 26Gb/s BERTScope provides coverage for next generation testing needs Low noise floor enables measurements of small data eyes for compliance testing and receiver calibration
  - Only 6.25Gb/s hardware serial trigger to capture protocol events that are causing failures or interoperability problems

- Expertise
  - Actively engaged in the USB Working Groups
  - Regional support by Tektronix Application Engineering Experts
Extensive application information at:

www.tek.com
Introduction to USB 3.0 SuperSpeedPlus
Disclaimer

**Presentation Disclaimer:** All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of USB-IF or other member companies.
# USB 3.0 and 3.1 Comparison

<table>
<thead>
<tr>
<th></th>
<th>SuperSpeed</th>
<th>SuperSpeedPlus</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Rate</strong></td>
<td>5 Gb/s</td>
<td>10 Gb/s</td>
</tr>
<tr>
<td><strong>Encoding</strong></td>
<td>8b/10b</td>
<td>128b/132b</td>
</tr>
<tr>
<td><strong>Target Channel</strong></td>
<td>3m + Host/Device channels (-17dB, 2.5 GHz)</td>
<td>1m + board ref channels (-20dB, 5 GHz)</td>
</tr>
<tr>
<td><strong>LTSSM</strong></td>
<td>LFPS, TSEQ, TS1, TS2</td>
<td>LFPSPlus, SCD, TSEQ, TS1, TS2,</td>
</tr>
<tr>
<td><strong>Reference Tx EQ</strong></td>
<td>De-emphasis</td>
<td>3-tap (Preshoot/De-emphasis)</td>
</tr>
<tr>
<td><strong>Reference Rx EQ</strong></td>
<td>CTLE</td>
<td>CTLE + 1-tap DFE</td>
</tr>
<tr>
<td><strong>JTF Bandwidth</strong></td>
<td>4.9 MHz</td>
<td>7.5 MHz</td>
</tr>
<tr>
<td><strong>Eye Height (TP1)</strong></td>
<td>100 mV</td>
<td>70 mV</td>
</tr>
<tr>
<td><strong>TJ@BER</strong></td>
<td>132 ps (0.66 UI)</td>
<td>71 ps (0.714 UI)</td>
</tr>
<tr>
<td><strong>Backwards compatibility</strong></td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td><strong>Connector</strong></td>
<td>Std A</td>
<td>Improved Std A with insertion detect</td>
</tr>
</tbody>
</table>
128b/132b Encoding and Compliance Patterns

- 4-bit block header (0011 -> control, 1100 -> data)
- 128-bit (16 bytes) non-encoded payload
- Similar to PCI Express but with 4-bit header
  - 1 bit error (self correcting)
  - 2 bit error (detection)
- Higher order scrambler ($X^{23}$ vs. $X^{16}$)
  - Improves EQ training with long, rich pattern
- Compliance with scrambled data (00h) and Nyquist (Ah)
- Pattern toggle between Gen1 and Gen2
  - Order TBD
Reference Transmitter Equalization

- USB channel profiles are dynamic (consumer)
- Need flexible solution space for link optimization
- Below are recommended Tx settings for good margin with target reference channels

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preshoot (dB)</td>
<td>2.2±1.0</td>
<td></td>
</tr>
<tr>
<td>De-emphasis (dB)</td>
<td>-3.1±1.0</td>
<td></td>
</tr>
<tr>
<td>$C_3$</td>
<td>-0.083</td>
<td>Normative requirement</td>
</tr>
<tr>
<td>$C_1$</td>
<td>-0.125</td>
<td></td>
</tr>
<tr>
<td>Nominal Boost (dB)</td>
<td>4.7</td>
<td>Informatively – for reference only</td>
</tr>
<tr>
<td>Va/Vd</td>
<td>0.834</td>
<td></td>
</tr>
<tr>
<td>Vb/Vd</td>
<td>0.584</td>
<td></td>
</tr>
<tr>
<td>Vc/Vd</td>
<td>0.750</td>
<td></td>
</tr>
</tbody>
</table>

\[
preshoot = 20 \log_{10} \left( \frac{V_{CPRX}}{V_{CPTR}} \right) = 20 \log_{10} \left( \frac{V_C}{V_B} \right) = 20 \log_{10} \left( \frac{-C_{3}+C_{6}+C_{1}}{C_{4}+C_{6}+C_{1}} \right)
\]

\[
deemphasis = 20 \log_{10} \left( \frac{V_{CPRX}}{V_{CPTR}} \right) = 20 \log_{10} \left( \frac{V_B}{V_C} \right) = 20 \log_{10} \left( \frac{C_{3}+C_{6}+C_{1}}{C_{4}+C_{6}-C_{1}} \right)
\]

* TxEQ requirements defined by ECR.
Reference Receiver Equalizer

- seven pre-defined Rx EQ settings including CTLE gain and 1-tap DFE.
- Used for transmitter compliance testing
- Behavioral reference for receiver design

\[ H(s) = A_{ac} \frac{\omega_p}{s + \omega_p} \]

\[ y_k = x_k - d_1 \text{sgn}(y_{k-1}) \]
\[ 0 \leq d_1 \text{sgn}(y_{k-1}) \leq 50mV \]
End-to-end PHY Validation
PHY Test Tools

- Similar process for USB 3.0 Gen1 Tx/Rx compliance testing
- Individual subsections (Tx, Rx, etc.) evaluated within system budget
  - ‘Far End’ Tx measurement including reference channels
- Next few slides outline current approach for electrical validation
- Let’s start with an example for Tx
Transmitter Validation Example - SDLA

- Capture CP9 (Scr0) and CP10 (Ah)
- Input reference channel models

USB3 Reference Channel

CP9 Scrambled Pattern (TP0)

CP9 Scrambled Pattern (TP1)
Transmitter Validation Example - SDLA

- Find optimum Eye height vs. Rx EQ

40 mV - Fail

73 mV - Pass
Transmitter Validation Example - DPOJET

- Recall DPOJET SSP setups

- Check JTF settings ($f_{3db}$ 7.5 MHz, 40dB slope)
Transmitter Validation Example - DPOJET

- Measure Eye height and jitter at TP1
Recommended Transmitter Solution

- ≥20 GHz BW, 100 GS/sec preferred
  - DSA72004C or higher recommended
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation. Increase memory depth if interpolation will be enabled, or if >1MUI captures are desired.
- Option DJA Advanced DPOJET required, signal analysis
- Option SLA Advanced SDLA required, cycle through 7 CTLE/1 DFE settings
- Option USBSSP-Tx recommended, provides USB3 TX specific measurements

For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.
Receiver Testing

- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions
**Receiver Jitter Tolerance**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Gen 1</th>
<th>Gen 2</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>Tolerance corner</td>
<td>4.9</td>
<td>7.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>J_{RJ}</td>
<td>Random Jitter</td>
<td>0.0121</td>
<td>0.0100</td>
<td>UI rms</td>
<td>1</td>
</tr>
<tr>
<td>J_{RJ_{p-p}}</td>
<td>Random Jitter peak- peak at 10^{-12}</td>
<td>0.17</td>
<td>0.141</td>
<td>UI p-p</td>
<td>1,4</td>
</tr>
<tr>
<td>J_{P_{L500kHz}}</td>
<td>Sinusoidal Jitter</td>
<td>2</td>
<td>2.56</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{L1Mhz}}</td>
<td></td>
<td>1</td>
<td>1.28</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{L2MHz}}</td>
<td></td>
<td>0.5</td>
<td>0.64</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{L4MHz}}</td>
<td></td>
<td>N/A</td>
<td>0.32</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{Lf1}}</td>
<td></td>
<td>0.2</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{L50MHz}}</td>
<td></td>
<td>0.2</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{P_{L100MHz}}</td>
<td></td>
<td>N/A</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>V_{full_swing}</td>
<td>Transition bit differential voltage swing</td>
<td>0.75</td>
<td>TBD</td>
<td>V p-p</td>
<td>1</td>
</tr>
<tr>
<td>V_{EQ_level}</td>
<td>Non transition bit voltage (equalization)</td>
<td>-3</td>
<td>Pre=2.2 Post=-3.1</td>
<td>dB</td>
<td>1</td>
</tr>
</tbody>
</table>

**Notes:**

1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate J_{Pj} at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-19.

*Rx Jtol RJ & Tx EQ updated by ECR.
BERTScope USB 3.1 RX Test Configuration
Summary

- New opportunity for growth with USB 10 Gb/s
- Adds additional challenges beyond legacy requirements (backwards compatibility)
- Higher performance, more complex design but feasible within current infrastructure
- Extensive PHY validation tools for early designs
  - New USB SSP DPOJET setups for Tx validation
  - BERTScope USB library with JTOL templates
  - DSA8300 Sampling oscilloscope for channel characterization
  - Test procedures documented in Methods of Implementation (MOI)
Memory Interface Verification and Debug
Memory Validation Challenges

**Speed**
Upward trend to meet the ever increasing application needs
Widely used High Speed Parallel Bus, resulting in more signal integrity issues

**I/O Voltage**
Downward Trend to improve Battery Life in portable devices
Reduce power consumption in Data Centers resulting in smaller data eyes

**Capacity**
Upward Trend, Multi-Core CPU’s ability to handle large data sets
Multiple Channels, Slots per Channel, Ranks per Slot introduces probing complexity

**Form Factors**
DIMM, SODIMM, RDIMM, LRDIMM, PoP, BGA
Multiple form factors for different applications needs introduces probing complexity

**System level Visibility**
Critical cross bus dependencies increase with speed
Signal Access and Time-correlated visibility across multiple buses
Memory Validation Continuum

- **Analog Validation**
  - Instruments
  - Probes
  - Analysis SW

- **Digital Validation**
  - Instruments
  - Probes
  - Analysis SW

- **Execution Validation**
  - Instruments
  - Probes
  - Analysis SW
DDR Analog Verification and Debug

Signal Acquisition
- Automatically trigger and capture Memory Interface signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis

Signal Access - Probing
- Easy but reliable physical connectivity
  - access to various measurement points on DRAM device
- Maximum signal integrity
  - sufficient performance for signal speeds

Signal Analysis
- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator
Signal Acquisition and Analysis
Triggering, ASM, DDRA and DPOJET
## DDRA Features and Benefits

**Complete Solution for Memory Interface Physical Layer Test**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Validation and Debug</td>
<td>Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3 the newest standards targeted for Server/Computer and Mobile handsets.</td>
</tr>
<tr>
<td>Selectable Speed Grades</td>
<td>Support for various JEDEC specification defined speed grades as well as custom speeds</td>
</tr>
<tr>
<td>Auto Configuration Wizard</td>
<td>Easily set up the test configuration for performing the analysis.</td>
</tr>
<tr>
<td>Qualified Multi-Rank Measurements</td>
<td>Isolate measurements to a rank of interest by using the chip select signal in a multi rank configuration</td>
</tr>
<tr>
<td>Cycle Type Identification</td>
<td>Navigate and Timestamp all the READ and WRITE cycles in an acquired record using Search and Mark</td>
</tr>
<tr>
<td>Visual Trigger / Pin Point Triggering</td>
<td>Quickly trigger, isolate and capture events of interest with Pin-Point HW Triggering combined with Visual Trigger and Active Search and Mark capabilities in Tektronix Oscilloscopes, making them an indispensable tool for Memory Interface Validation.</td>
</tr>
<tr>
<td>De-embedding</td>
<td>De-embed the effects of the Interposers and Probes to provide more accurately representation of the signal.</td>
</tr>
<tr>
<td>Test Selection</td>
<td>Provides the ability to select the Memory specification and the Speed Grade against which the analysis needs to be done as well as individual tests or group of tests to perform targeted analysis.</td>
</tr>
<tr>
<td>Reporting</td>
<td>Automatically generate consolidated reports that include pass/fail results, statistical measurement information as well as details about the test setup</td>
</tr>
<tr>
<td>Conformance and Debug</td>
<td>Quickly switch into debug mode in case a system fails conformance tests and use the DPOJET jitter analysis package</td>
</tr>
<tr>
<td>Probing Solutions</td>
<td>P7500 Trimode Probe Family and Micro-Coax Tips combined with Nexus Technology Interposers for various memory standards and packaging types results in a complete probing system that provides easy access to memory interface signals and allows making differential, single-ended, and common mode measurements accurately and definitively</td>
</tr>
<tr>
<td>Digital Channels on MSO</td>
<td>Address/Command signals acquired on the digital channels of the Mixed Signal Oscilloscope can be used to precisely qualify bus cycles or events of interest as well as perform timing measurements</td>
</tr>
<tr>
<td>Analysis and Debug Tools</td>
<td>Tektronix provides a broad range of tools for Electrical Test, Logic Debug and Execution Validation.</td>
</tr>
</tbody>
</table>
Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>JEDEC Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>JESD79E</td>
</tr>
<tr>
<td>DDR2</td>
<td>JESD79-2F</td>
</tr>
<tr>
<td>DDR3</td>
<td>JESD79-3F</td>
</tr>
<tr>
<td>DDR3L</td>
<td>JESD79-3-1</td>
</tr>
<tr>
<td>DDR4</td>
<td>JESD79-4</td>
</tr>
<tr>
<td>LPDDR</td>
<td>JESD209A</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>JESD209-2E</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>JESD209-3</td>
</tr>
<tr>
<td>LPDDR4</td>
<td>JESD209-4</td>
</tr>
<tr>
<td>GDDR5</td>
<td>JESD212</td>
</tr>
</tbody>
</table>
Memory Technology Overview

- **DRAM - Dominant Memory Technology**
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMM, SODIMM
  - Embedded systems
    - Cell phones, Ultra-Thin Notebooks, iPads
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR4 release on 26th Sep 2012 Maximum 3200 MT/s data rates transfer
    - LPDDR3-E planned can go unto 2133MT/s
    - DDR3L* operates at 1.35V
  *The "L" in DDR3L stands for low-voltage 1.5V – DDR3

- **DRAM variants**
  - DIMM based - Speed and Performance
    - DDR, DDR2, DDR3 and DDR4
  - Low Power DDR
    - LPDDR, LPDDR2, LPDDR3, LPDDR3E, LPDDR4
  - Graphic DDR - Optimized for Speed - faster access
    - GDDR3, GDDR5 @ 5500 MT/s
  - Low Voltage DDR
    - DDR3L, DDR3U
Memory Market Trends – Main Stream

New Roadmap

More realistic roadmap is 2015

DDR4

DDR3

800-2133

2133-4266

DDR2

400-800

DDR1

200-400

SDRAM

66-133

1999

2002

2006

2010

2015

This creates the need for faster DDR3 bins

And pushes DDR4 higher
Memory Market Trends - LPDDR

Mobile DRAM Technology Trend

- Bring up right technology at right on time
  - LP2-800 ('10) → LP3-1600('12) → LP4-3200('14)

<table>
<thead>
<tr>
<th></th>
<th>'10</th>
<th>'11</th>
<th>'12</th>
<th>'13</th>
<th>'14</th>
<th>'15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface VDD/VDDQ</td>
<td>LPDDR2 1.2V/1.2V</td>
<td>LPDDR3 1.2V/1.2V</td>
<td>LPDDR4</td>
<td></td>
<td>WIO and WIO2</td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>6.4GB/s</td>
<td>8.5GB/s</td>
<td>12.8GB/s</td>
<td>25.6GB/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>2Gb</td>
<td>4Gb</td>
<td>8Gb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PKG</td>
<td>Up to 4 die stacks: 1.0 mm → 0.9mm and below</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Source: Samsung Presentation JEDEC Mobile Event Seoul*
# Oscilloscope Bandwidth Requirement

<table>
<thead>
<tr>
<th>Memory Technology</th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR3</th>
<th>DDR3L</th>
<th>LPDDR3</th>
<th>DDR4</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed</strong></td>
<td>all rates</td>
<td>to 400MT/s</td>
<td>to 800MT/s</td>
<td>to 1600MT/s</td>
<td>to 2400MT/s</td>
<td>to 1600MT/s</td>
<td>to 1600MT/s</td>
<td>to 3200MT/s</td>
<td>to 4267MT/s</td>
</tr>
<tr>
<td><strong>Max slew rate</strong></td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>8</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td><strong>Typical V swing</strong></td>
<td>1.8</td>
<td>1.25</td>
<td>1.25</td>
<td>1</td>
<td>1</td>
<td>0.9</td>
<td>0.6</td>
<td>0.8</td>
<td>0.3</td>
</tr>
<tr>
<td><strong>20-80 risetime (ps)</strong></td>
<td>216</td>
<td>150</td>
<td>150</td>
<td>60</td>
<td>50</td>
<td>45</td>
<td>45</td>
<td>27</td>
<td>27</td>
</tr>
<tr>
<td><strong>Equivalent Edge BW</strong></td>
<td>1.9</td>
<td>2.7</td>
<td>2.7</td>
<td>6.7</td>
<td>8.0</td>
<td>8.9</td>
<td>8.9</td>
<td>15.0</td>
<td>15.0</td>
</tr>
<tr>
<td><strong>Recommended Scope BW</strong> (Max Performance)</td>
<td>2.5</td>
<td>3.5</td>
<td>4.0</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>16</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td><strong>Recommended Scope BW</strong> (Typ Performance)</td>
<td>2.5</td>
<td>2.5</td>
<td>3.5</td>
<td>8.0</td>
<td>12.5</td>
<td>12.5</td>
<td>16</td>
<td>16</td>
<td></td>
</tr>
</tbody>
</table>

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 LPDDR3 and LPDDR4 is supported only on DSA/MSO/DPO70000C/D models only
- LPDDR4 is a separate license
Specialized Measurements for DDR

- JEDEC Standards specify measurements & methods

9 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>DDR3-800, 1066, 1333, and 1600</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{O_{HP}}$</td>
<td>DC output high measurement level (for IV curve linearity)</td>
<td>$0.8 \times V_{DDQ}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{O_{UP}}$</td>
<td>DC output and measurement level (for IV curve linearity)</td>
<td>$0.5 \times V_{DDQ}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{O_{LP}}$</td>
<td>DC output low measurement level (for IV curve linearity)</td>
<td>$0.2 \times V_{DDQ}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{O_{HLP}}$</td>
<td>AC output high measurement level (for output SR)</td>
<td>$V_{TT} = 0.1 \times V_{DDQ}$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>$V_{O_{LDP}}$</td>
<td>AC output low measurement level (for output SR)</td>
<td>$V_{TT} = 0.1 \times V_{DDQ}$</td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE 1. The swing of $0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 $\Omega$ and an effective test load of 25 $\Omega$ to $V_{TT} = V_{DDQ}/2$.

9.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of differential signals.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>DDR3-800, 1066, 1333, and 1600</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{O_{HLP}}$</td>
<td>AC differential output high measurement level (for output SR)</td>
<td>$0.1 \times V_{DDQ}$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>$V_{O_{LDP}}$</td>
<td>AC differential output low measurement level (for output SR)</td>
<td>$-0.1 \times V_{DDQ}$</td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE 1. The swing of $0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 $\Omega$ and an effective test load of 25 $\Omega$ to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.
DDR4 DDRA Measurements

Broad range of JEDEC-specified measurements

- Example measurements list for DDR4

<table>
<thead>
<tr>
<th>Write Burst</th>
<th>Read Burst</th>
<th>Clock(Diff)</th>
<th>DQS(Single Ended)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Eye Height</td>
<td>Data Eye Height</td>
<td>tDVAC(Ck)</td>
<td>AC-Overshoot(DQS)</td>
</tr>
<tr>
<td>Data eye Width</td>
<td>Data eye Width</td>
<td>tRPRE</td>
<td>AC-Overshoot(DQS#)</td>
</tr>
<tr>
<td>tDQSH</td>
<td>tRPST</td>
<td>tCLK(avg)</td>
<td>AC-Overshoot(DQ)</td>
</tr>
<tr>
<td>tDQL</td>
<td>tQSH</td>
<td>tCCH(avg)</td>
<td>AC-Undershoot(DQS)</td>
</tr>
<tr>
<td>tDSS-Diff</td>
<td>tQSL</td>
<td>tCCH(abs)</td>
<td>AC-Undershoot(DQ#)</td>
</tr>
<tr>
<td>tDVAC(DQS)</td>
<td>tDQSCK-Diff</td>
<td>tCCK(abs)</td>
<td>AC-Undershoot(DQ)</td>
</tr>
<tr>
<td>tDQSS-Diff</td>
<td>tDQSQ-Diff</td>
<td>tCCL(abs)</td>
<td>AC-UndershootArea(DQS)</td>
</tr>
<tr>
<td>tWPST</td>
<td>tQPST</td>
<td>tSRQdiff(Rise(DQS))</td>
<td>AC-UndershootArea(DQS#)</td>
</tr>
<tr>
<td>TdIPW-High</td>
<td>tQH</td>
<td>tSRQdiff(Fall(DQS))</td>
<td>AC-OvershootArea(DQ)</td>
</tr>
<tr>
<td>TdIPW-Low</td>
<td>tDVAC(DQS)</td>
<td>tSRQse(Rise(DQ))</td>
<td>Vix(ac)DQS</td>
</tr>
<tr>
<td>VIHL AC</td>
<td>SRQdiff(Rise(DQS))</td>
<td>tSRQse(Fall(DQ))</td>
<td>VSEH(DQS)</td>
</tr>
<tr>
<td>SRIN_dIVW_Rise</td>
<td>SRQse(Rise(DQ))</td>
<td>tLR(DQ)</td>
<td>VSEL(DQS)</td>
</tr>
<tr>
<td>SRIN_dIVV_Fall</td>
<td>SRQse(Fall(DQ))</td>
<td>tHZ(DQ)</td>
<td>VSEL(DQS#)</td>
</tr>
</tbody>
</table>

- Clock Single Ended
  - Vix(ac)CK
  - VSEH(CK)
  - VSEL(CK)
  - VSEL(CK#)
  - AC-Overshoot(CK)
  - AC-Overshoot(CK#)
  - AC-Undershoot(CK)
  - AC-Undershoot(CK#)
  - AC-OvershootArea(CK)
  - AC-OvershootArea(CK#)
  - AC-UndershootArea(CK)
  - AC-UndershootArea(CK#)

- Address/Command
  - tIPW-High
  - tIPW-Low

- tERR(Per) n - 13 TO 50
Test Setup and Configuration

- All the tests are logically grouped based on the input source requirement
  - READ
  - WRITE
  - CLOCK
  - ADDR/CMD
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.
- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.
Burst Detection

- Read / Write bursts are automatically detected for analysis purposes
- Several different techniques are used for Read/Write Burst Separation
  - DQ/DQS phase alignment: DQ and DQS have different phase relationship in Read and Write bursts
  - CS, Latency + DQ/DQS Phase Alignment: CS is used to qualify the occurrence of a burst, followed by DQ/DS phase relationship to distinguish between Read/Write
  - Logic State + Burst latency: The command bus probed using the digital channels on the MSO is used to identify Read/Write commands on the command bus are quality and distinguish Read and Write bursts
- Options are provided to adjust the levels to improve burst detection in systems with lower signal integrity
Digital + Analog Probing for MSO70K

- 16 Digital Channels in addition to 4 Analog Channels

---

<table>
<thead>
<tr>
<th>TSF Format</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>File Radix</td>
<td></td>
</tr>
<tr>
<td>+ Version 2.1.0 PATTERN</td>
<td></td>
</tr>
<tr>
<td>Command</td>
<td>Command</td>
</tr>
<tr>
<td>Symbol Name</td>
<td>Pattern</td>
</tr>
<tr>
<td># CS RAS CAS WE (D3 D2 D1 D0)</td>
<td></td>
</tr>
<tr>
<td># MODE_REG</td>
<td>0000</td>
</tr>
<tr>
<td>REFRESH</td>
<td>0001</td>
</tr>
<tr>
<td>PRECHARGE</td>
<td>0010</td>
</tr>
<tr>
<td>ACTIVATE</td>
<td>0011</td>
</tr>
<tr>
<td>WRITE</td>
<td>0100</td>
</tr>
<tr>
<td>READ</td>
<td>0101</td>
</tr>
<tr>
<td>NOP</td>
<td>0111</td>
</tr>
<tr>
<td>DESELECT</td>
<td>1XXX</td>
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---

- RAS#
- WE#
- CAS#
- CS#

- DQ0
- DQS0
- Clock
# Uncompromised Analog/Digital Acquisition

## Banner Specifications

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Digital
MSO DDRA Integration – makes a powerful tool

- DDRA integrated with MSO 70k Digital channels
  - Makes a perfect tool for DDR Analysis.

- The following is a direct quote from an Agilent application note, evaluating different approaches to DDR PHY-layer testing:
  - “By connecting the control signals to the MSO’s digital inputs, you can trigger on different operation modes (read, write, etc)… However, the MSO solution has low bandwidth… Otherwise, an MSO is a perfect solution for DDR signal debugging.”
Burst Detection

- Easily Identify, Mark & Measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL Reads/writes within an acquisition
Reports

- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes:
  - Measurement results
  - Pass/Fail test results based on specification values
  - Summary and detail plots
  - Oscilloscope screenshots
  - Measurement and Instrument configuration summary
- Report contents are user definable content
- Provision to append more results later
Beyond DDRA

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark
Signal Analysis & Debug

**DDRA + DPOJET**

- DDRA is not a closed tool – seamlessly links directly to DPOJET for measurement analysis
- Opportunity to change or fine-tune settings, add new measurements as needed

- DPOJET - powerful measurement engine for DDRA
- All settings are explicit – you can see them and change them.

“One Click” access to DPOJET & back
DPOJET Analysis Overview

Waveform

- Live Analog
- Live Digital
- Reference Memory

Link Analysis (SDLA)

Math

Jitter

Eye

Timing

Period

Acquire

DPOJET works with the following data sources:
- Analog
- Digital
- Math
- Reference

Transform

Data from a data source can be post processed to achieve visibility at multiple test points or after math transformations.

Measure / Analyze

Measure simultaneously across multiple test points and measurement configurations.
Plot and zoom on worst case to provide deeper levels of insight.

Reporting

Get a test report with measurement results, pass fail limits, plots, user comments and instrument configurations.
DPOJET Debug Tools

- “Find Worst Case Events” feature
  - Zoom to waveform from Min / Max for each measurement
Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
  - FastAcq shows any disparities on signals, like infrequent glitch’s
Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 verticies
- Areas are “keep in” or “keep out” and can be applied to either trigA or trigB.
- Can be used to
  - Separate Read / Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams
Visual Trigger Used For DQ Pattern Detection

010000X Pattern
Eye Mask testing
DRAM Input RX Mask

- For DDR4 JEDEC is moving to a mask based approach for DQ eye measurement at Rx input
- After the Eye is built using DDRA Using the built in Mask Measurement capability the Pass/Fail results can be obtained.

Mask = 136mV x 125ps (0.2UI)
Signal Access
Probing
TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements: \(((V+) + (V-))/2\) with respect to ground

- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!
Before and After

**Before TriMode Probing**
1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode

**After TriMode Probing**
1 Probe and 1 setup for Differential, SE and Common Mode
Analog Solder-In Probing Solutions

P7500 Series Tri-Mode Probes

Socket Cable 020-2954-xx

TriMode Micro-Coax Tip 4GHz

P75TLRST Solder Tip up to 20GHz
BGA Chip Access For DDR2, DDR3

- Unique, reusable socket design allows for multiple chip exchanges
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models
Memory Probing

- Computer Systems use standardized DIMM’s for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- Memory Components use BGA or PoP Packages
  - Reduces the parasitics, enabling performance at higher speeds
  - Mandate from JEDEC
- Probing a BGA or PoP package is Difficult
  - Unable to probe at the Balls of the Device
  - Probing at a connector, trace, or a via is not the same as probing at the device
  - Not a true representation of the signal
Memory Component Interposers

- Provide easy access to signals of Interest
- Controller Impedance path with embedded resistor for good signal Integrity
- De-embed filters to remove effects of interposer tap trace
- SPICE model available upon request for simulation and analysis

<table>
<thead>
<tr>
<th>Memory Standard</th>
<th>Supported Form Factors</th>
<th>Interposer Types</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2</td>
<td>- BGA</td>
<td>- Socketed Interposer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Direct Attach Interposer</td>
</tr>
<tr>
<td>DDR3</td>
<td>- BGA</td>
<td>- Socketed Interposer</td>
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<td></td>
<td></td>
<td>- Direct Attach Interposer</td>
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<tr>
<td></td>
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<tr>
<td></td>
<td></td>
<td>- Instrumented DIMM</td>
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<tr>
<td>DDR4</td>
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<td>- Direct Attach Perimeter Interposer</td>
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<tr>
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<td>LPDDR2</td>
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<td></td>
<td>- PoP</td>
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<td></td>
<td></td>
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Interposer Types

Socketed Interposers
- Comes with a Custom BGA Socket that needs to be soldered to Target
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

PoP Interposers
- Comes with a Custom BGA Socket that needs to be soldered to Application Processor
- Allows snap-in/snap-out of components using micro socket
- Full BGA visibility
- No Special design or routing requirements needed
- Quickly swap TLA & oscilloscope interposers on the same target.
- Quickly Swap Memory Components on the Target

Direct Attach Interposers
- Interposer is soldered to Target
- Memory Component is soldered to Interposer
- Full BGA visibility
- No Special design or routing requirements needed
Interposer Types

**Direct Attach Perimeter Interposers**
- Interposer is soldered to the Target
- Memory component is soldered to Interposer
- Signals are brought to pads on edge of the Interposer
- KoV of the interposer is the same size as the BGA component
- Because of limited space around the edge not all signals can be probed
- Choose between wide / narrow Address or data

**MSO Interposers**
- Provides a quick and easy access of the Addr/CMD signals to MSO digital channel
- Allows the Addr/cmd triggers to correlate Analog Inputs
- Combine with Component Interposers for high fidelity analog analysis
Interposer Filter File Integration

- Additional step in the setup process
- Integrates the application of the de-embed filter useful for characterization
- UI is XML driven new selections can be added to the menu’s by editing XML
- Supports custom filter application
De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will be available for the interposers upon request. These de-embedding filters are developed assuming nominal values.
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used.
Why use SDLA Visualizer

Remove Reflections

- Probing at non-ideal locations can cause reflections on the acquired signal, which are not present at the ideal probe location.
- With SDLA visualizer, reflections from Memory interfaces can be compensated for with limited DUT knowledge.

Transmission Line Delay

Package Model

Receiver Input Impedance
Remove Reflections

Estimate Load Resistance and Transmission Line Delay

- Use cursors to get ratio of reflected to incident voltage.
- Compute resistance as:
  \[ R = Z_0 \left( \frac{1 + \Gamma}{1 - \Gamma} \right) \]
  \[ \Gamma = \frac{V_2 - V_1}{V_1} \]
  \[ \Gamma = \frac{1.25 - 0.75}{0.75} \]
  \[ R = 200 \]
- Tune R to get best results. 220 ohms was used

- Use cursor measurement to get delay for round trip reflection.
- Then divide by 2.
  \[ T_d = \frac{660\text{ps}}{2} \]
  \[ T_d = 330\text{ps} \]
Remove Reflections

*De-Embed Results…*

- White is original acquired signal with the reflection.
- Purple is the de-embedded result showing reflection removal.
Memory Information Resources

- Tektronix  
  - www.tektronix.com/memory
- Nexus Technology  
  - www.nexustechnology.com
- Memory Implementers Forum  
  - www.memforum.org
- JEDEC  
  - www.jedec.org
Summary – World’s Best Memory Test Solution

Complete
- Provides JEDEC validation, characterization and full measurement support
- Comprehensive coverage of multiple memory standards in one single package

Performance
- Based upon high performing oscilloscopes and software analysis tools
- TriMode probing that enables three measurements with a single probe connection
- Read/Write burst identification on all bursts
- Automated setup with JEDEC pass/fail limits

Comprehensive Analog Verification and Debug Tools for Memory Interface
Thank You