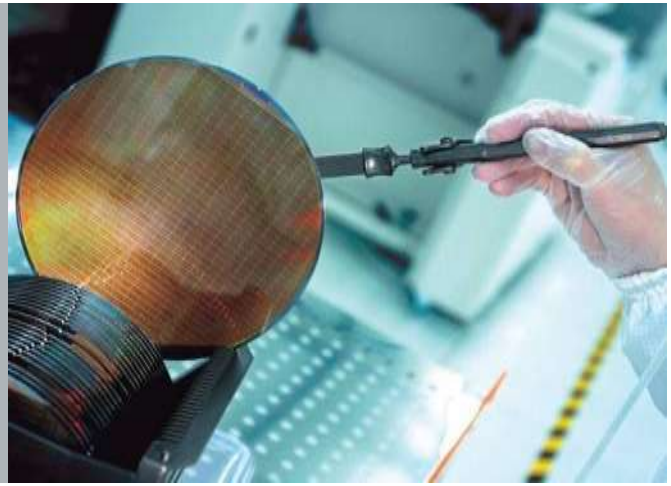
2014年泰克测试测量技术研讨会-厦门

信号完整性测试及实时数字系统分析解决方案



泰克科技（中国）有限公司　王宏军

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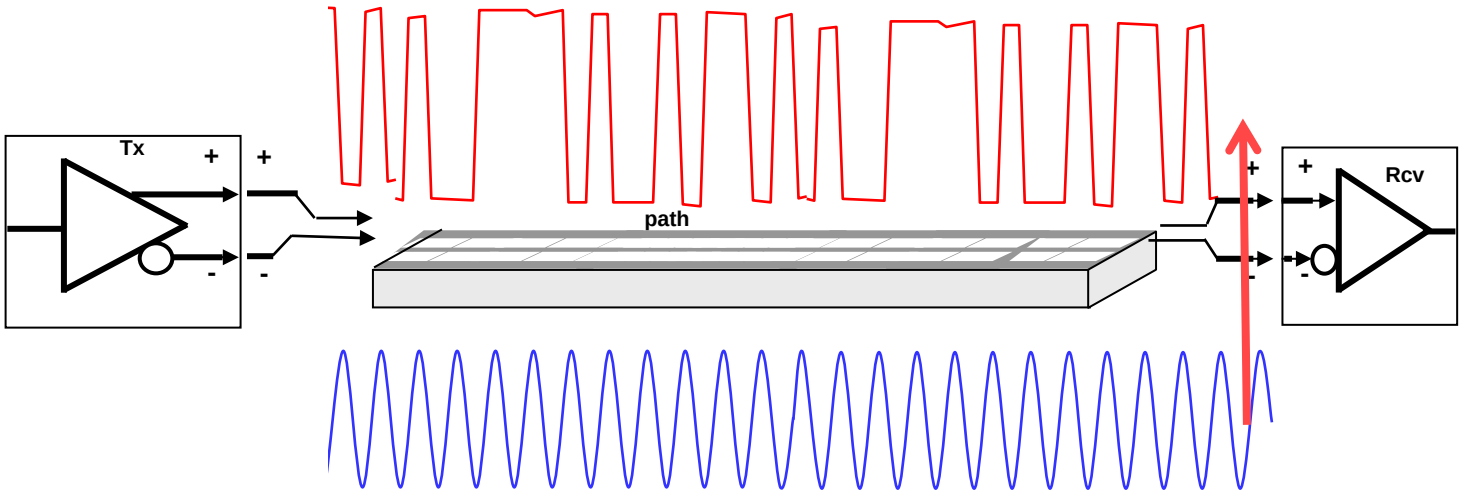
并行传输原理



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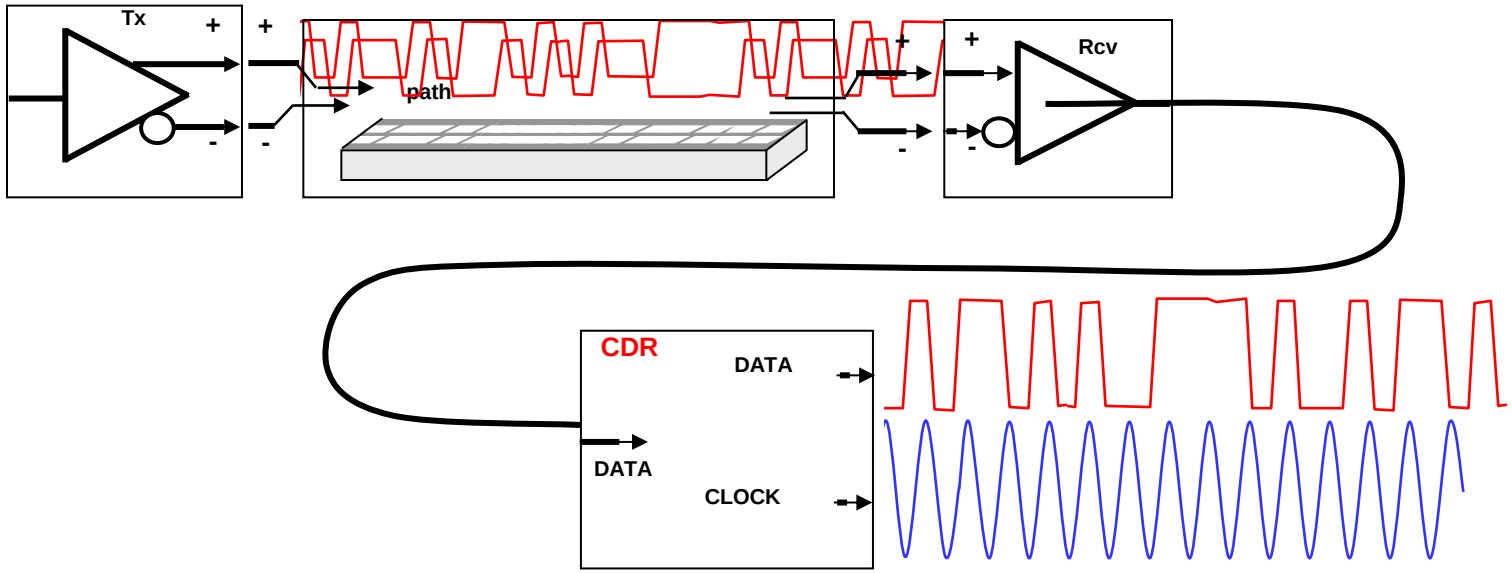
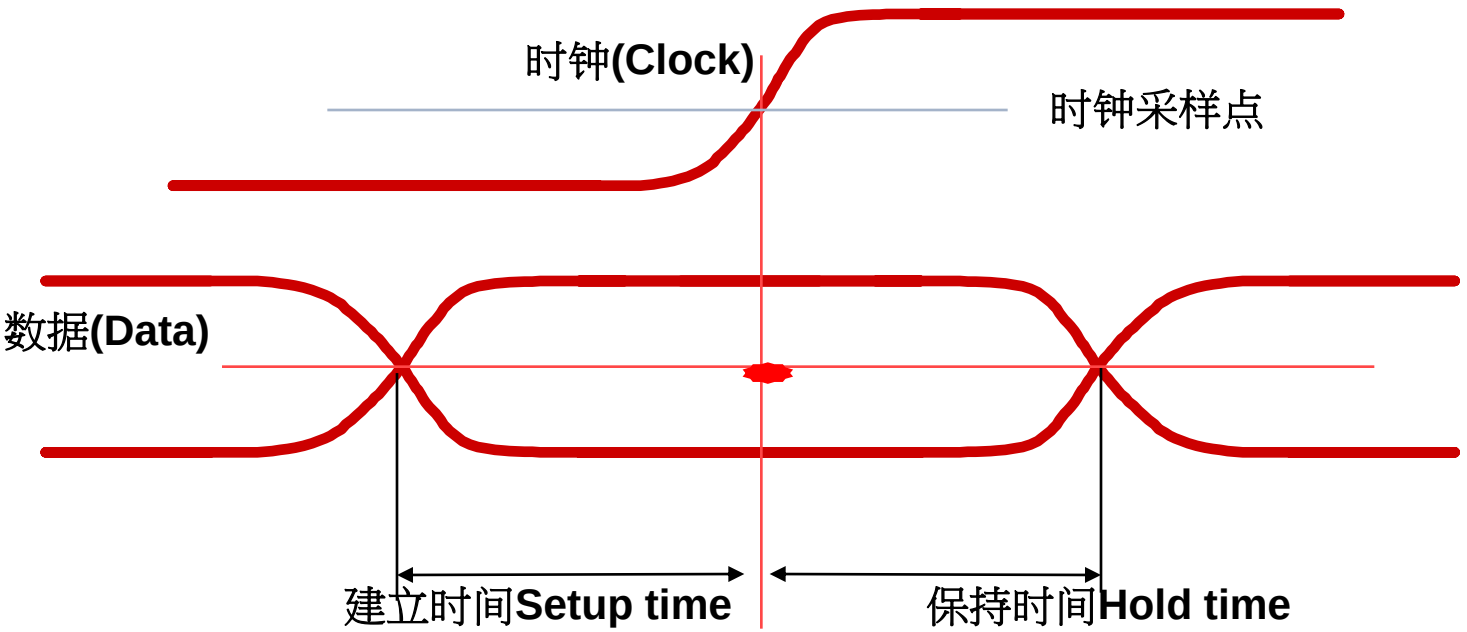
串行传输原理-所有的串行最终都会转成并行



硬件系统不稳定的根源-误码（Bit Error)

- 误码的根源：
  1.信号采样的时候建立保持时间不足(水平方向)
  2.信号的幅度不够（垂直方向）



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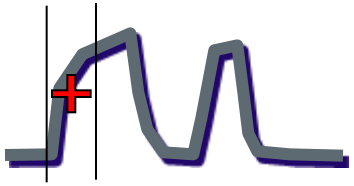
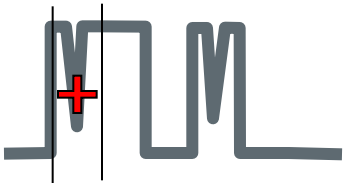
由于各种原因引起的误码

Example System Issues

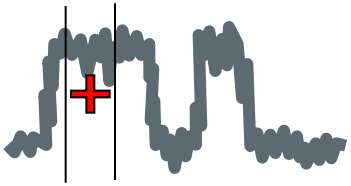


Circuit Board Dispersion
Fiber Dispersion
PMD

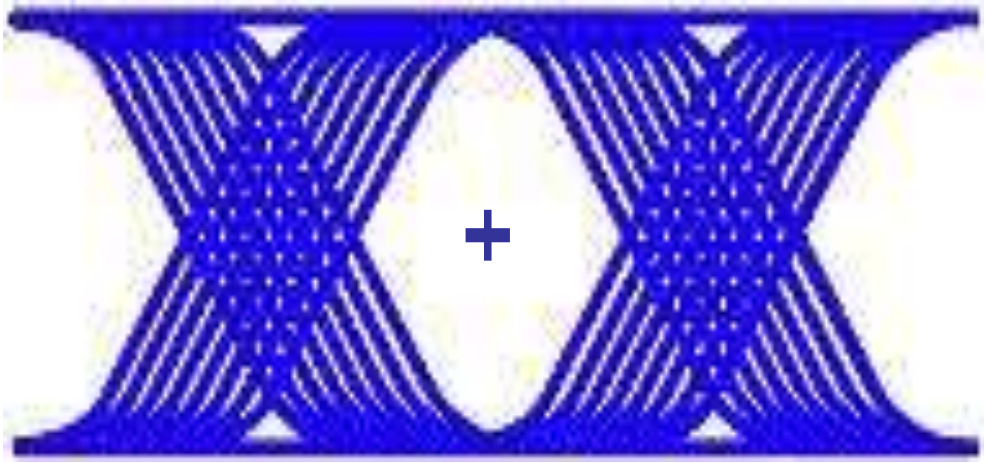
Edge Movement:
Frame slips
Frame overhead repetition
Pattern Sensitivity



External interference
Crosstalk

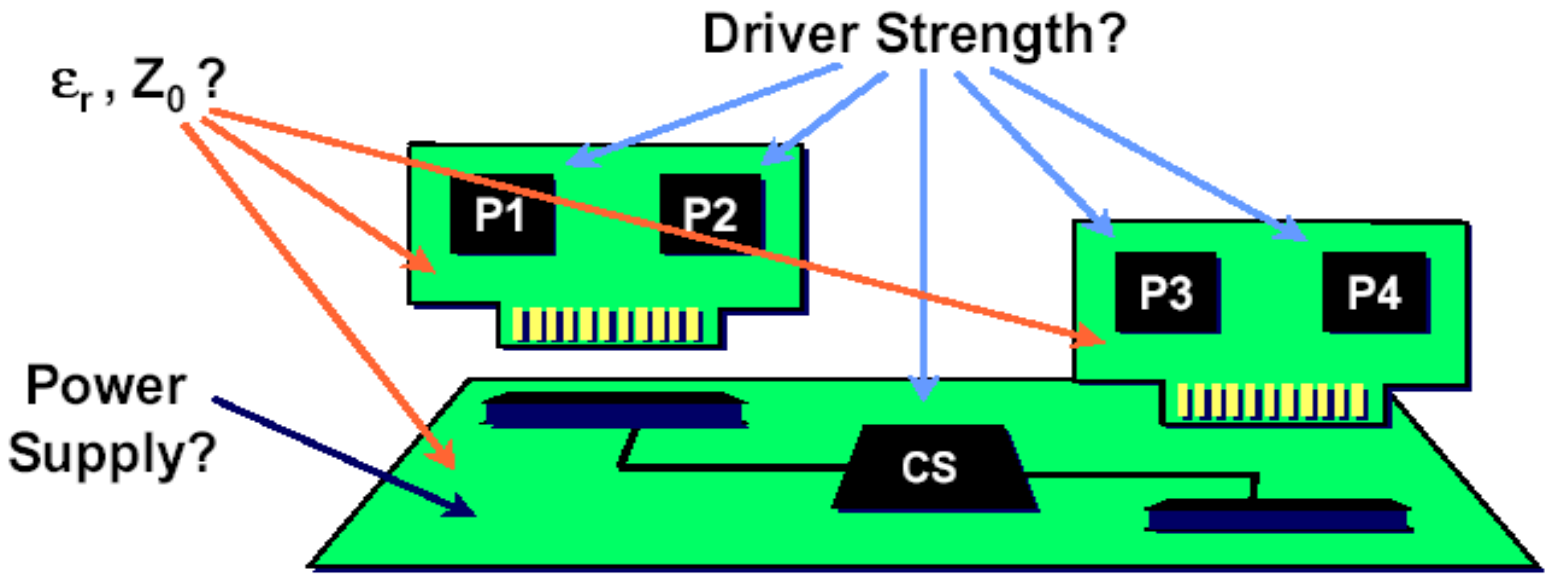


Low signal level
Other random effects



信号完整性

- 波形完整性（Waveform integrity）
- 时序完整性（Timing integrity）
- 电源完整性（Power integrity）
- 信号完整性分析的目的就是用最小的成本，最快的时间使产品达到波形完整性、时序完整性、电源完整性的要求。



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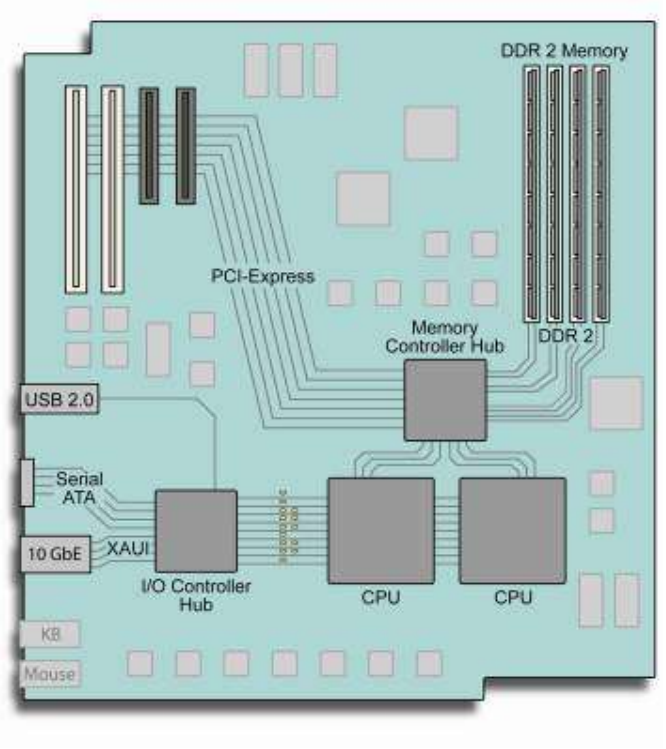
系统、单板设计中可能引起信号完整性的因素

At clock frequencies in the hundreds of megahertz and above, every design detail is important:

- **Clock distribution**
- **Signal path design**
- **Stubs**
- **Noise margin**
- **Impedances and loading**
- **Transmission line effects**
- **Signal path return currents**
- **Termination**
- **Decoupling**
- **Power distribution**



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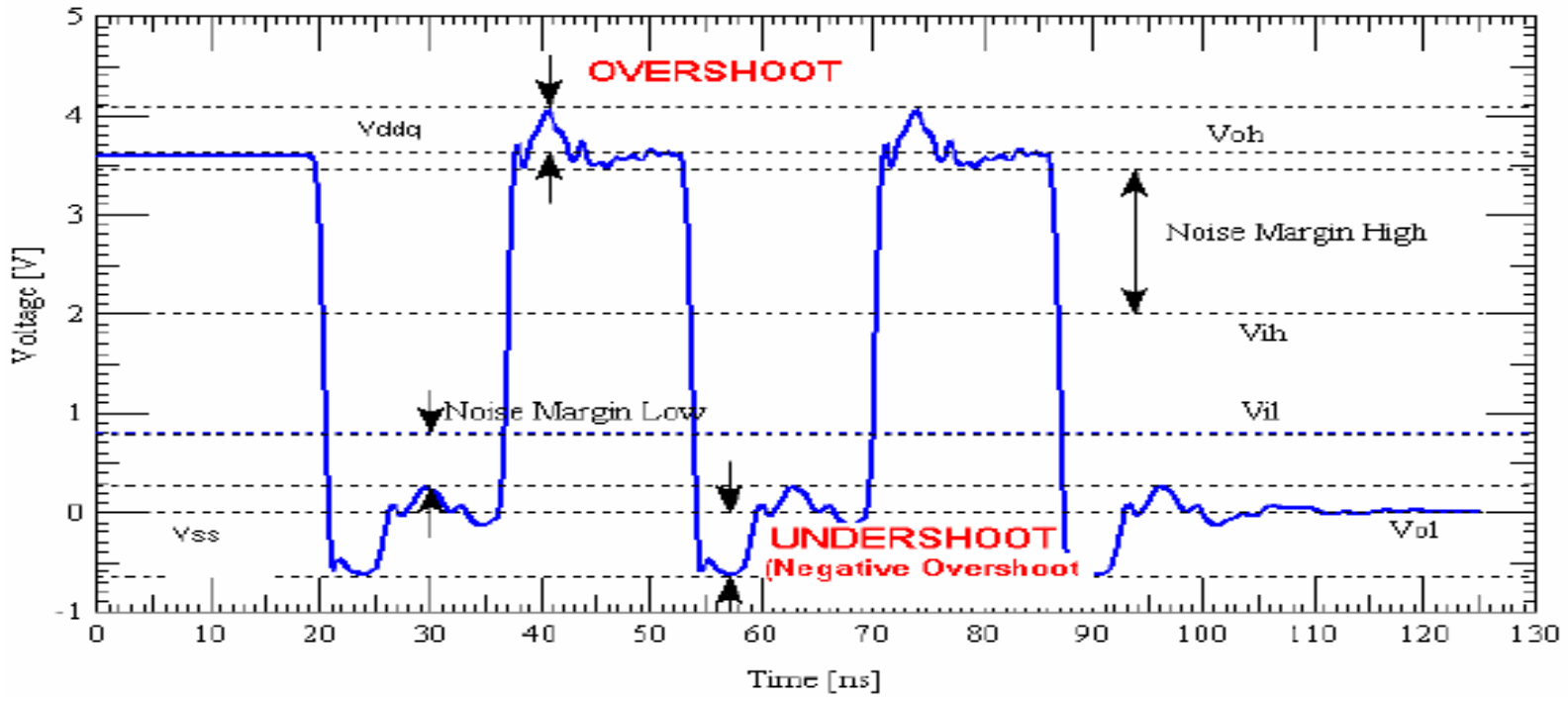
波形完整性Waveform integrity

- 单调性（monotonic)
- 过冲（overshoot, undershoot)
- 振铃（ringing）
- 衰减



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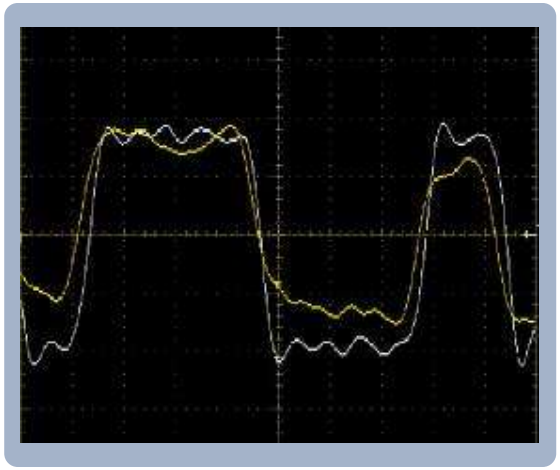
幅度和边沿的变化

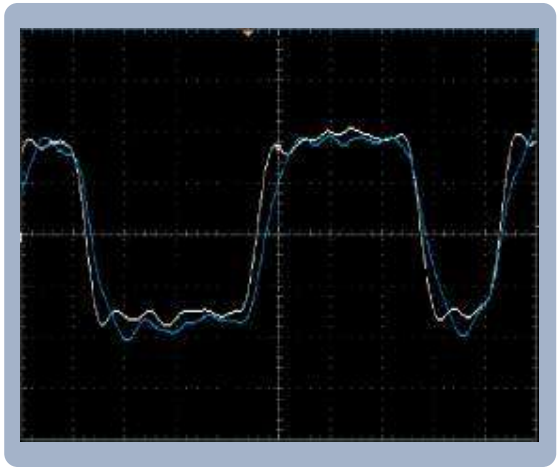
Amplitude Problems:

- Ringing
- Droop
- Runt pulses



Edge Aberrations:

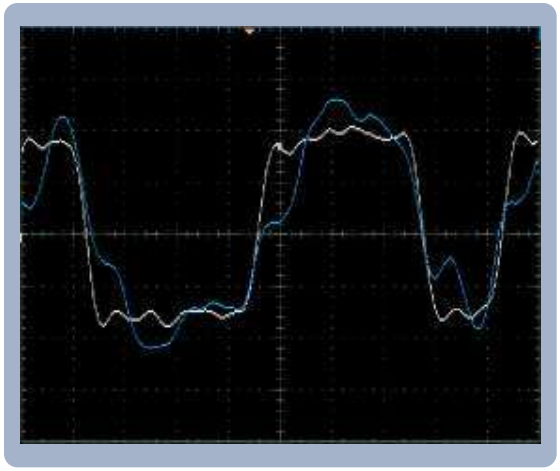
- Board layout issues
- Improper termination
- Circuit problems



反射（非单调）和地弹

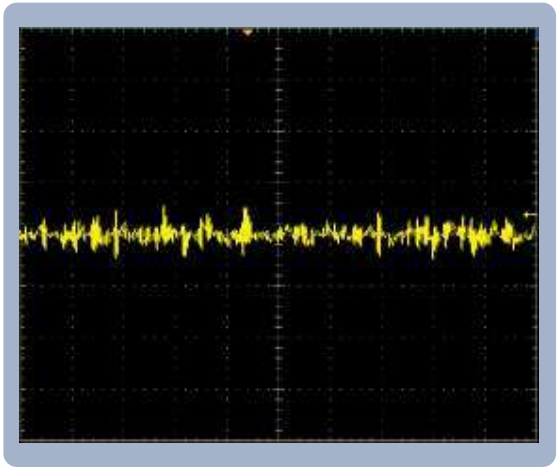
Reflections:

- **Board layout issues**
- **Improper termination**



Ground Bounce:

- **Excessive current draw**
- **Resistance in power supply and ground return paths**



出现波形完整性问题的原因

- 引起信号的非单调，过冲，振铃的原因：

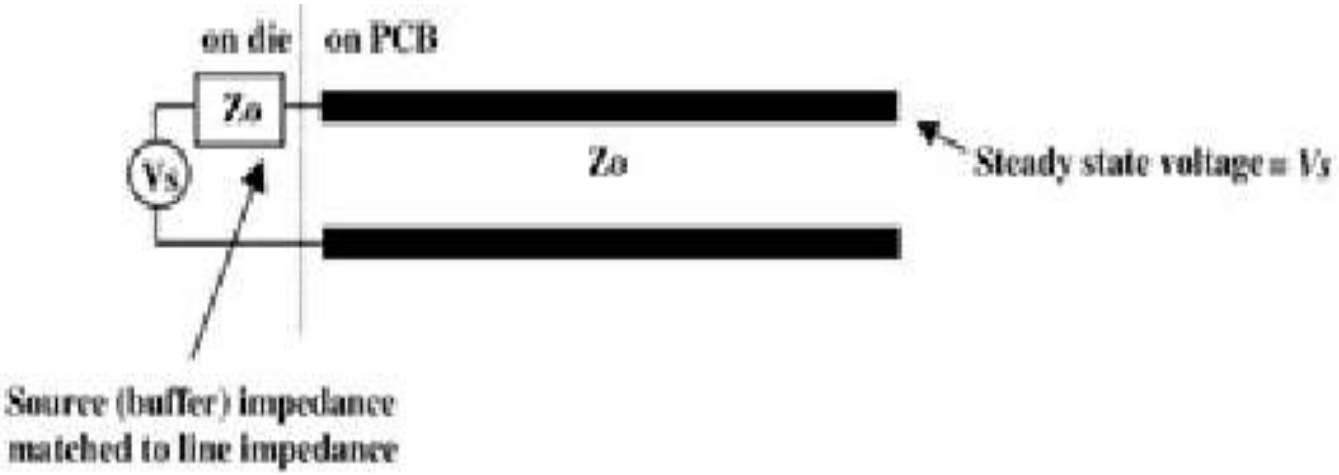
1) 驱动芯片的信号驱动能力过强，不足。
2) 驱动端为了减少EMI添加了磁珠。
3) 驱动和接收端阻抗不匹配造成反射。
4) 链路阻抗不匹配。
5) 链路的衰减。

消除反射的方法——端接

- 传输线上的反射会对数字系统性能有重要的负面影响，为了最小化反射的负面影响，必须想办法消除或减弱它。基本上有三种方法：第一降低系统的频率以使传输线上的反射将在另一个信号驱动到线上之前达到稳态。第二种是缩短PCB走线长度以使反射在更短的时间内达到稳态。第三种方法就是给传输线两端端接一个等于特征阻抗的阻抗，以消除反射。
- 第一种方法，不现实，否则就是一个低速系统了；第二种方法可能不现实也可能需要更多的代价比如更多的叠层等；第三种是最实际的利于我们采用的方法。
- 常用的端接方法有：片上源端端接、串联源端端接、带电阻负载的负载端接、交流负载端接。

常用的端接方法——片上源端端接

- 片上源端端接要求输出缓冲器I-V曲线在工作范围内非常线性，并输出一个阻抗与传输线阻抗非常接近的I-V曲线。
- 理论上，这是最佳方案但不现实，因为这不要求任何额外的元件而导致增加成本和浪费板空间。然而很多变量能彻底地影响缓冲器地输出阻抗，所以很难达到缓冲器阻抗和传输线阻抗之间的良好匹配。这些变量包括硅制作过程中的偏差、电压、温度、功率输出因数和同步开关噪声等。



片上源端终接

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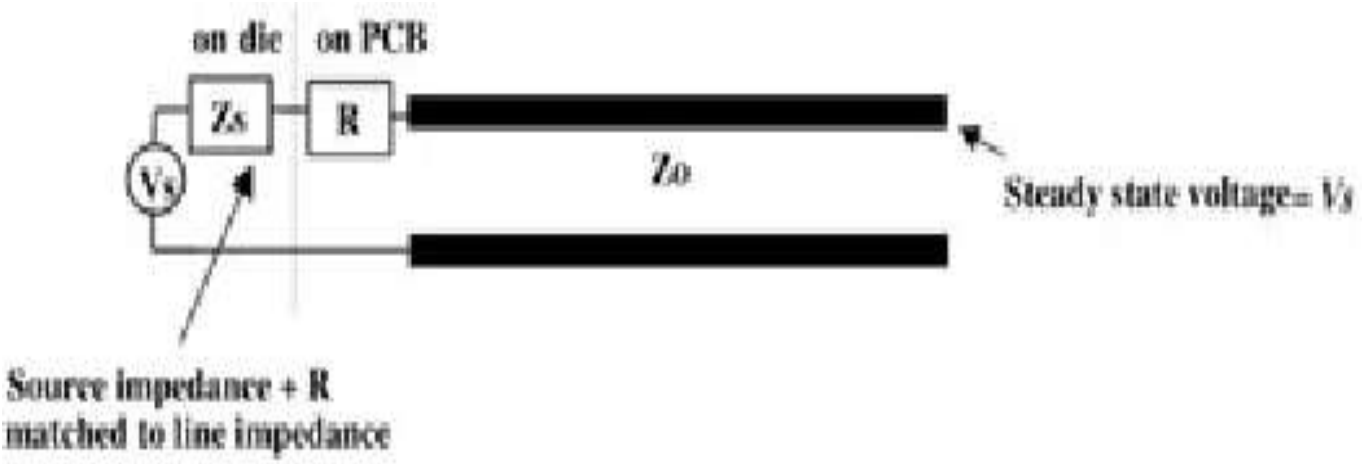
常用的端接方法——串联源端端接

- 串联源端端接要求加一个电阻与输出缓冲器串联。要求缓冲器阻抗和电阻值的和等于传输线的特征阻抗
- 通常设计输出缓冲器I-V曲线产生一个极低阻抗，以至于从源端看进去的阻抗的大部分都包含在电阻，因此选择精密电阻可以使总偏差降到很低，因为电阻包含了大部分的阻抗。这种方法的缺点就是电阻增加了板的成本并且占用有效的板面积。



串联源端终接

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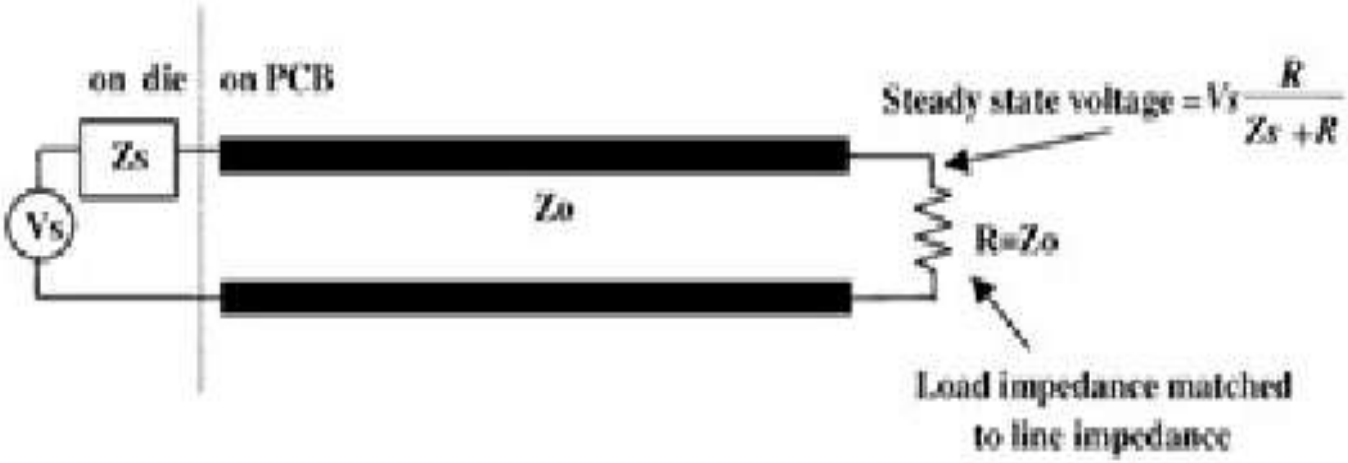
常用的端接方法——带电阻负载的负载端接

- 可以使用精密电阻，负载或带电阻负载的并联端接消除了缓冲器阻抗相关的未知变量。反射在负载端消除，并可使用低阻抗输出缓冲器。缺点是大部分的直流电流被分流到地，这加大了功率输出和发热问题。另外稳态电压也有源端电阻和负载电阻之间分压来确定，这引起更强大缓冲器地要求。



带电阻负载的负载终接

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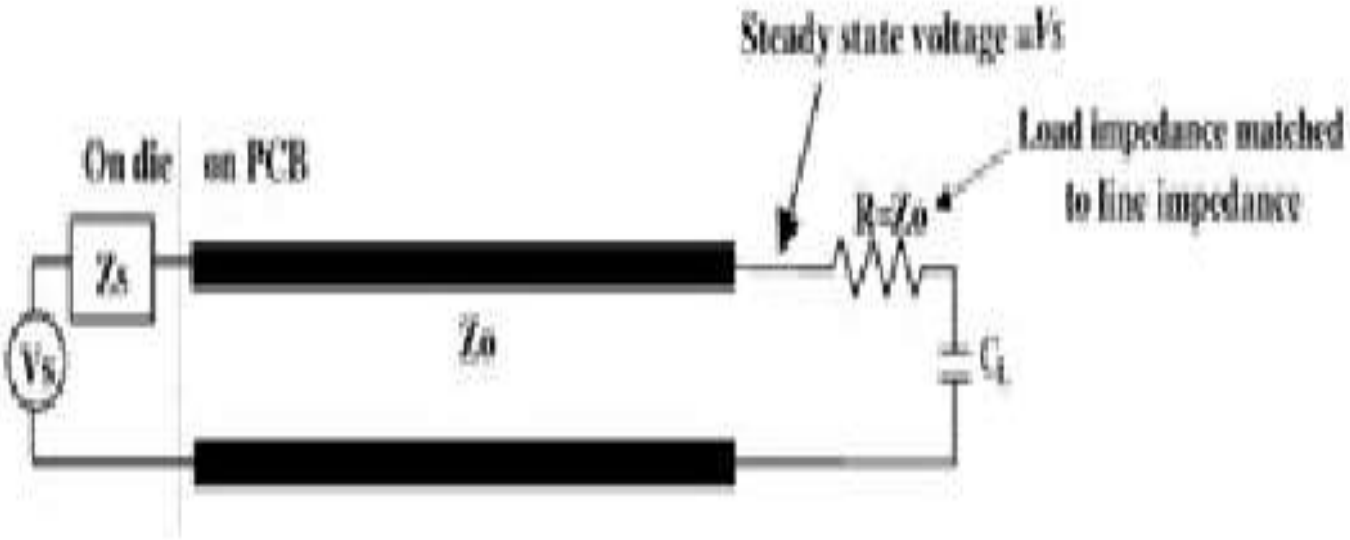
常用的端接方法——交流负载端接

- 交流负载端接在传输线的负载末端使用串联的电阻和电容以消除反射。电阻R应等于传输线的特征阻抗，而电容C应选择负载端的RC时间常数近似等于一个或两个上升时间。对于具体设计，建议使用仿真以选择最优的电容。
- 优点是在负载端上反射被消除，并且不产生直流功耗。缺点是电容负载将减缓负载端的上升或下降时间而增加信号延迟。另外附加的电阻和电容占用了板子空间并增加了成本。



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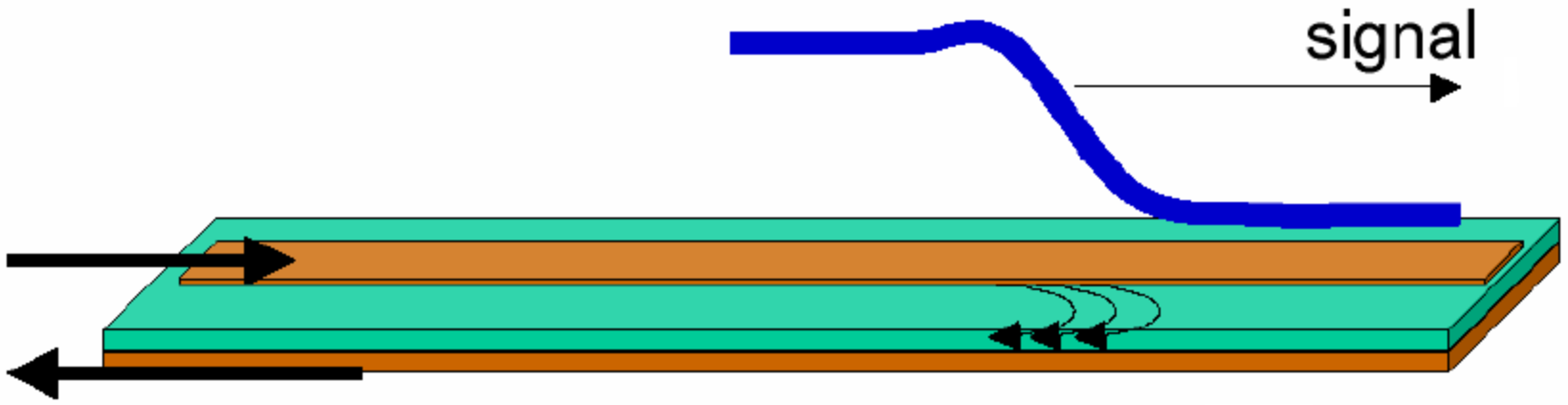
链路的阻抗匹配

特性阻抗：

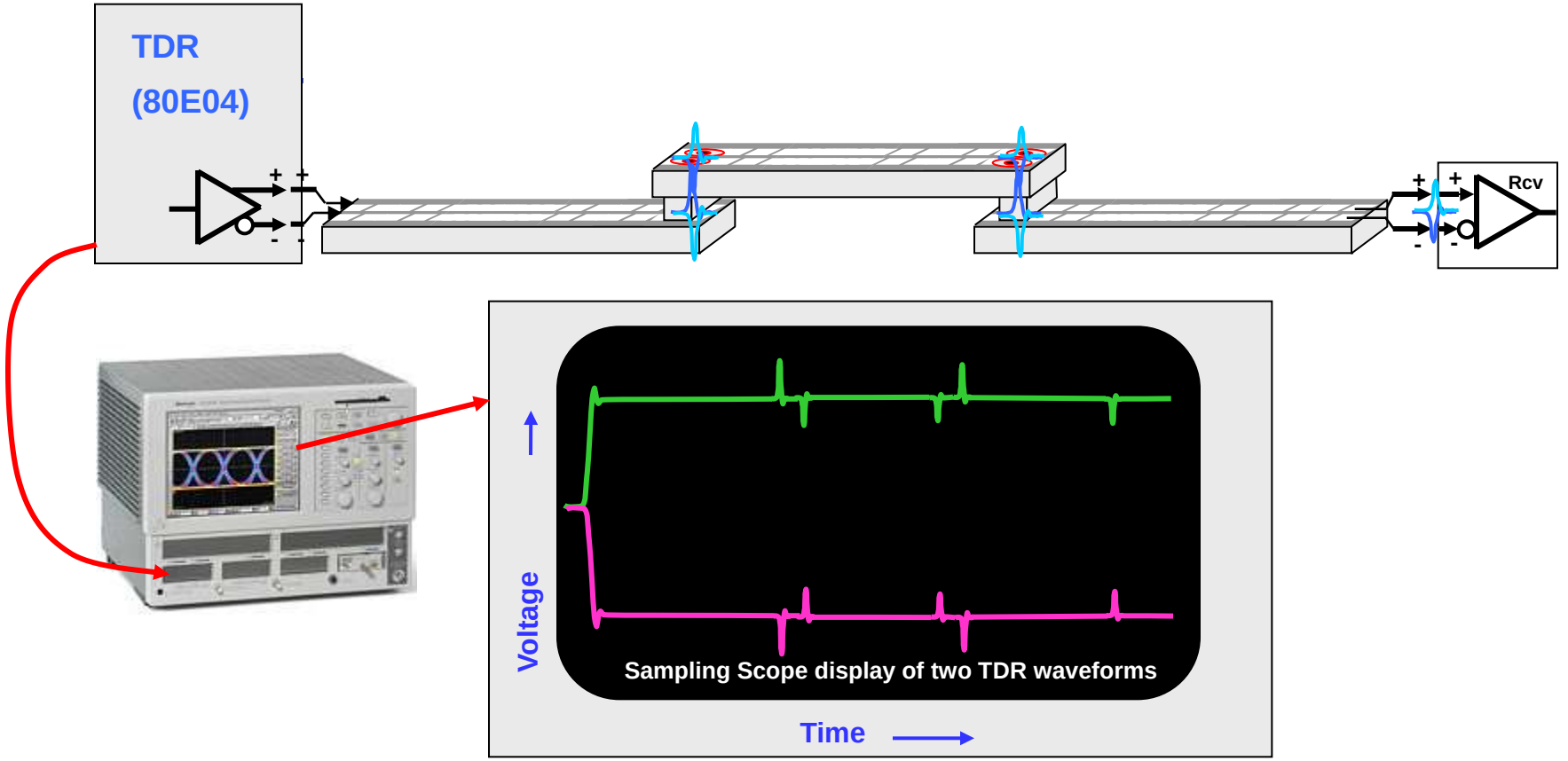
- 一个阶跃信号注入一个开路的信号线，信号线上的电压是不会突变的，信号线对地之间其实是存在动态的回路的。
- 有回路就存在电流。也就是说存在电阻。（动态的）
- 这个电阻是只有该阶跃信号本身所能“看到”的。



传输线的原理

- 信号沿传输线传播过程当中，如果传输线上各处具有一致的信号传播速度，并且单位长度上的电容也一样，那么信号在传播过程中总是看到完全一致的瞬间阻抗。
- 由于在整个传输线上阻抗维持恒定不变，我们给出一个特定的名称，来表示特定的传输线的这种特征或者是特性，称之为该传输线的特征阻抗。
- **特征阻抗**是指信号沿传输线传播时，信号看到的瞬间阻抗的值。
- 如果信号沿传输线在传播的过程当中，任何时候信号看到的特征阻抗都保持一致的话，那么这样的传输线就称为**受控阻抗的传输线**。

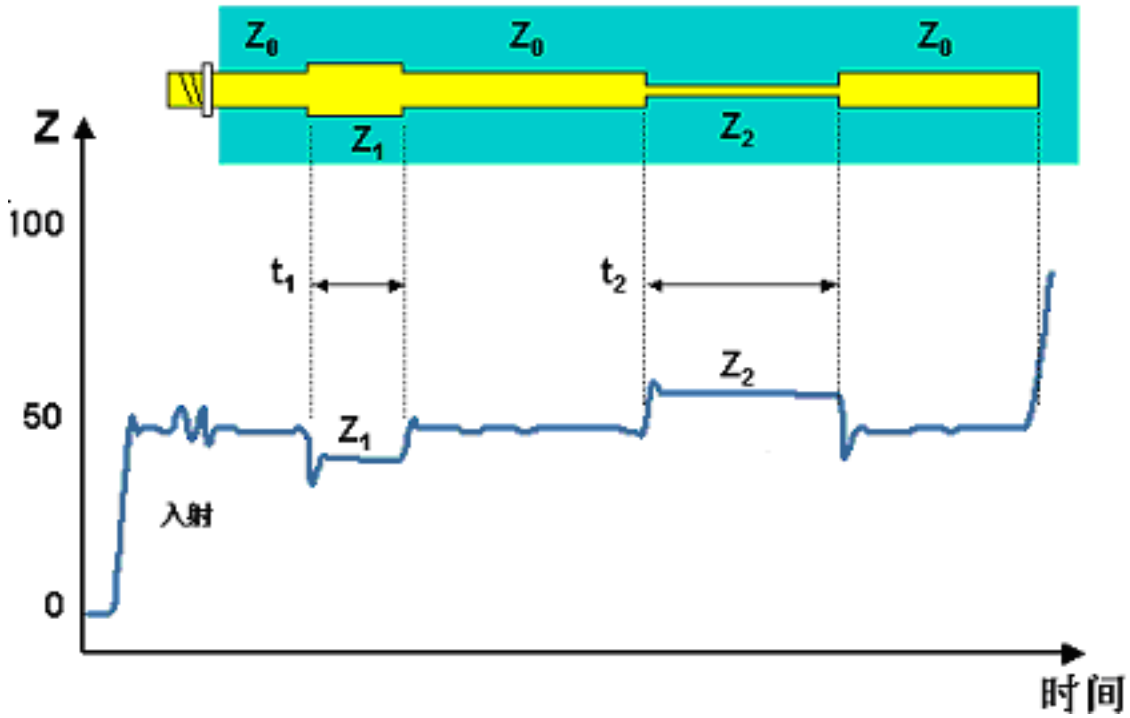
使用TDR的方法可以传输线的阻抗匹配问题



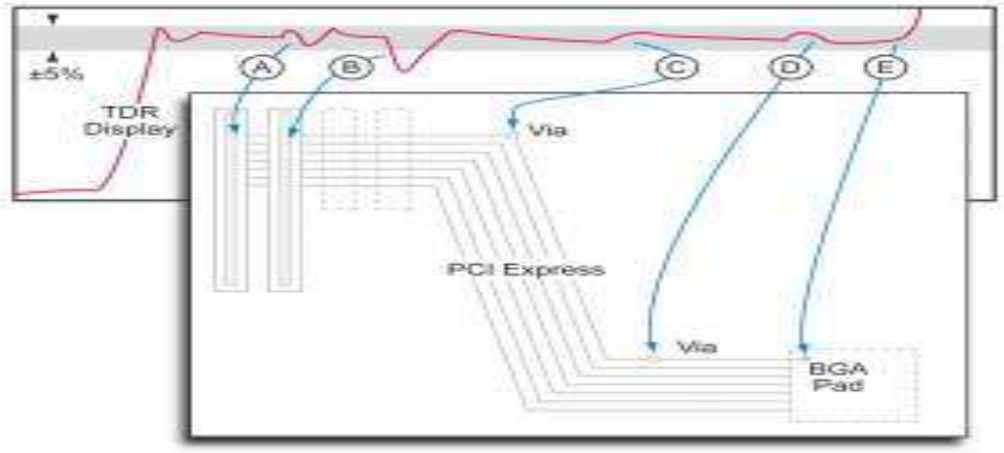
- ***Two TDR sampling channels allow the differential impedance between the DATA+ and DATA- serial paths to be measured.***

TDR曲线映射着传输线的各点

- 其中 ρ 是反射系数，Z_0是参考阻抗（一般为50ohm，由测试系统决定），Z是待测阻抗。由此仪器可以计算显示出传输线各个点的阻抗，从而可以在仪器的屏幕上显示一条TDR曲线，曲线的每一点对应传输线上的每一点的反射系数或特征阻抗。



通过TDR定位故障的实例



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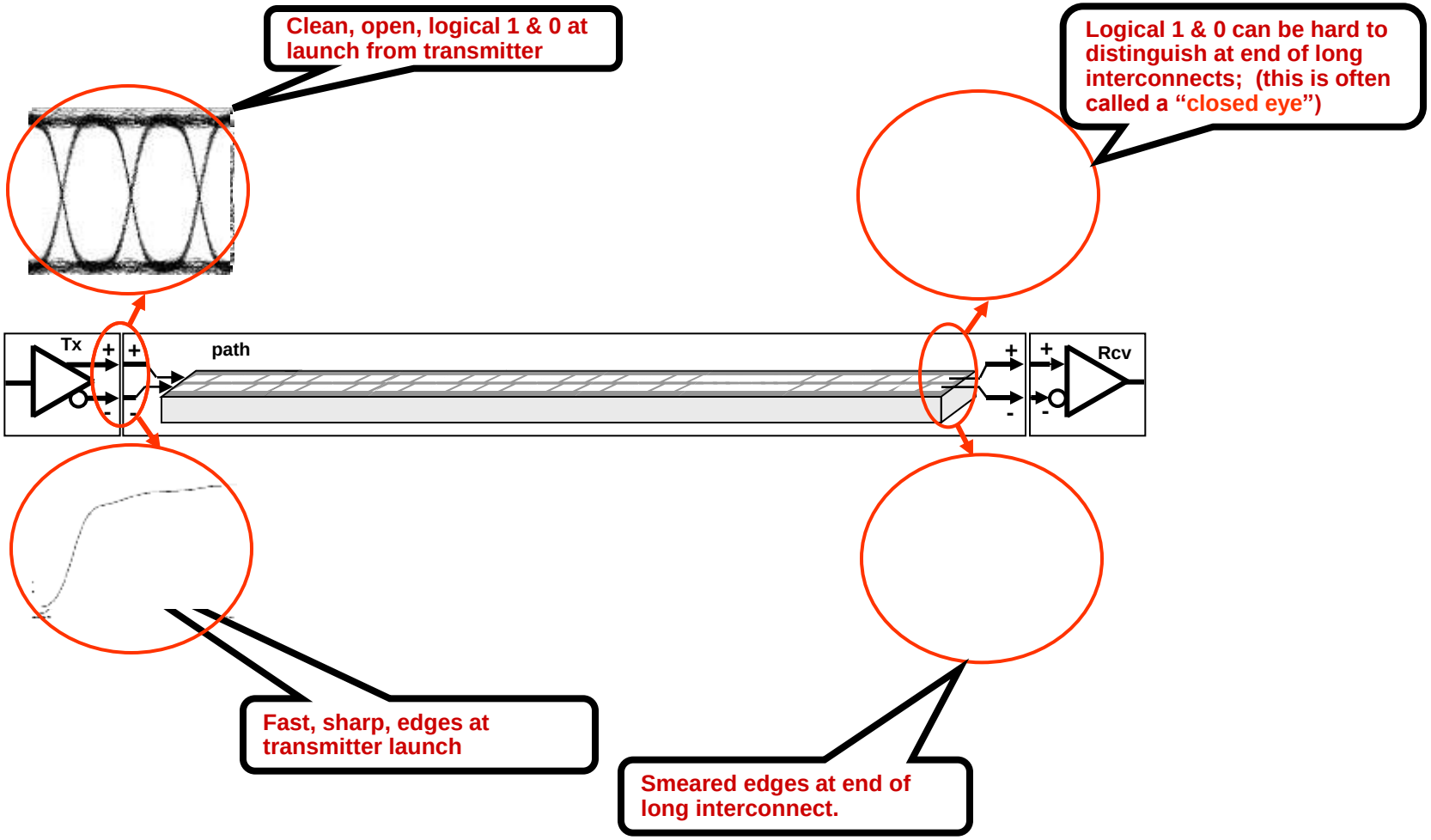
链路的损耗



Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)

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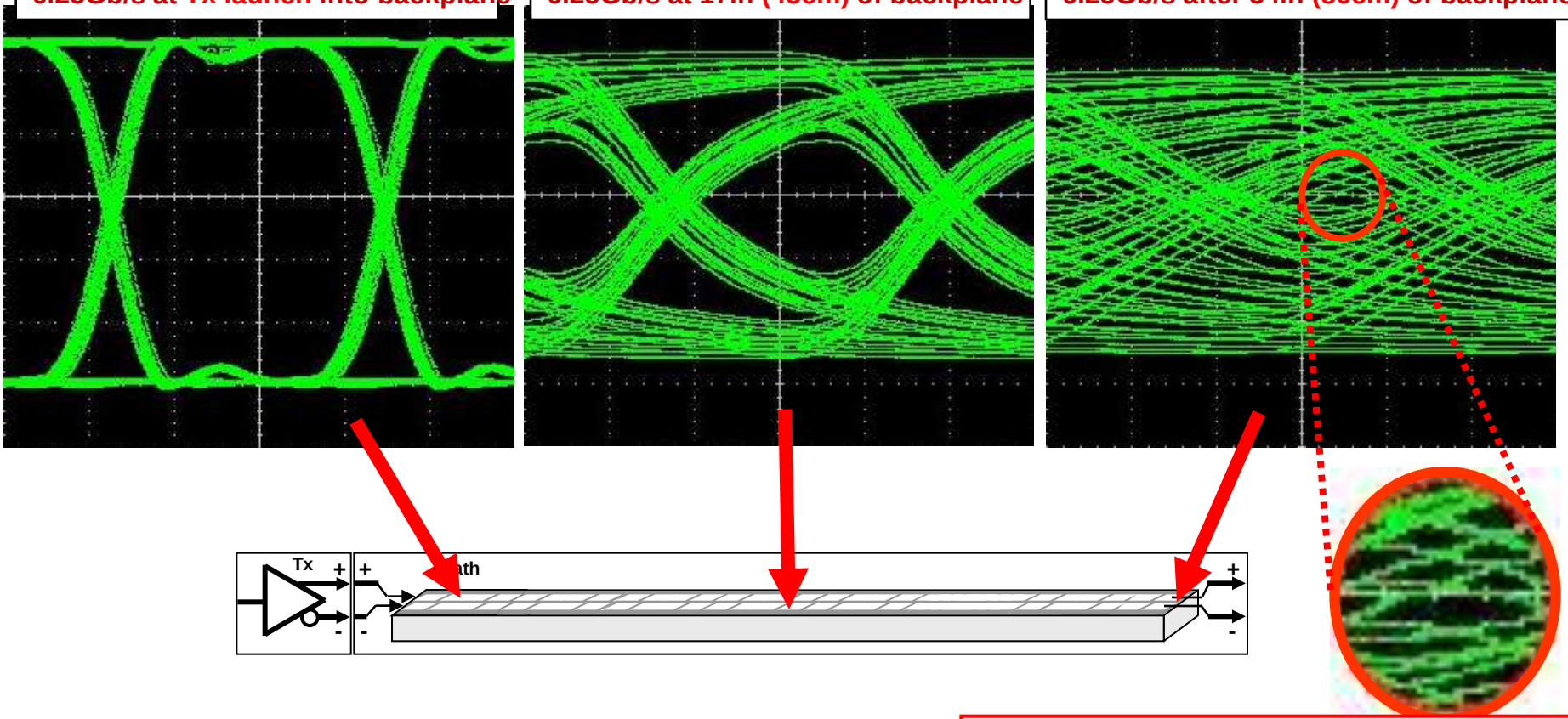
链路的损耗-实际案例

6.25Gb/s at Tx launch into backplane

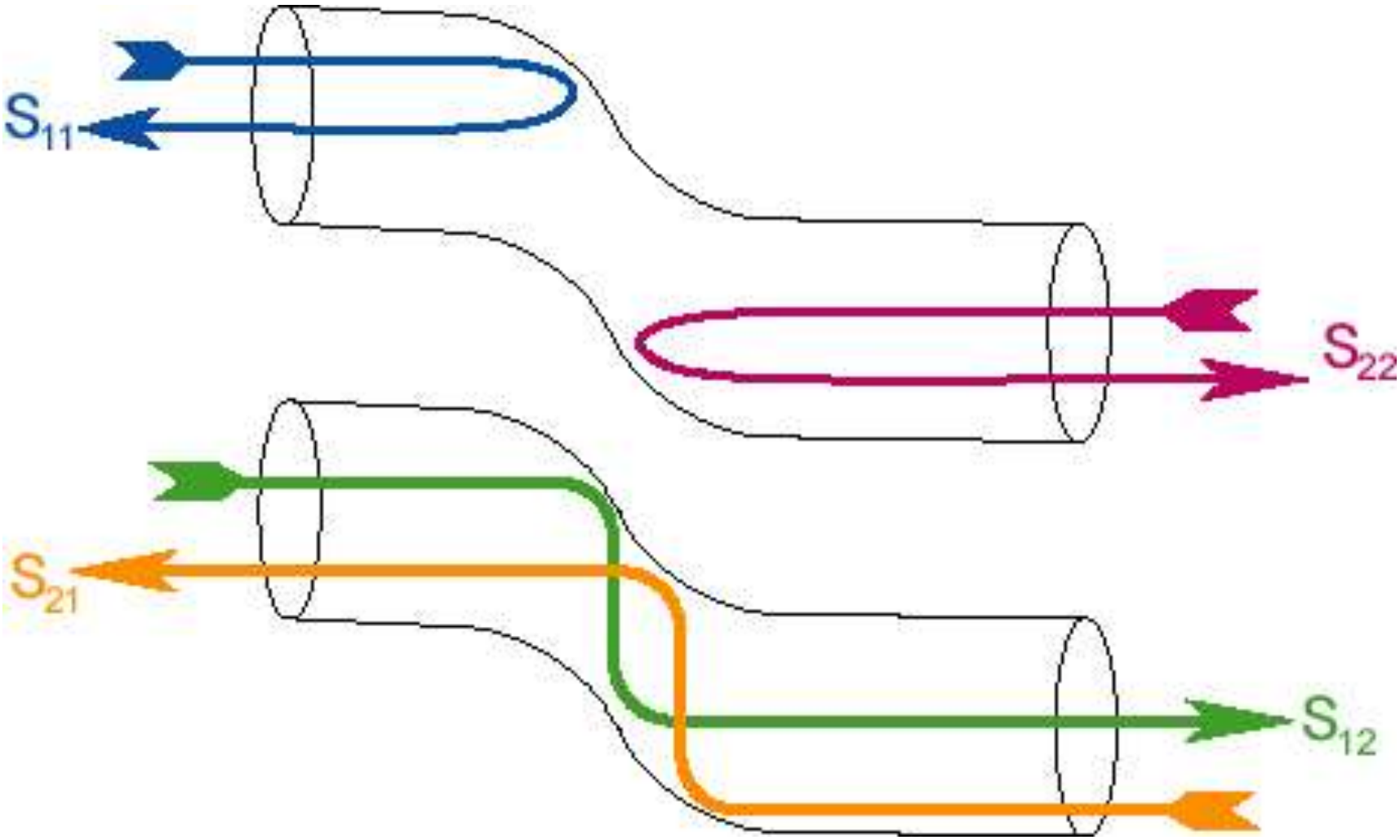
6.25Gb/s at 17in (43cm) of backplane

6.25Gb/s after 34in (86cm) of backplane

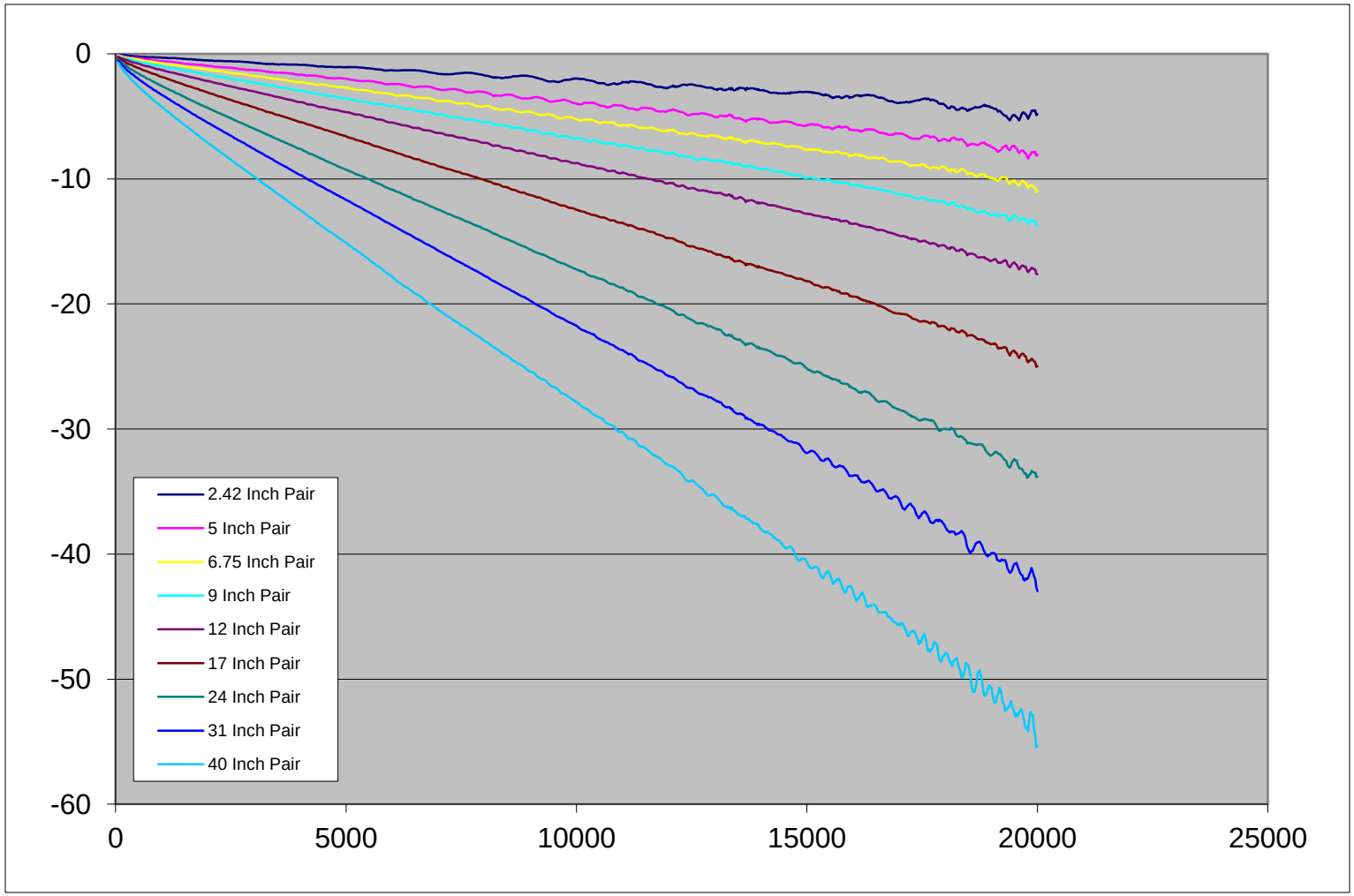


Small differences in levels being measured

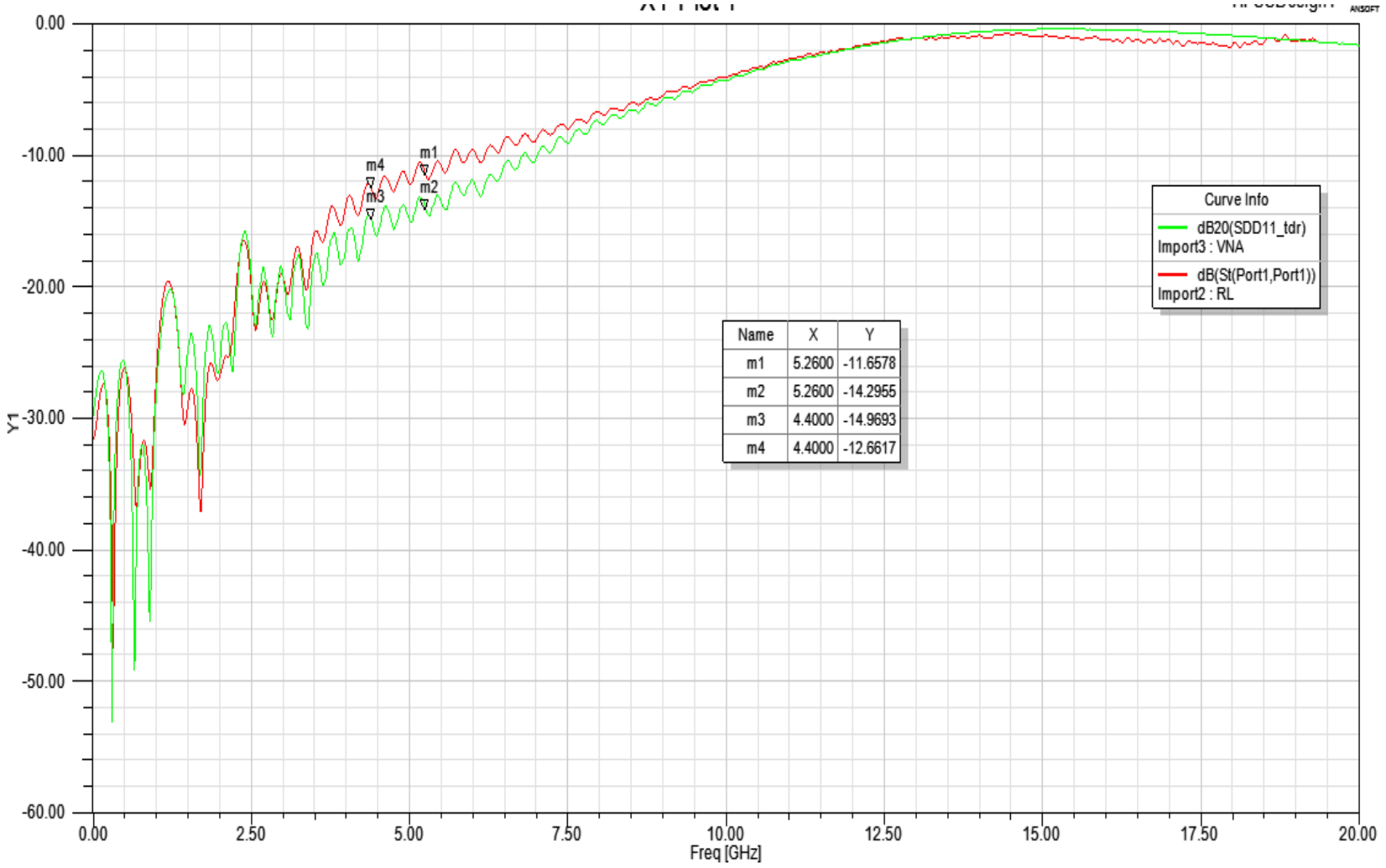
信号的衰减/链路损耗-通过S参数来评估



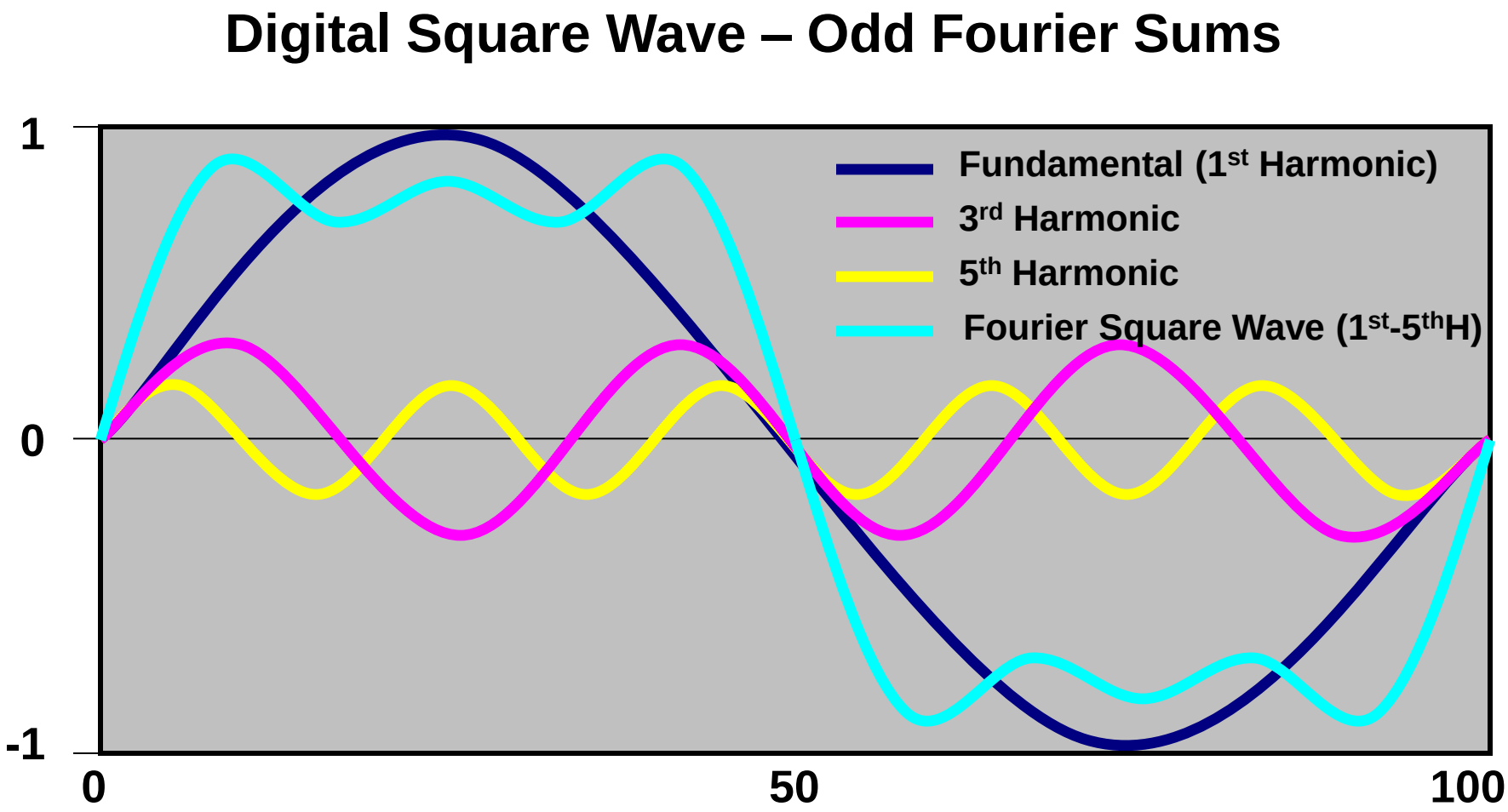
插入损耗S21曲线-实例 不同走线长度的PCB的损耗



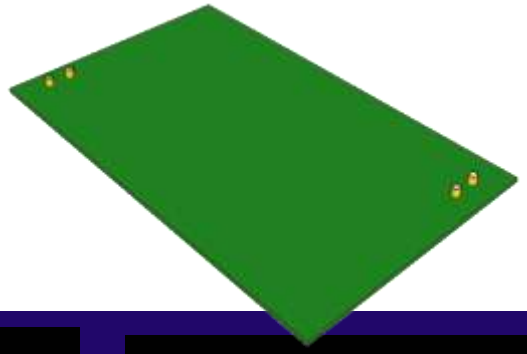
回波损耗S11曲线-实例

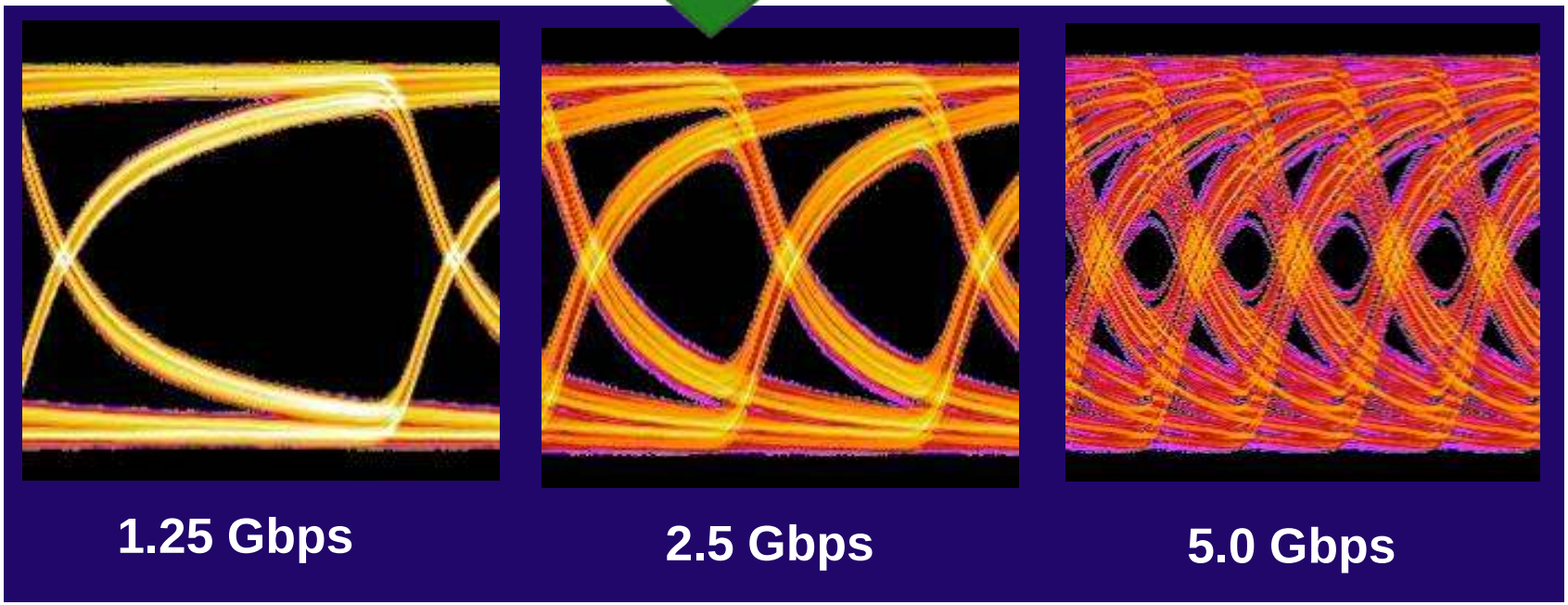


信号在传输线上的损耗，需要考虑3-5次谐波



传输线的损耗（带宽）对不同速率的信号的影响





Noise/jitter closes-down the available headroom in the eye opening

Measured eye diagrams from a 40” PCI-Compliance ISI Trace, PRBS-7 Pattern

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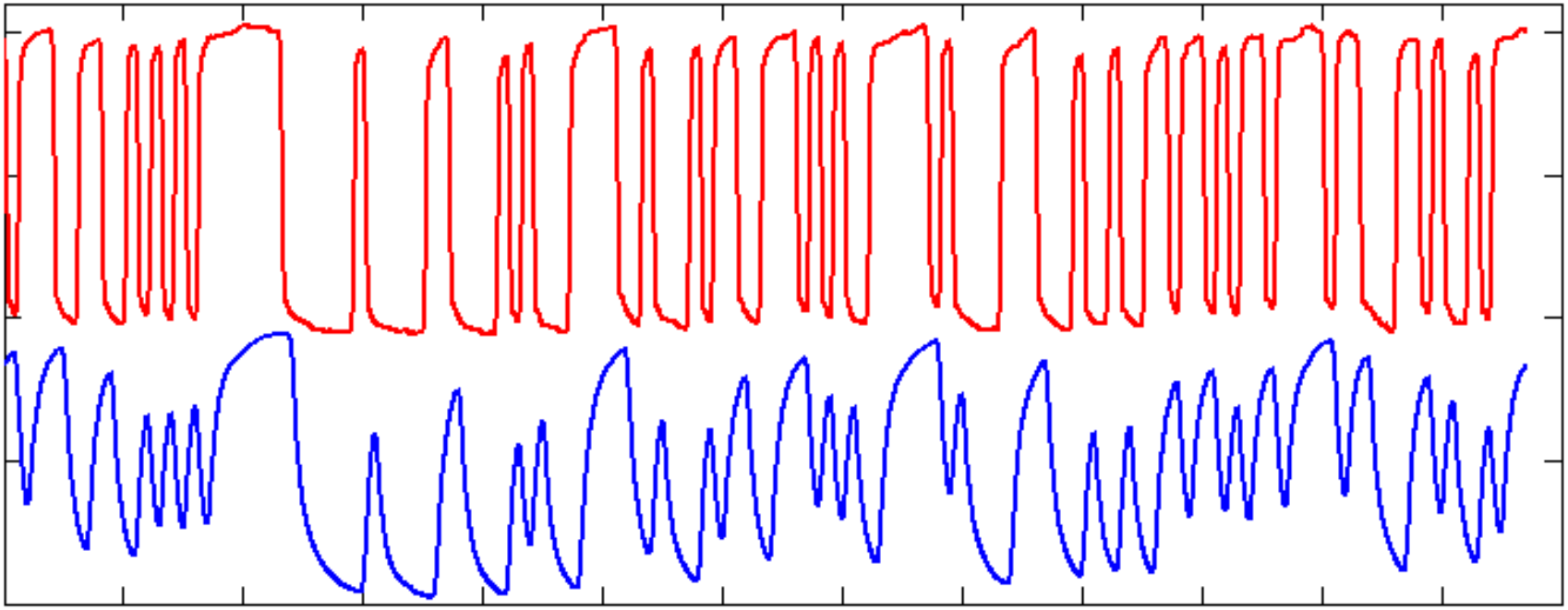
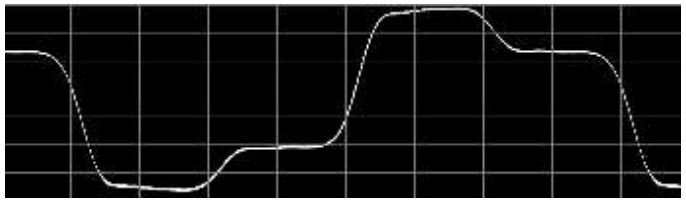
数据传输中不同码型会有不同的损耗



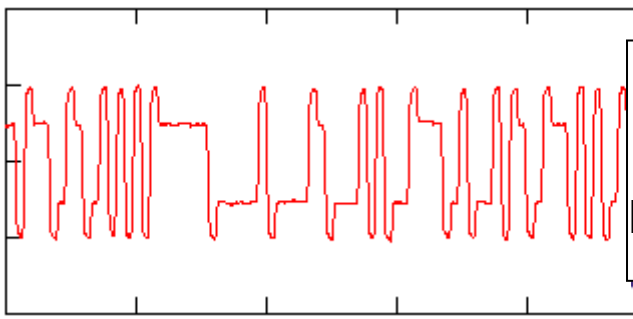
通过发送端对信号进行预加重来补偿信号的衰减

2-Tap –6dB Pre-emphasis



1.

Applied to PRBS Data

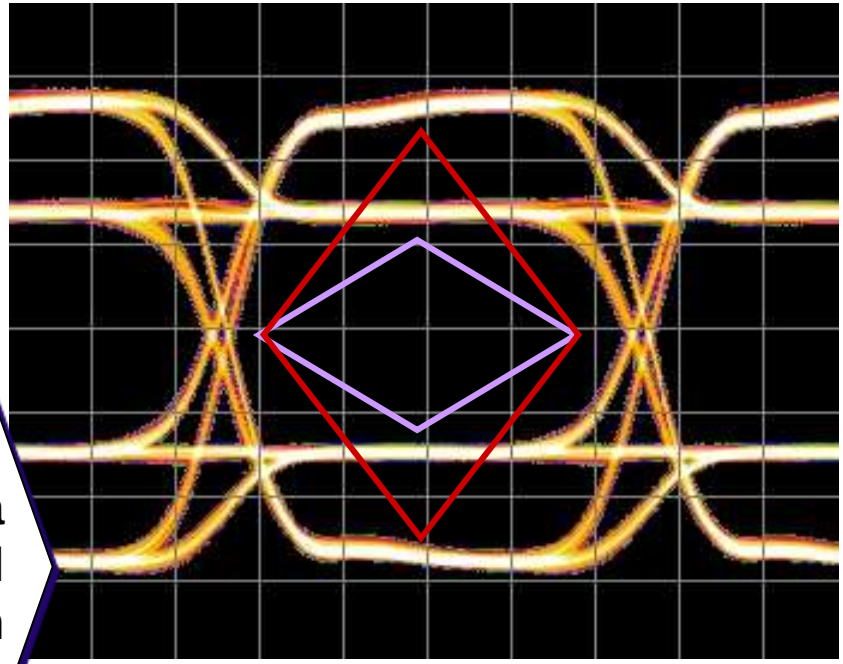


2.

Causes a Multi-level Eye Diagram

3.

Measurement of Eye Mask Testing On BERTScope



This complicates Tx mask testing - 2 masks are needed

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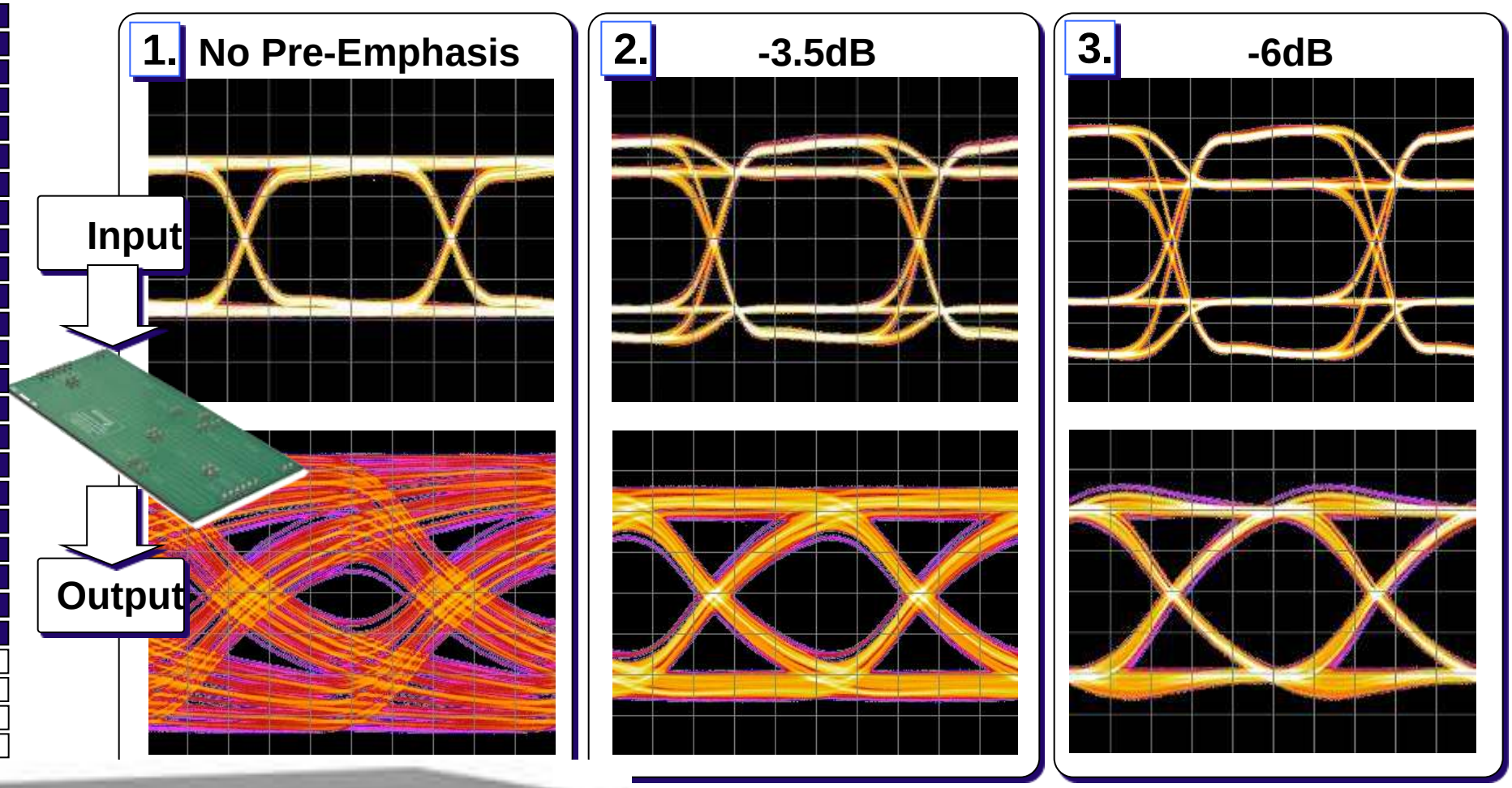
实例：不同的预加重下在接收端得到的眼图



Measurement of Eye Diagrams on BERTScope

CI Compliance ISI Board, 5Gbps PRBS-7 Data

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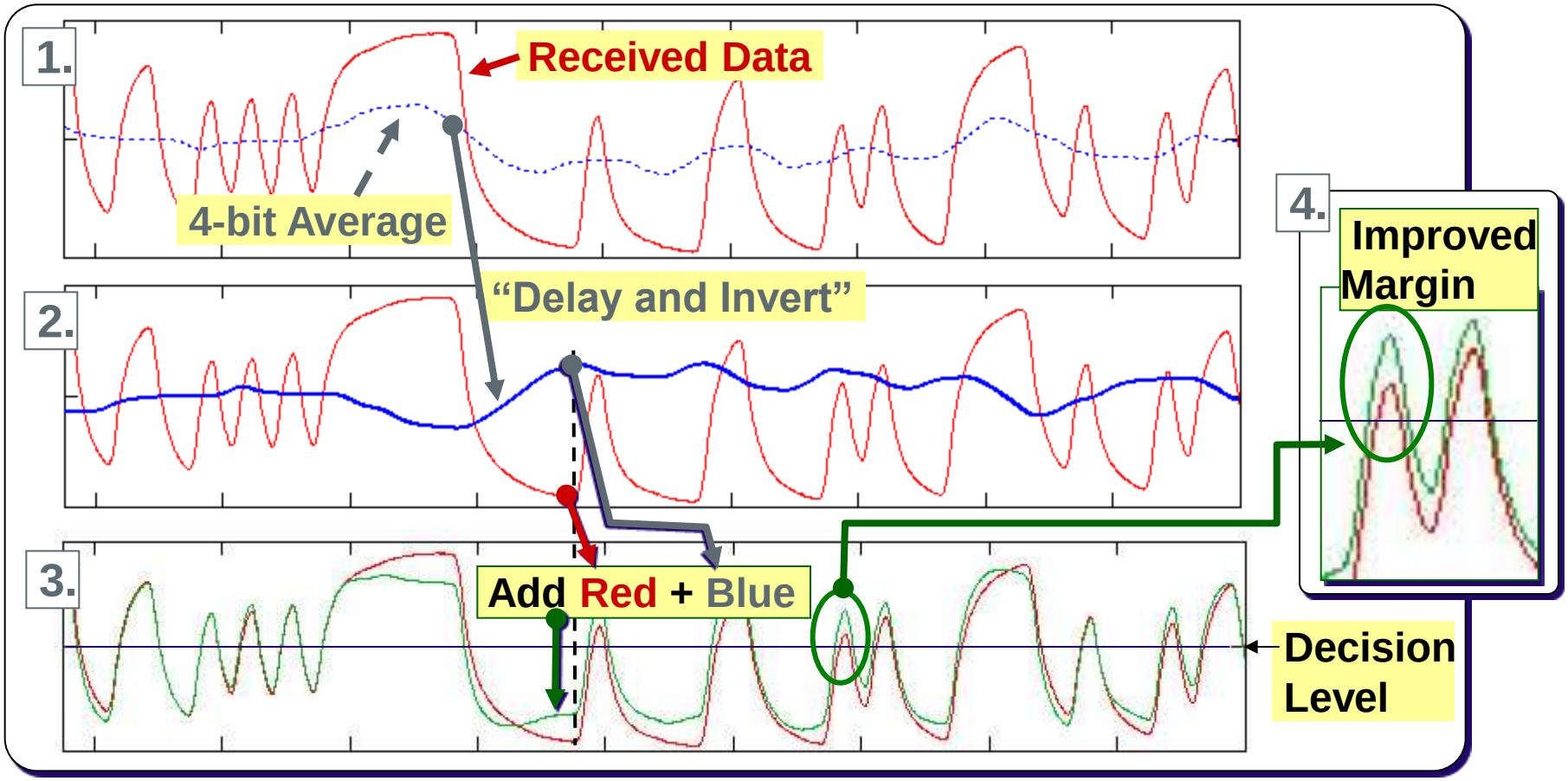
接收端的均衡(Equalization)来补偿链路的衰减

- **DFE,FFE,CTLE…**
- **在USB3.0,PCIE 3.0,SAS,10G等标准中广泛采用均衡**



40" PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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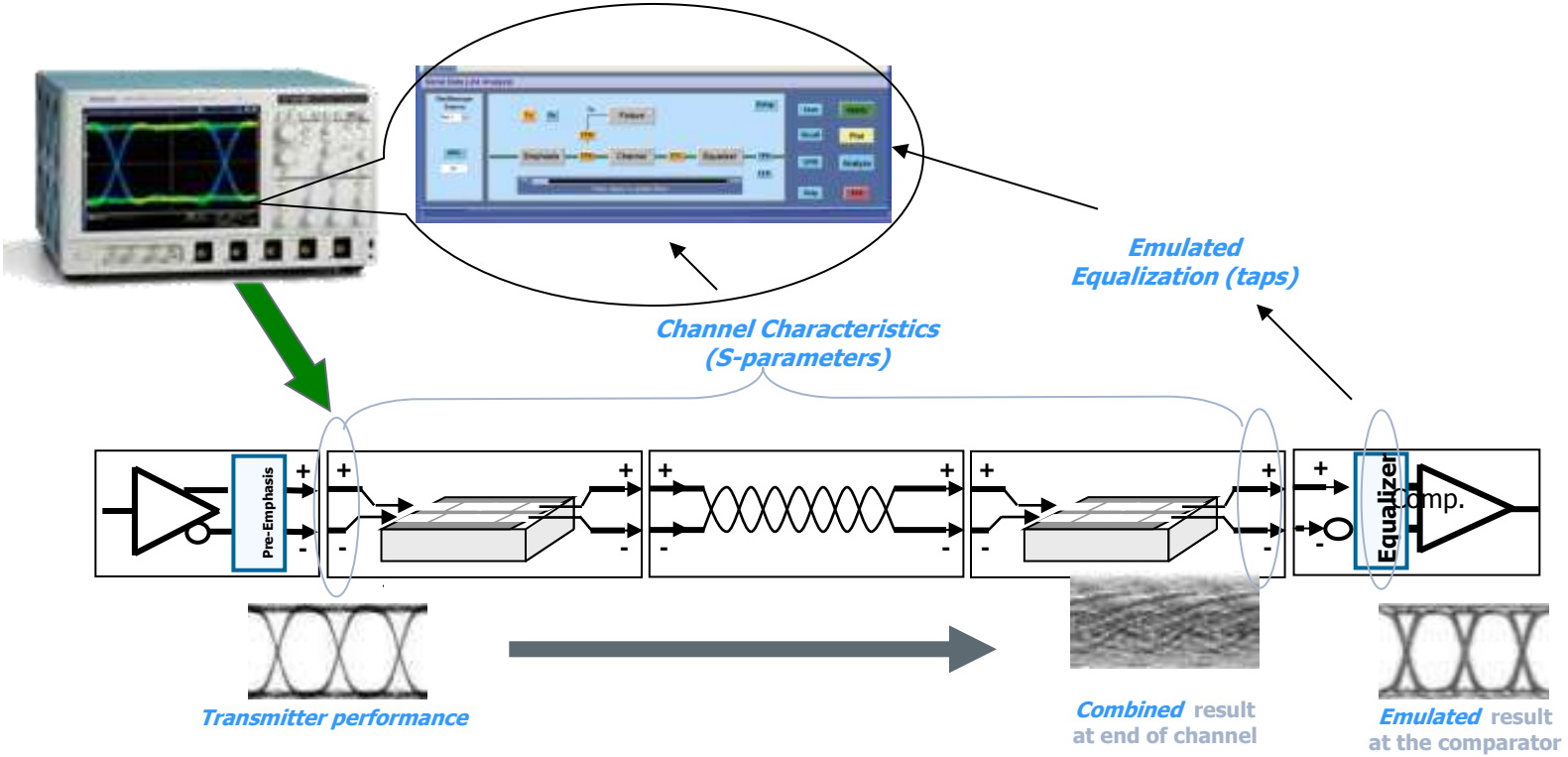
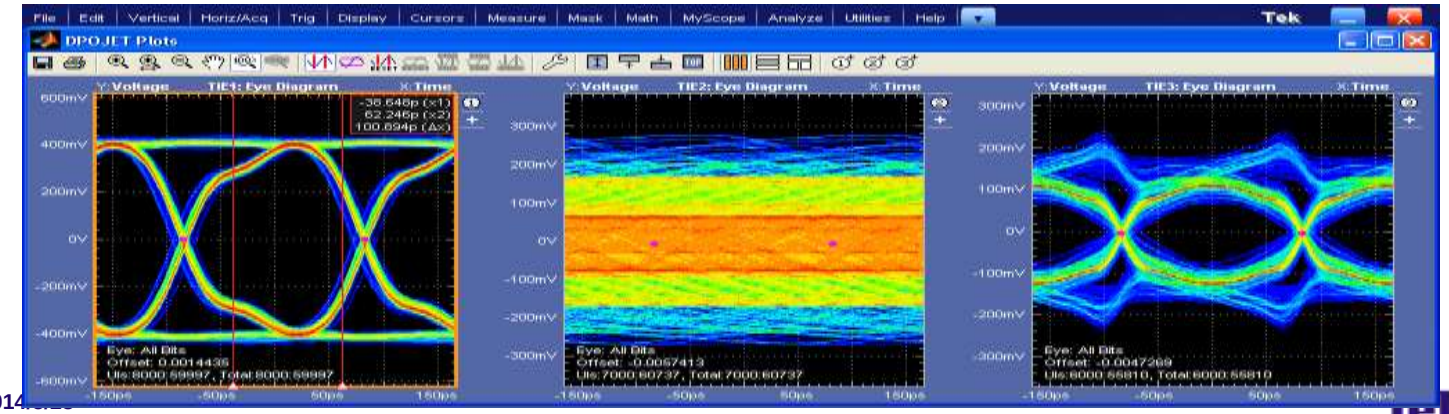
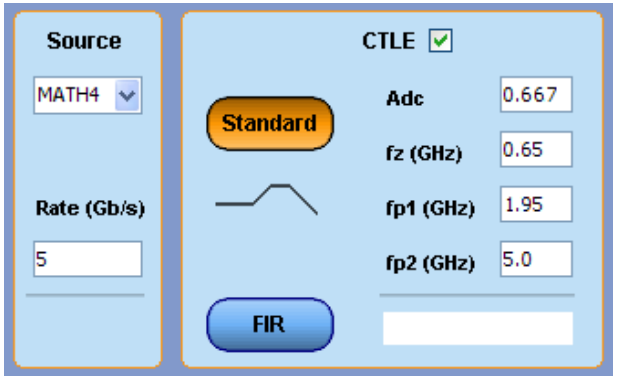
使用软件模拟接收端芯片内部均衡的效果

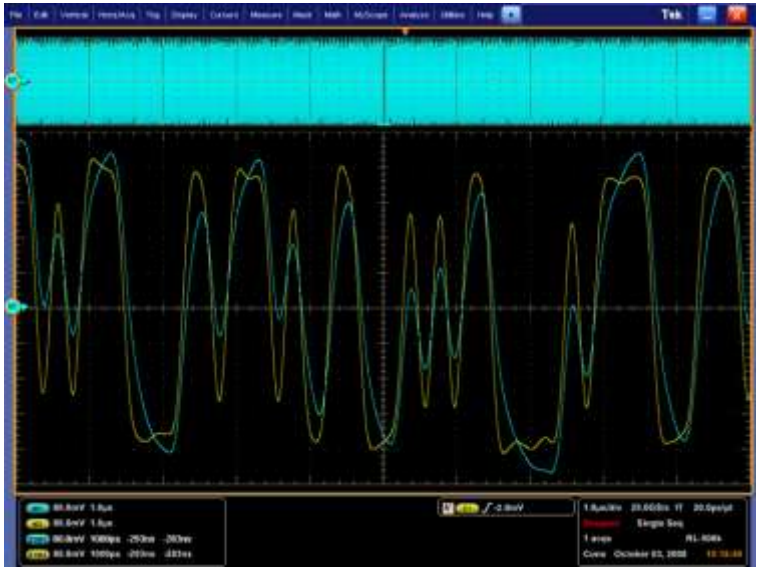


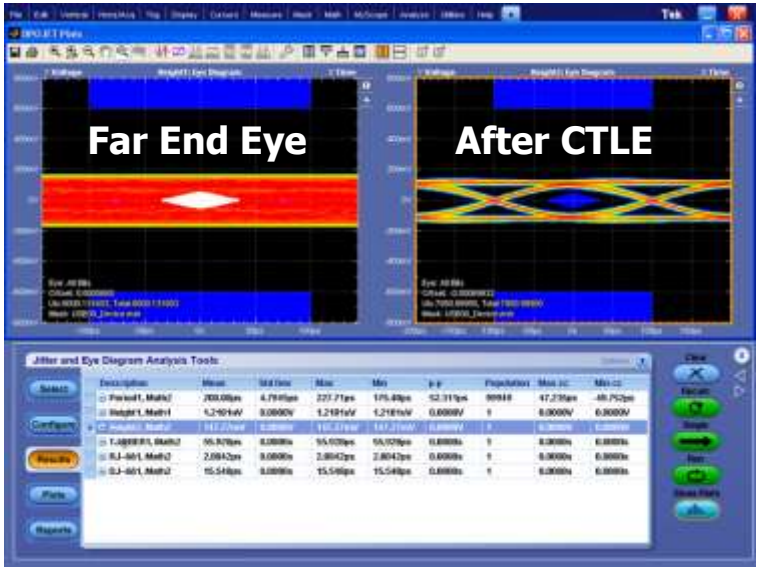


USB 3.0的测试实例，均衡前后的对比

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix' USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)







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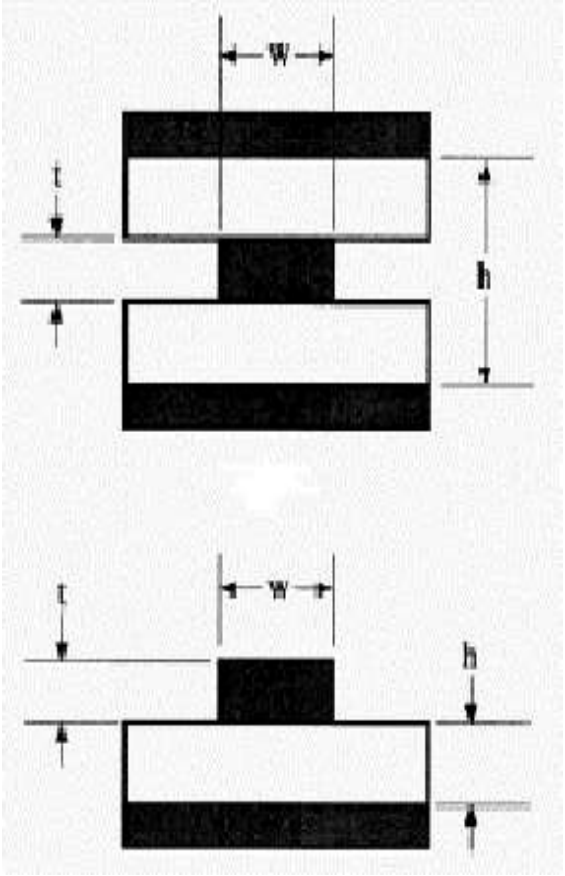
如何进行传输线设计来优化信号质量

- 仅从PCB设计角度来看，我们只能碰到两种传输线：带状线（stripline）和微带线（microstrip）。带状线是指信号线夹在两个平面层之间，理论上它能最好的传输信号。微带线在外层。
- 从信号质量的保证来讲：带状线优于微带线
- 从EMI/EMC角度讲：带状线优于微带线



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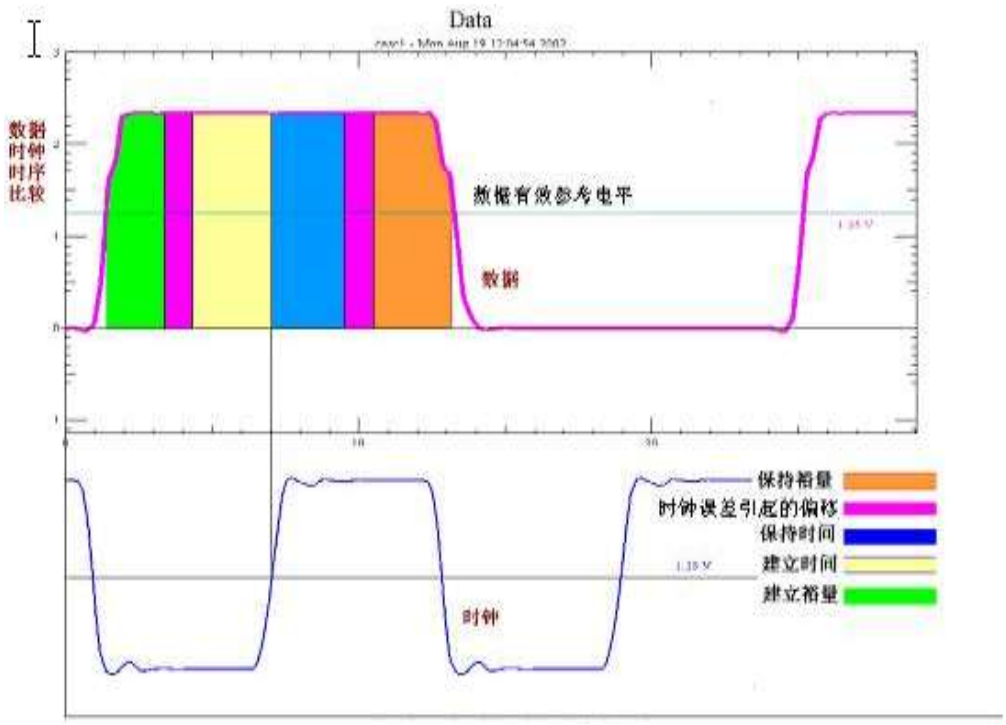
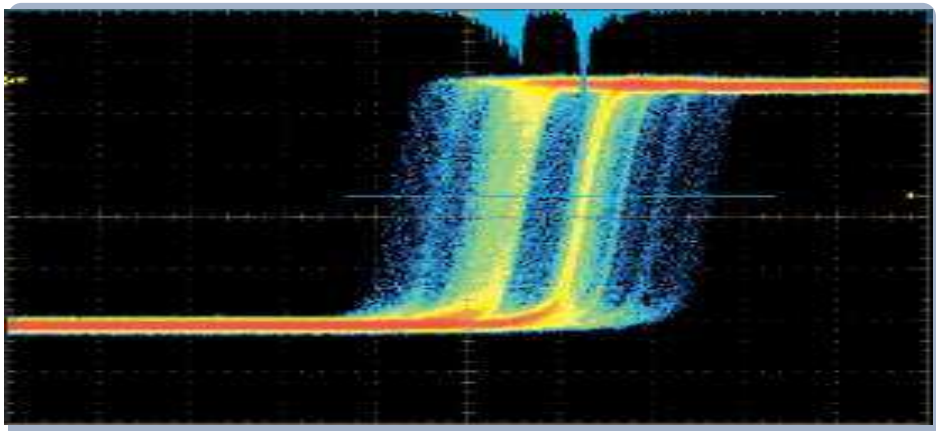
减小损耗的方法

- 材料：选用损耗小的材料，但价格会贵
- 减小走线长度
- 改善信号完整性：连接器、过孔、背钻、微带线or带状线、线宽

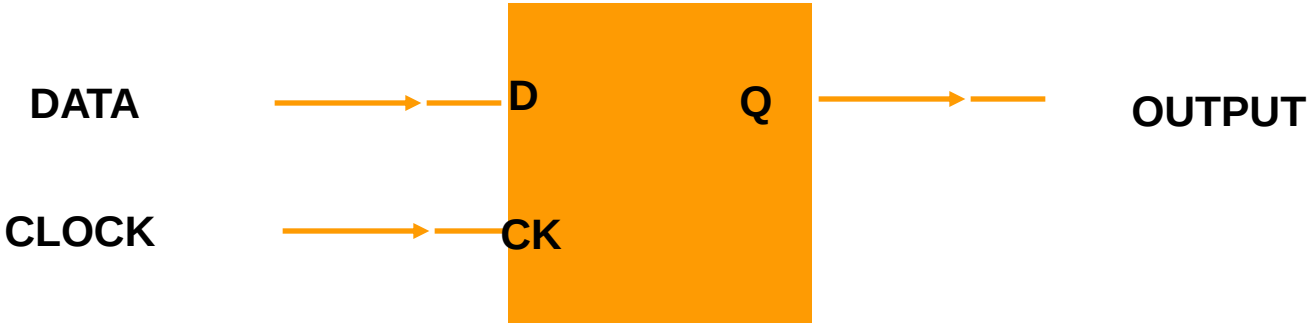
时序完整性Timing integrity

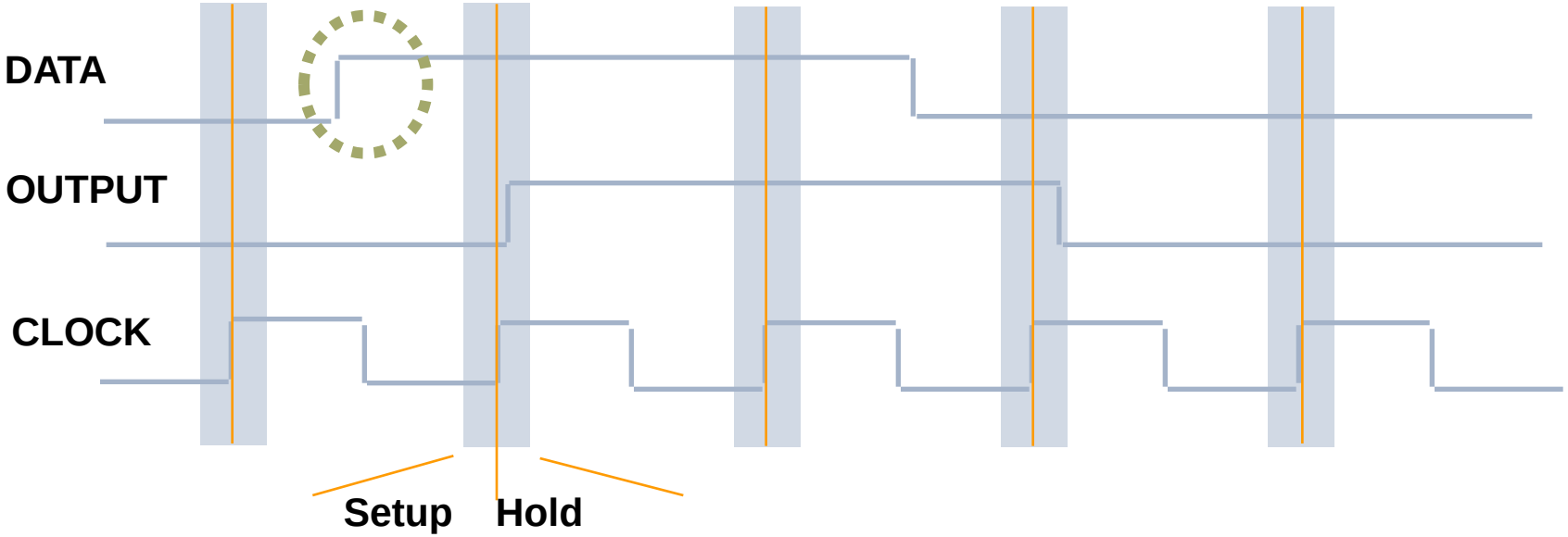
- 建立保持时间（setup/hold time）
- 时序抖动（timing jitter）





通过示波器或者逻辑分析仪的建立保持时间违规触发来发现问题





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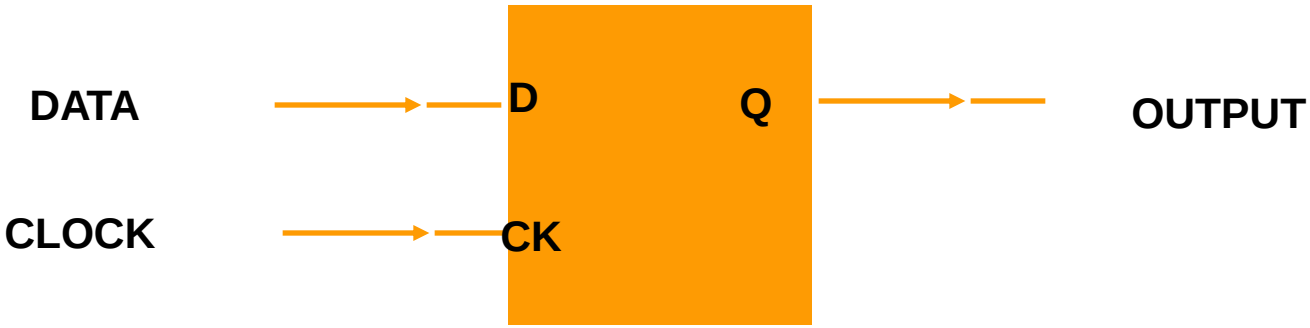
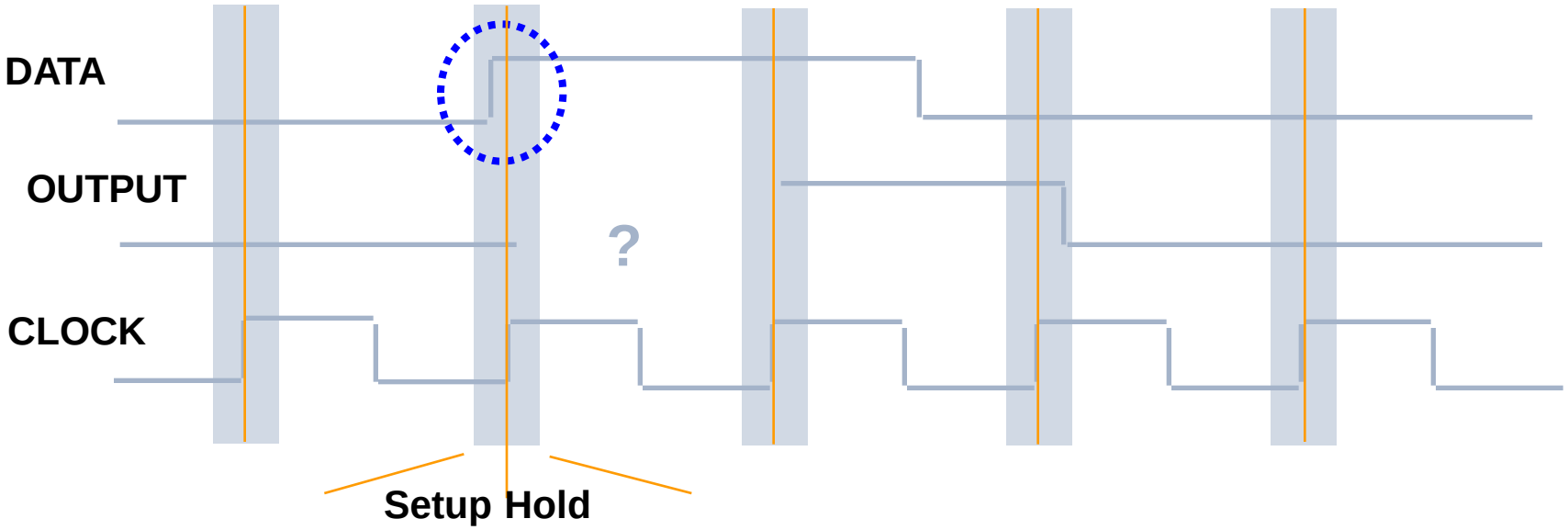
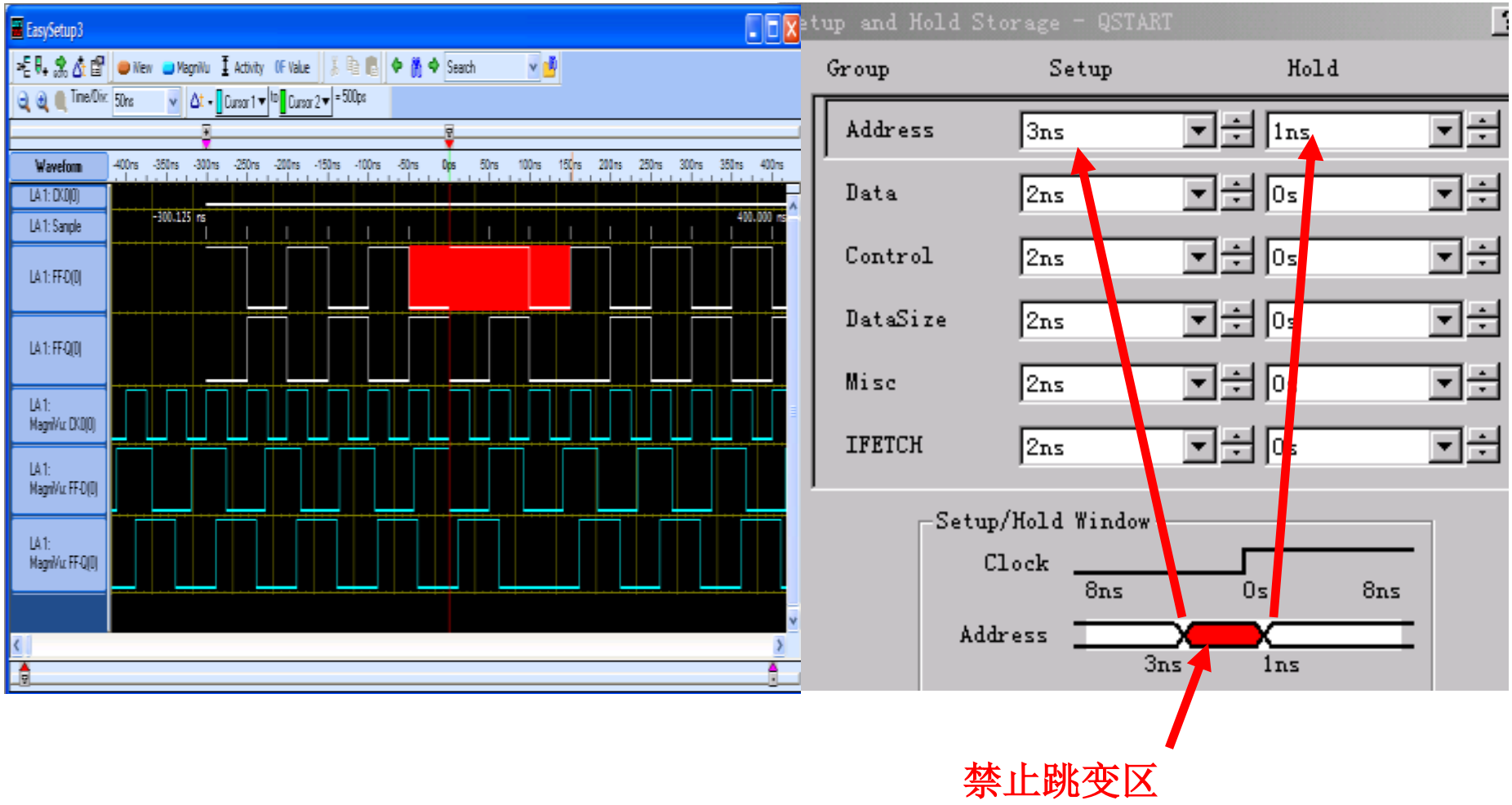
违反建立时间

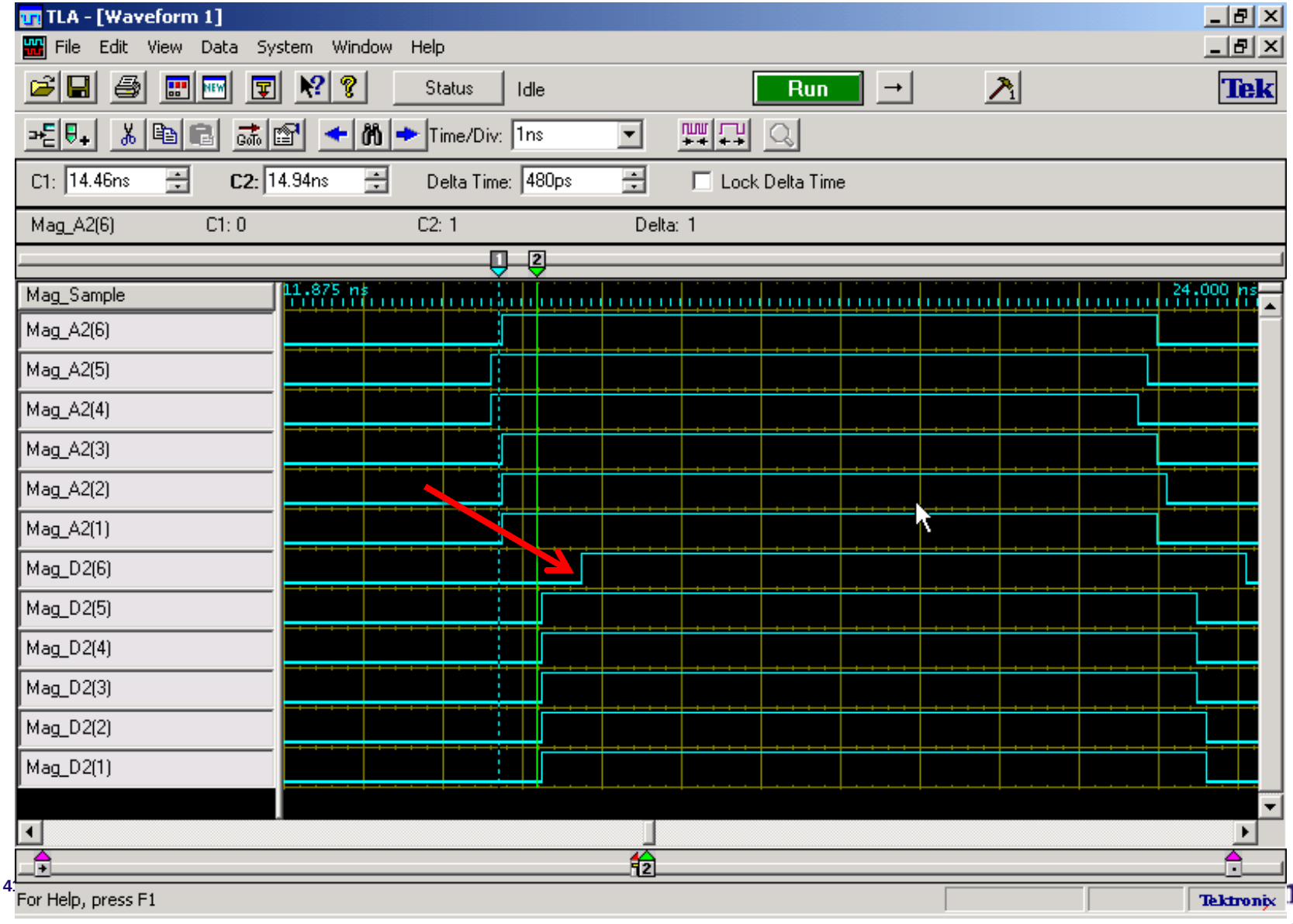




逻辑分析仪可以对多路数据进行监控

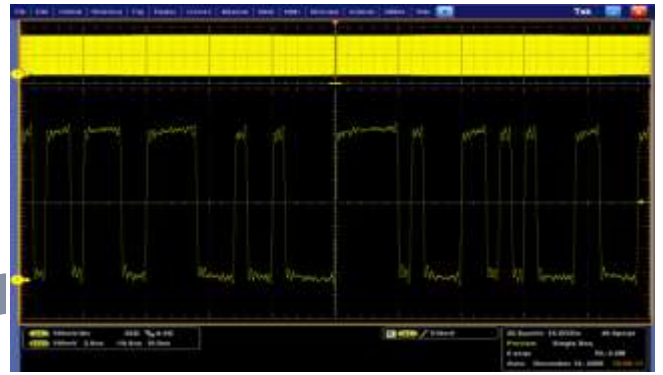


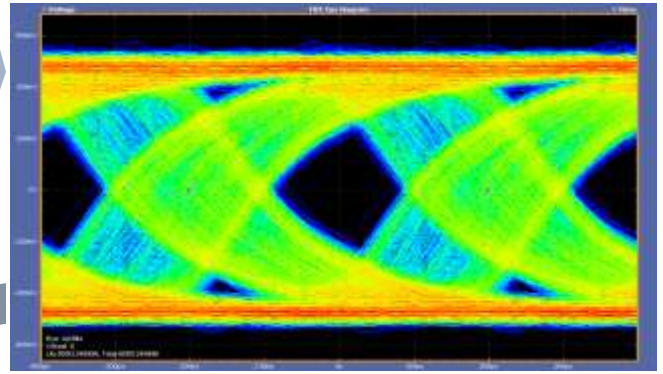
并行总线的传输延迟差异可以导致建立保持时间违规



眼图和抖动的测试分析

- **Deep memory capture**
  - Long records needed for low frequency events (SSC, periodic jitter, low speed clocks)
  - Frequency window related to time capture
    - 1 SSC cycle (33kHz) => Need 30us time record
- **Eye Diagram Analysis**
  - Quick visual indicator of voltage and timing performance
  - Related to Bit Error Rate (BER)
- **Debugging Jitter**
  - Knowledge of jitter types and sources aids in debug
  - Common jitter sources
    - Power supply coupling
    - PLL (tracking or overshoot)
    - Limited channel bandwidth and reflections (ISI)
    - Driver imbalance (Rise/fall time asymmetry)





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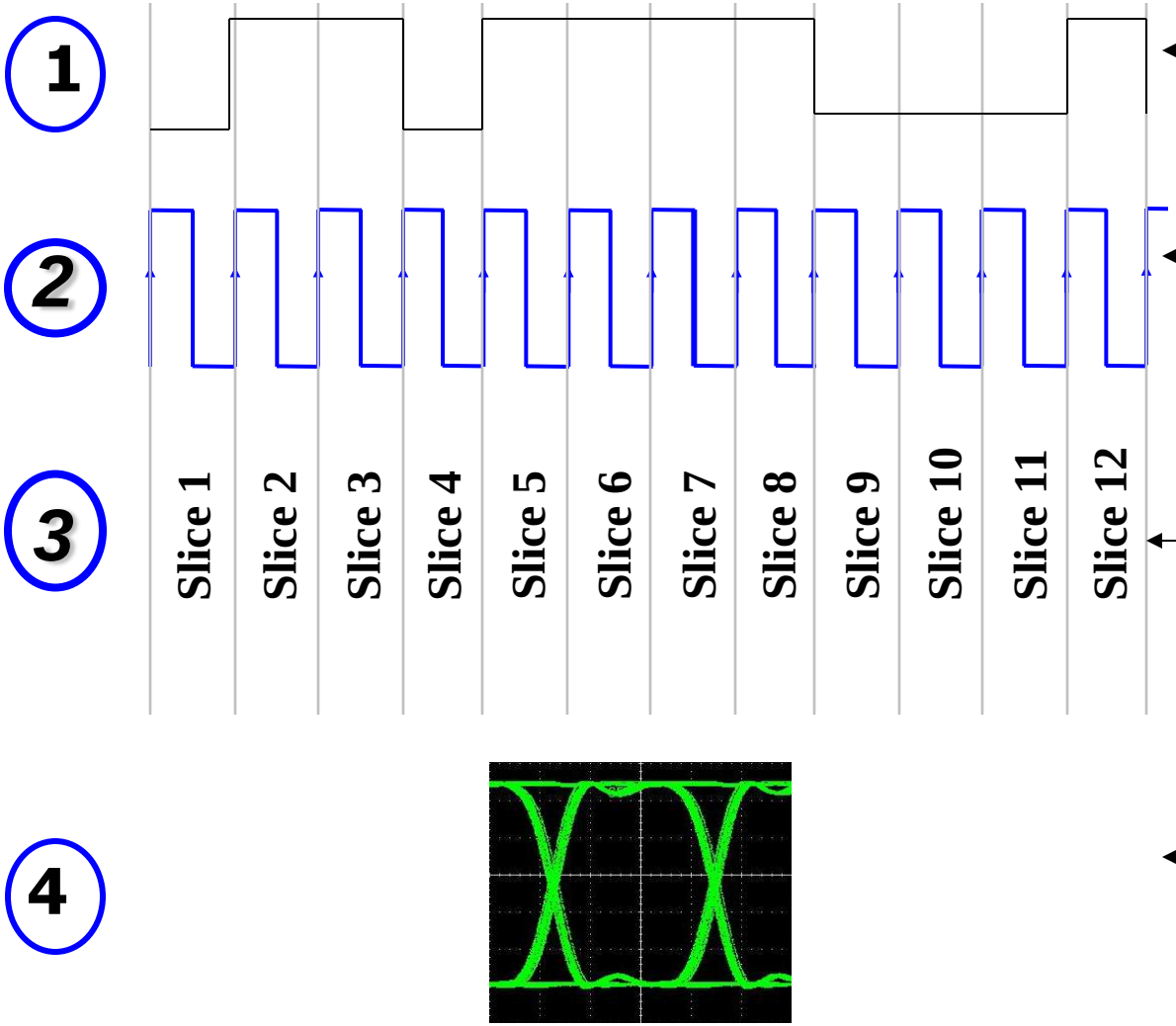
眼图形成的原理



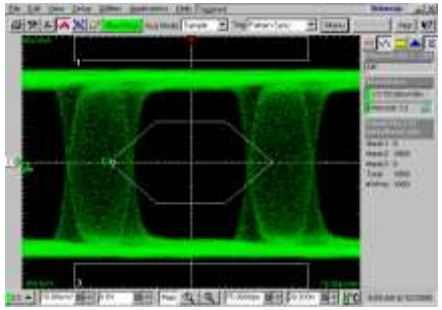
一次触发捕获连续多个比特位

使用软件PLL进行时钟恢复

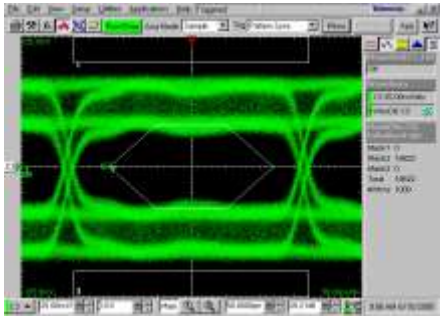
将数据按单位间隔 UI分解，逐位按恢复时钟进行切割

将切割得到的数据按时间单位排列进行叠加形成眼图

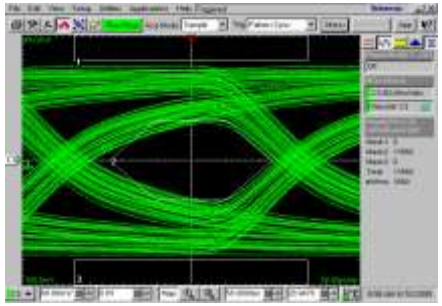
影响眼图质量的几种原因（垂直噪声和水平抖动）



Jitter dominated signal impairment



Noise dominated signal impairment



Jitter & Noise signal impairment

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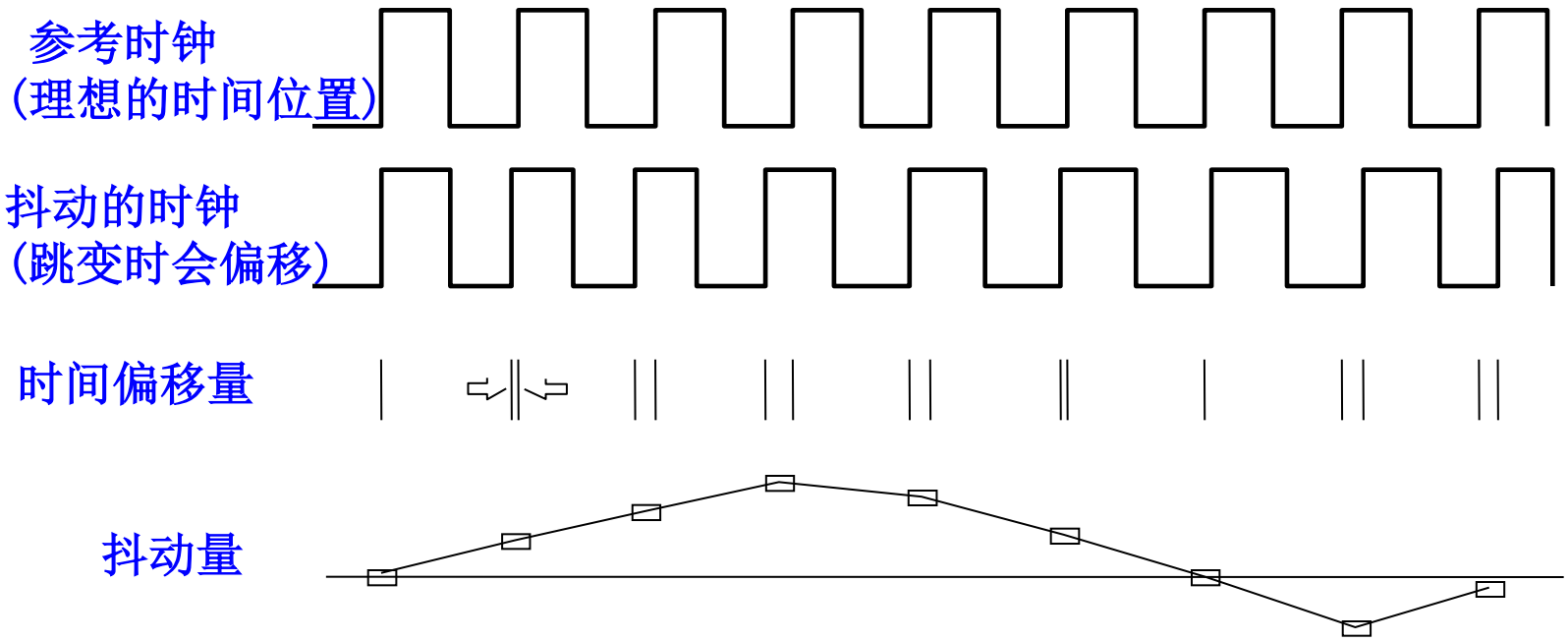
抖动的定义

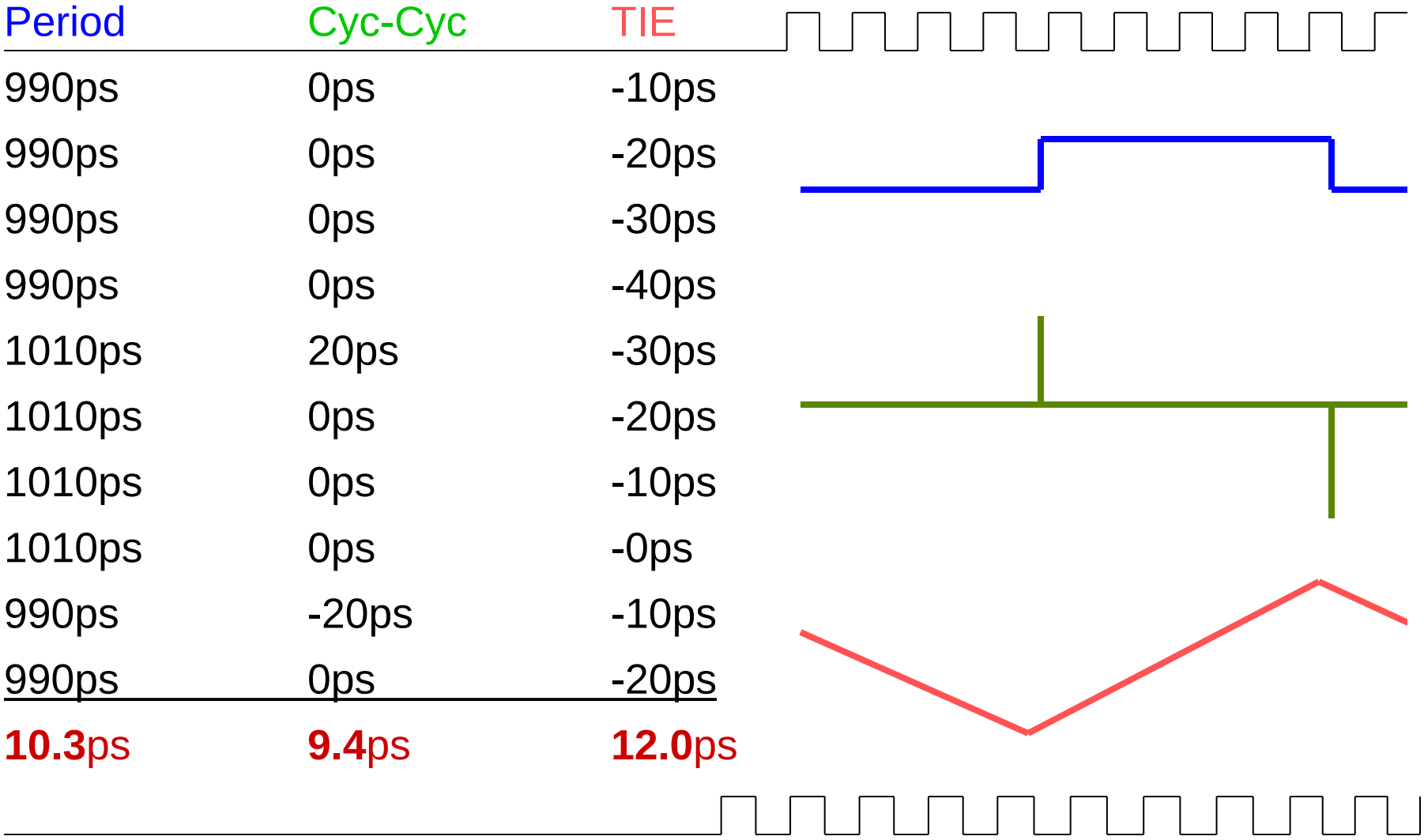
抖动可以定义为

“一个信号在跳变时，相对其理想时间位置的偏移量”



Period, Cycle to Cycle, and TIE Jitter

Period	Cyc-Cyc	TIE
990ps	0ps	-10ps
990ps	0ps	-20ps
990ps	0ps	-30ps
990ps	0ps	-40ps
1010ps	20ps	-30ps
1010ps	0ps	-20ps
1010ps	0ps	-10ps
1010ps	0ps	-0ps
990ps	-20ps	-10ps
990ps	0ps	-20ps
10.3ps	**9.4**ps	**12.0**ps



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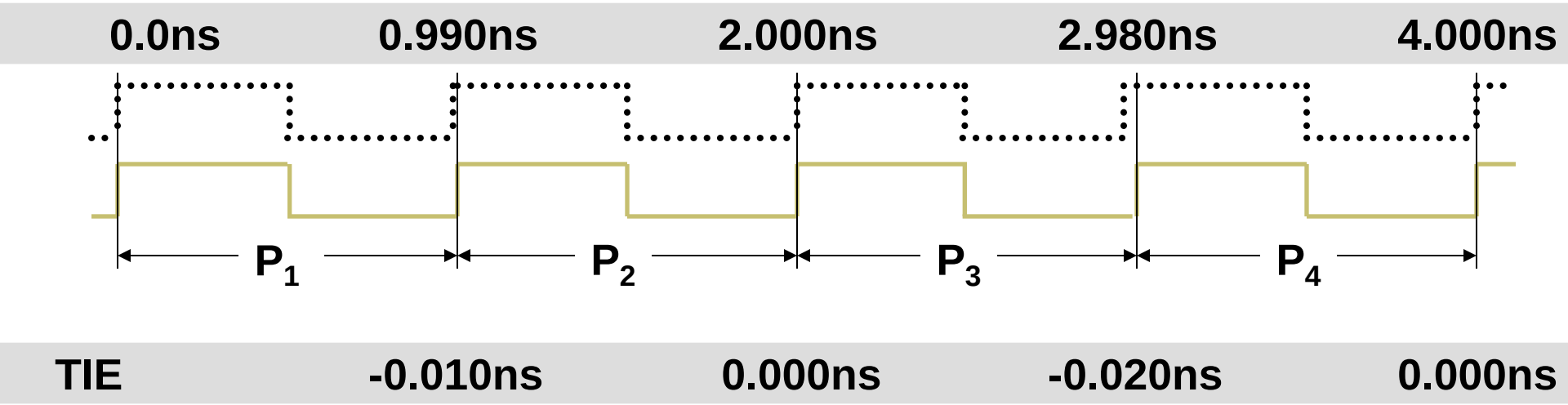
Definition: TIE Jitter Measurement



Example: Ideal clock edge every 1 ns

TIE = 9.6ps StdDv **(-0.010/0.000/-0.020/0.000)**

Definition: TIE Jitter is the measurement of a signal's timing error relative to a known or recovered clock

TIE is typically called simply "Jitter" in serial data…

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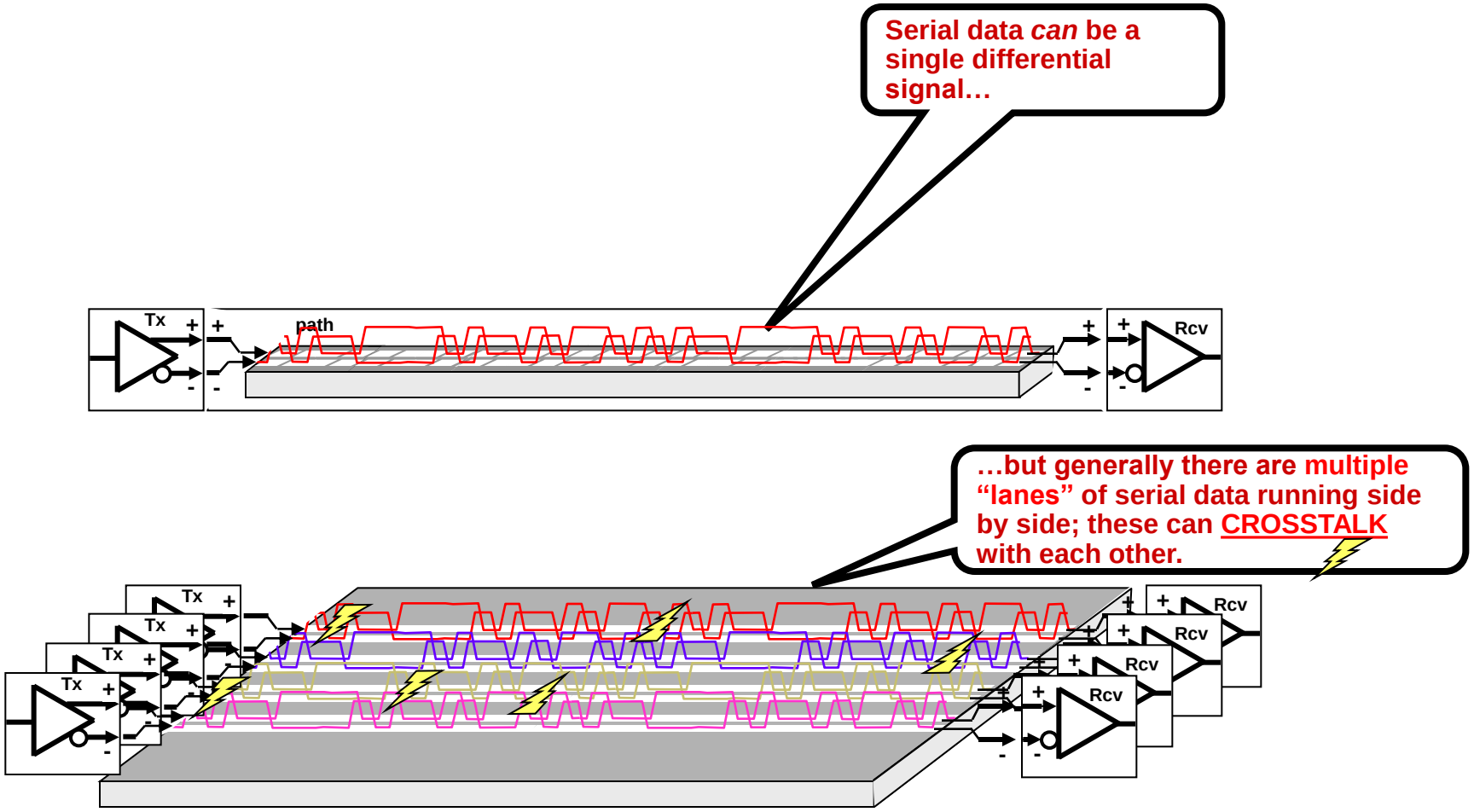
TIE抖动的分类

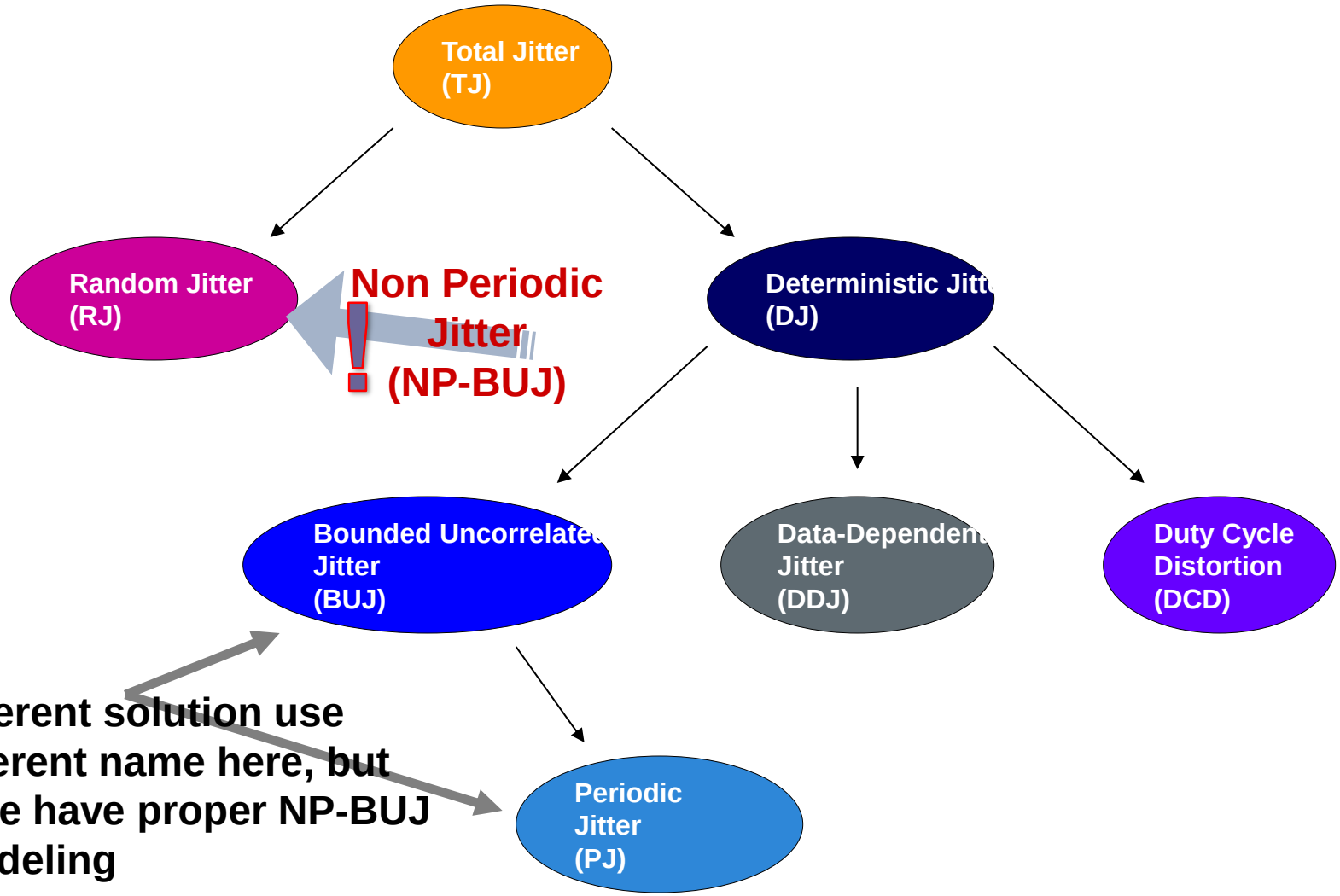
What about Tj/Rj/Dj?

- Tj = Total Jitter in a signal（总体抖动）
- Rj = random jitter in a signal（随机抖动）
- Dj = deterministic jitter in a signal（固有抖动或者确定性抖动）
  - Periodic Jitter（周期性抖动）
  - Data Dependent Jitter (ISI)（数据相关性抖动）
  - Duty Cycle Jitter（占空比失真抖动）

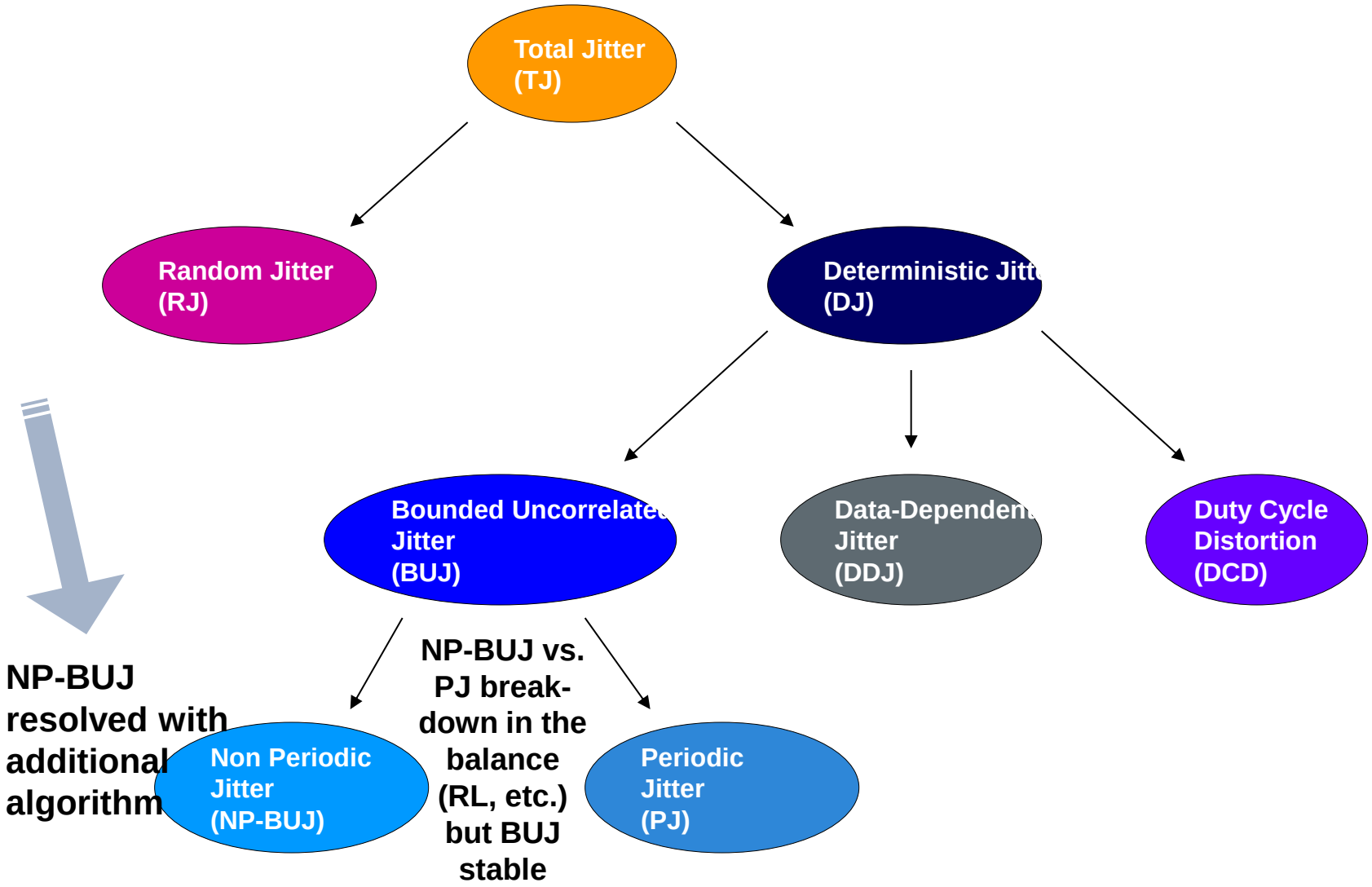
NPBUJ:串扰引起的抖动分量速率越高越明显



抖动细分（忽略串扰引起的抖动）



抖动细分（考虑串扰引起的抖动）



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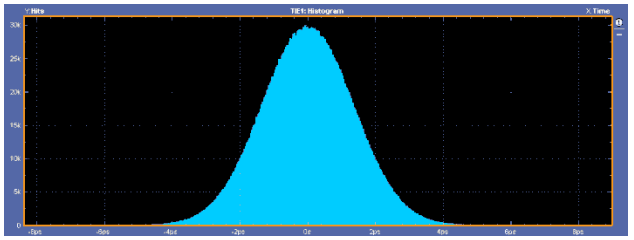
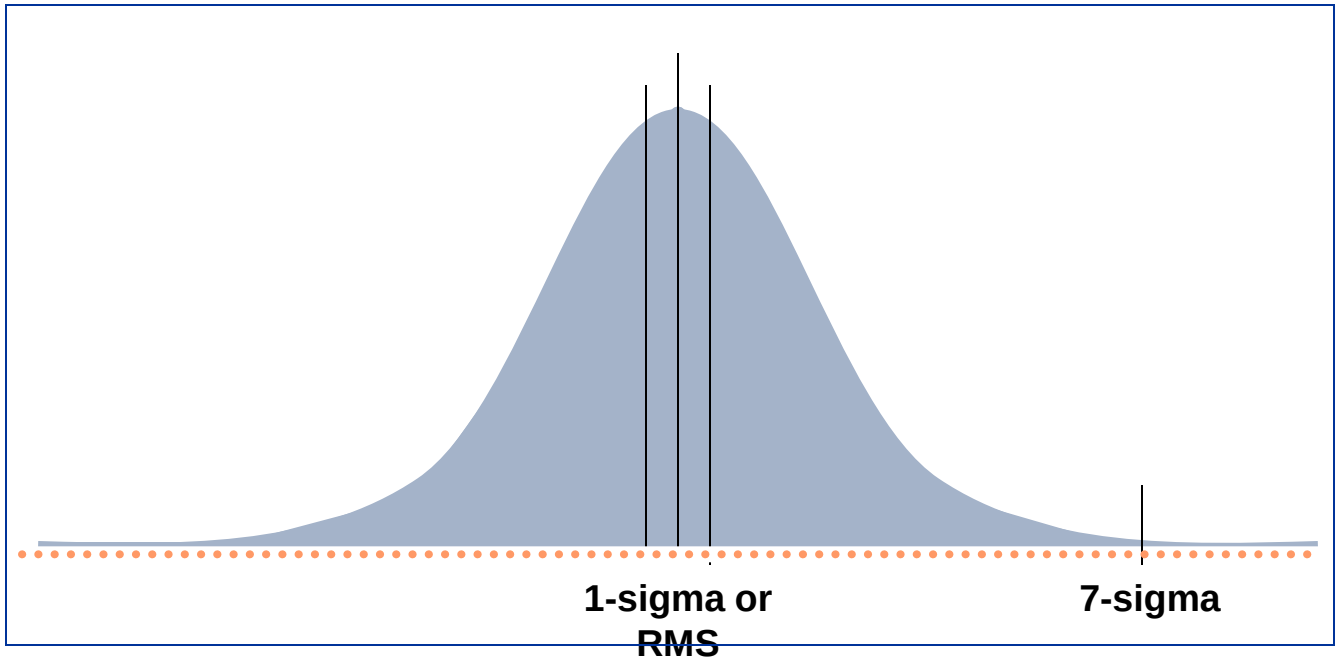
Random Jitter



- Jitter of a random nature has Gaussian distribution
- Histogram (estimate) ↔ pdf (mathematical model)
- Peak-to-Peak = … unbounded!



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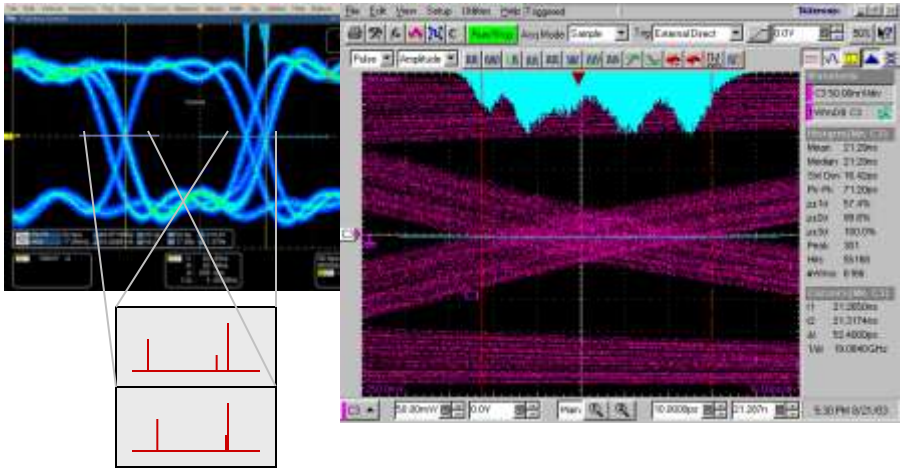
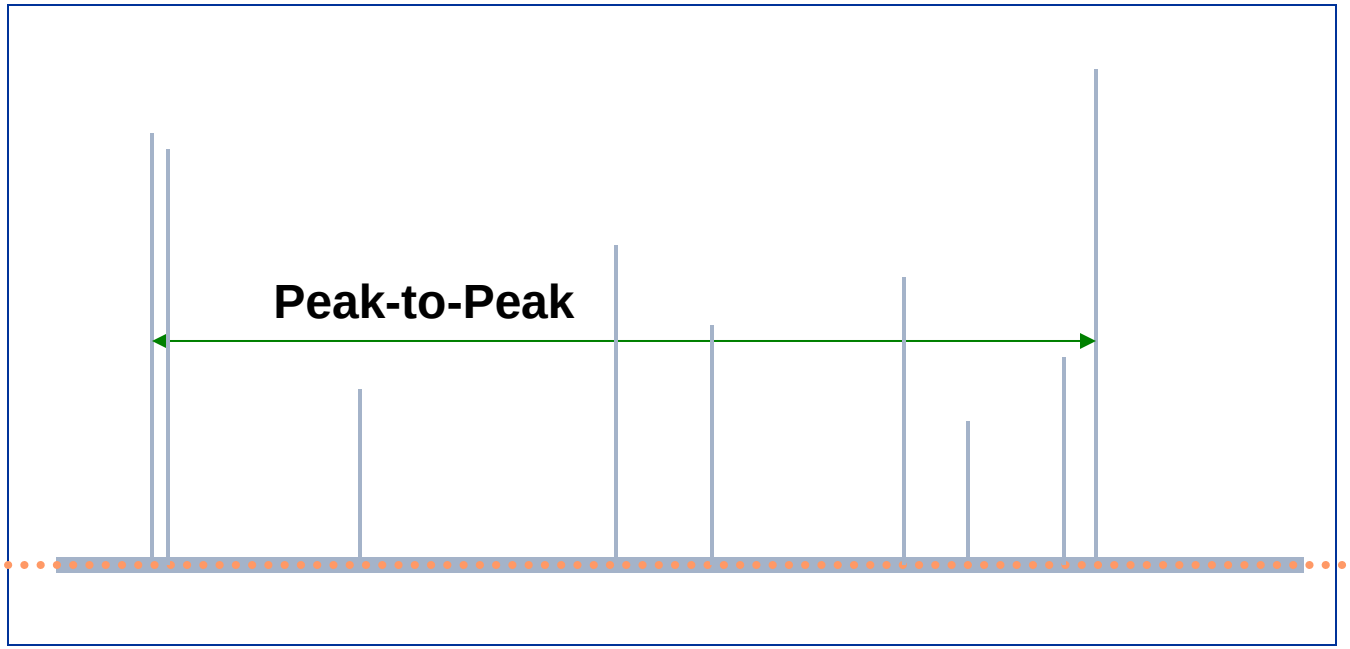
Deterministic Jitter

- Deterministic jitter has non-Gaussian distribution and is bounded.





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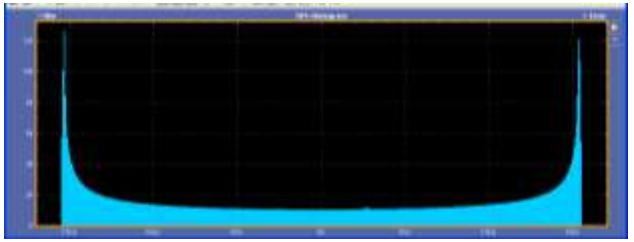
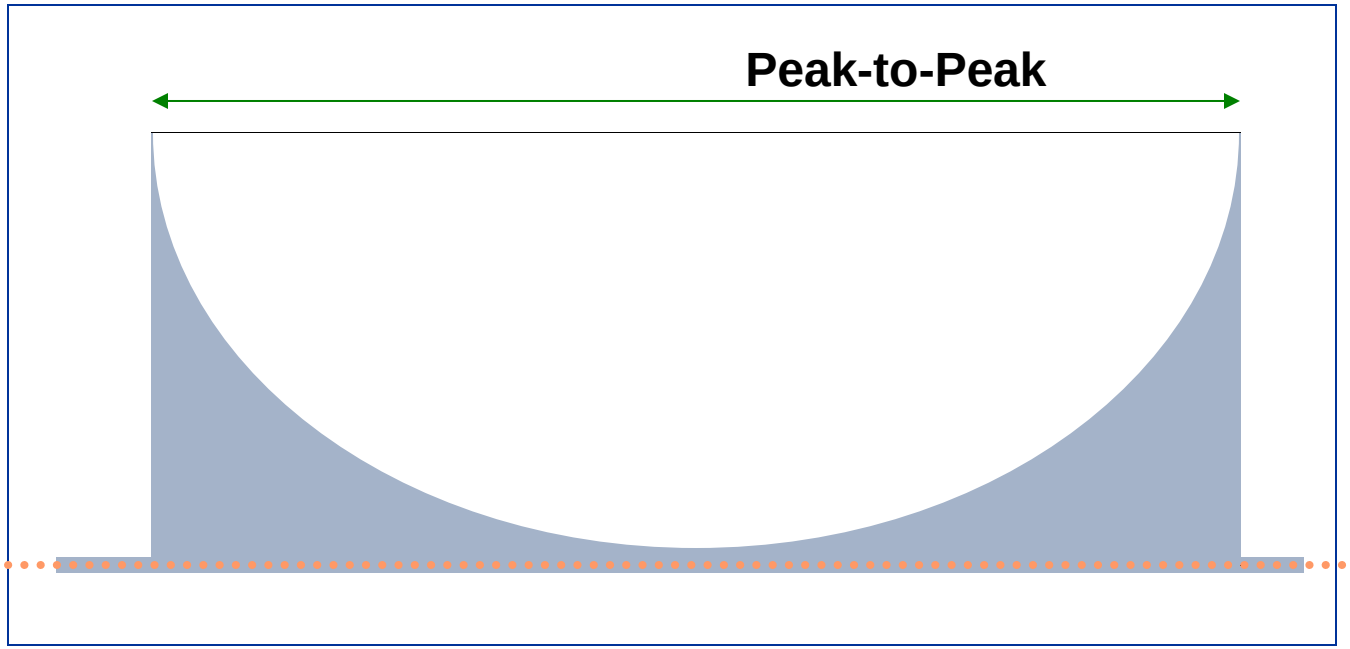
Periodic Jitter

- TIE vs. time is a repetitive waveform
- Periodic jitter is equivalent to Phase Modulation (PM) which relates to Frequency Modulation (FM)





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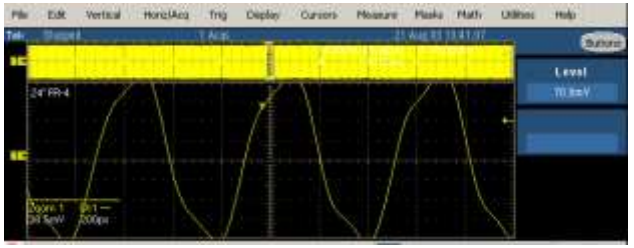
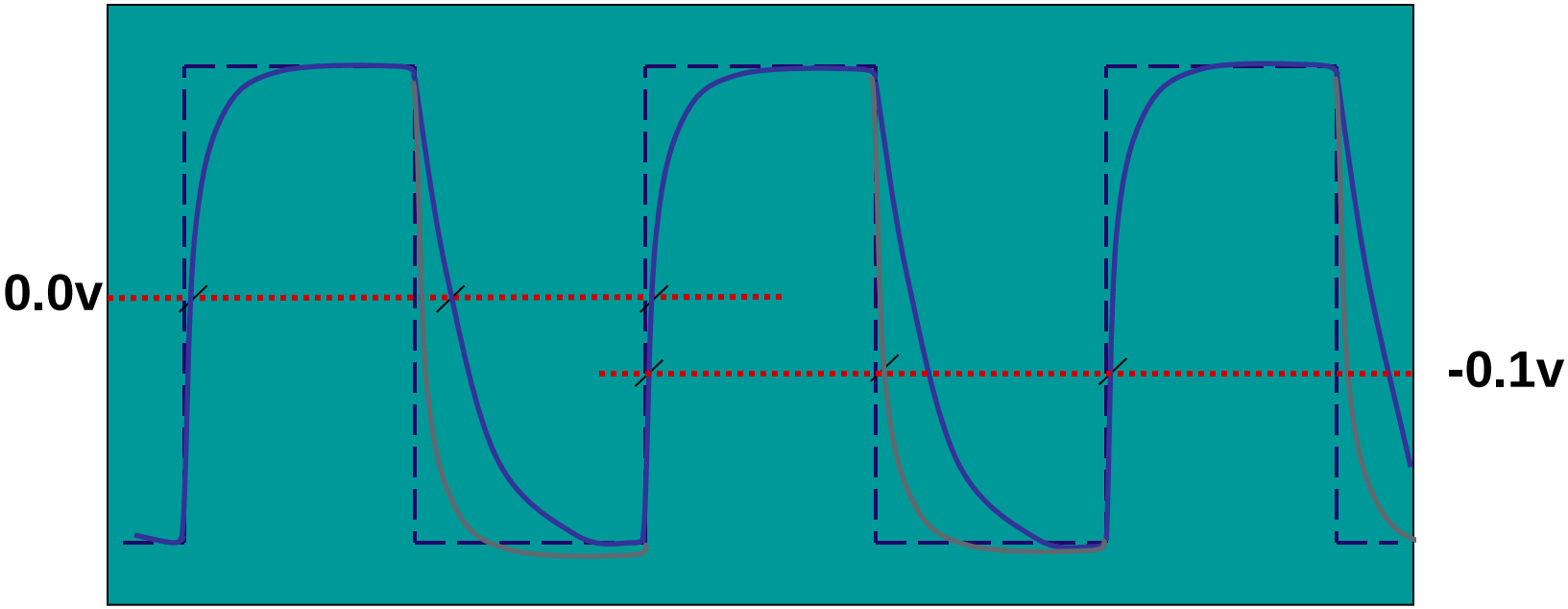
Duty Cycle Distortion

- Asymmetrical rise-time vs. fall-time
- Non-optimal choice of decision threshold





Well, ALMOST never a dual-Dirac histogram!

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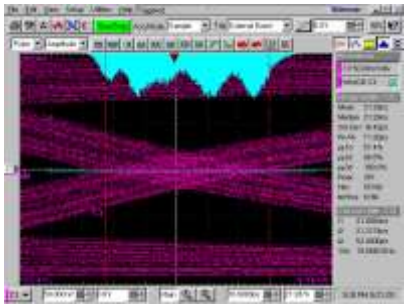
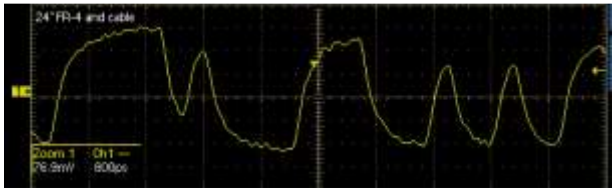
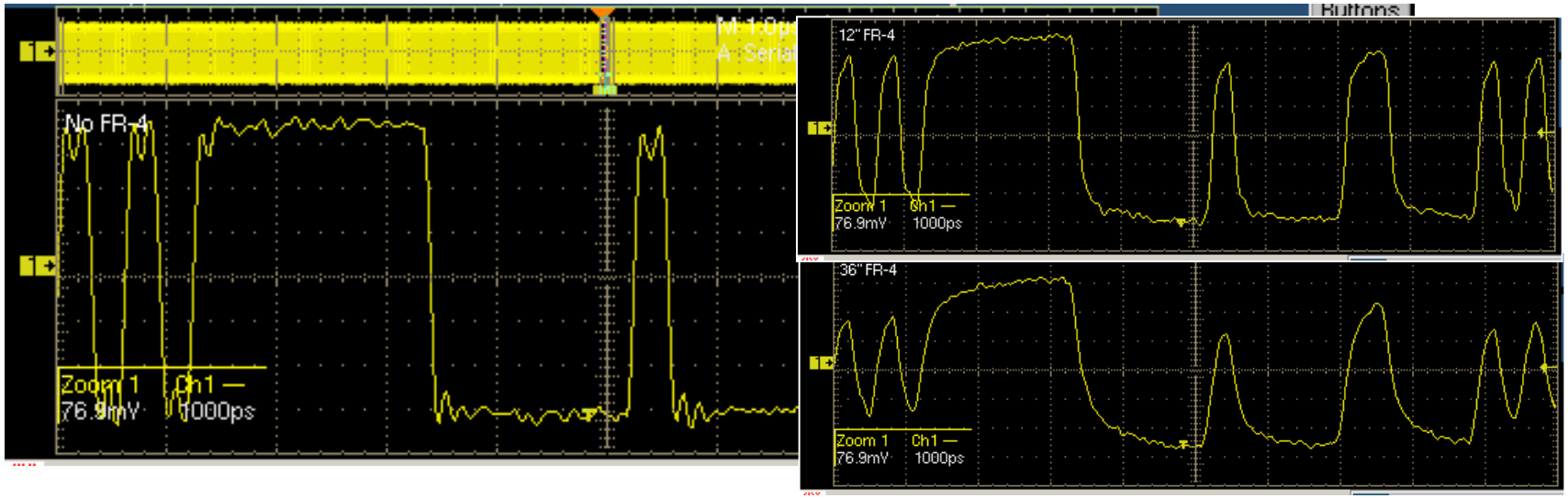
Inter-Symbol Interference



- DDJ or PDj – used interchangeably, sometimes the term ISI is also used.
- How a pattern effects subsequent bits
  - Due to transmission line effects, reflections, etc.





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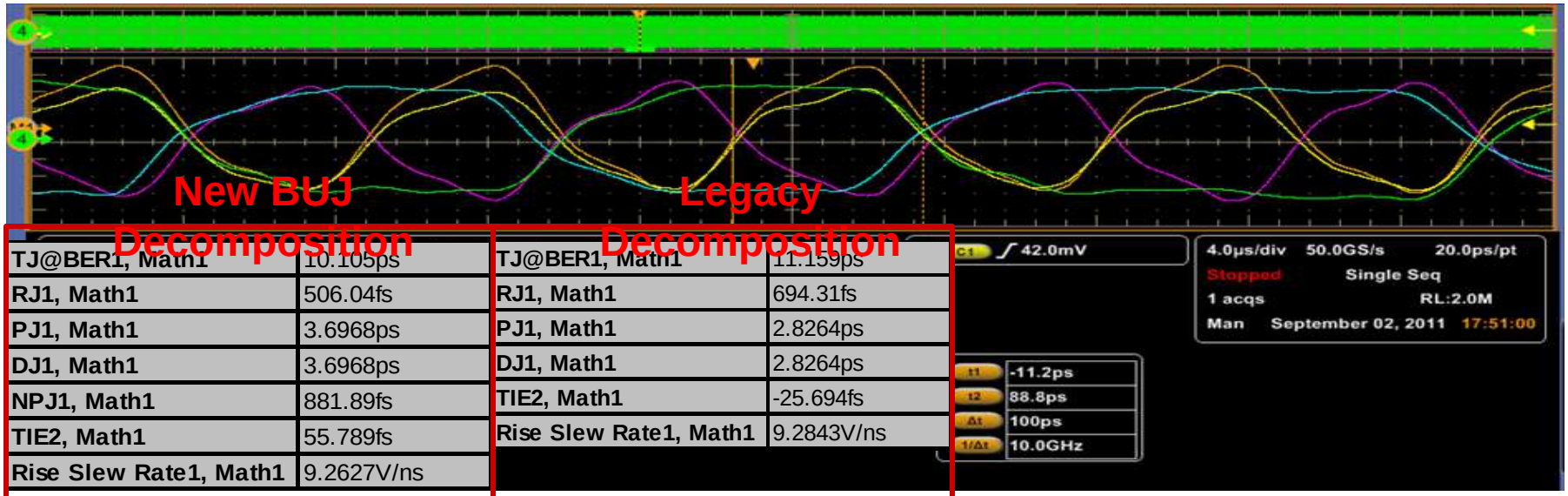
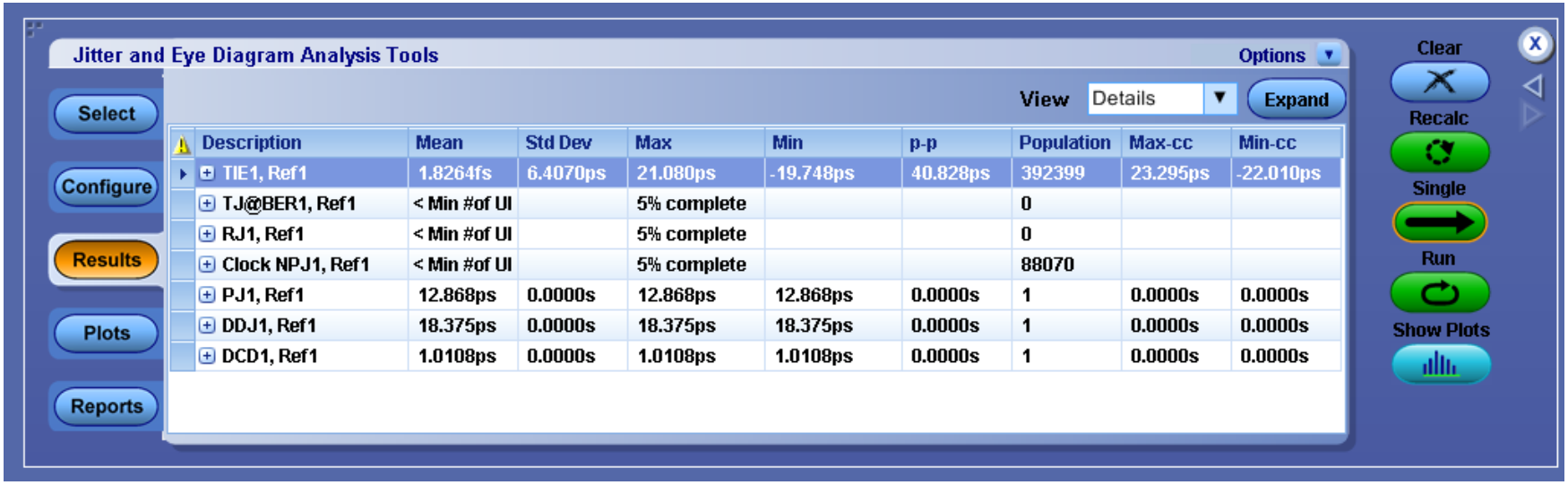
抖动眼图分析软件


New BUJ Decomposition
Legacy Decomposition
TJ@BER1, Math1 10.105ps
RJ1, Math1 506.04fs
PJ1, Math1 3.6968ps
DJ1, Math1 3.6968ps
NPJ1, Math1 881.89fs
TIE2, Math1 55.789fs
Rise Slew Rate1, Math1 9.2627V/ns
TJ@BER1, Math1 11.159ps
RJ1, Math1 694.31fs
PJ1, Math1 2.8264ps
DJ1, Math1 2.8264ps
TIE2, Math1 -25.694fs
Rise Slew Rate1, Math1 9.2843V/ns
C1 42.0mV
4.0µs/div 50.0GS/s 20.0ps/pt
Stopped Single Seq
1 acqs RL:2.0M
Man September 02, 2011 17:51:00
t1 -11.2ps
t2 88.8ps
Δt 100ps
1/Δt 10.0GHz


Jitter and Eye Diagram Analysis Tools
Options
Select
Configure
Results
Plots
Reports
View Details
Expand
Clear
Recalc
Single
Run
Show Plots
Description | Mean | Std Dev | Max | Min | p-p | Population | Max-cc | Min-cc
TIE1, Ref1 | 1.8264fs | 6.4070ps | 21.080ps | -19.748ps | 40.828ps | 392399 | 23.295ps | -22.010ps
TJ@BER1, Ref1 | < Min #of UI | | 5% complete | | | 0 | |
RJ1, Ref1 | < Min #of UI | | 5% complete | | | 0 | |
Clock NPJ1, Ref1 | < Min #of UI | | 5% complete | | | 88070 | |
PJ1, Ref1 | 12.868ps | 0.0000s | 12.868ps | 12.868ps | 0.0000s | 1 | 0.0000s | 0.0000s
DDJ1, Ref1 | 18.375ps | 0.0000s | 18.375ps | 18.375ps | 0.0000s | 1 | 0.0000s | 0.0000s
DCD1, Ref1 | 1.0108ps | 0.0000s | 1.0108ps | 1.0108ps | 0.0000s | 1 | 0.0000s | 0.0000s

抖动分类的意义

- 理解抖动产生的原因就能准确的定位到抖动
- Random Jitter
  - 使用低抖动的器件
  - 减少器件个数
  - 改善电压噪声
- Deterministic Jitter
  - 改善串扰和耦合（NP-BUJ)
  - 增加互连的带宽(ISI)
  - 改善时钟分配(PJ)
  - 改善PLL的设计(PJ)
  - 改善电源、参考分割(PJ)
  - 改善芯片的驱动(DCD)