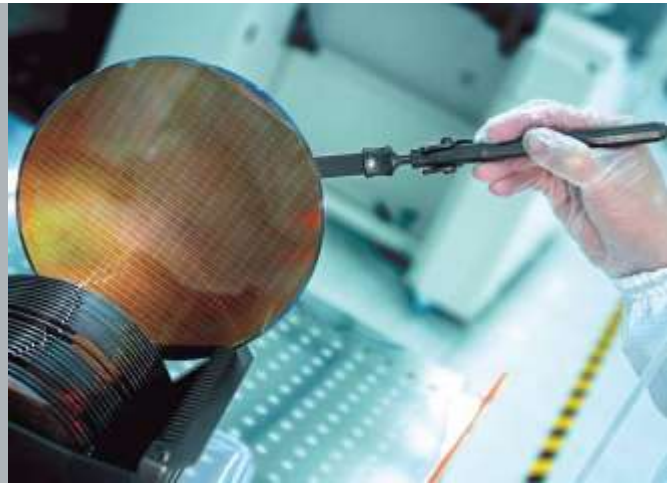
# 移动终端总线测试方案

## ----MIPI/USB3.0/MHL/eDP



余岚
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泰克科技（中国）有限公司

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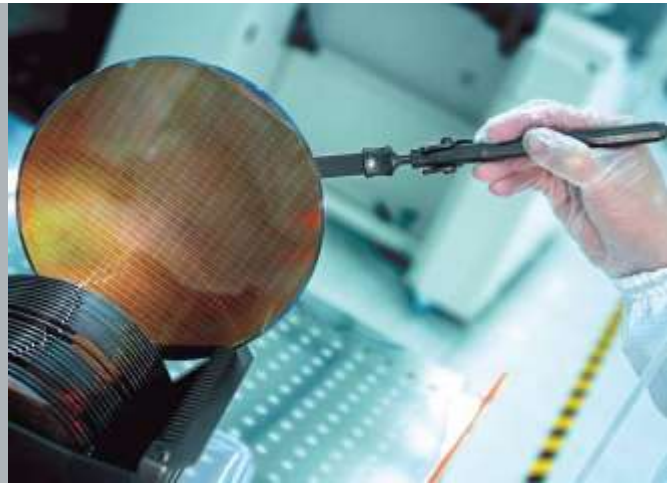
# MIPI Physical Layer Test Solutions

## D-PHY and M-PHY



MIPI® Solutions Team
Updated March, 2012

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# Agenda

- MIPI® Technologies & Tek Strategic Involvement
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx (New update Mar'12)
  - Scopes-Decodes:, 8b-10b, DigRF, LLI (New), &UniPro (New)
  - Rx
- SLIMbus, H.S.I, &DigRF testing
- Summary, Q&A

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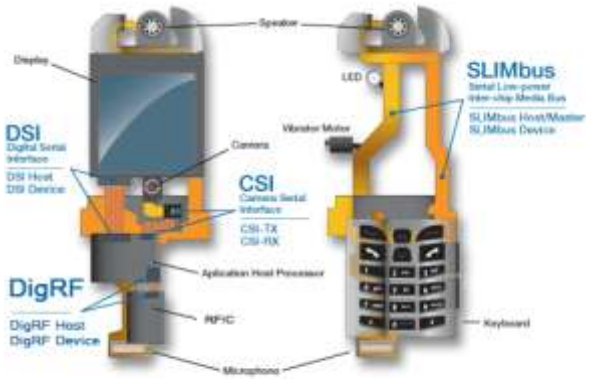
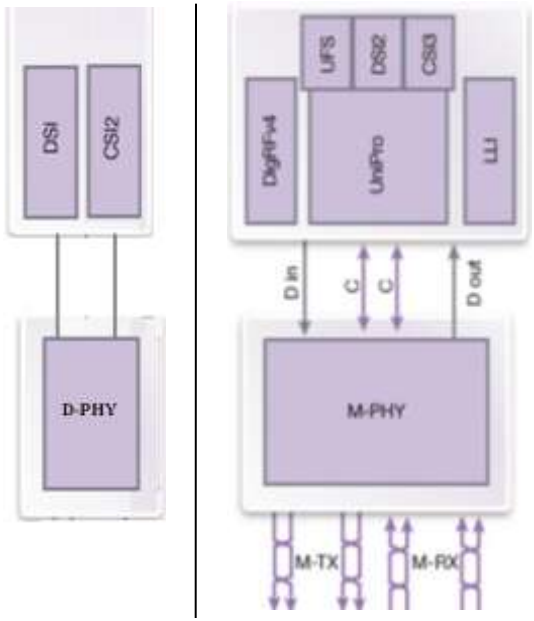
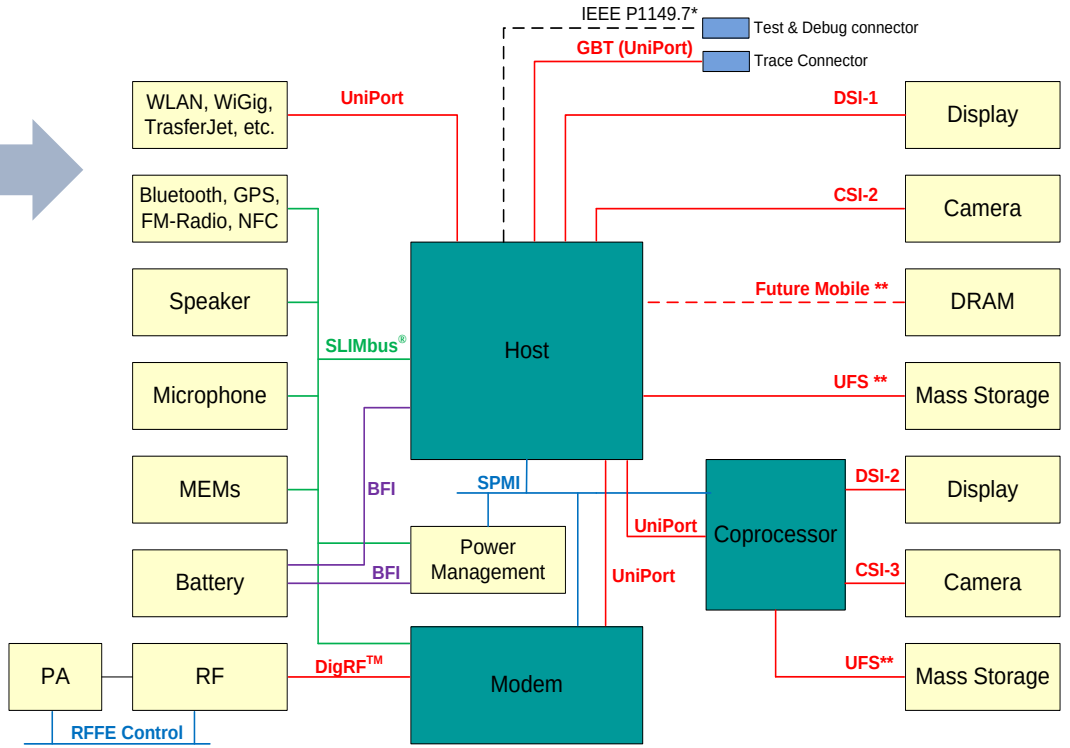
# MIPI Technologies Overview
## Example of a Mobile Platform




D-PHY/M-PHY based
SLIMbus
SPMI/RFFE

**UniPort :** UniPro + D-PHY or M-PHY

(*) Transferred to IEEE
(**) Liaison with JEDEC

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# Tek Strategic Involvement

## With MIPI Alliance &UNH-IOL

- Tektronix is a ***Contributor Member*** of the MIPI Alliance
- M-PHY Tx/Rx CTS Test Document ***"Co-Authored"*** by Tektronix
- Tektronix has a close working relationship with UNH-IOL.
- ***Joint Press-Releases*** of Tek with MIPI Alliance and UNH.
  - http://www2.tek.com/cmswpt/prdetails.lotr?ct=PR&cs=News+Release&ci=19076&lc=EN
  - "As an active MIPI contributor, Tektronix products speed the assessment of D-PHY and M-PHY performance and signal integrity. Tektronix is helping to simplify physical-layer test and validation."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2011*
  - http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6
  - "…Tektronix spurring the adoption of D-PHY and M-PHY specifications.."
    - *Joel Huloux, Chairman of the MIPI Alliance, Sept'2010*
  - "Tektronix has been supportive of UNH-IOL's collaborative efforts of physical layer measurement methodologies"
    - *Andy Baldman, MIPI Interop - R&D technical staff, UNH-IOL, Sept'2010*

iol mipi alliance Tektronix

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  - Scopes-Decodes: 8b-10b (New), DigRF, LLI (New), &UniPro (New)
  - Rx (New)
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- Summary, Q&A

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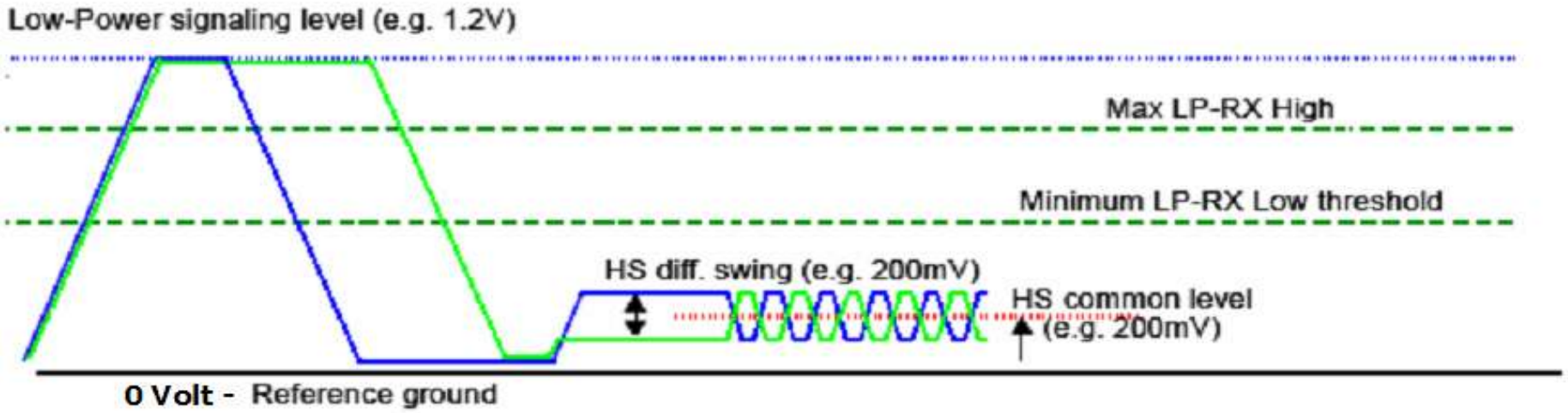
# What is D-PHY ?

- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP

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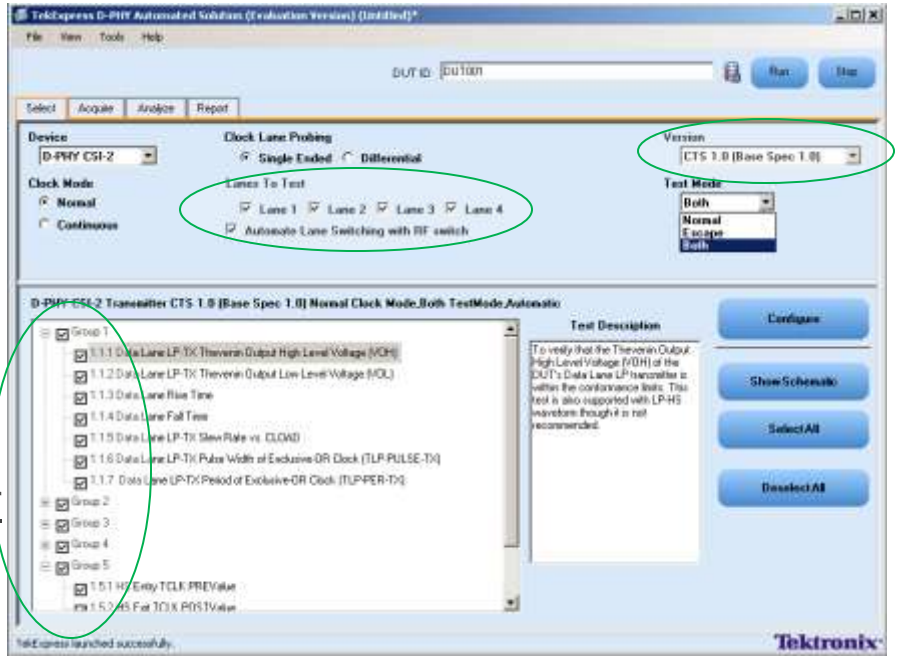
# D-PHY Testing Challenges

- Logo testing is not required, but Optional.
  - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, similar to a DDR bus.
  - Mobile Phones do not need compliance logo, unlike USB/SATA devices
- No two MIPI devices are the same
  - Variable Data Rates
  - Up to 4 lanes of Data traffic,
  - Multiple different data formats
  - Specification enables custom limits.
- Characterization is significantly important
  - Mobile OEMs select the suppliers based on characterization reports.

- **Many measurements – 49**
  - **Clock Lane**
  - **Data Lane**
  - **Clock data Timing**
- **Test Equipment &Setups need to be Very Flexible**

# D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for  Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.TEKEXP is Pre-Requisite
- Differentiation
  - **Un-parallel** Automation (Auto-Cursors)
  - **100%** Widest Test Coverage
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.0)
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber




- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & "Zoom-in" Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready

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# D-PHY Tx: Results Correlations

## Tek D-PHYTX and UNH-IOL DPHYGUI

| | | Tek Result | | | UNH Result | | Deviation in % | |
|---|---|---|---|---|---|---|---|---|
| Test ID | Measurement name | Dp | Dn | Unit | Dp | Dn | Dp | Dn |
| 1.1.1 | Data Lane LP-TX Thevenin Output High Level Voltage (VOH) | 1.212 | 1.209 | V | 1.212 | 1.209 | 0.00 | 0.00 |
| 1.1.2 | Data Lane LP-TX Thevenin Output Low Level Voltage (VOL) | 0.024 | 0.021 | V | 0.204 | 0.213 | -88.24 | -90.14 |
| 1.1.3 | Data Lane Rise Time | 24.35 | 23.89 | nS | 28.06 | 24.9 | -13.22 | -0.83 |
| 1.1.4 | Data Lane Fall Time | 14 | 13.52 | nS | 13.97 | 13.4 | 0.21 | 0.90 |
| 1.2.1 | Clock Lane LP-TX Thevenin Output High Level Voltage (VOH) | 1.191 | 1.209 | V | 1.191 | 1.209 | 0.00 | 0.00 |
| 1.2.2 | Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL) | 0.009 | 0.045 | V | 0.219 | 0.415 | -95.89 | -88.89 |
| 1.2.3 | Clock Lane Rise Time | 22.92 | 22.1 | nS | 22.83 | 22.1 | 0.39 | -0.49 |
| 1.2.4 | Clock Lane Fall Time | 14.2 | 10.68 | nS | 14.42 | 10.7 | -1.53 | 2.59 |
| 1.3.1 | Data Lane HS Entry: Data Lane TLPX Value | | 70.08 | nS | | 70.1 | -0.03 | -0.03 |
| 1.3.2 | Data Lane HS Entry: THS-PREPARE Value | | 72.32 | nS | | 72.4 | -0.11 | -0.11 |
| 1.3.3 | Data Lane HS Entry: THS-PREPARE + THS-ZERO Value | | 178.88 | nS | | 178.7 | 0.01 | 0.01 |
| 1.3.4 | Data Lane HS-TX Differential Voltages ($V_{OD(1)}$, $V_{OD(0)}$) | -211.6 | 217.2 | mV | -214.8 | 218.3 | -1.49 | -0.50 |
| 1.3.5 | Data Lane HS-TX Differential Voltage Mismatch ($\Delta V_{OD}$) | | 5.6 | mV | | 3.5 | 37.50 | 37.50 |
| 1.3.6 | Data Lane HS-TX Single Ended Output High Voltages ($V_{OHHSDP}$, $V_{OHHSDN}$) | 456 | 453 | mV | 417.5 | 417 | 8.44 | 7.95 |
| 1.3.7 | Data Lane HS-TX Common-Mode Voltages ($V_{CMTXDP}$, $V_{CMTXDN}$) | 305.96 | 306.78 | mV | 305.2 | 306.7 | 0.25 | 0.03 |
| 1.3.8 | Data Lane HS-TX Common-Mode Voltage Mismatch ($\Delta V_{CMTX(0,1)}$) | | 0.408 | mV | | 0.7 | -41.71 | -41.71 |
| 1.3.9 | Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz | | 13.59 | mVpk | | 14.3 | -4.97 | -4.97 |
| 1.3.10 | Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{CP}$ | | 7 | mVrms | | 7 | 0.00 | 0.00 |
| 1.3.11 | Data Lane HS-TX 20%-80% Rise time ($t_R$) | | 223.6 | pS | | 223.5 | 0.04 | 0.04 |
| 1.3.12 | Data Lane HS-TX 80%-20% Fall time ($t_F$) | | 228.6 | pS | | 228.6 | -0.44 | -0.44 |
| 1.3.13 | Data Lane HS Exit: $T_{HS-TRAIL}$ Value | | 62.45 | nS | | 62.4 | 0.18 | 0.18 |
| 1.3.14 | Data Lane HS Exit: 30%-80% Post-EoT Rise Time($T_{REOT}$) Value | | 17.04 | nS | | 16.3 | 2.47 | 2.47 |
| 1.3.15 | Data Lane HS Exit: TEOT Value | | 79.49 | nS | | 78.7 | | -0.66 |
| 1.3.16 | Data Lane HS Exit: THS-EXIT Value | | 10.98 | nS | Not Available | | | |
| 1.4.1 | Clock Lane HS Entry: $T_{LPX}$ Value | | 71.28 | nS | | 71.5 | 0.04 | 0.04 |
| 1.4.2 | Clock Lane HS Entry: $T_{CLKPREPARE}$ Value | | 51.9 | nS | | 50.1 | 3.26 | 3.26 |
| 1.4.3 | Clock Lane HS Entry: $T_{CLKPREPARE}$ +$T_{ZERO}$ Value | | 294.6 | nS | | 298.1 | -1.24 | -1.24 |
| 1.4.4 | Clock Lane HS-TX Differential Voltages ($V_{OD(1)}$, $V_{OD(0)}$) | -188.31 | 136.99 | mV | -184.7 | 132.7 | 1.95 | 1.95 |
| 1.4.5 | Clock Lane HS-TX Differential Voltage Mismatch ($\Delta V_{OD}$) | | 51.33 | mV | | 58.2 | -11.80 | -11.80 |
| 1.4.6 | Clock Lane HS-TX Single Ended Output High Voltages ($V_{OHHSDP}$, $V_{OHHSDN}$) | 447 | 471 | mV | 378.6 | 404.1 | 15.30 | 14.20 |
| 1.4.7 | Clock Lane HS-TX Common-Mode Voltages ($V_{CMTX(1)}$,VCMTX$_{(0)}$) | 314.06 | 310.84 | mV | 314.1 | 310.9 | -0.01 | -0.02 |
| 1.4.8 | Clock Lane HS-TX Common-Mode Voltage Mismatch ($\Delta V_{CMTX(0,1)}$) | | 1.61 | mV | | 1.6 | 0.63 | 0.63 |
| 1.4.9 | Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz | | 17.3 | mVpk | | 12.2 | 29.48 | 29.48 |
| 1.4.10 | Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_C$ | | 7.46 | mVrms | | 7.4 | 0.81 | 0.81 |
| 1.4.11 | Clock Lane HS-TX 20%-80% Rise time ($t_R$) | | 277.3 | pS | | 263.2 | 5.36 | 5.36 |
| 1.4.12 | Clock Lane HS-TX 80%-20% Fall time ($t_F$) | | 275.39 | pS | | 258.3 | 6.62 | 6.62 |
| 1.4.13 | Clock Lane HS Exit: $T_{CLK-TRAIL}$ Value | | 93.32 | nS | | 92.7 | 1.23 | 1.23 |
| 1.4.14 | Clock Lane HS Exit: 30%-80% Post-EoT Rise Time($T_{REOT}$) Value | | 17 | nS | | 17.5 | -2.91 | -2.91 |
| 1.4.15 | Clock Lane HS Exit: TEOT Value | | 70.31 | nS | | 70.8 | | -0.19 |
| 1.4.16 | Clock Lane HS Exit: THS-EXIT Value | | 178.24 | nS | Not Available | | | |
| 1.4.17 | Clock Lane HS Clock Instantaneous ($UI_{INST}$) | Min 1.134 Mean | Max 1.38 | pS | Min NA Mean | Max 1.39 | Min NA Mean | Max 1.77 1.20 |
| 1.5.1 | HS Entry $T_{CLKPREP}$ Value | | 87.28 | nS | | 89.3 | -2.26 | -2.26 |
| 1.5.2 | HS Exit $T_{CLKPOST}$ Value | | 10361.52 | nS | | 10297.7 | 0.62 | 0.62 |
| 1.5.3 | HS Clock Rising Edge Alignment to First Payload Bit | | | | | | | |
| 1.5.4 | Data-to-Clock Skew (TSKEW[TX]) | | | | | | | |
| | Clock UI | | 1.25 | nS | | 1.25 | | 0.00 |
| | Maximum Data to clock skew | | -275 | mUI | | -263 | | -4.73 |
| | Minimum Data to clock skew | | -452 | mUI | | -448 | | 5.09 |
| | Mean Data to clock skew | | -346 | mUI | | -358 | | 3.41 |

**Setup:** MSO 20GHz scope, 4x P6248 probes, Termination board and probing board from UNH.

* As LP HS waveform is used in this use-case, Tek algorithm finds the LP-00 region and computes VOL in that region, whereas the UNH algorithm considers t computing VOL. If LP signal is used, the same measurement has 100% correlation.

| Deviation in % | |
|---|---|
| Dp | Dn |
| 0.00 | 0.00 |
| -88.24 | -90.14 |
| -13.22 | -0.83 |
| 0.21 | 0.90 |
| 0.00 | 0.00 |
| -95.89 | -88.89 |
| 0.39 | -0.49 |
| -1.53 | 2.59 |
| -0.03 | -0.03 |
| -0.11 | -0.11 |
| 0.01 | 0.01 |
| -1.49 | -0.50 |
| 37.50 | 37.50 |
| 8.44 | 7.95 |
| 0.25 | 0.03 |
| -41.71 | -41.71 |
| -4.97 | -4.97 |
| 0.00 | 0.00 |
| 0.04 | 0.04 |
| -0.44 | -0.44 |
| 0.18 | 0.18 |
| 2.47 | 2.47 |
| | -0.66 |
| | |
| 0.04 | 0.04 |
| 3.26 | 3.26 |
| -1.24 | -1.24 |
| 1.95 | 1.95 |
| -11.80 | -11.80 |
| 15.30 | 14.20 |
| -0.01 | -0.02 |
| 0.63 | 0.63 |
| 29.48 | 29.48 |
| 0.81 | 0.81 |
| 5.36 | 5.36 |
| 6.62 | 6.62 |
| 1.23 | 1.23 |
| -2.91 | -2.91 |
| | -0.19 |
| | |
| Min | Max |
| NA | 1.77 |
| Mean | 1.20 |
| -2.26 | -2.26 |
| 0.62 | 0.62 |
| | |
| | 0.00 |
| | -4.73 |
| | 5.09 |
| | 3.41 |


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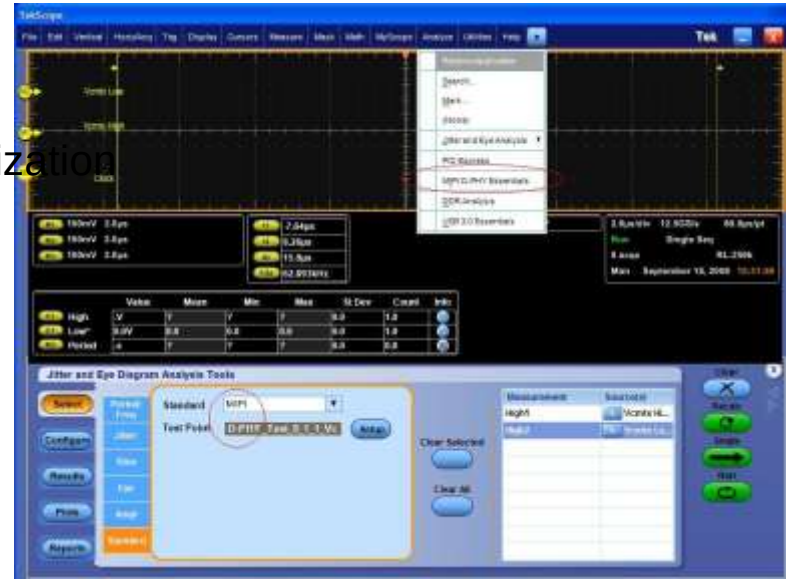
# D-PHY Tx : Opt.D-PHY Debug and Analysis Solution

- Opt.D-PHY : D-PHY Essentials
  - DPOJET option for Setup Library &MOI
  - Provides Debug Analysis and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.DJA is Pre-Requisite
- Differentiation
  - Fully-Flexible for Debug Analysis &Characterization
  - Breadth of Tests Coverage
  - Based on State-of-the-art DPOJET tool



- Value proposition
  - Tek 3.5GHz scope is the Minimal Configuration for accurate testing
  - Single tool (DPOJET) for both MIPI Phy standards - Opt.M-PHY &Opt.D-PHY
  - Comprehensive DPOJET Reports.
  - D-PHY extension spec (1.5G) ready

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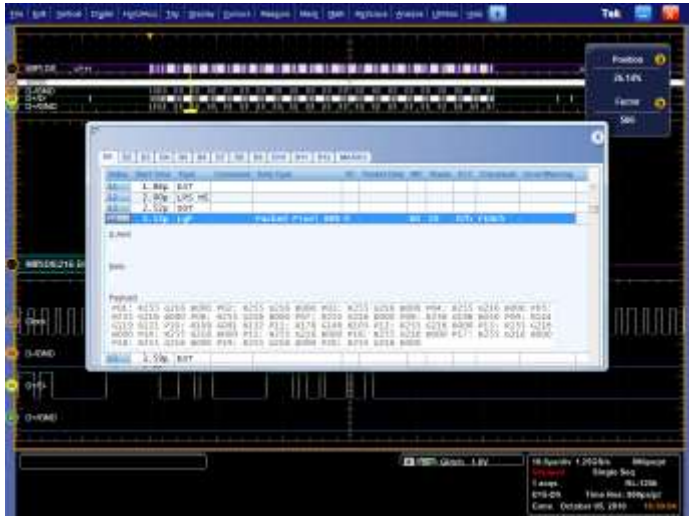
# D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

## Timestamps

- Decodes LP &HS states, BTA, DCS, ECC, Checksum, Escape Mode, etc
- Decodes SoT, EoT, Data Type, Virtual Channel, Word Count, Short / Long packet, Number of pixels, Each pixel values shown in R-B-G format.
- Timestamps for each Event &Event Table
- Zoom on a row of pixels



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# D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

## Errors/ Warnings indicated in Decode waveform &Event Table

Missing Sync

Checksum Error

ECC error

Errors and Warnings indicated in event table

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# D-PHY Tx &Decode: Recommended Test Setup

www.tek.com/MIPI

- Scope
  - DPO7354 or DPO/DSA/MSO70404/B/C or higher for rise time accuracies
- Probes
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500 (clock is non-continuous), or 3x TDP3500 (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- Scope Software
  - Opt.D-PHYTX on TEKEXP for Conformance Test
  - Opt.D-PHY on DPOJET for Debug, Analysis &Characterization
  - Opt.SR-DPHY for Decode of CSI &DSI traffic
- Fixtures
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups:
    - No standard fixture is defined.
    - We recommend following UNH-IOL Termination boards: www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc

P7380 probe used with a probe-tip

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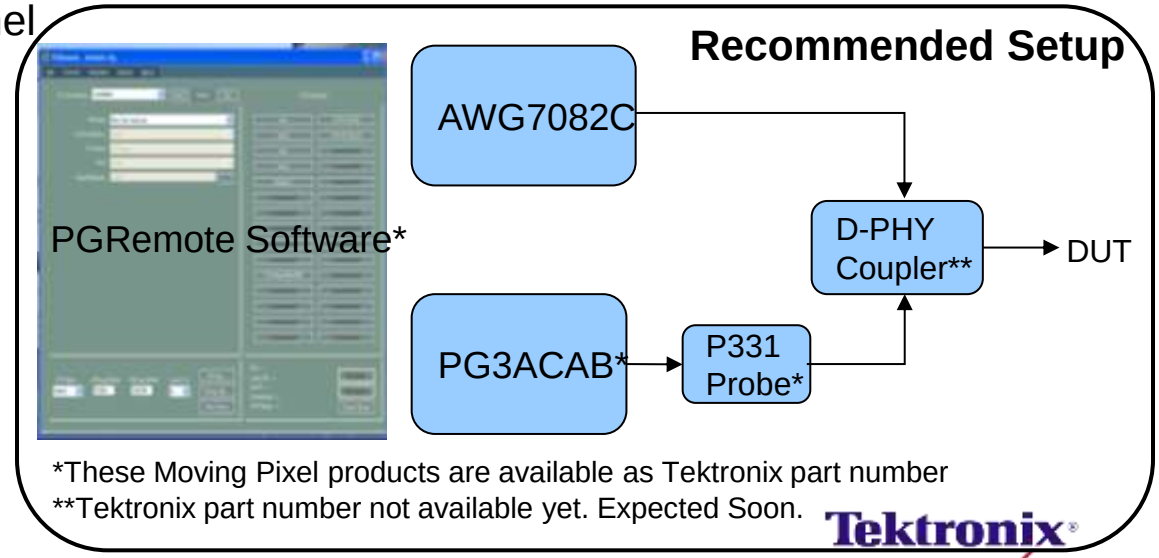
# D-PHY Rx : Test Solution Overview

## Simple, Quick, Easy and Re-usable

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals



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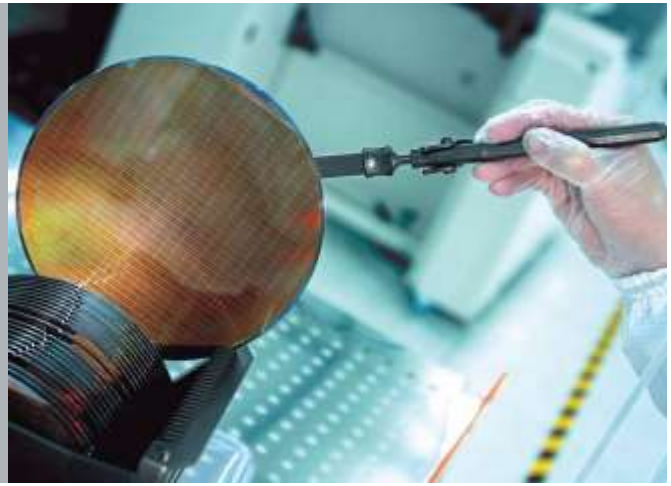
# USB 3.0 Physical Layer Testing



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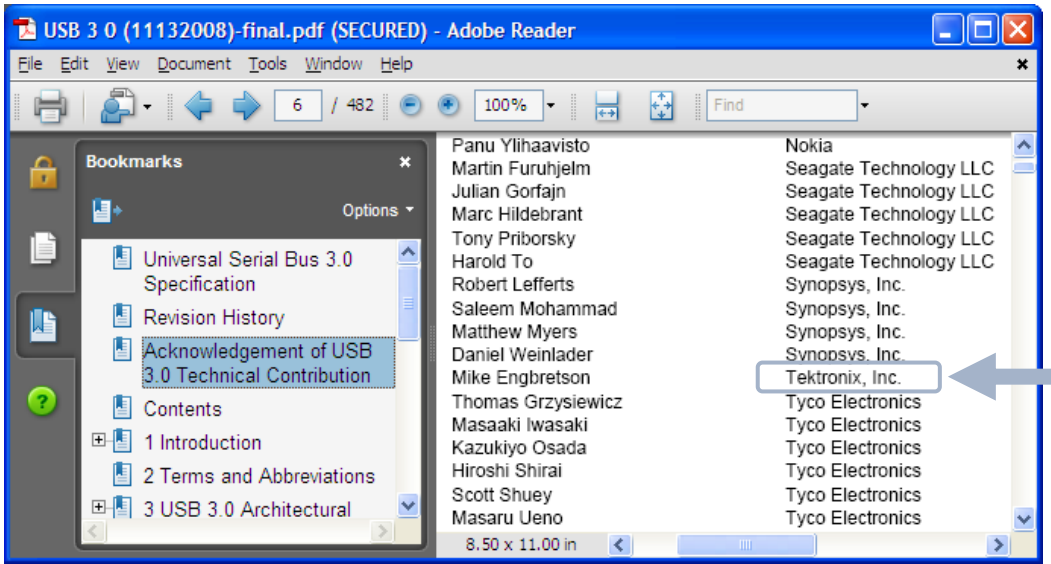
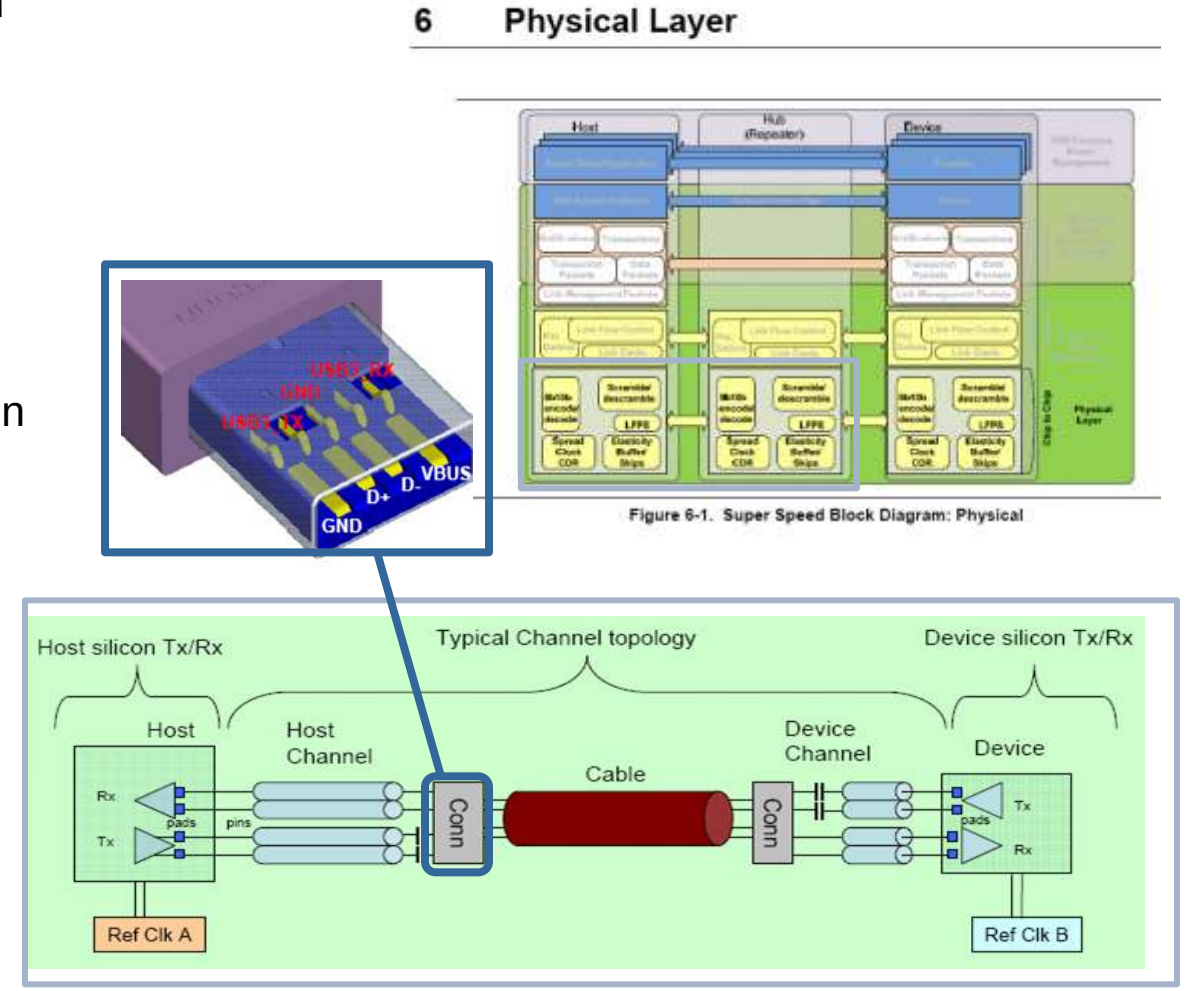
# USB Industry Leadership

- Tektronix 1st to market for USB 2.0
- Only approved Method of Implementation (MOI) for WiMedia
- Millions of certified products shipped, enabled by Tektronix USB solutions
- Tektronix is only T&M Technical Contributor in the USB 3.0 specification!
- Actively engaged with USB 3.0 industry leaders in the development of Tektronix' USB 3.0 Solutions



# USB 3.0 Key Considerations

- Receiver Testing Now Required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel Considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Test Strategy
  - Cost-effective tools
  - Flexible solutions




**Source: USB 3.0 Rev 1.0 Specification**





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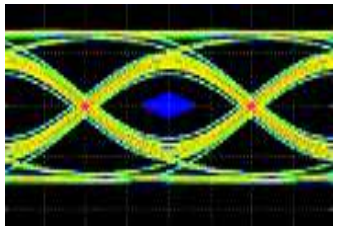
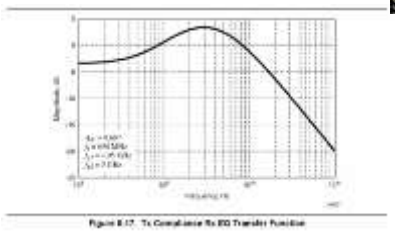
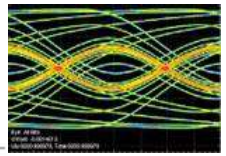
# USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
  - Reference channel is embedded and CTLE is applied
- USB 3.0 Reference Channels
  - Host Reference Channel
    - 11” back panel is applied for device testing
  - Device Reference Channel
    - 5” device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels
- USB 3.0 Reference Equalizer
  - Attenuates the low frequency content of the signal to open the eye



CTLE





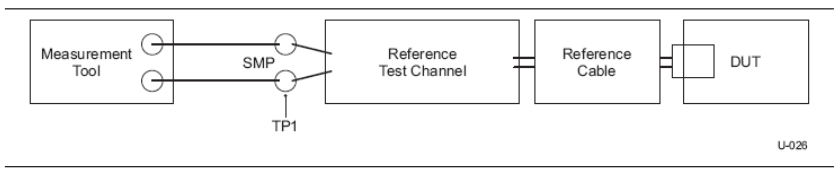
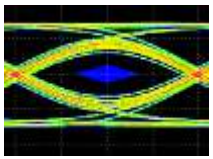


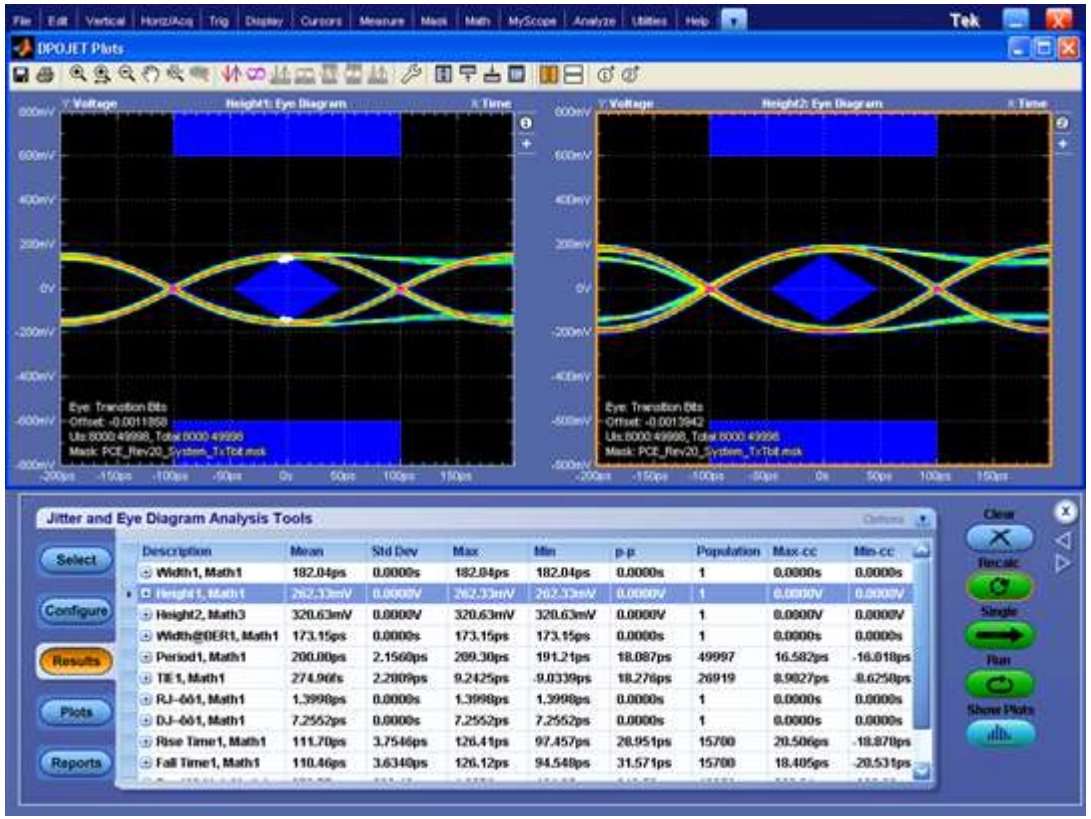

Figure 6-14. Tx Normative Setup with Reference Channel



# Fixture and Channel De-Embedding

- Why de-embed – Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins
- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software

**Before** → **After**

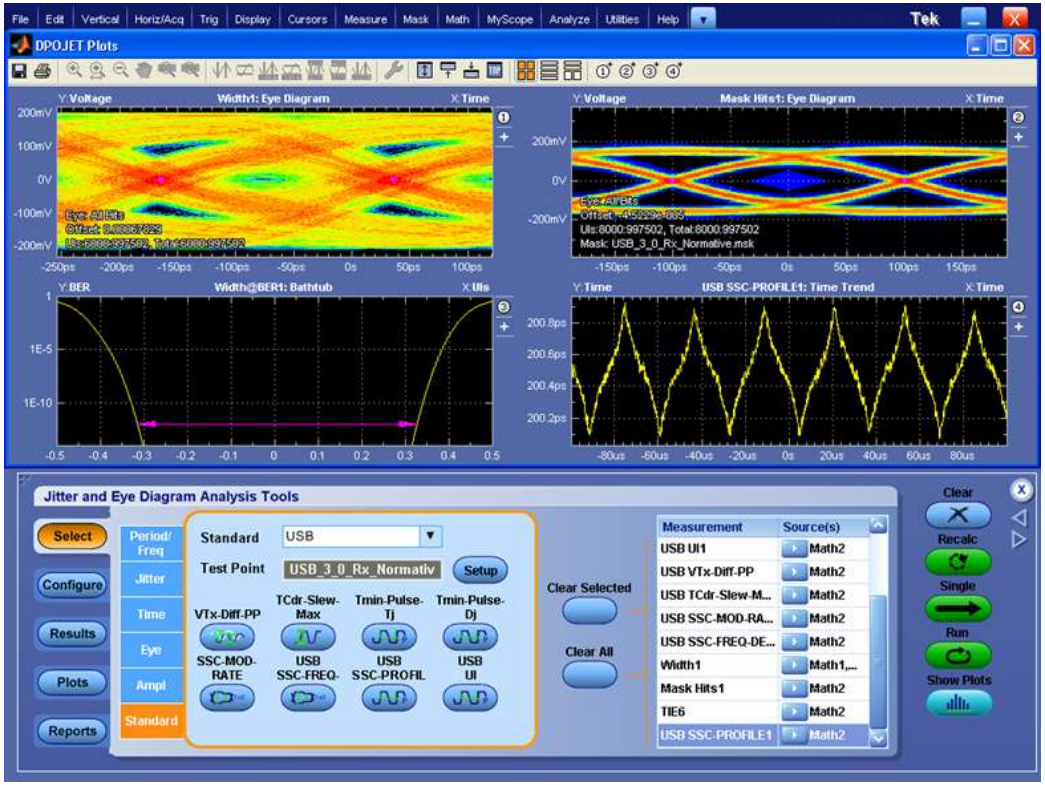




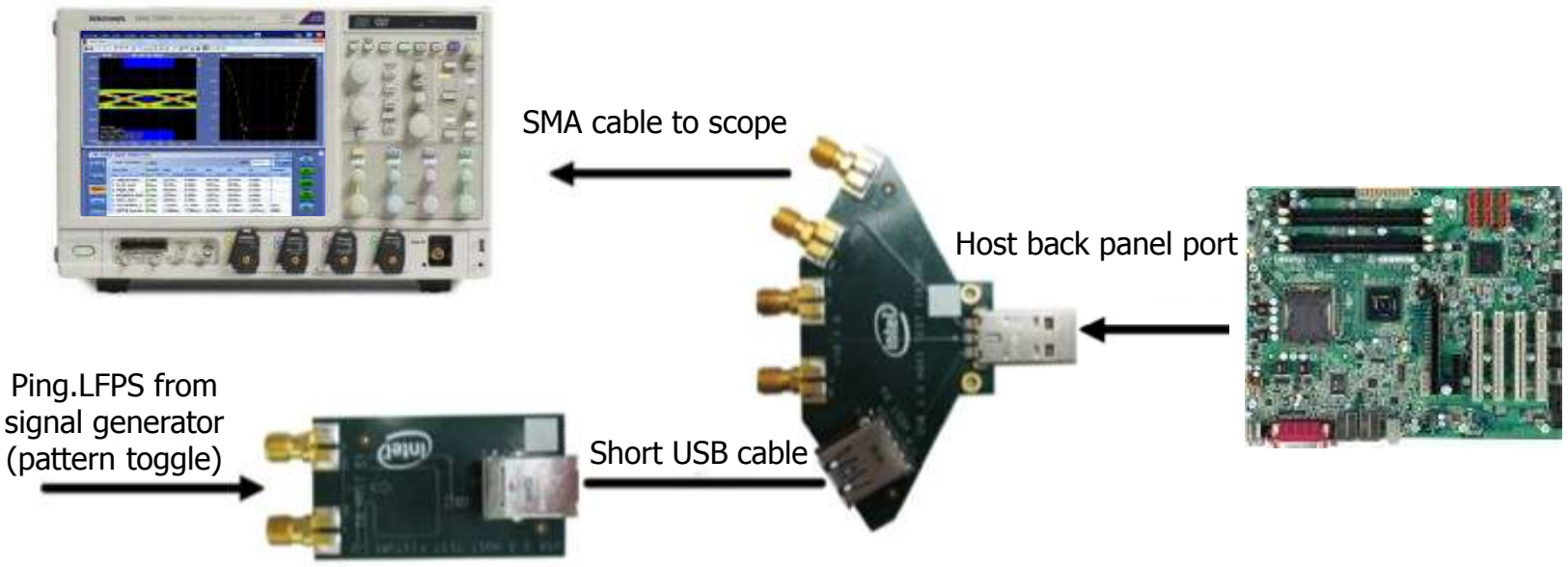

  

# USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation

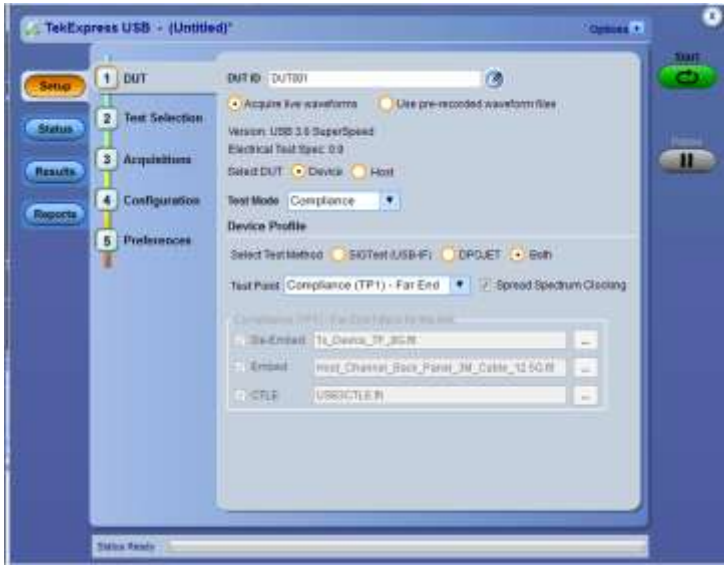


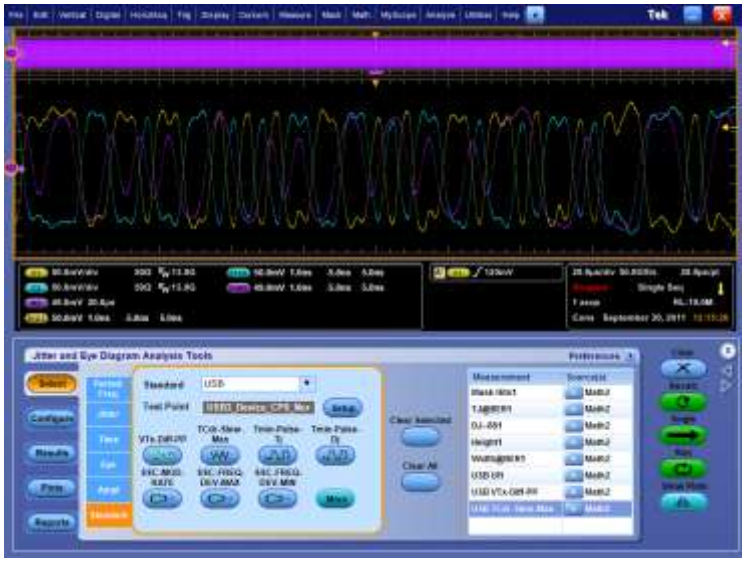
# Example Host Test Setup



# Transmitter Solutions

- Comprehensive Solution Goes Beyond Compliance
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results
- Complete Toolset for Characterizing USB 3.0 Designs
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG





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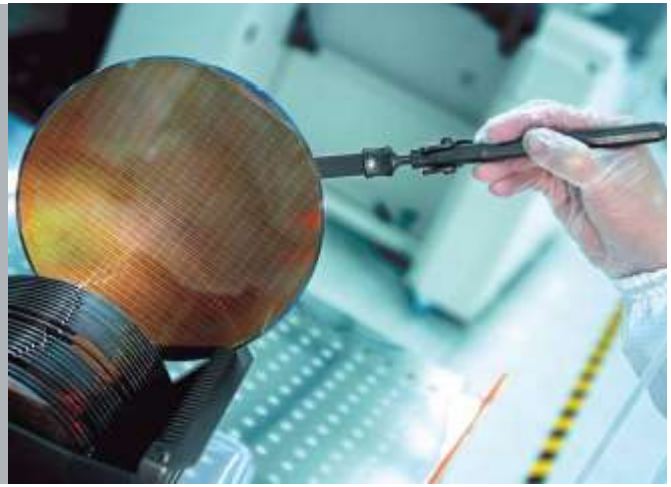
# USB 3.0 Receiver Testing



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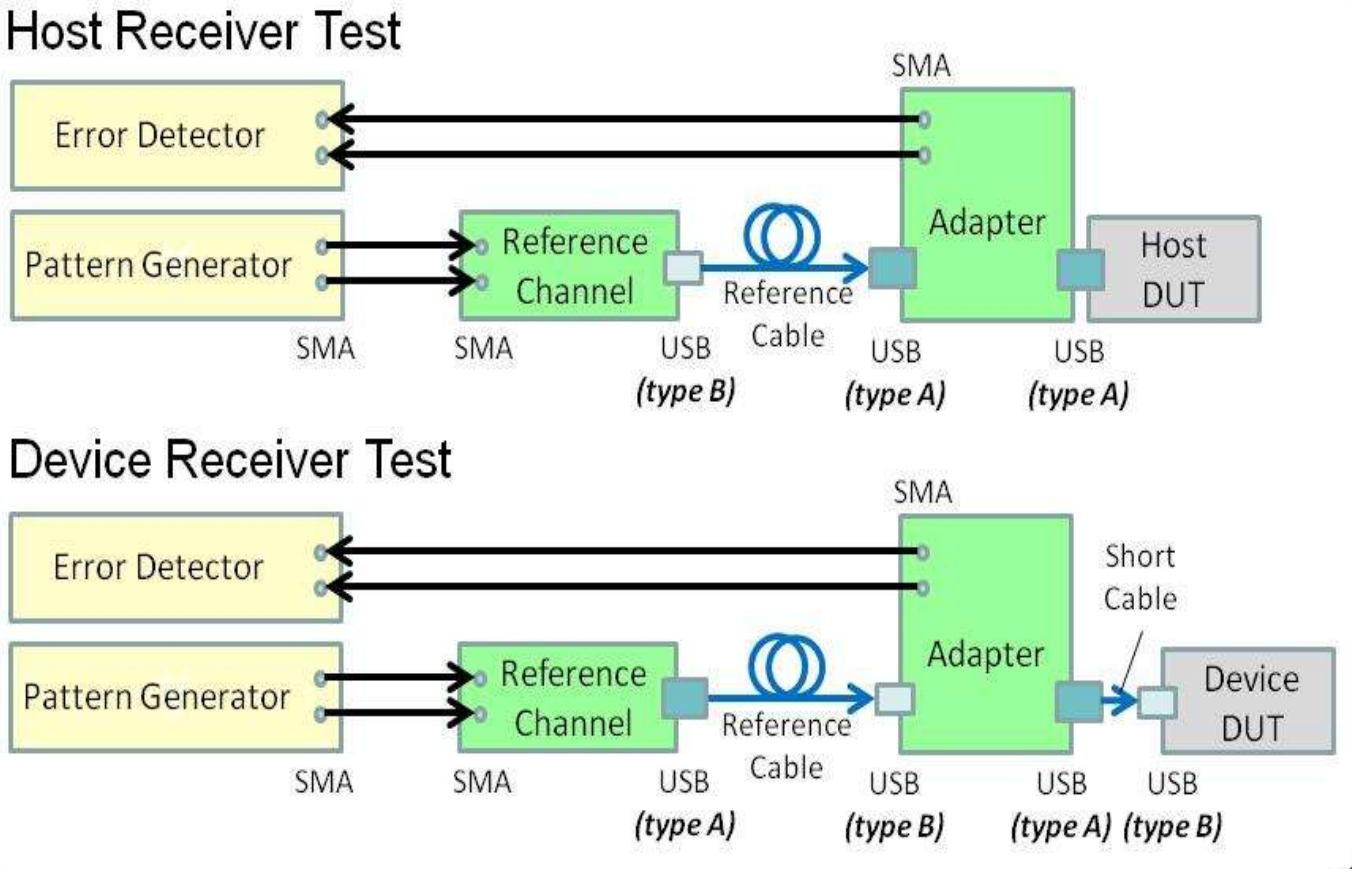
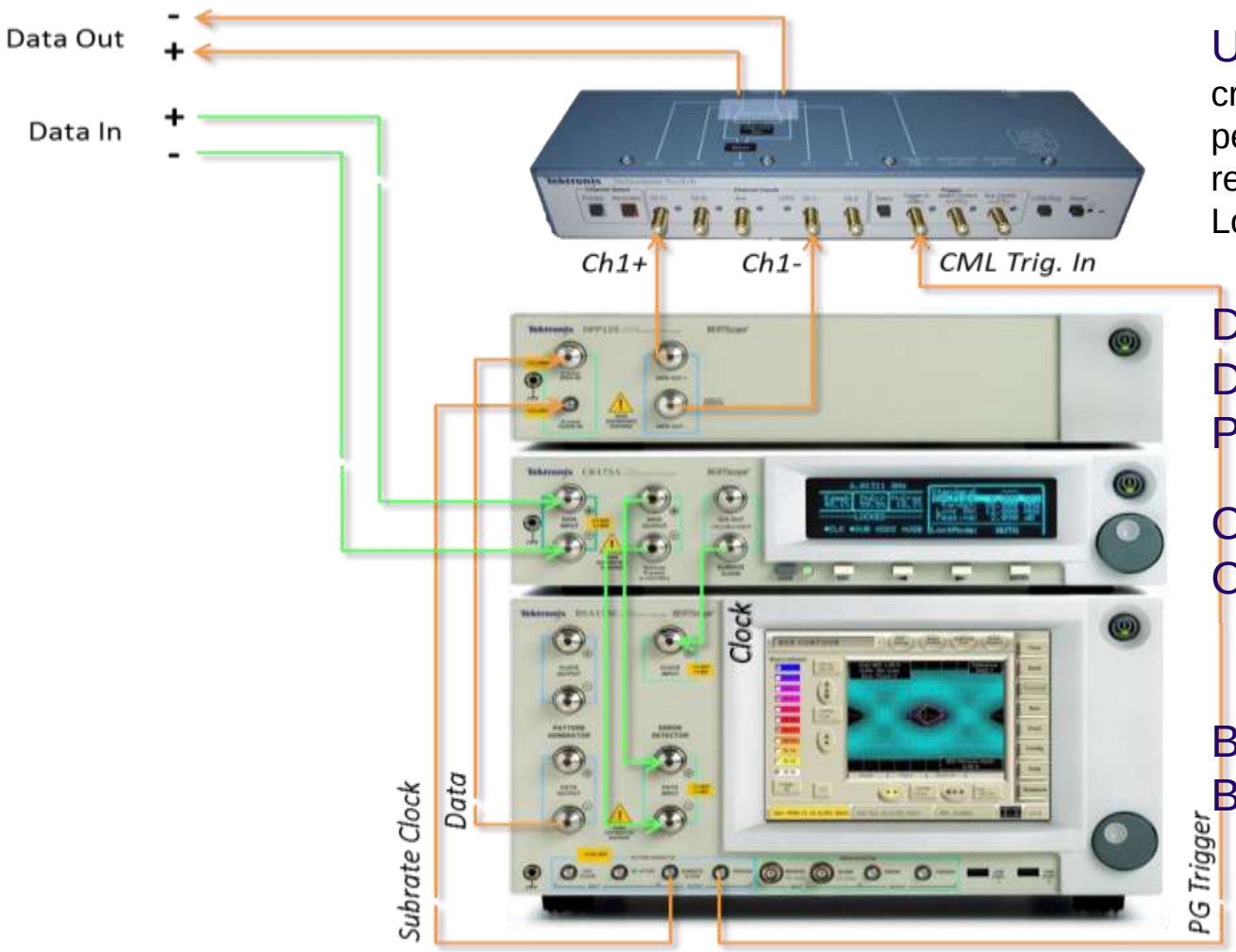
# Generic USB 3.0 RX Test Configuration



# BERTScope USB 3.0 RX Test Configuration




**USB Switch**
creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

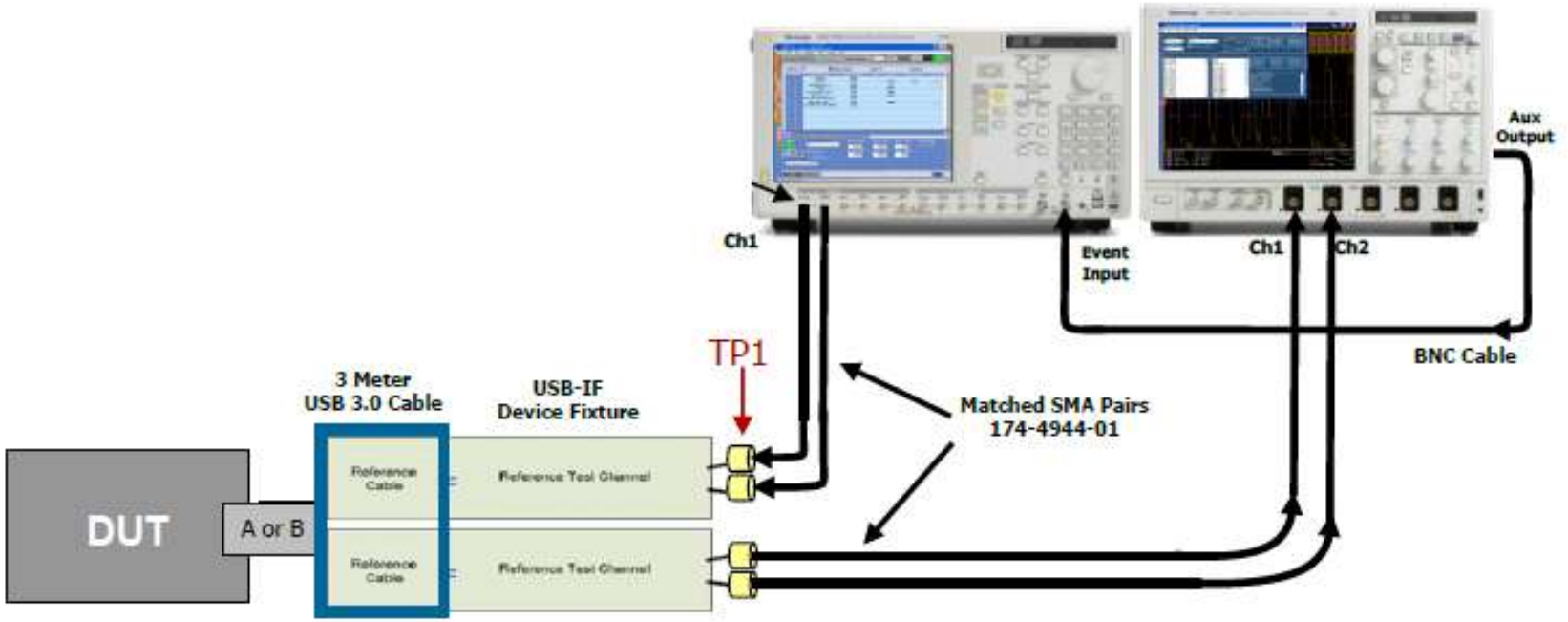
**DPP125B**
**De-emphasis Processor**

**CR125A**
**Clock Recovery**

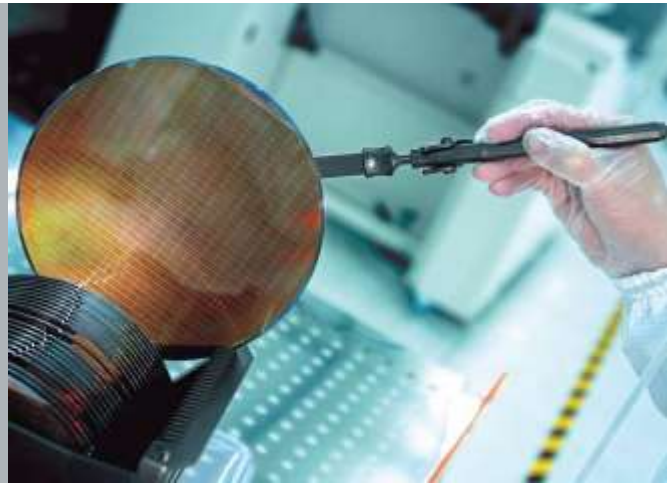
**BSA85C**
**BERTScope**

# AWG USB 3.0 RX/TX Test Configuration

- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)



# Tektronix MHL 2.1 Solution



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# MHL – An Introduction

- Why MHL interface?
  - Connector agnostic….




**Source: MHL.org**



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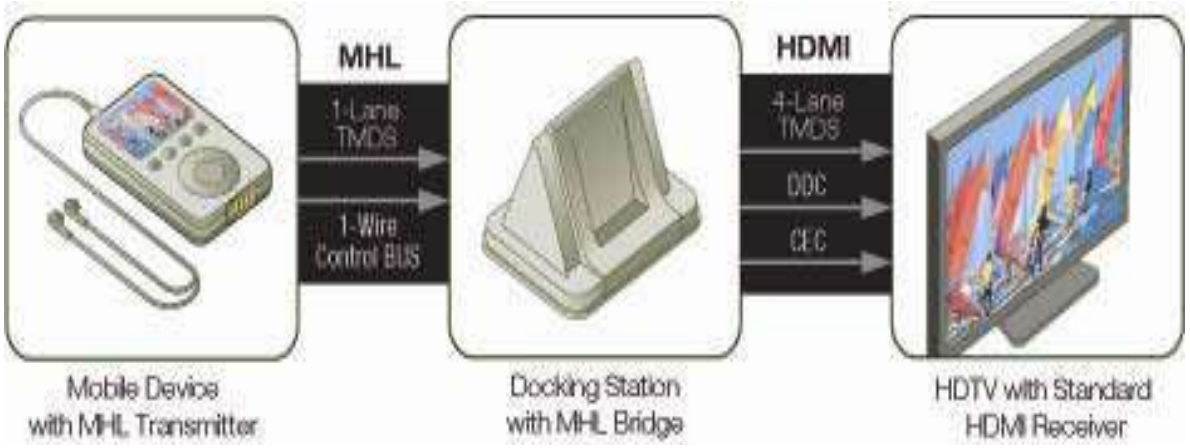
# MHL Introduction




**Source: MHL.org**

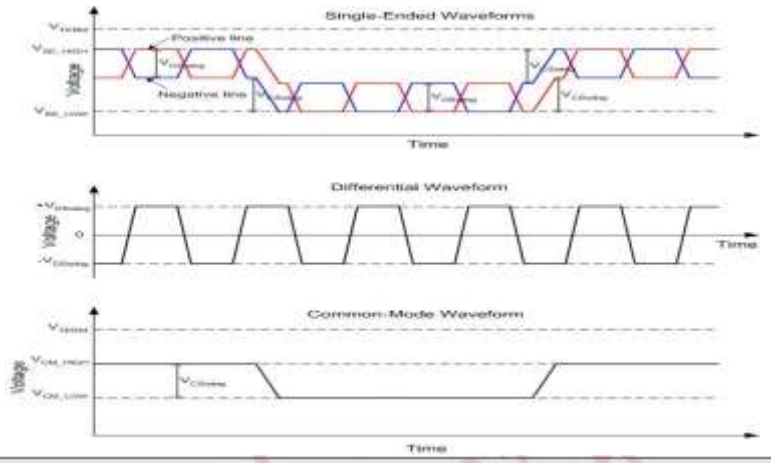
- Mobile HD Link (MHL) technology is a low pin count HD audio and video interface that connects portable electronics devices such as mobile phones, digital cameras, camcorders and portable media players, to HDTVs.
- The technology allows mobile devices to output digital 1080 Full HD resolution via the existing mobile connector without the real estate and cost of another dedicated video connector.
- Together with an MHL-to-HDMI bridge, the MHL-enabled mobile device becomes a fully compliant HDMI source and can connect to the television's standard HDMI input port.

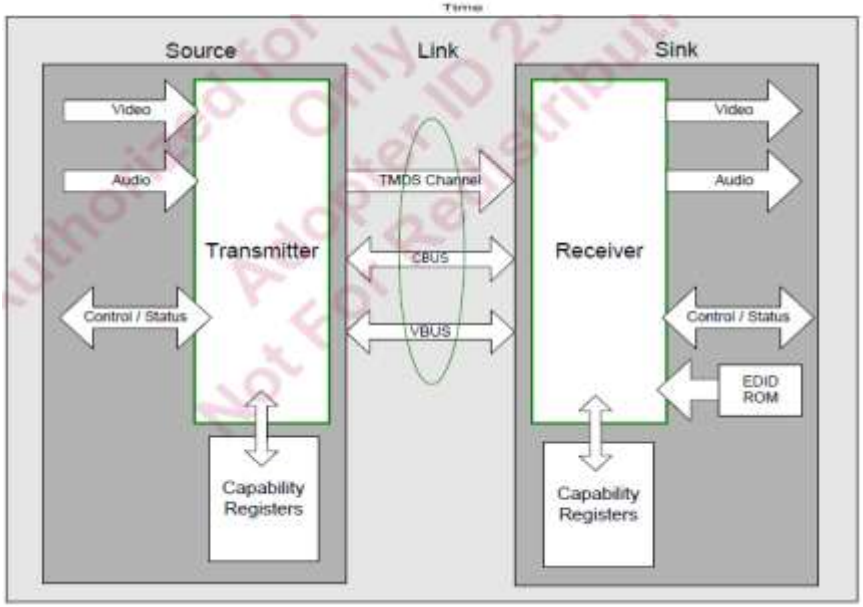
# MHL Introduction

- MHL Consortium was formed in Sept 2009 with the following founding members:
  - NOKIA
  - SAMSUNG
  - Silicon Image
  - Sony
  - Toshiba
- The Specification 1.1 version was announced in Q12011 , Specification 1.2 in Dec 2011, Specification 2.0 in Feb 2012 and Specification 2.1 NOW.

  The Consortium released CTS 1.1 version in June 2011, CTS 1.2 in Jan 2012, CTS 2.0 in Sept 2012 and CTS 2.1 is just announced.

  COMPLETE TEKTRONIX SOLUTION APPROVED in CTS1.1 , CTS 1.2 , CTS 2.0 and CTS 2.1 solution
- Tektronix is a **Contributor adopter** and actively involved in defining the CTS 2.1.




**Source: MHL 1.2 specification document**



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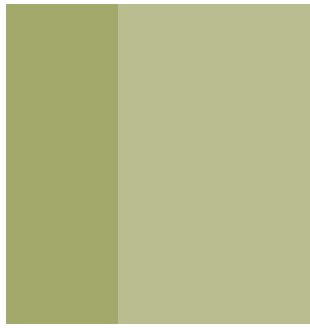
# Tektronix MHL Solution





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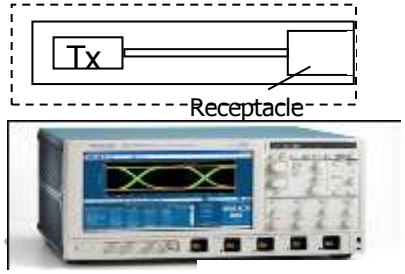
# MHL Ecosystem and Tektronix Solution

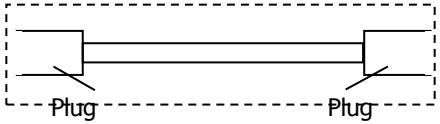
- Tektronix Offers Complete MHL 2.1 Solution.
- Industry's first  1 BOX solution for Physical and Protocol testing.
  - Seamless transition between Protocol and Phy layer
  - Simple setup leads to faster test times


Source Devices

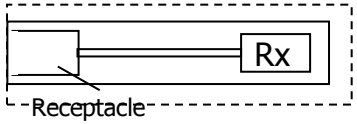



Electrical and Protocol

Cable Assemblies




Sink Devices




Electrical and Protocol



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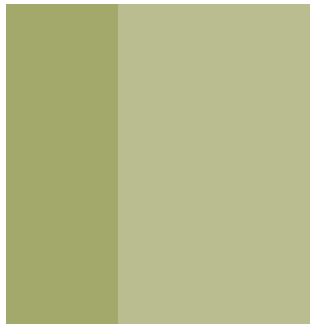
# Tektronix MHL Transmitter Solution





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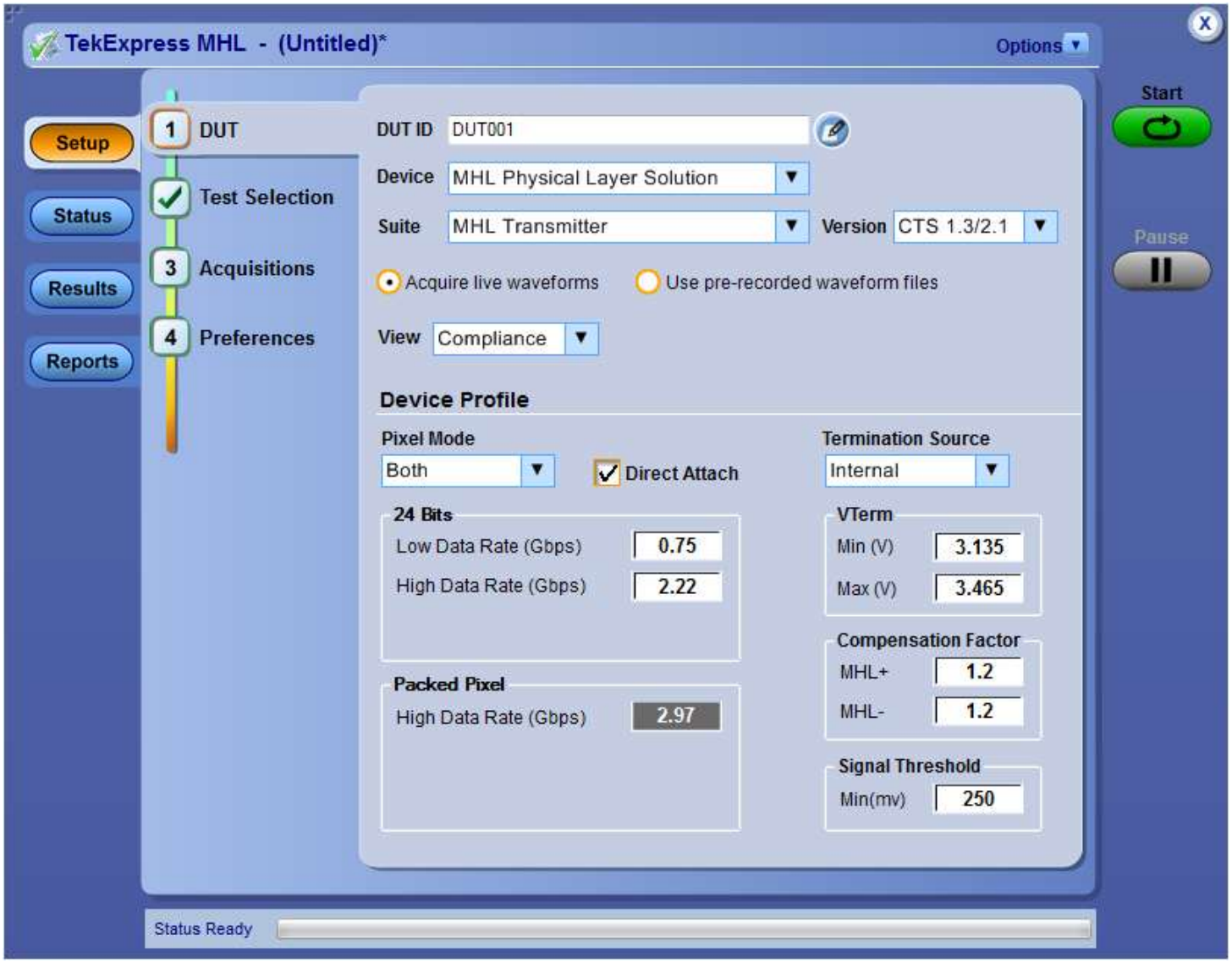
# Tektronix MHL 2.1 Tx Solution with Direct Attach test support



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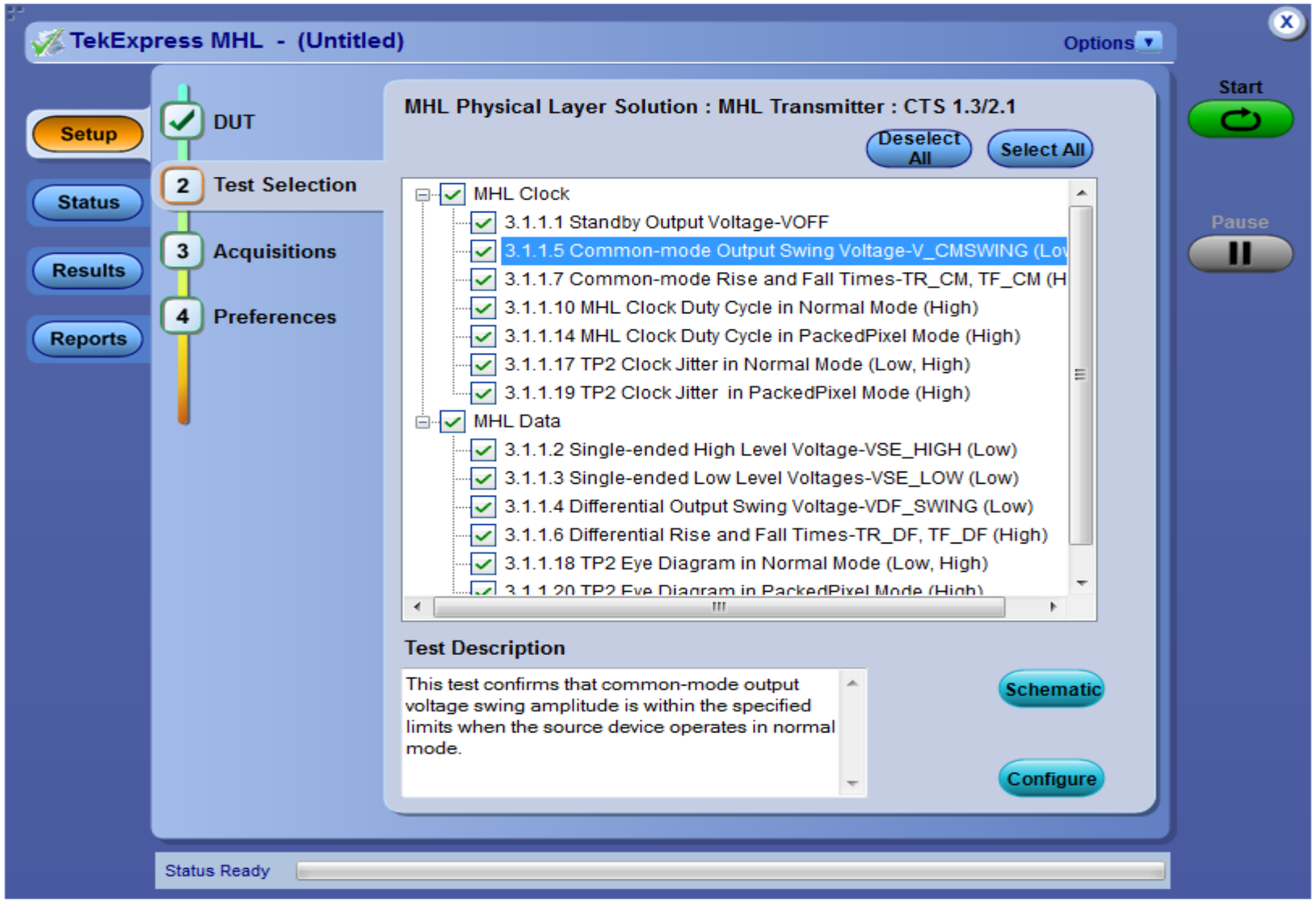
# MHL 2.1 Compliance Software for Automated Tx Tests: Option MHD



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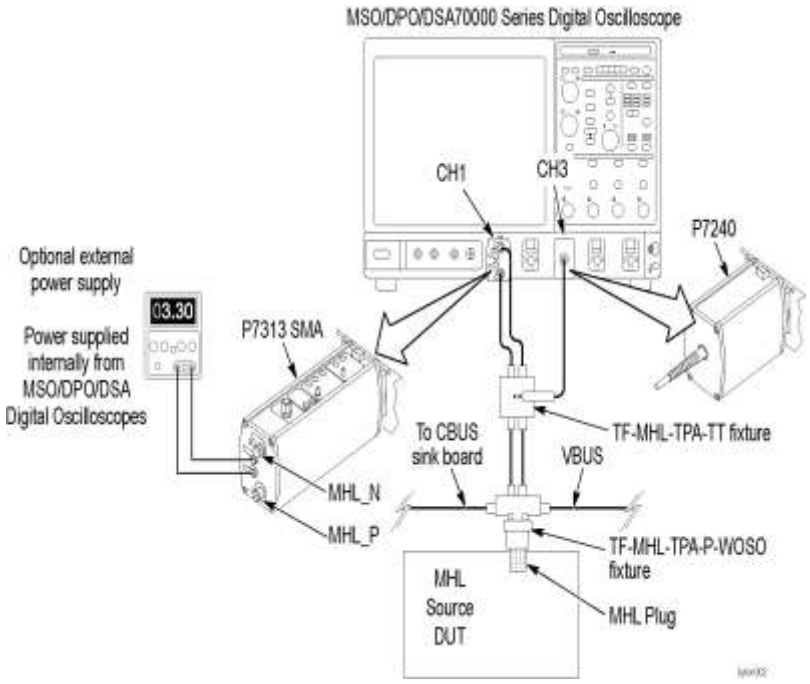
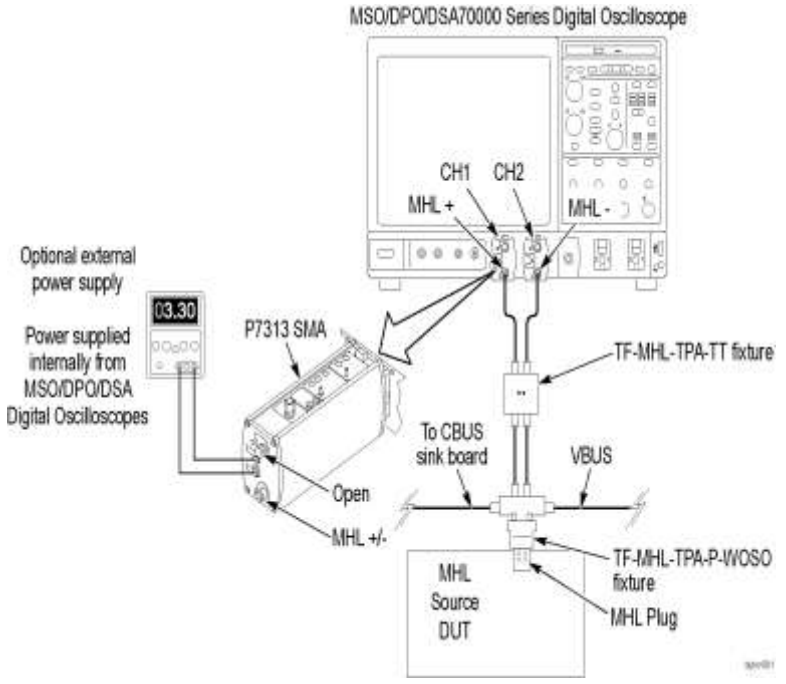
# Tektronix MHL Tx Setup




**MHL Differential and CM Test Setup**
**6 tests**




**Single Ended and Intra Pair Skew Test Setup**
**6Tests**

**Also same setup is used for MHL Protocol Testing**

** C-Bus Sink and Source Board is needed for hand shaking and is available from Tektronix



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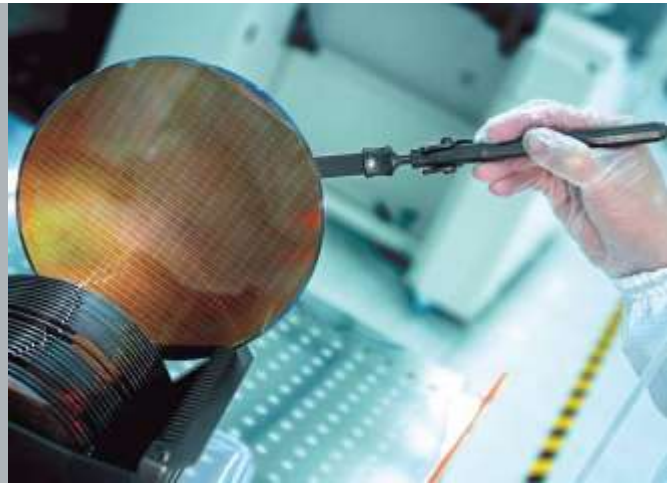
# Tektronix MHL 2.1 Solution

- DPO/DSA/MSO 70804B/C Series Real Time Oscilloscope with BW ≥ 8GHz
- MHL Compliance Software – Option MHD
- Innovative MHL Protocol Software from Third party – TEK-PGY-MHL-PA-SW
- Probes – P7313SMA  (two) and P7240 (one)
- MHL Test Fixture including Direct Attach Fixture – Available from Tektronix.
- AWG7122C with Opt 01,02 or 06 and 08 for the innovative direct Synthesis based MHL Rx/Dongle testing.
- C-Bus Sink and Source board is needed and is available from Tektronix
- DSA8200 or Equivalent with 80E03/80E04 and I-Connect Software for MHL cable testing ( performed manually using MOIs)

Please contact  local Tektronix account managers for further details.

# Innovative MHL Protocol Analyzer Solution

## Introducing Tektronix' MHL Protocol Solution



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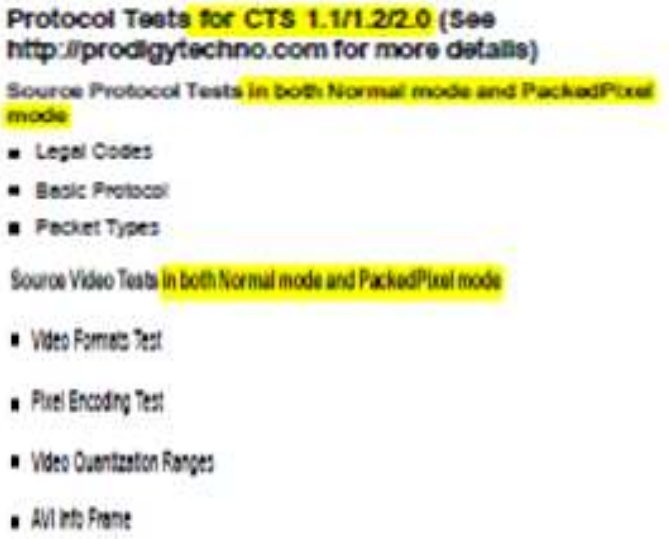
# Tektronix MHL Protocol Analysis Solution

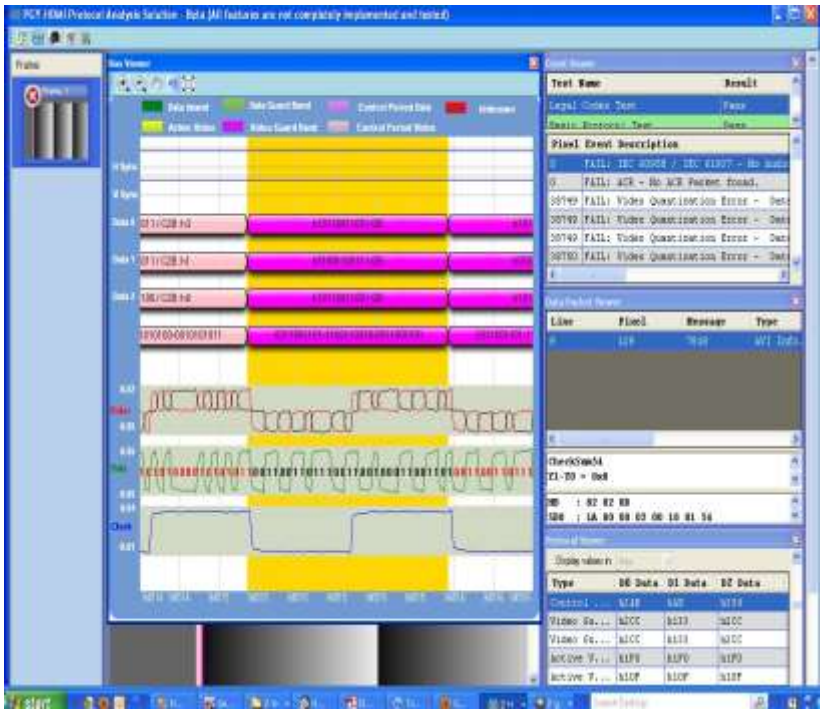
- MHL Protocol Analysis software running on the Tektronix REAL TIME Oscilloscope
  - Unique value proposition as the same real time scope is used for both Physical layer testing and Protocol testing.
  - Gives the seamless transition from Phy layer to Protocol.
  - Cost effective solution.
- Features
  - Multi View support
    - Bus Analysis
    - Frame Viewer
    - Event Viewer
    - Protocol Viewer
    - Linked to the analog waveform
- Tektronix Nomenclature – TEK-PGY-MHL-PA-SW



# Tektronix MHL Protocol Analyzer: Seamless PHY and Link Layer Testing


**SELECT**


**CONFIGURE**



**MULTI VIEW**

**BUS ANALYSIS-Physical Layer to Link Layer**


**REPORT**



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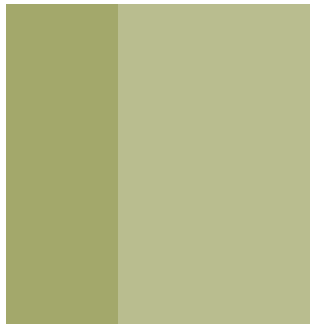
# Tektronix MHL Receiver Solution - Electrical and Protocol tests



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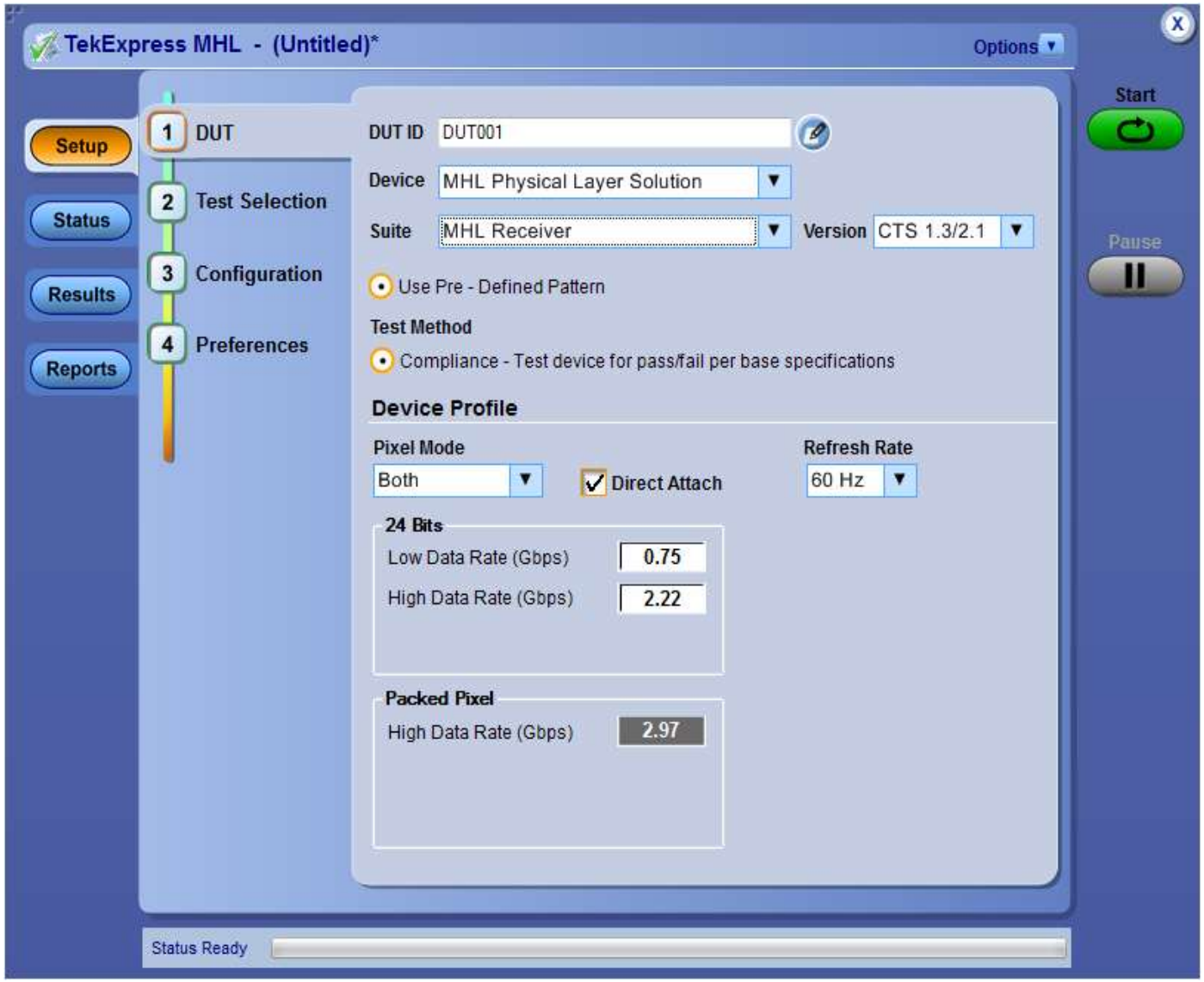
# Tektronix MHL 2.1 Rx Solution with Direct Attach Test Support



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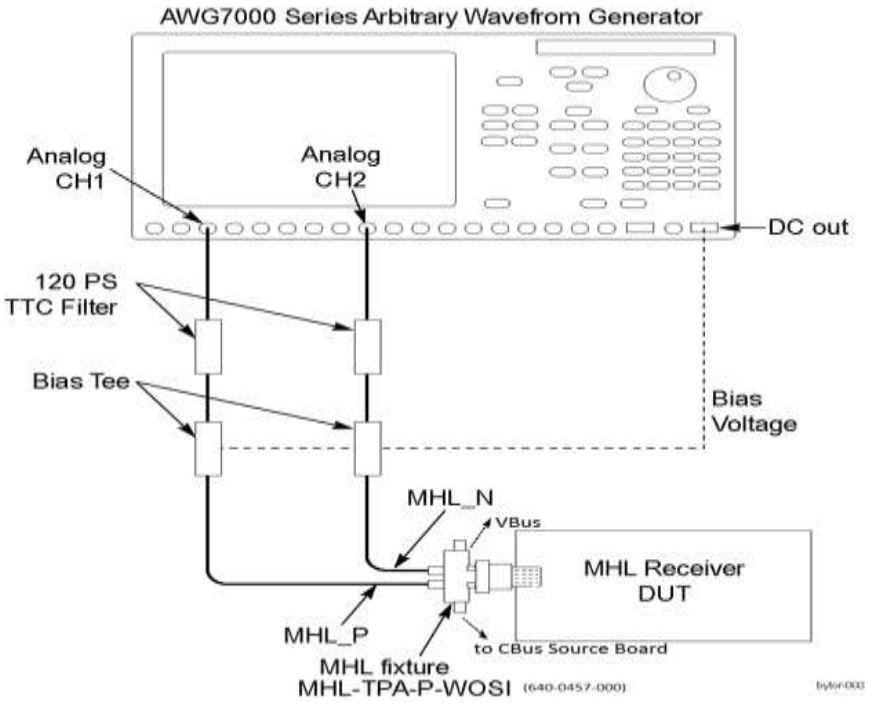
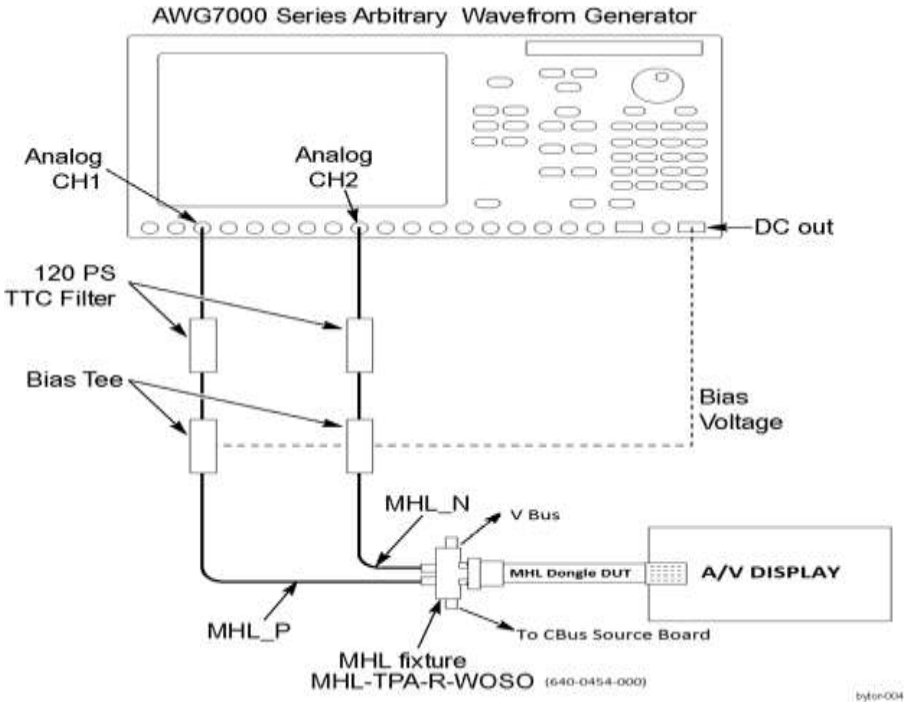
# Tektronix MHL Solution Setup: Simple and Easy Sink and Dongle Testing (all tests except Min/Max test)-1

Setup based on Direct Synthesis Capability of AWG7122C Series

**Test Setup for Sink Tests**




**Test Setup for Dongle Tests**



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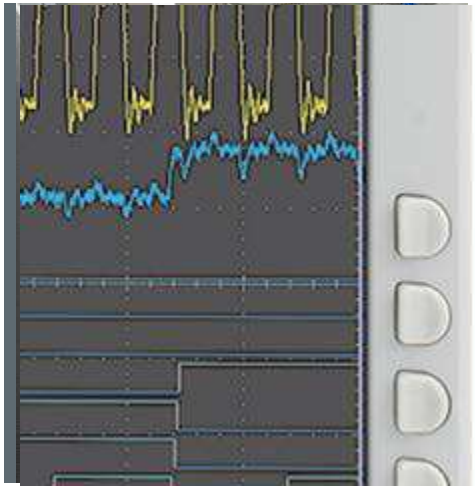
# DisplayPort Solutions-Customer Presentation

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# DisplayPort – Technology Overview

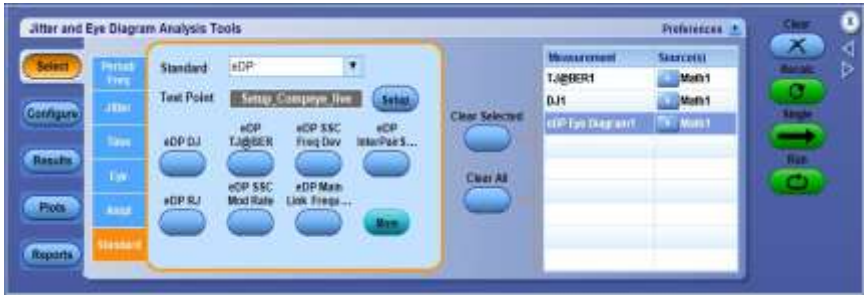
DisplayPort is expanding its foot print

- Standard DisplayPort
  - Specification Version 1.2
  - CTS Version 1.2b
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Box to Box ( 1, 2, 4 lanes)
- eDP
  - Specification Version 1.4
  - CTG in progress
  - Data Rates 1.62Gbps to 5.4Gbps
  - Embedded(single box – Laptops) (1,2,4 lanes)
- MyDP
  - Specification Version 1.0
  - CTS Version 1.0 (in approval)
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Mobiles ( 1 lane)
- iDP
  - Specification Version 1.1
  - CTG
  - Data Rates 3.24 , 3.78
  - LVDS replacement

# Embedded Display Port-eDP

Option EDP is designed to provide component and system designers with a comprehensive verification and debug solution the latest Embedded DisplayPort Specification 1.4.

Using the familiar DPOJET look and feel the user can select the setup based on their specific measurements requirements. In addition, as the 1.4 specification allows the data rate to be anywhere within a range of speeds from RBR to HBR2 rates opt EDP will provide the dynamic mask generation required to ensure proper testing







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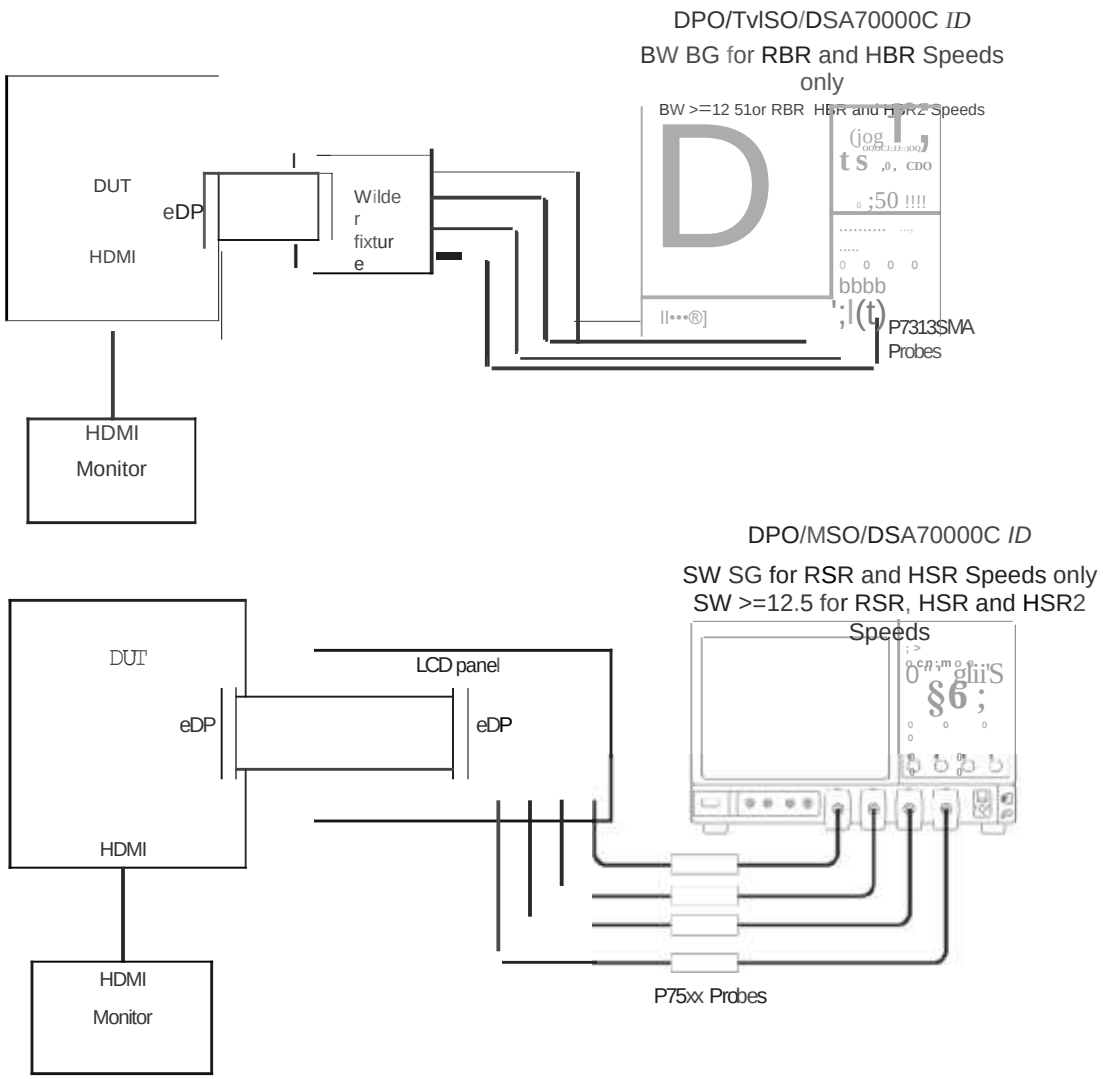
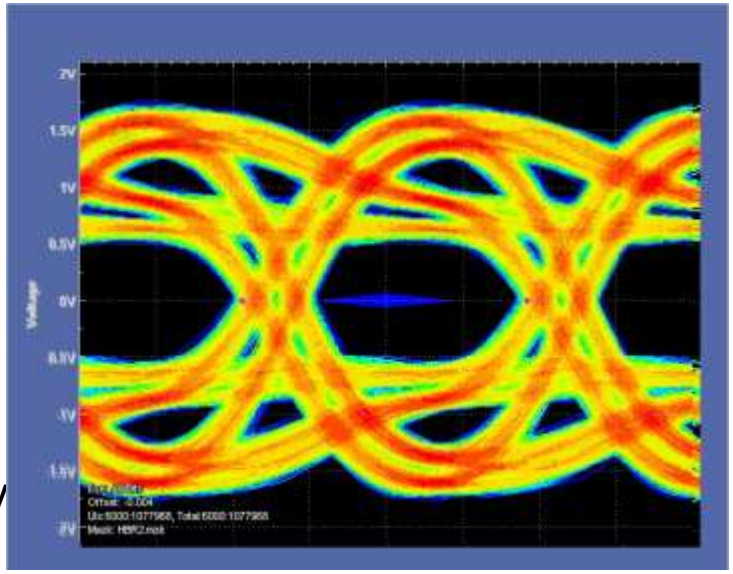
# Embedded Display Port-eDP Typical connection



# Embedded Display Port-eDP

**eDP source measurements:**

Test 3.1 - Eye Diagram Test
Test 3.2 - Inter Pair Skew test
Test 3.3 - Non-ISI Jitter Measurements
Test 3.4 - Total Jitter
Test 3.5 - Deterministic jitter
Test 3.6 - Random Jitter
Test 3.7 - Main Link Frequency Stability
Test 3.8 - Spread Spectrum Modulation Frequency
Test 3.9 - Spread Spectrum Modulation Deviation



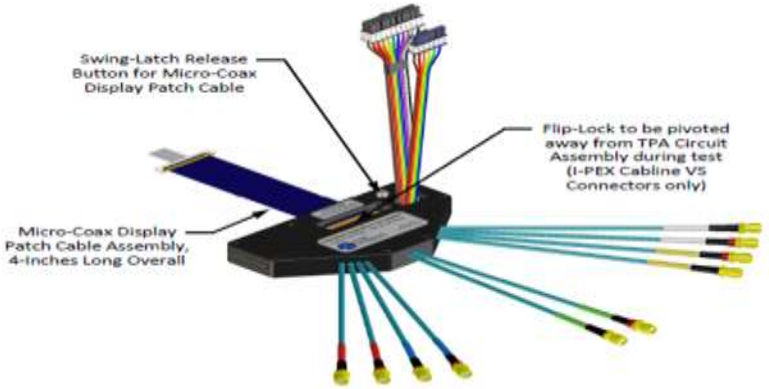
# Embedded Display Port-eDP

**Oscilloscope Requirements**

- Option EDP requires a DPO/DSA/MSO 70K scope running firmware version
- 6.4.0 or higher and DPOJet version 6.0 or higher.
- For customers testing RBR (1.62 Gb/sec) and HBR (2.7 Gb/sec) a minimum bandwidth of 8Ghz is required.
- For customers testing HBR2 (5.4 Gb/sec) a minimum 12.5GHz BW is required.

**Probing**

- For customers testing RBR (1.62 Gb/sec) or HBR (2.7 Gb/sec) Qty 4 P7380 or P7380SMA are required if testing more then two lanes at one time.
- For customers testing HBR2 (5.4 Gb/sec) and HBR (2.7 Gb/sec) and RBR
- (1.62 Gb/sec) Qty 4 P7313 or P7313MA are required if testing more then two lanes at one time.
- An optional eDP fixture is available on the Tektronix PAL:TF-EDP-TPA-PRC



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