BERTScope™

Combating Closed Eyes – Design & Measurement of Pre-Emphasis and Equalization for Lossy Channels

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Why Test the Receiver?

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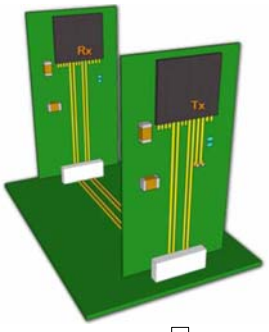
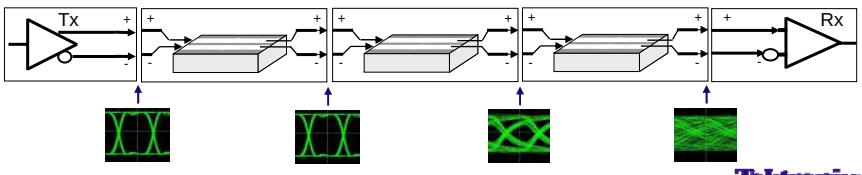
- Serial Data communications standards have always specified both the **transmitter** and **receiver** physical layer characteristics
- Historically receivers have not been tested in compliance workshops except in communication standards
- *Why?*
  - Receiver testing was perceived as “difficult”
    - In reality – not familiar
    - Testing requires different instruments
    - Test set up requires “calibration” before use.
  - There was enough margin to assure system testing covered through transmitter test and interoperability





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Why Receiver Testing is Different

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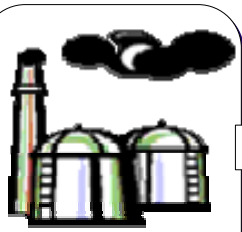
Receivers

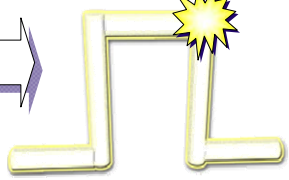
Poor quality bits in….

"Receiver", "Re-Timer"
"Decision Circuit", "SERDES"



Receiver

Pristine bits out…



- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance…. ….the eye shape only tells how nice the output stage is.

Bright… Shiny… New…

Wrong?

Receivers are Tested with BER

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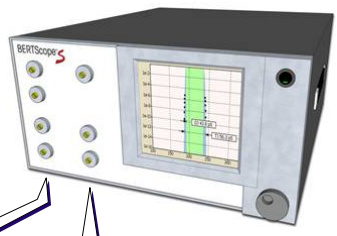
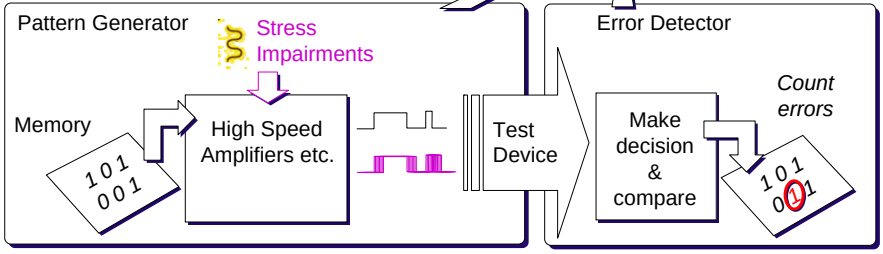
Introducing the BERT

BERTScope™

- The Bit Error Ratio Tester is the basic instrument used for receiver testing.
- The BERT is comprised of two main components
  - Pattern Generator
  - Error Detector





(Sometimes device being tested contains built in PG & ED, but not usually stress)

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Creating the Stressed Signal

Dynamically Change Data Rate, Stress, Pattern

1 Clock *Drives Data Rate*

2 Stress Modulator *Applies Stress (SJ, RJ, BUJ)*

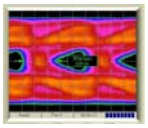
Data Rate, Applied Stress, and Data Pattern can be changed on the fly, *independent* of each other. *Changes happen instantly.*

Easy adjust with turn of the knob

Easy adjust with turn of the knob

3 Data Pattern *Choose PRBS or User Pattern*

Stressed Data



Two clicks changes data pattern, including PRBS-31

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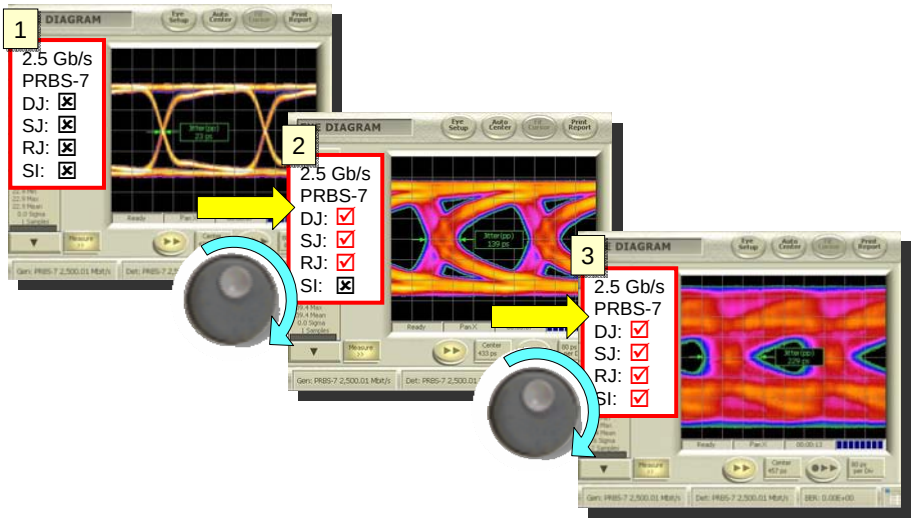
Creating the Stressed Signal

Dynamically change Data Rate, Stress, Pattern



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Stressed Receiver Tolerance Testing

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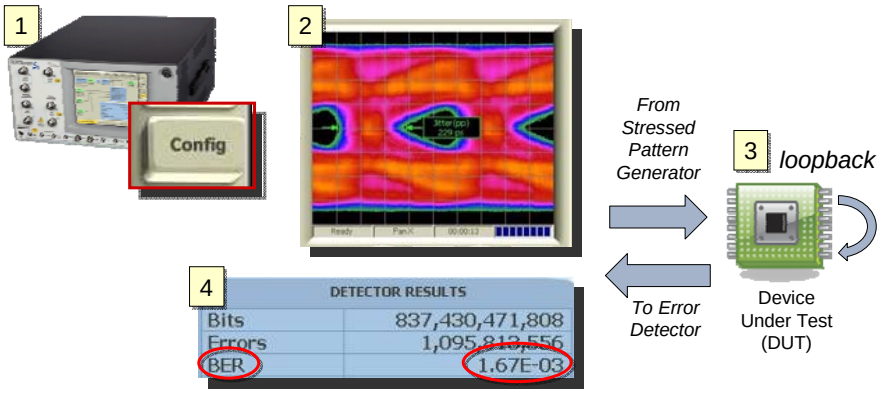
Start Testing Quickly



1. Recall stressed eye configuration
2. Apply stressed eye signal to DUT's receiver
3. DUT loops received bits back to BERTScope Error Detector
4. BERTScope counts any errors

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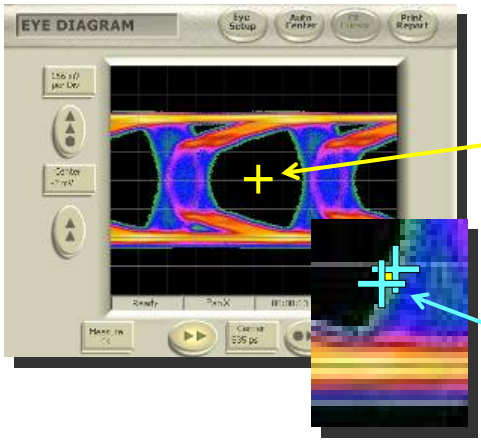
BER-Based Analysis

BERTScope™

Deep Insight with the BERTScope Toolkit

The BERTScope Eye Diagram



1. With one sampler, we can compare bits coming in to the expected pattern of bits in memory -> BER measurement

2. With two samplers, we can measure how many traces fall between the two samplers –> eye diagram!

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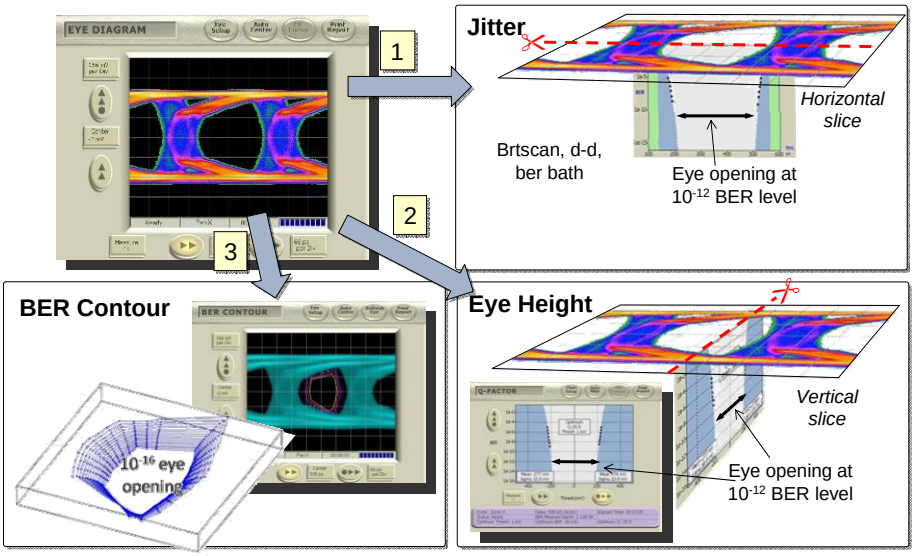
BER-Based Analysis

Deep Insight with the BERTScope Toolkit



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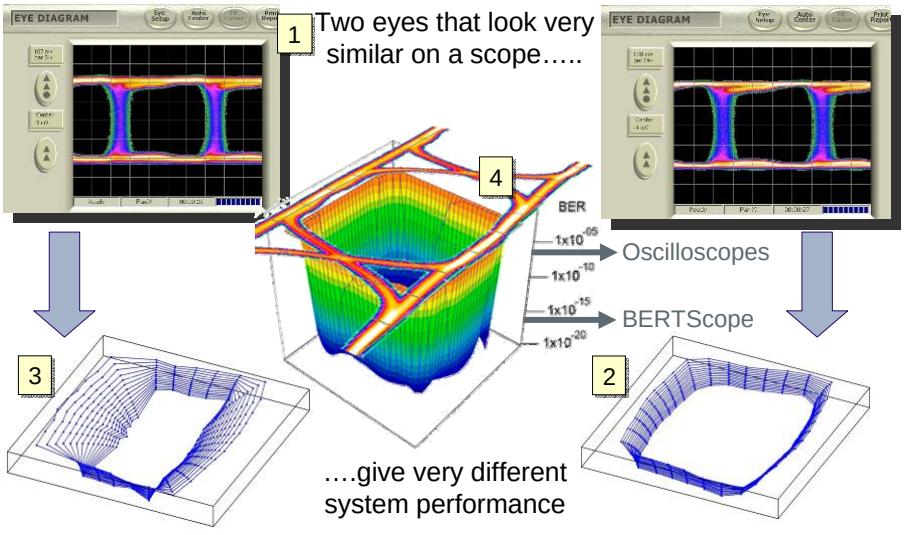
BERTScope Depth of Measurement

Deeper Insight



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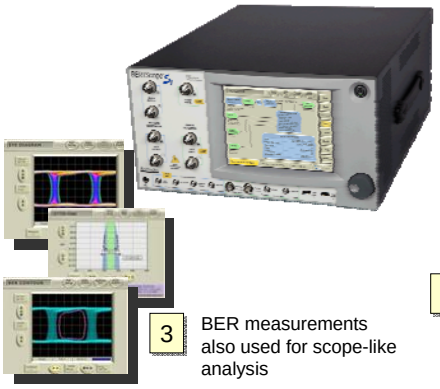
What is a BERTScope?

A Combination BERT and Scope for Computer Bus and Communications Serial Data Applications

1 Pattern Generator (with optional Stress) sends bits, e.g. a PRBS pattern

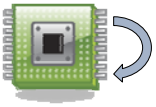


3 BER measurements also used for scope-like analysis

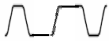
A Typical Receiver Test Setup

From Stressed Pattern Generator

loopback



To Error Detector



Device Under Test (DUT)

2 Bits come back from DUT to Error Detector and compared to expected pattern for Bit Error Ratio (BER) measurement.

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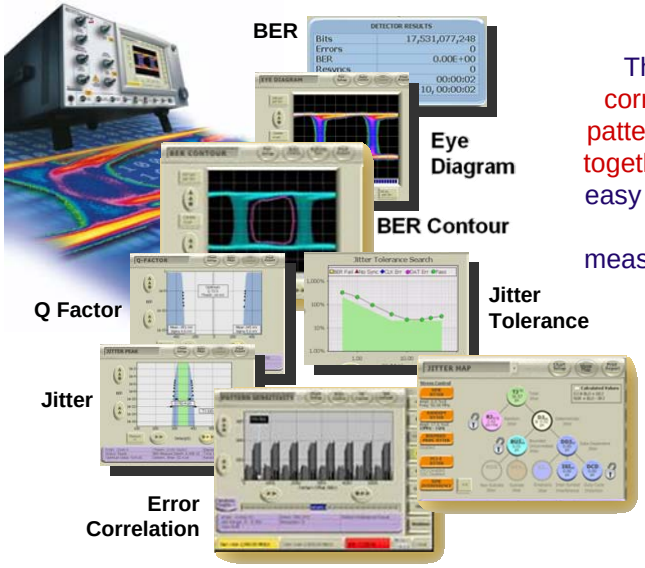
Easy Transition from Test to Debug

The BERTScope Toolkit



The BERTScope correlates eye, jitter, pattern, bit error effects together in a way that is easy to understand and with depth of measurement unique to BERTs.

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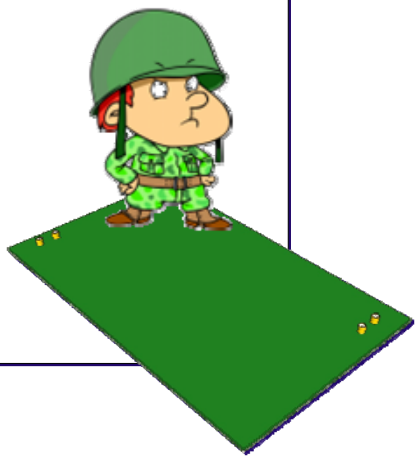
BERTScope

Agenda

- So What's the Problem?
- What Can Happen to Data?
- Measuring Insertion Loss
- Methods of Compensation
- Impulse Responses & FIRs
- PCIe Pre-Emphasis Example
- Designs of Equalization
- Summary



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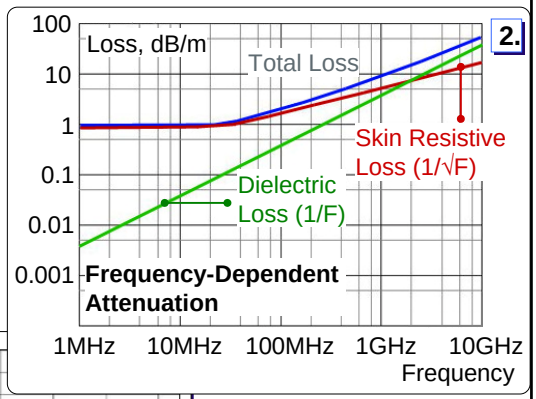
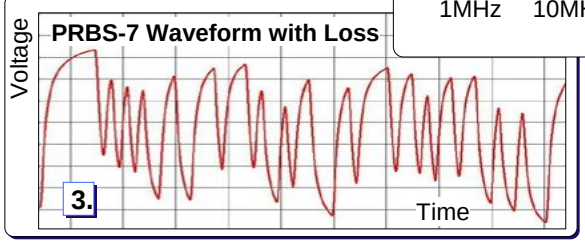
Pre-Emphasis & Equalization… What's the Big Deal?

- Higher data rates, longer distances, cheaper materials are a recipe for trouble **1.**
- Bandwidth limitations are caused by frequency - dependent losses in all types of media
  - E.g. 40" of FR-4 Material





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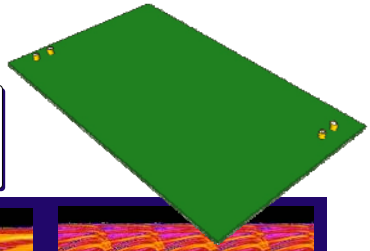
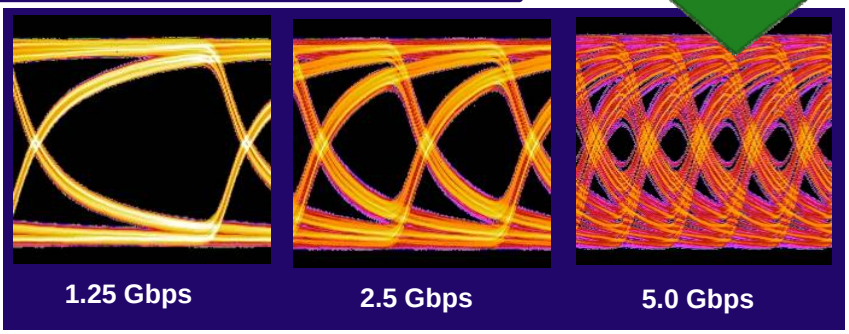
Impact of Bandwidth Limitations



- Bandwidth limitations create inter-symbol interference which eventually limit the ability to distinguish one bit from another



Noise/jitter closes-down the available headroom in the eye opening

Measured eye diagrams from a 40" PCI-Compliance ISI Trace, PRBS-7 Pattern

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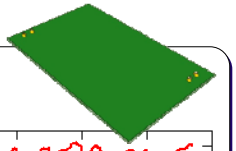
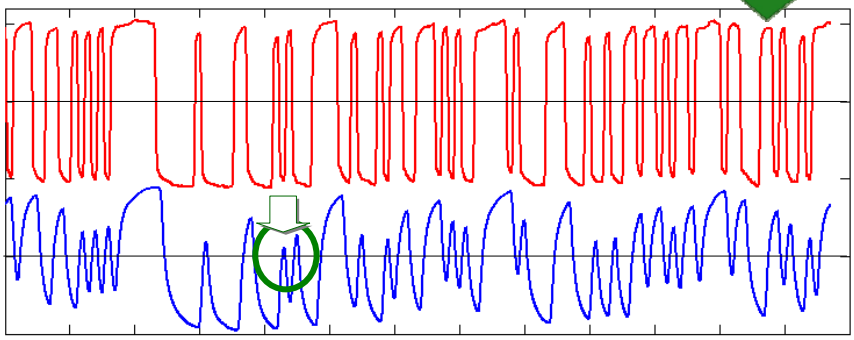
What Happens to Data?



- Using a 40" PCI-Compliance ISI channel at 5Gbps, PRBS data is significantly distorted



- Baseline wander follows consecutive bits in the bit pattern
- Certain bit patterns cause the worst opening
  - These will have high bit error rates

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Channel Loss Causes Bit Errors
Pattern Dependent

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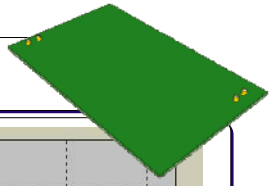
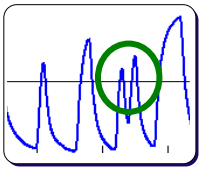
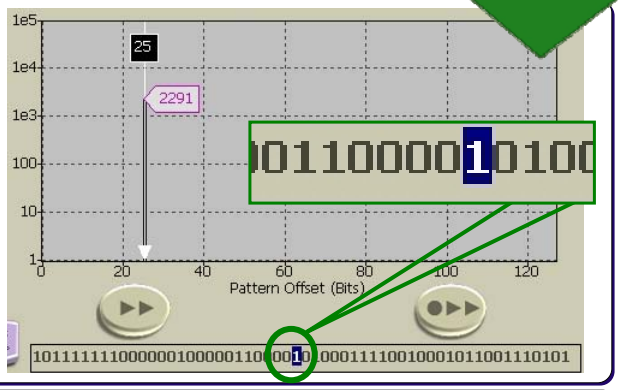
- In these types of channels, we can study bit error locations in the received pattern…







Measurement of Pattern Sensitivity (to PRBS-7 Pattern)

- Here we have found 2,291 bit errors that all happened at this most-distorted bit in the PRBS pattern

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Loss Impact on Jitter Margin

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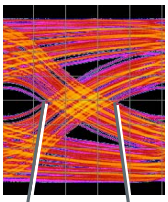
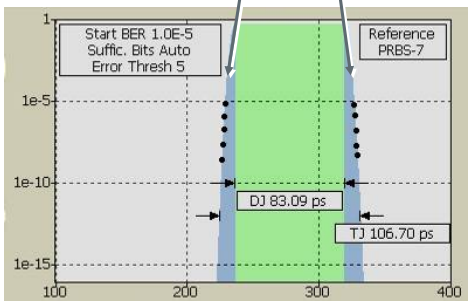
- ISI adds to Deterministic Jitter
- RJ remains close to the same
- This closes-down the eye…
  …and makes less margin
- At 5Gbps, 53% of eye is lost to jitter

We want to avoid this…





Measurement of Jitter Peak (BER Bathtub)

40” ISI Compliance Channel
5 Gbps, PRBS-7 pattern

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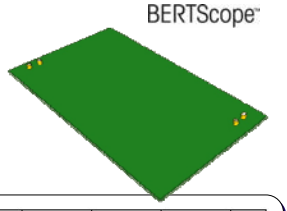
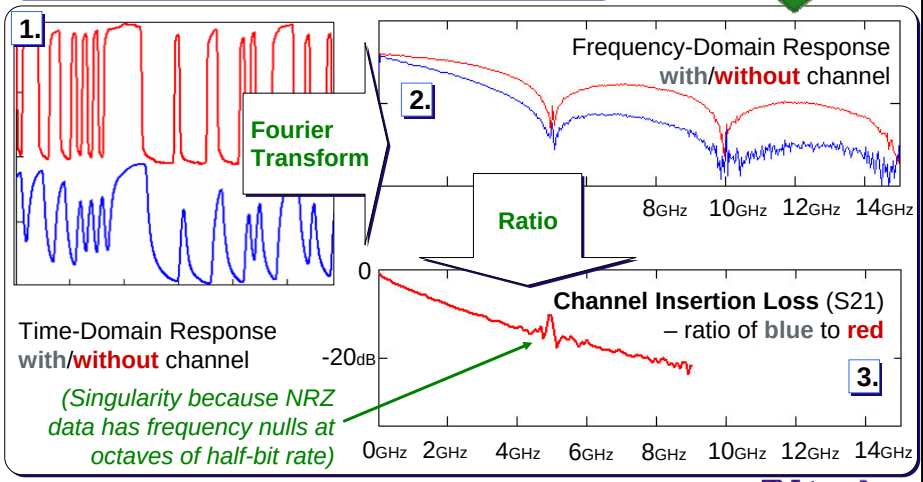
Insertion Loss of Channel

BERTScope™



- Its easy to measure channel insertion loss (S21) with PRBS data…



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Insertion Loss of Channel (continued)

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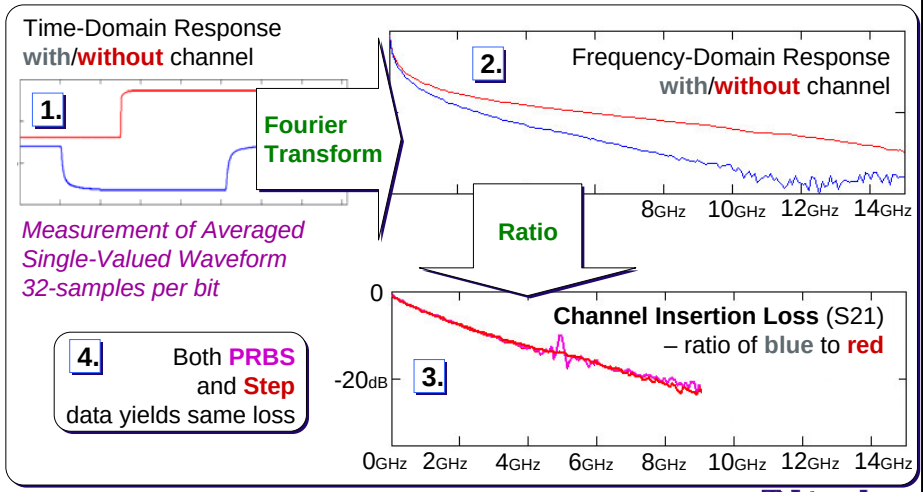
- Same can be done with a single step response…



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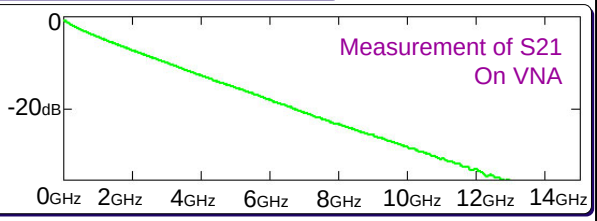
Insertion Loss Measurement Comparison

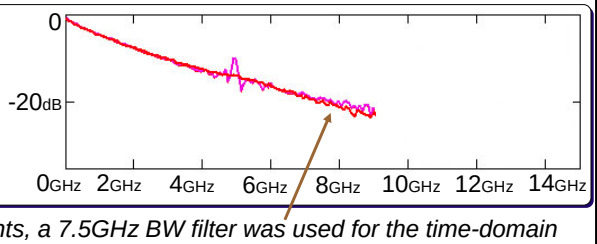
- A common but expensive way to measure insertion loss is with a Vector Network Analyzer (VNA)

1.



2.

Time-Domain
(BERTScope,
Sampling Oscilloscope)



(For all these PCIe experiments, a 7.5GHz BW filter was used for the time-domain captures, removing this filter increases S21 measurement range to >20GHz)

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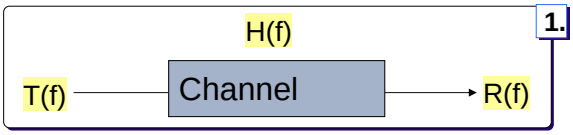
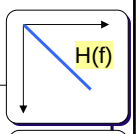
How Could You Correct For This?
Linear Signal Processing

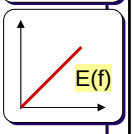
Eq BERTScope™

1.



2.





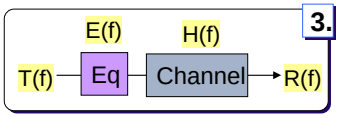
T(f) * H(f) = R(f)

Adding another filter, E(f) (equalizer) to the chain, we have

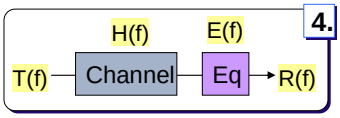
T(f) * H(f) * E(f) = R(f)

So, if E(f) = 1/H(f), then R(f) = T(f) – the ideal condition

3.

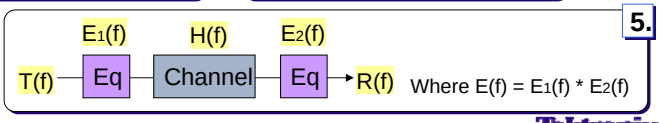


4.



Or even,

5.



Where E(f) = $E_1(f) * E_2(f)$

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Why Choose One Architecture Over Another?

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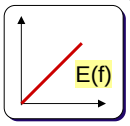
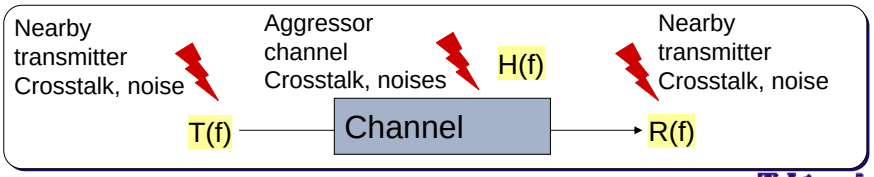
- Channels have **high frequency loss**
  - so equalizers must have **high frequency gain**
- Equalizers therefore amplify high frequencies
- This **amplifies noise** as well as signal
- **Noise is added** by cross-talk, processing physics or noise interference at transmitters, receivers or channels
- Pre-emphasizing a transmitter **avoids noises** induced to the channel or receiver from being amplified
- In **dynamic** systems, a receiver is required to **estimate** how much equalization is required which can motivate **receiver-based equalization**
- **Different architectures imply different IC space/power requirements**





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Synthesizing the Equalization Filter

Time-domain or Frequency domain

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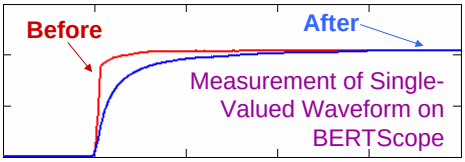
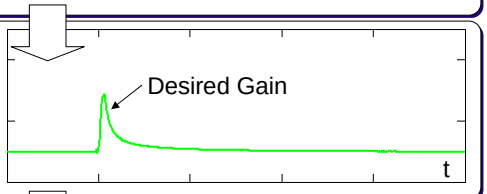
Time-Domain

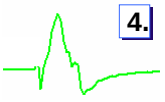
1. High-frequencies found in step transitions must be exaggerated



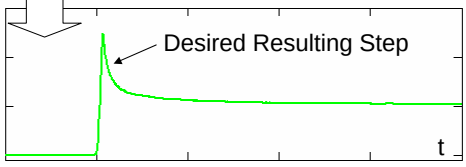
2. This amount of Gain needs to be applied to a step…



4. dGain/dt is the impulse response of the required filter



3. The resulting step response is required to pass through the channel unharmed



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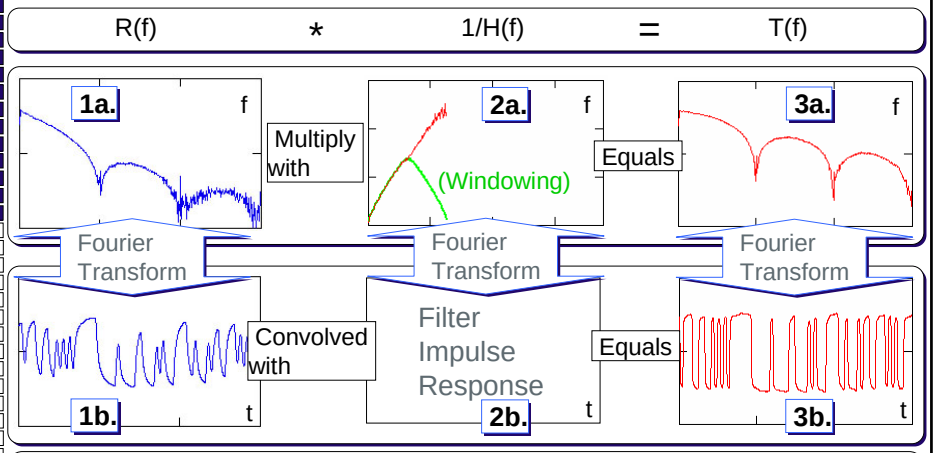
Synthesizing the Equalization

Time-domain or Frequency domain (continued)

BERTScope



Filter response can be found by either transforming the inverse channel or by Deconvolving the time responses

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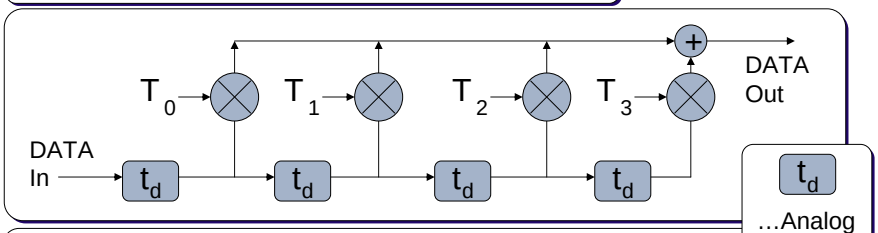
Finite Impulse Response (FIR) Filters

BERTScope

- **Linear** Implementation that offers flat phase response



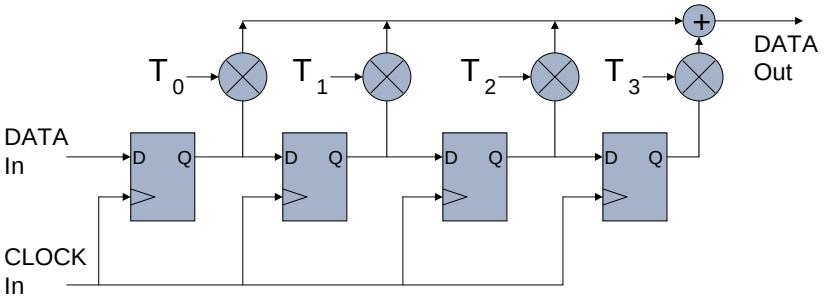
- This circuit performs a **convolution** of **Data-In** with **Taps-heights**
- An impulse in, yields tap-heights spaced by t_d out
  - **Tap-heights**, therefore, are **set to be the impulse response**
- **A step in**, yields an **integration of the Tap-heights out**
- Any number of taps can be used to generate any length of impulse response
  - But **creating analog delays** can be **troublesome**

Tektronix

Digital Finite Impulse Response (FIR) Filters

BERTScope

- A clock is required and only digital 1's and 0's are processed



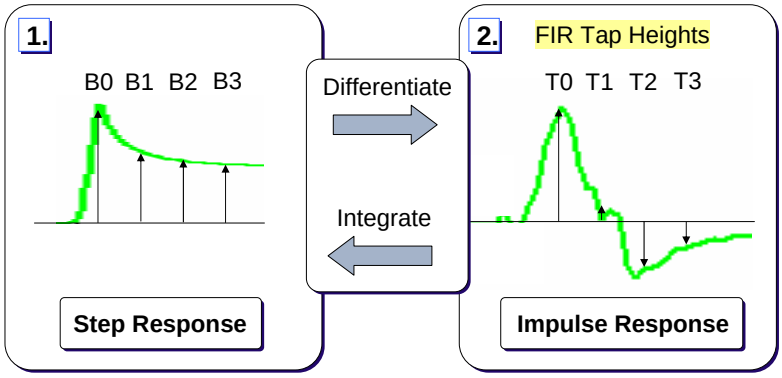
- Again, flat phase response
- Again, **Tap-heights** are set to the **impulse response desired**
- **Delays** elements implemented with clocking input
  - This **tracks data rate**

Tektronix

Desired Synthesized Response to an FIR
Need to Calculate Tap Heights

BERTScope

- After we've synthesized the desired step response, to use an FIR filter, we need to compute the tap heights



Tektronix

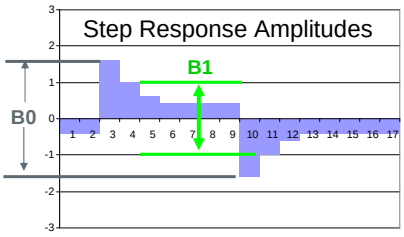
Relating Tap-Heights to Step Responses

BERTScope™

Digital FIR's only need simple addition/subtraction

Calculate Tap Heights from Step Amplitudes

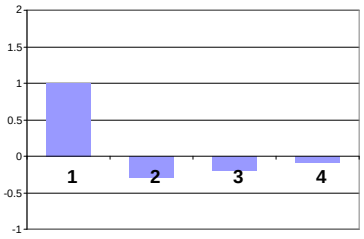
1.



T0	1		=(B0+B3)/4
T1	-0.3		=(B1-B0)/4
T2	-0.2		=(B2-B1)/4
T3	-0.1		=(B3-B2)/4

2.

Calculate Bit Amplitudes from Tap Heights



B0 Ampl	3.2	units	=2*(T0-T1-T2-T3)
B1 Ampl	2	units	=2*(T0+T1-T2-T3)
B2 Ampl	1.2	units	=2*(T0+T1+T2-T3)
B3 Ampl	0.8	units	=2*(T0+T1+T2+T3)

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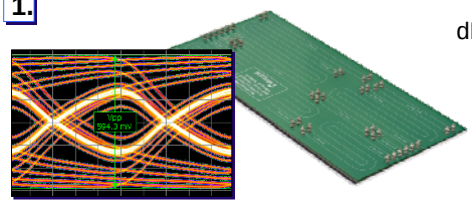
Relating to Gen2 PCIe Example

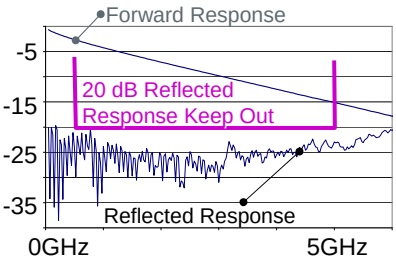
BERTScope™

5 Gbps over variable trace lengths

- The Compliance ISI channel is a 40" trace
  - Used to create 5:1 ratio of eye closure

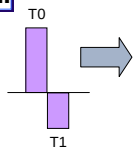
1.

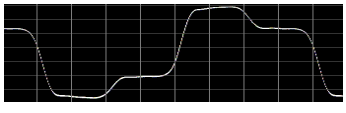


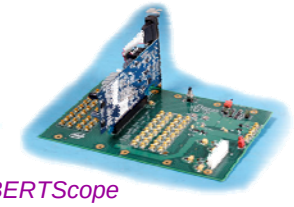


- 2-tap Pre-emphasis is used to compensate for losses

2. -3.5dB or –6dB [20*LOG(B0/B1)]







Measured Single Valued Waveform on BERTScope

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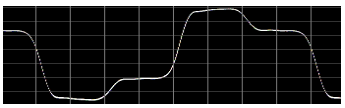
BERTScope™

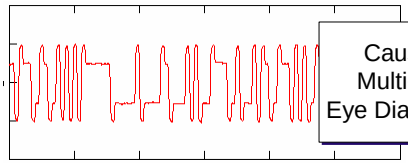
PCIe Eye Diagram

2-Tap –6dB Pre-emphasis



1.

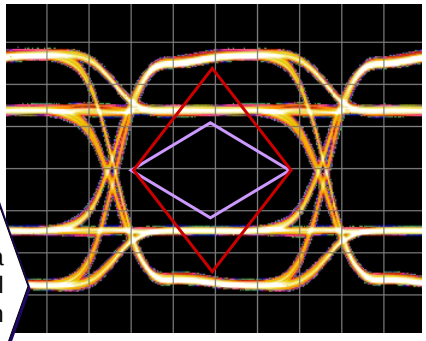
Applied to PRBS Data



Causes a Multi-level Eye Diagram

2.

3. Measurement of Eye Mask Testing On BERTScope



This complicates Tx mask testing - 2 masks are needed

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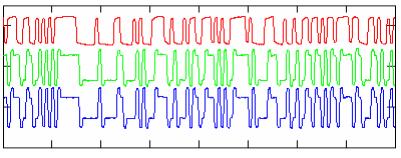
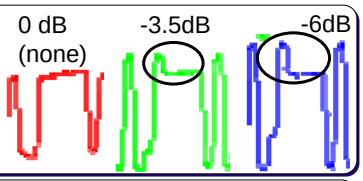
Impact of 2-tap Pre-Emphasis on PCIe Compliance Channel – Frequency Domain

BERTScope™

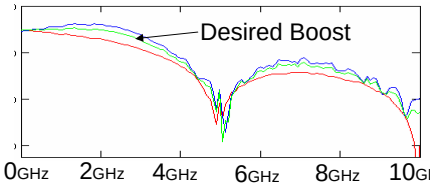
PRBS Time-Domain Response

1.





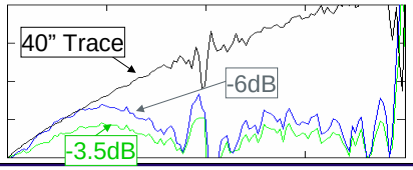
Freq. Content



2.

By taking ratios of frequency content of pre-emphasized data as compared to non-pre-emphasized data…

Pre-Emphasis Gain



3.

…we can see what frequency boost is accomplished and compare that to the inverse of the measured trace loss.
-6dB is required for this 40" trace

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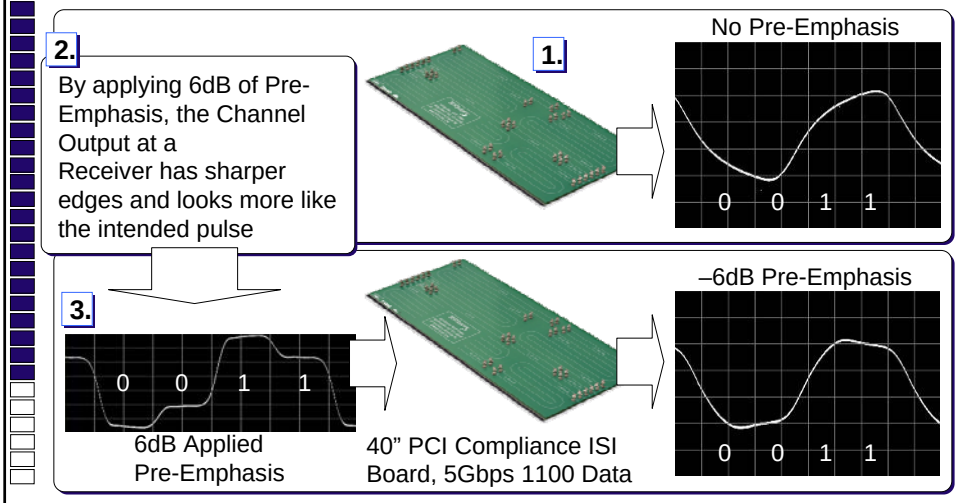
Impact on Pulses – Time Domain



Measurement of Single-Valued Waveforms On BERTScope

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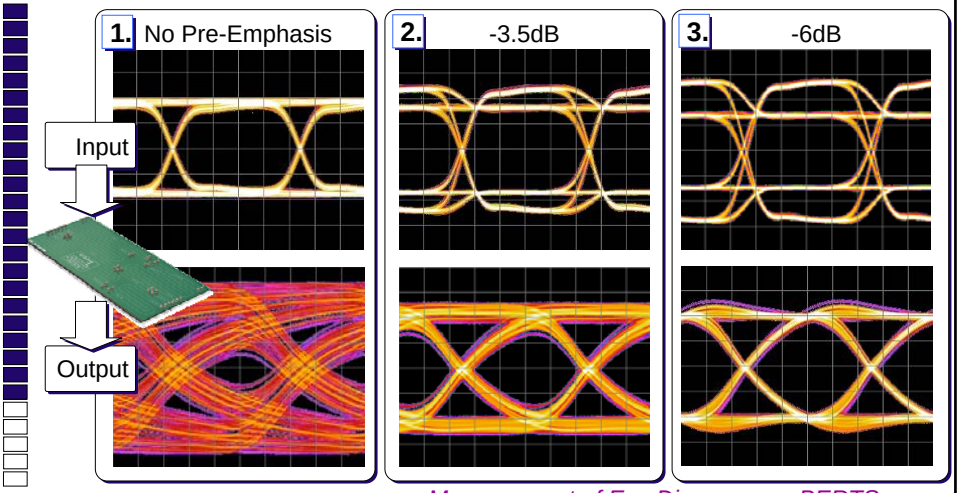
Pre-Emphasis Impact on Eye Diagrams



Measurement of Eye Diagrams on BERTScope

40" PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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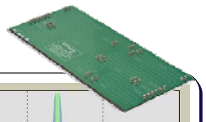
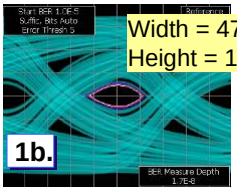
Pre-Emphasis
Impact on BER and Eye Margin

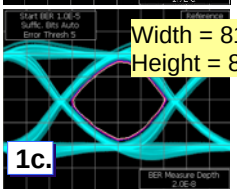
BERTScope



Eye Opening 1.
(BER Contour Measurement)

Measurements on BERTScope





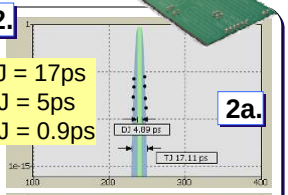
No Channel a.

40” Trace, no Pre-Emphasis b.

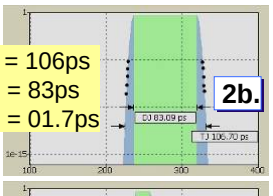
40” Trace, 6dB Pre-Emphasis c.

Jitter Peak 2.
(Bathtub)

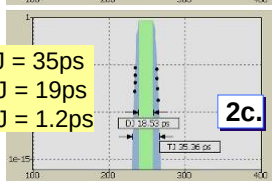
TJ = 17ps
DJ = 5ps
RJ = 0.9ps
2a.



TJ = 106ps
DJ = 83ps
RJ = 01.7ps
2b.



TJ = 35ps
DJ = 19ps
RJ = 1.2ps
2c.



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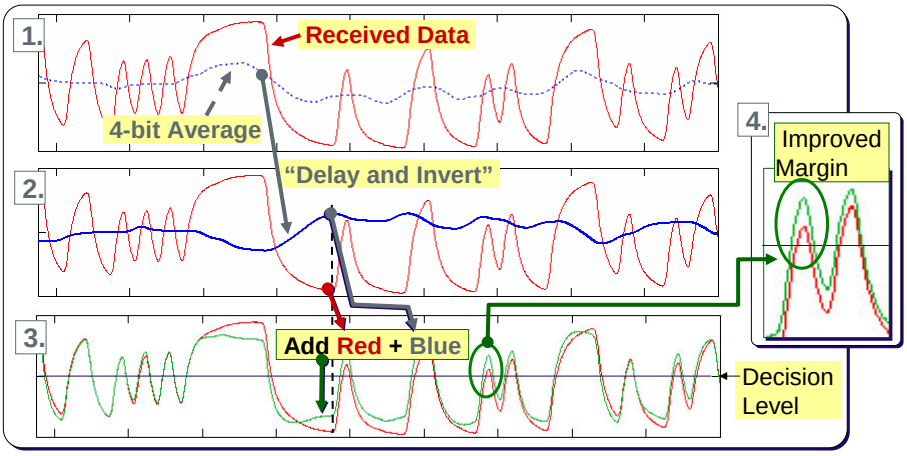
Decision Feedback Equalization
Effectively further open the eye

BERTScope

Correct baseline wander of received data stream by subtracting-off a portion of recent history



40” PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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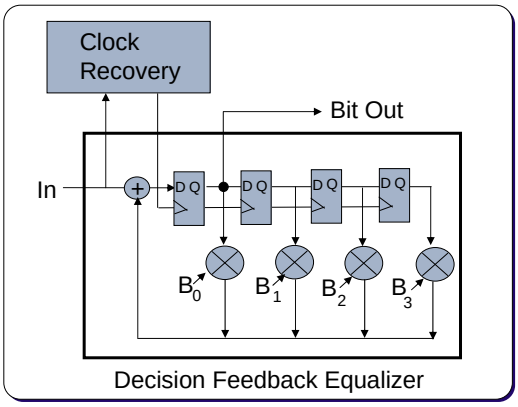
Decision Feedback Equalization
Block Diagram

BERTScope



- Clock recovery is required for the DFE to operate
- More or Less flip-flops can be used
  - This varies the amount of equalization

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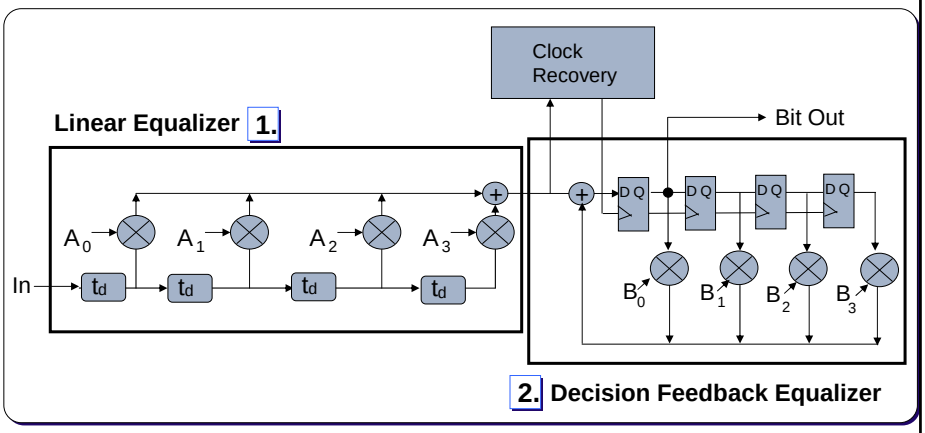
High-End Receiver-Side Equalization
Block Diagram

BERTScope



- Implements a 4 tap linear equalizer with a 4 tap DFE

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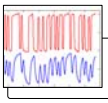
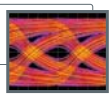
Conclusion

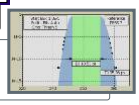
- Channel Losses can be **overcome** using a combination of **Pre-Compensation** and/or **Equalization** to reverse the channel impact
- Many **time-domain** and **frequency-domain** **measurements** are used when studying equalization and channel losses



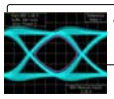
a. **Eye Diagrams:** Bandwidth, Low Jitter



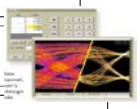
Single-Valued Waveforms: Sample resolution, # of samples b.



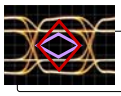
c. **Jitter Peaks (BER Bathtub):** Real BER measurement, time resolution



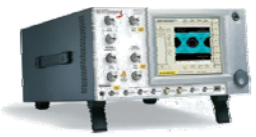
BER Contour: Speed of measurement, time/threshold resolution d.



e. **PatternVu :** Continuous Time Linear Equalizer



Eye Mask Testing: Depth of measurement, sub-rate triggers f.



All these measurements were made with BERTScope

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BERTScope™

Product Summary

BERTScope
- Main product
- BERT & Scope
- Serial & Communications

- ☑ 26G
- ☑ 17.5G
- ☑ 12.5G
- ☑ 8.5G

Clock Recovery
- Used with BERTs & Scopes
- Jitter measurement

- ☑ 28.6G
- ☑ 17.5G
- ☑ 12.5G

Pre-Emphasis
- Add-on to BERTScope Generator
- Boost output to overcome loss

- ☑ 12.5G

Bitanalyzer
- Basic BERT & Scope

- ☑ 1.5G/1.6G

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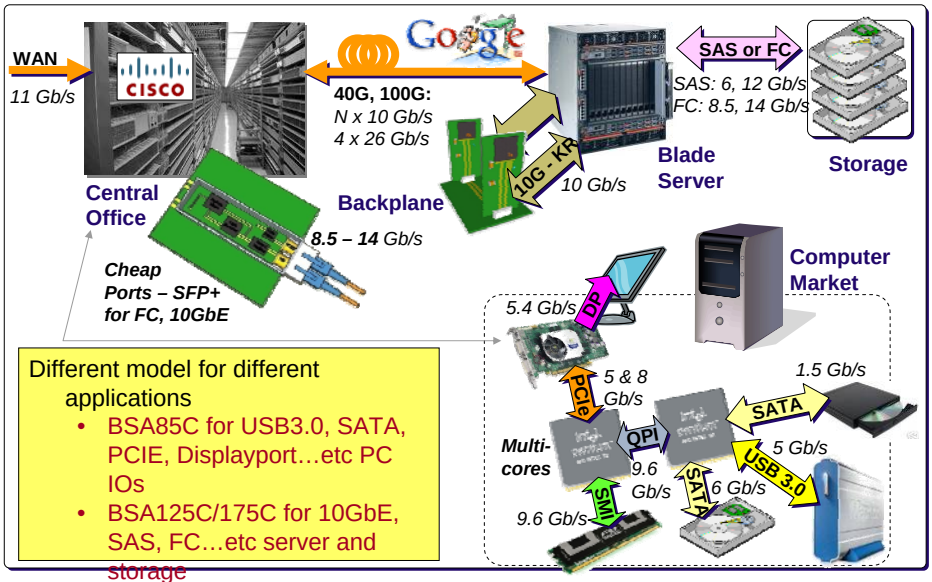
BERTScope

BERTScope's Applications In High Speed Serial Data



Different model for different applications

- BSA85C for USB3.0, SATA, PCIE, Displayport…etc PC IOs
- BSA125C/175C for 10GbE, SAS, FC…etc server and storage
- BSA260C for 40/100GbE

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Questions?

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Thank You

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