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Dual Channel Pulse Testing Simplifies RF Transistor Characterization

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Device engineers and test managers are under tremendous pressure to make sure products get to market quickly and perform reliably. This is especially true of RF transistors destined for hot communications market segments. Whether the technology is based on III-V compounds or LDMOS, RF transistor tests must accurately characterize design and performance – and do it cost effectively. Pulse I-V (PIV) testing is becoming indispensable in meeting these goals, because it avoids the negative effects of self-heating and transient trapped charges, which usually result in misleading data. (In the testing of compound semiconductors, dispersion is the terminology used to describe self-heating and carrier trapping – basically anything that causes DC test results to differ from pulse I-V test results.)

PIV Testing Overview

The rationale for PIV testing is better modeling of RF transistor behavior. PIV uses a pulse source to stimulate the transistor, followed by a corresponding pulse measurement. Since RF transistors are primarily used in applications where non-linear responses are the norm, such as switches and amplifiers, large signal analysis is typically the goal of PIV testing. The two main test methodologies are PIV sweeps and transient (single pulse) testing (***Figure 1***). By using a dual-channel pulse source-measure system, this type of testing is made simple and cost effective.

PIV sweeps produce results similar to familiar DC tests, such as a V_d-I_d family of curves under different bias conditions. This means the base of the pulses have a non-zero value for both gate and drain voltage, often referred to as the operating point or quiescent point (q-point). The technique in this type of testing is application of a low duty cycle pulse (typically <1%) to the device under test (DUT), which avoids self-heating and carrier trapping. As shown in the left view of ***Figure 1***, each point on the curve is the result of a pulse measurement made on the DUT during the settled or flat portion of the pulse. In practice, many pulse measurements are averaged to improve the quality of measurement results.

The second type of PIV testing is the transient or single pulse test (right view in ***Figure 1***). In this case, the test results are presented as a view of the measurement pulse, or an average of multiple pulses. The measured signal is plotted as the DUT's voltage or current versus time response, showing any time-varying changes, such as the onset of self-heating or charge trapping.

A wide range of pulse widths can be useful in PIV testing, depending on the device or material type and test parameters. For millisecond pulse widths, ordinary source-measure units (SMUs) can be used. However, shorter pulses (microseconds to nanoseconds) are generally more effective for avoiding self-heating and charge trapping effects. Therefore, short-pulse PIV testing of RF transistors generally allows the creation of more useful models.

Small Signal vs. Large Signal Testing

A useful dichotomy in describing RF transistor characterization is the distinction between small signal and large signal testing. Small signal (s-parameter) data is useful for accurately representing linear devices, such as cables, filters, connectors, and couplers, i.e., devices governed by Maxwell's equations, which are linear. This means that s-parameter extractions require linear responses to feed the modeling process. In

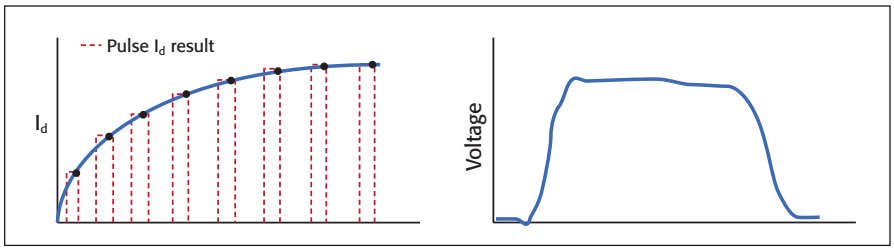

Figure 1. PIV methods: DC-like sweeps (left) and single-pulse transient testing (right).

contrast, RF transistors are primarily used in applications where non-linear responses are the norm, so large signal analysis is most useful.

There are a few different approaches to large signal analysis:

- Use of a Large Signal Network Analyzer (LSNA)
- Non-50Ω test environments
- PIV

LSNA is a method that extends the use of network analyzers into the large signal space. A consensus on the theoretical basis of this methodology is still being developed, and the present installed base is relatively small. In addition, there are challenges in using the hardware to create and control the large signals that are required.

Another methodology tests RF transistors in a non-50Ω environment, and there are two common approaches. The load pull approach varies the impedance at the output of the transistor (or other active device), then measures various performance parameters such as gain, compression, saturated power, efficiency, and linearity. The output load is varied across several areas of the Smith chart. The source pull method varies the impedance seen at the input of the transistor while measuring the desired parameters, such as signal-to-noise (SN) ratio.

PIV also permits the use of large signals and is fairly straightforward from a theoretical basis. The key advantage of pulse testing is the ability to leverage an extensive body of knowledge from DC modeling and analysis. In addition, it avoids self-heating in the DUT and charge carrier trapping effects.

In general, these different methodologies are not competitive. Frequently, multiple methods are used to better characterize a DUT's large signal response. In any case, the advantages of PIV testing are driving the increased use of this methodology.

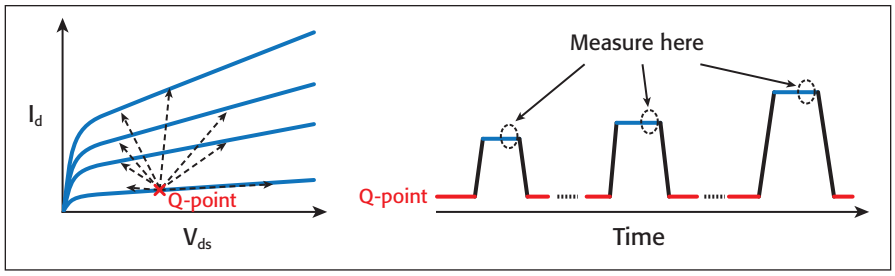

Figure 2. Two ways of looking at a non-zero bias point, i.e., quiescent point.

PIV Test Requirements and Challenges

PIV testing carries with it certain requirements in terms of test techniques and instrument capabilities. These include:

- Pulsing from a non-zero base or value (i.e., bias point/quiescent point/DC offset)
- Bias voltage pulsing of both the gate and drain
- Using scaled down test structures or devices, and lower power than the typical operating point for high-power RF transistors
- Use of a current sense resistor along with a software routine for load line compensation
- Software routine for cable and other interconnect compensation
- Tools to address system and device oscillation

Fortunately, there are commercially available instruments that provide all of these features.

Non-zero bias point sweeps. Also referred to as the quiescent point (q-point), a non-zero bias is illustrated by the diagrams in ***Figure 2***, which are based on PIV sweeps. The q-point is a non-zero value, shown as the red lines in the right diagram. This non-zero value, for both the gate and drain, results in a point in the V_d-I_d graph shown in the left view as the red X. The pulse waveform has a non-zero base, represented by the red features on both diagrams.

During an I-V sweep, the pulse height is varied as shown in the right diagram of ***Figure 2***. Measurements are made within the pulse as detailed by the black arrows on the right. Note that the measurements are also detailed in the left diagram, again shown as black arrows pointing towards the measurements and away from the q-point. This indicates that the device is returned to the q-point condition between every measurement.

Figure 3 illustrates a PIV sweep in the testing of a depletion mode transistor. A depletion mode transistor is normally on with a 0V signal at the gate. This means that a negative voltage is applied to turn off the device, and the transistor is fully on (or nearly so) with $V_g = 0V$.

So, PIV testing of a depletion mode transistor requires a V_g bias point that is negative to either partially or fully turn off the DUT. In the case of ***Figure 3***, the device is partially turned on by using a small voltage for V_g and V_d. Note that the V_g sweep starts at a negative value and then sweeps up to slightly above 0V. V_d is swept from 0 to 27V. This example also shows a negative bias point (q-point) for the gate, and a positive q-point for the drain. Note that the pulse waveform, including the bias point (DC offset), is provided by the pulse instrumentation.

Dual pulsing and power issues. PIV testing requires an instrument with dual channel capabilities for comprehensive q-point testing, as previously illustrated for depletion mode transistors. While it is possible to do

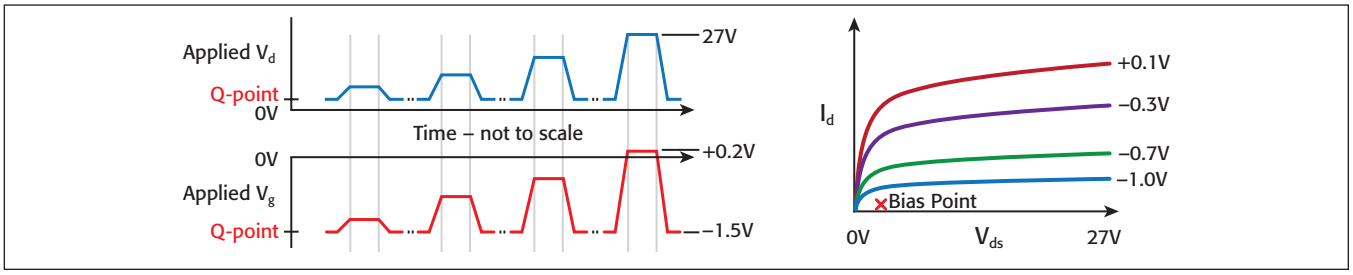

Figure 3. Example of PIV test results on a depletion mode transistor.

PIV testing with a DC bias on the transistor drain and pulse only the gate, this may not cover all the DUT test conditions of interest. It's true that a DC bias on the drain provides a simpler test method. However, it does not allow a q-point value to be used for both the gate and drain when doing a V_d-I_d test, because the drain signal is always sweeping and is not at the V_d bias point. So, to support full bias point operation, both the gate and drain must be pulsed simultaneously.

Another instrument issue is that many RF transistors are used for power amplification and may handle power levels up to 200W. A pulse source capable of this power level would be expensive. Therefore, to moderate costs and simplify testing requirements, the DUT is usually a scaled-down version of the transistor to be characterized (***Figure 4***). This still requires around 30W of pulse power for PIV testing.

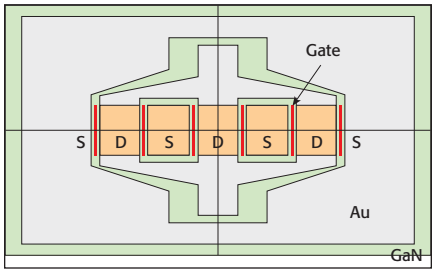

Figure 4. PIV test structure (top view), which is a smaller scale version of the RF transistor being studied.

Test Implementation

Figure 5 is a simplified block diagram illustrating a hardware configuration for PIV q-point testing. The system chassis for this semiconductor parameter analyzer contains source-measure unit (SMU) modules that independently bias gate and drain during DC testing. Similarly, independent pulsers supply the V_g and V_d pulse stimuli to the DUT. These are shown in the upper left and right areas of the diagram, respectively. The SMUs and pulsers are connected and disconnected from the signal paths via on-board switching. ***Figure 5*** shows the switching in a standby condition, with the test equipment disconnected (switches open) from the DUT. During PIV, the SMUs are not connected to the device under test. Naturally, the pulser used for the drain has higher power capabilities than the one used for the gate. A dual-channel oscilloscope module allows independent measurements of the DUT gate signal and drain response. These two channels are shown as separate blocks in the diagram, but are actually contained in a single module within the system chassis.

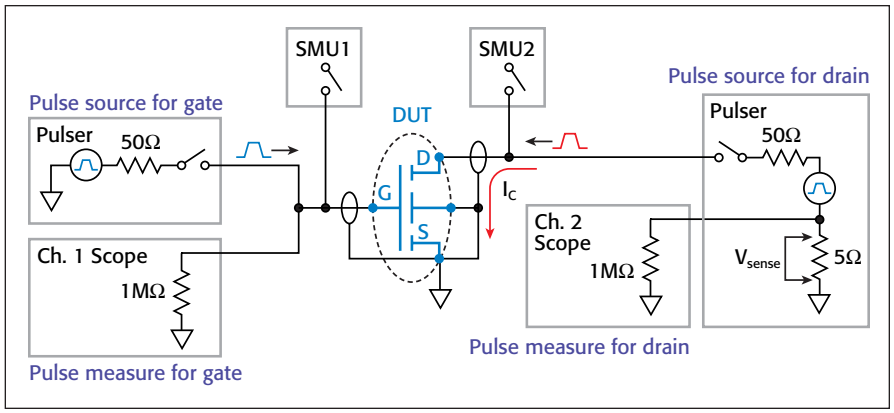

Figure 5. Example hardware configuration for a PIV q-point test system (based on Keithley's Model 4200-SCS Semiconductor Characterization System with a PIV-Q software package).

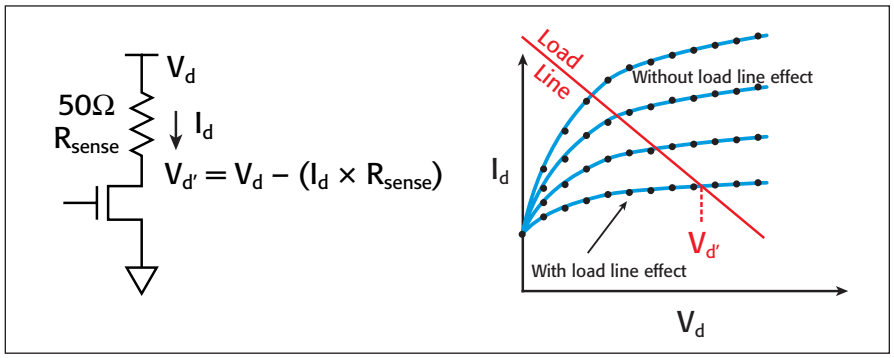

Figure 6. Use of a sense resistor to measure drain current has the effect of reducing the voltage applied to the drain of the DUT and thereby the range of data points collected.

It's important to note that the gate pulse source has 50Ω output impedance, while the drain pulser has 55Ω impedance. The latter is due to the addition of a 5Ω sense resistor (circled in blue) to derive the drain current and voltage. The technique of measuring voltage across a sense resistor to capture current is basically a shunt ammeter circuit, which is used because it provides high bandwidth and is straightforward in its implementation. The voltage across the 5Ω resistor, V_{sense}, is measured on scope Channel 2.

Compensating for load line effect. The use of the shunt ammeter approach does have trade-offs, the main one being a reduction in the applied drain voltage. This is commonly referred to as the load line effect and is a direct result of using a sense resistor to measure drain current.

As drain current flows, there is a voltage drop across R_{sense}. This voltage drop means that the source voltage, V_d, is not the voltage at the drain pin, V_d'. If this drop is not taken into account, then the family of curves is limited to the load line of R_{sense}, as shown by the graph in the right view of ***Figure 6***.

However, there are load line compensation (LLC) algorithms that can correct for this effect. In addition to providing the desired test voltage range, the LLC algorithm also provides the regular spacing, or stepping, of the voltage during the V_d sweep. Thus a full V_d-I_d characterization of the DUT is achieved. This also means that post-processing of the data to get the V_d values "on-grid" is eliminated, which reduces the time required to get the test results from the instrument and into the modeling software.

Cable compensation. Another challenge in PIV testing is related to the cabling and its impedance, which can induce propagation delays and reduce measurement accuracy. This often crops up in pulse test systems that are in-house, custom-built creations.

Many PIV systems in use today were designed and built by the user, because of difficulties in finding a commercial system with the flexibility to do the job at hand. Still,

designing and implementing a PIV test system for specific devices and test needs can be a significant struggle. The capability of a homegrown system to make quality PIV measurements is often overestimated. In an absolute sense, it is usually desirable to achieve correlation of PIV results and DC results, because the PIV system is being used to provide DC-like I-V sweeps. This means that interconnect details and their effects on system performance must be addressed.

The cable interconnect impedances must be determined and corrected somehow, or the system will not provide the best results. This requires a cable compensation routine that measures and corrects for these attributes. For example, in the Keithley 4200-SCS PIV system, it is a simple, short procedure used during initial setup and after any cabling or other interconnect changes. Since the routine includes a through or short test, even pin-to-pad impedance is incorporated into the compensation.

Retarding oscillation. Another problem in testing RF transistors is the potential for oscillations. These disturbances are due to high cutoff frequencies (FC >> 1GHz), coupled with the inherent instabilities created by intrinsic (device) and extrinsic (instrument) feedback paths. These conditions are exacerbated by the fact that the test environment cannot completely match the product environment. Typically, testing requires a wider range of parameters than found in a product's application.

For an experienced PIV user, it is usually straightforward to identify oscillation, or even detect the onset of oscillation, just by viewing the characteristic shape of the PIV plots. However, for new structures and devices, or less experienced users, a more direct method of oscillation detection may be useful. In these cases, looking at an oscilloscope display of the actual pulse is quite helpful. This permits visual confirmation of oscillation and can demonstrate whether or not a particular remedy has suppressed it. (See ***Figure 9*** later in the text.)

The general approach in retarding oscillation is to reduce loop gain, which can be done by adding capacitance or inductance. However, that tends to be rather complicated, as reactance has a large impact on system bandwidth and greatly reduces PIV test performance. It is usually much simpler to add resistance and has less effect on bandwidth.

There are a couple of requirements for adding resistance in the feedback path, typically referred to as ballast resistors. First, adding the resistance must not impede PIV measurements. Second, the test instrument must account for the added ballast resistance and provide corrected results.

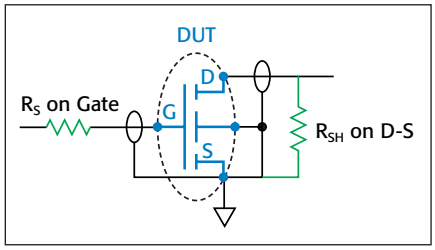

Figure 7. Placement of ballast resistors to retard oscillations during PIV testing.

When pulse testing RF transistors, a series resistance is appropriate for the gate, and a parallel resistor can be placed between the source and drain (***Figure 7***). In the latter case, the shunt-to-ground resistance is designed to reduce loop gain while counteracting the effect of negative slopes on the I-V curves (i.e., negative differential conductivity). Ballast resistance may be added in either or both locations. The ballast resistors are used to reduce or eliminate oscillation, but with the cost of reduced voltage and current at the DUT. For example, all the current flowing through R_{SH} on the drain is not available for the DUT drain.

It should be noted that determining the use of ballast resistors and their resistance values involves a qualitative, iterative process. However, some commercial test systems may come with a set of low reactance resistors, plus software routines that correct test results when ballast resistors are used.

Samples of Test Results

Figure 8 is a screen capture of test results comparing PIV and DC sweeps. It clearly shows the effects of self-heating caused by DC testing in the middle and upper sets of curves. Note that in the lowest power curves (bottom set), DC and PIV results are virtually identical. However, I_d in the top (PIV) curve of the upper set is about 230mA (50%) higher than the blue DC curve. In the latter, significant self-heating has caused a collapse in the I_d characteristic.

Single pulse tests can be used to characterize transient behavior and to check for oscillations. ***Figure 9*** illustrates typical results. The blue curve is the voltage pulse applied to the gate, and the red curve is the resulting drain current. Note that both curves are well behaved, without any overshoot, ringing, or oscillation. When verifying a setup, viewing the pulse shape can be valuable to ensure that proper cabling and contact to the device pads has been made.

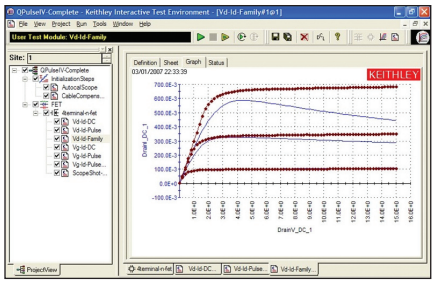

Figure 8. Comparison of PIV sweeps (red curves) with DC sweeps (blue curves) of an RF transistor. Self-heating causes the sags in the DC sweeps at higher currents.

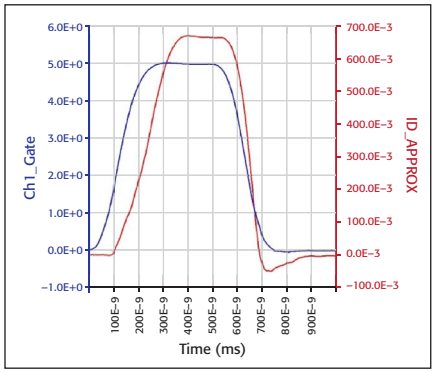

Figure 9. Single pulse PIV test results: the blue curve is the gate voltage pulse, while the red curve is drain current.

To examine the DUT's transient behavior, look for a time-varying change in the device response due to self-heating, charge trapping, or other time-varying phenomena. ***Figure 10*** is an example of self-heating that causes a reduction in drain current vs. time. In this figure, I_d starts at about 630mA, but is down to 590mA after 10ms, a reduction of about 6%.

Conclusions

Dual-channel PIV testing with non-zero bias on the gate and drain of RF transistors is a powerful test tool. It allows accurate characterization under a wide variety of conditions that simulate large signal (non-linear) operation. With appropriate test hardware and software, a wide variety of single pulse

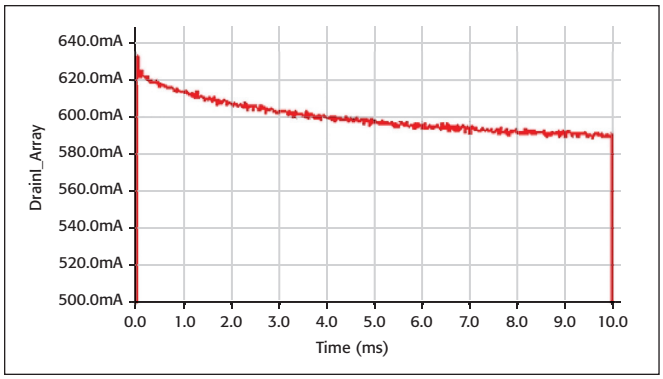

Figure 10. Example of a transistor's transient (single-pulse) response showing the effects of self-heating, which causes a reduction in the drain current vs. time curve.

and multiple sweep test routines are available and easy to run. (See, for example, the test list on the left side of ***Figure 8***.)

Many times, device characterization is an iterative process, therefore a system designed for interactive testing is highly desirable. Some important features to look for include:

- A wide range of PIV parameters for FETs such as HEMT, pHEMT, and LDMOS devices
- Sub-microsecond pulse timing parameters
- Ability to modify test parameters and compare new results to previous run(s) on the fly
- Comparison of DC and PIV tests for dispersion effects
- Comprehensive data analysis and easy export of results into other applications
- Interconnects and software that enable q-point testing and cable compensation
- Software routines for load line compensation
- Ballast resistors to retard oscillation, and software that corrects results when they are used.

About the Author

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