
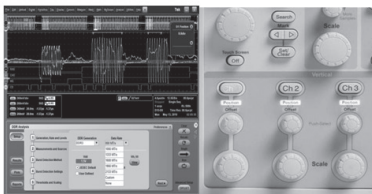











## Memory Interface Verification and Debug

Customer Presentation  
Version 1.0

**Tektronix**

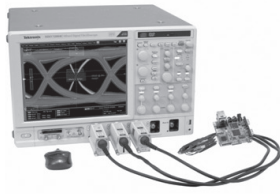

## Memory Validation Continuum

	Analog Validation	Digital Validation	Execution Validation
Instruments			
Probes			
Analysis SW			

**Tektronix**

## Memory Interface Analog Validation

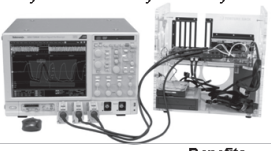
*Measure the analog signal characteristics; trtf, Vmin/max, jitter, eye size, crossover, strobe/clock alignment, etc.*

**Tektronix**

## DDR4 Features and Benefits

*Complete Solution for Memory Interface Physical Layer Test*



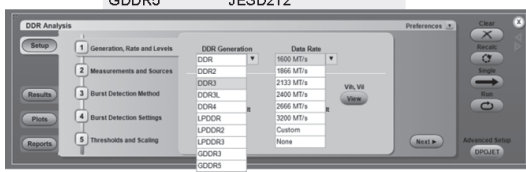
Feature	Benefits
<b>Memory Validation and Debug</b>	Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3 the newest standards targeted for Server/Computer and Mobile Handsets. Support for various JEDEC specification defined speed grades as well as custom speeds
<b>Selectable Speed Grades</b>	Easily set up the test configuration for performing the analysis.
<b>Auto Configuration Wizard</b>	Isolate measurements to a rank of interest by using the chip select signal in a multi rank configuration
<b>Qualified Multi-Rank Measurements</b>	Navigate and Timestamp all the READ and WRITE cycles in an acquired record using Search and Mark
<b>Cycle Type Identification</b>	Quickly trigger, isolate and capture events of interest with Pin-Point HW Triggering combined with Visual Trigger and Active Search and Mark capabilities in Tektronix Oscilloscopes, making them an indispensable tool for Memory Interface Validation.
<b>Visual Trigger / Pin Point Triggering</b>	De-embed the effects of the Interposers and Probes to provide more accurately representation of the signal
<b>De-embedding</b>	Provides the ability to select the Memory specification and the Speed Grade against which the analysis needs to be done as well as individual tests or group of tests to perform targeted analysis.
<b>Test Selection</b>	Automatically generate consolidated reports that include pass/fail results, statistical measurement information as well as details about the test setup.
<b>Reporting</b>	Quickly switch into debug mode in case a system fails conformance tests and use the DPOJET jitter analysis package
<b>Conformance and Debug</b>	P7500 Trimode Probe Family and Micro-Coax Tips combined with Nexus Technology Interposers for various memory standards and packaging types results in a complete probing system that provides easy access to memory interface signals and allows making differential, single-ended, and common mode measurements accurately and definitively
<b>Probing Solutions</b>	Address/Command signals acquired on the digital channels of the Mixed Signal Oscilloscope can be used to precisely qualify bus cycles or events of interest as well as perform timing measurements
<b>Digital Channels on MSO</b>	Tektronix provides a broad range of tools for Electrical Test, Logic Debug and Execution Validation.
<b>Analysis and Debug Tools</b>	

**Tektronix®**

## Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings
- JEDEC Standards specify measurements & methods

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79-3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212

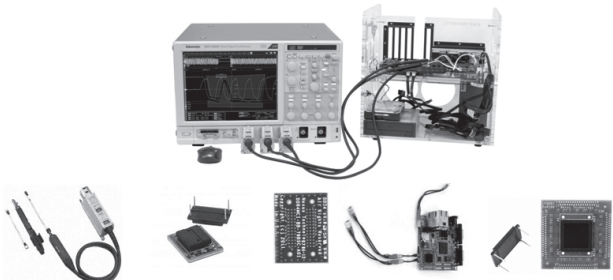


**Tektronix®**

## Oscilloscope Bandwidth Requirement

Memory Technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s
Max skew rate	5	5	5	10	12	12	8	16
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8
20-80 risetime (ps)	216	150	150	60	50	45	45	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0
Recommended Scope BW (Max Performance)	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16
Recommended Scope BW (Typ Performance)	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 and LPDDR3 is supported only on DSAMSO/DPO70000C/D models only

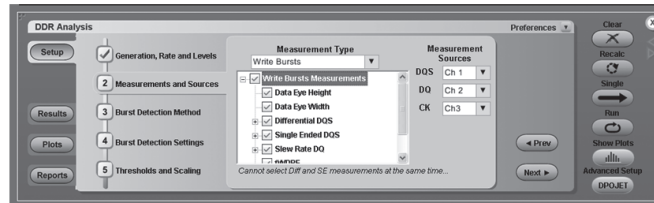


[www.tektronix.com/ddr](http://www.tektronix.com/ddr)

**Tektronix®**

### Test Setup and Configuration

- All the tests are logically grouped based on the input source requirement
  - READ
  - WRITE
  - CLOCK
  - ADDR/CMD
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.
- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.

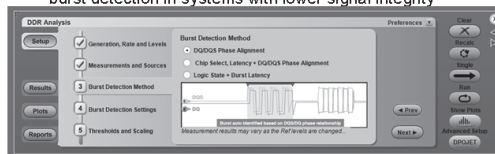
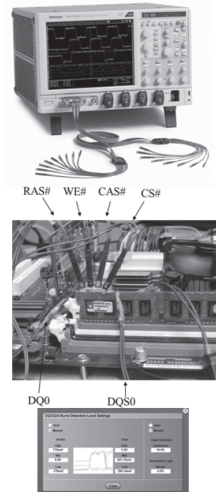


7



### Burst Detection

- Read / Write bursts are automatically detected for analysis purposes
- Several different techniques are used for Read/Write Burst Separation
  - DQ/DQS phase alignment: DQ and DQS have different phase relationship in Read and Write bursts
  - CS, Latency + DQ/DQS Phase Alignment: CS is used to qualify the occurrence of a burst, followed by DQ/DS phase relationship to distinguish between Read/Write
  - Logic State + Burst latency: The command bus probed using the digital channels on the MSO is used to identify Read/Write commands on the command bus are quality and distinguish Read and Write bursts
- Options are provided to adjust the levels to improve burst detection in systems with lower signal integrity

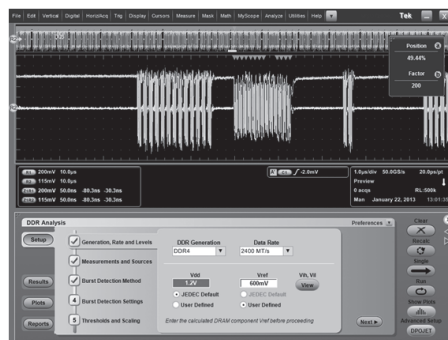


8



### Burst Detection

- Easily Identify, Mark & Measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL Reads/writes within an acquisition

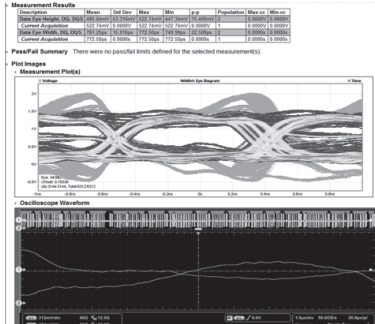


9

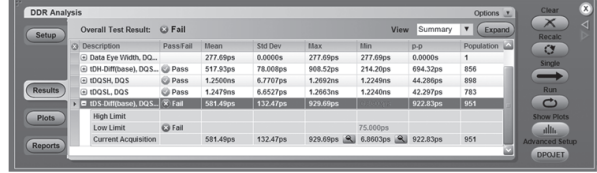


### Reports

- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes
  - Measurement results
  - Pass/Fail test results based on specification values
  - Summary and detail plots
  - Oscilloscope screenshots
  - Measurement and Instrument configuration summary
- Report contents are user definable content
  - Provision to append more results later



Description	Mean	Std Dev	Max	Min	p-p	Population	Max or Min or p-p
Current Acquisition	122.480ps	0.0000s	122.480ps	122.480ps	0.0000s	1	0.0000s
Current Mask	122.480ps	0.0000s	122.480ps	122.480ps	0.0000s	1	0.0000s
Current Measurement	122.480ps	0.0000s	122.480ps	122.480ps	0.0000s	1	0.0000s

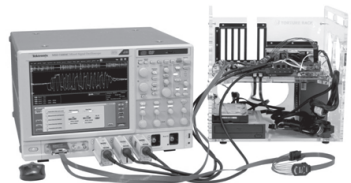


Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
Data Eye Width, DG...	Pass	277.69ps	0.0000s	277.69ps	277.69ps	0.0000s	1
QH DMPass, DQS...	Pass	517.83ps	78.00ps	908.52ps	214.20ps	694.32ps	856
QDSL DQS	Pass	1.2600ns	8.7107ps	1.2692ns	1.2220ns	44.20ps	898
QDSL DQS	Pass	1.2479ns	6.6527ps	1.2653ns	1.2240ns	42.297ps	783
DS DMPass, DQS...	Fail	581.49ps	132.47ps	929.69ps	6.8903ps	922.83ps	951
High Limit						75.00ps	
Low Limit						6.8903ps	
Current Acquisition		581.49ps	132.47ps	929.69ps	6.8903ps	922.83ps	951

10

### Beyond DDRA

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark

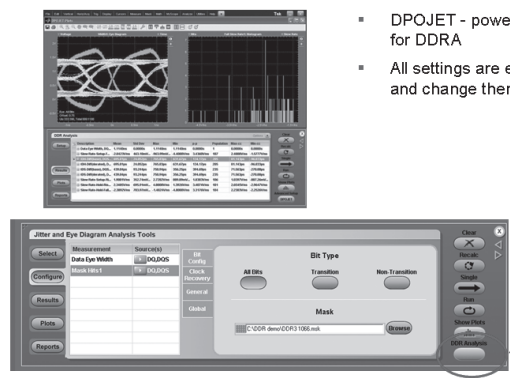


11

### Signal Analysis & Debug

#### DDRA + DPOJET

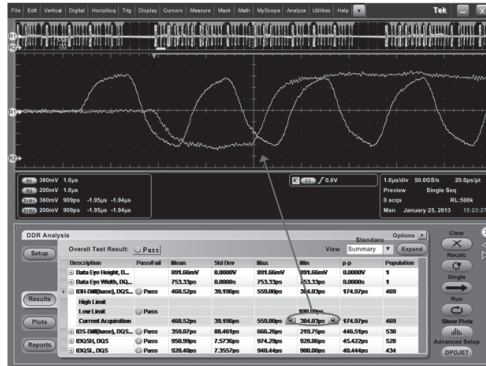
- DDRA is not a closed tool – seamlessly links directly to DPOJET for measurement analysis
- Opportunity to change or fine-tune settings, add new measurements as needed
  - DPOJET - powerful measurement engine for DDRA
  - All settings are explicit – you can see them and change them.



12

### DPOJET Debug Tools

- "Find Worst Case Events" feature
  - Zoom to waveform from Min / Max for each measurement

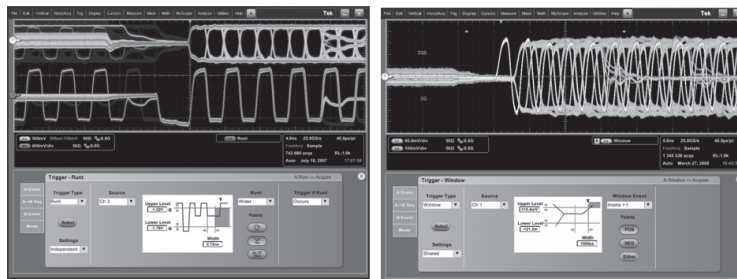


13



### Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you "the power to see what others can't"
  - FastAcq shows any disparities on signals, like infrequent glitch's

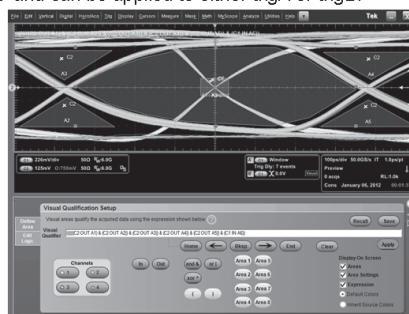


14



### Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 vertices
- Areas are "keep in" or "keep out" and can be applied to either trigA or trigB.
- Can be used to
  - Separate Read / Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams



15



### Visual Trigger Used For DQ Pattern Detection

#### 010000X Pattern

16

Tektronix

### Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
  - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
  - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA

17

Tektronix

### Advanced Search and Mark

- Tabular Results and Navigation
  - Events by Type – read/write or other events
  - Time stamps, delta-times between events
  - Intuitive navigation – Zoom on the burst of interest
- 'Stop on Found' works as a pseudo-trigger mode

Results: Counts			
Select	Type	Source	Count
1	DDR Read	Ch 1, Ch 2	138
2	DDR Write	Ch 1, Ch 2	157

Results: Mark Table									
Index	Type	Src	Location	Time Delta				Description	
				sec	ms	us	ns		
1	DDR Write	C1	-8.579us					DDR3 - WRITE - 1.066G	
2	DDR Write	C1	-8.496us	000	000	000	082	480	DDR3 - WRITE - 1.066G
3	DDR Write	C1	-8.414us	000	000	000	082	520	DDR3 - WRITE - 1.066G
4	DDR Write	C1	-8.331us	000	000	000	082	500	DDR3 - WRITE - 1.066G
5	DDR Write	C1	-8.29us	000	000	000	041	240	DDR3 - WRITE - 1.066G
6	DDR Write	C1	-8.208us	000	000	000	082	500	DDR3 - WRITE - 1.066G

Total Marks: 287

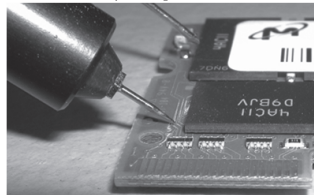
Search Marks: Save, Save All, Clear, Digits >>, << Digits, All Marks, Export, Clear, View, Count

18

Tektronix

### Memory Probing

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- Memory Components use BGA or PoP Packages
  - Reduces the parasitics, enabling performance at higher speeds
  - Mandate from JEDEC
- Probing a BGA or PoP package is Difficult
  - Unable to probe at the Balls of the Device
  - Probing at a connector, trace, or a via is not the same as probing at the device
  - Not a true representation of the signal



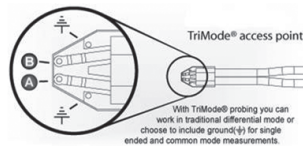
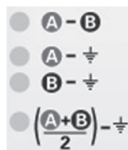
Courtesy Microw Technology



19

### TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements:  $((V+) + (V-))/2$  with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!

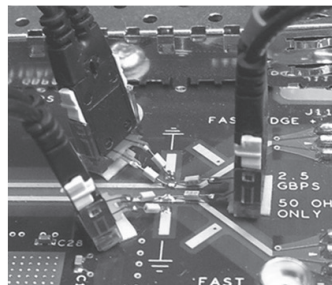


With TriMode® probing you can work in traditional differential mode or choose to include ground(ψ) for single ended and common mode measurements.

20

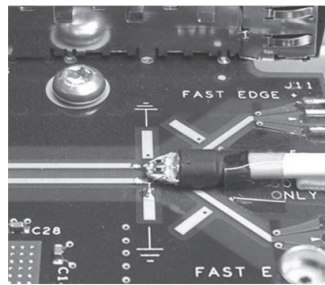


### Before and After



#### Before TriMode Probing

- 1 Probe for Differential
- 2 Probes for SE and Common Mode
- or
- 1 Probe Soldered and Re-soldered 3 times
- 2 Probes for Common Mode



#### After TriMode Probing

- 1 Probe and 1 setup for Differential, SE and Common Mode

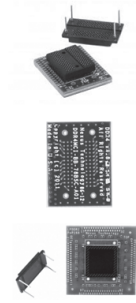
21



### Memory Component Interposers

- Provide easy access to signals of Interest
- Controller Impedance path with embedded resistor for good signal Integrity
- De-embed filters to remove effects of interposer tap trace
- SPICE model available upon request for simulation and analysis

Memory Standard	Supported Form Factors	Interposer Types
DDR2	- BGA	- Socketed Interposer - Direct Attach Interposer
DDR3	- BGA	- Socketed Interposer - Direct Attach Interposer - MSO DIMM Interposer - Instrumented DIMM
DDR4	- BGA	- Socketed Interposer - Direct Attach Perimeter Interposer - MSO DIMM Interposer - Instrumented DIMM
LPDDR2	- BGA - PoP	- Socketed Interposer - PoP Interposer
LPDDR3	- BGA - PoP	- Socketed Interposer - PoP Interposer
GDDR5	- BGA	- Socketed Interposer - Direct Attach Interposer

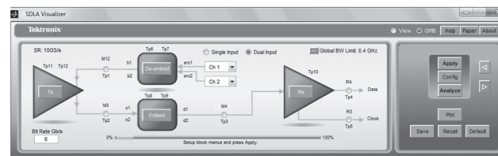


22



### De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will available for the interposers upon request. These de-embedding filters are developed assuming nominal values
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used



23



### Memory Interface Digital Validation

Measure the digital logic state and cycle based timing characteristics for diagnostic and troubleshooting purposes



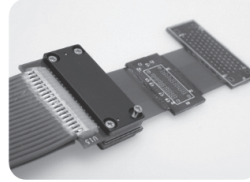
24





### DDR4 Memory Component Interposers

- MCI's are used for probing signals from individual Memory Components
- Comes with a Custom Socket that needs to be soldered to Target system
- Quickly swap TLA & oscilloscope interposers on the same target. Quickly move interposers to different target.
- No special footprints or special routing requirements
- Memory Component Interposer Types
  - Logic Analyzer and Oscilloscope
  - Direct Attach or Socketed interposers
  - x4/x8 and x16 Memory Component types

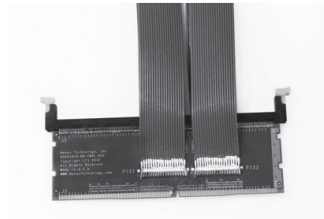
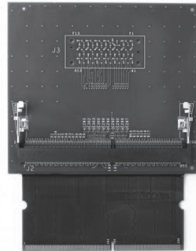


Tektronix Confidential

25

### DDR4 ACC Interposers

- Protocol / Execution Validation
  - DIMM and SODIMM Interposers
  - Targeted for protocol compliance analysis
  - Automated Setup
  - Use with Nexus Compliance Analysis S/W
  - Compatible with P6960HCD or NEX-PRB1XL



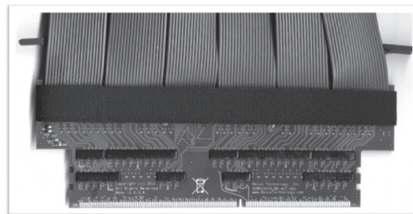
Sales University 2012 - Tektronix Confidential Course Title v1.x (Edit in View/Insert > Header and Footer)

26

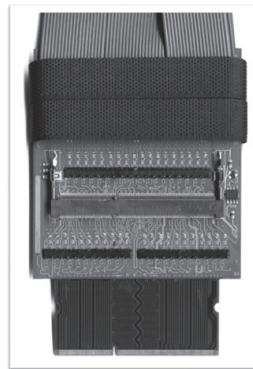
### Introducing New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

Gain Unprecedented Visibility Into Your DDR3/4 Signal Activity



DIMM Interposer



SODIMM Interposer

Collaborative design combining years of Logic Analyzer acquisition and DDR3 probing experience between Tektronix and Nexus Technology

27

### New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

- Provides significant performance improvements to DDR3 probing
  - Integrates Tektronix ultra-high performance SiGe Hybrid ASIC technology
  - Compensation for platform trace loss on writes
- Improved interposer input impedance (5.2k to 0.73V)
  - Reduces load on target with minimal effect on bus
  - Provides an accurate representation of the signal on the target
- Enables probing DDR3/4 speeds at 2400MT/s and beyond
- Enables probing lower voltage signals on LVDDR3/4
- Interposers compatible with UDIMM, RDIMM, LRDIMM

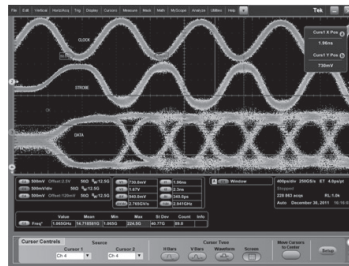
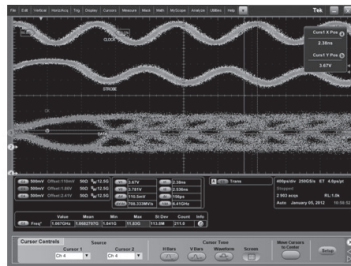
28



### Scope Screenshots at DDR3 2133MT/s – Writes

OLD Interposer

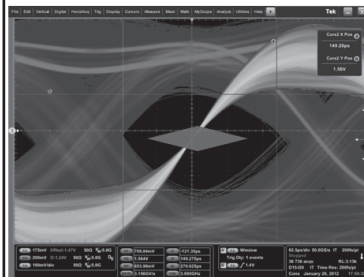
NEW Interposer



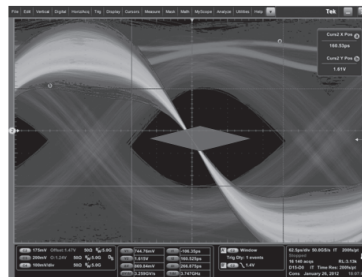
29



### Write Data Eye – DDR3 2400MT/s



Write data eye, rising strobe edge, 853mV x 270ps



Write data eye, falling strobe edge, 869mV x 266ps



Represents minimum TLA7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

30



### Scope Screenshots at DDR3 2133MT/s – Reads

OLD Interposer

NEW Interposer

ICi's Tool

**Tektronix®**

### Read Data Eye – DDR3 2400MT/s

Read data eye, rising strobe edge, 492mV x 252ps
Read data eye, falling strobe edge, 454mV x 266ps

Represents minimum 7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

**Tektronix®**

### TLA7BBx Logic Analyzer Modules

*Proven Technology for Analyzing DDR3 SDRAM*

DIGITAL CHARACTERISTICS	TLA7BB2	TLA7BB3	TLA7BB4
Digital Channels	68	102	136
High Speed Timing (MagniVu)	50GS/s (20ps)		
Deep Memory Timing	Up to 6.4GS/s		
State Speed	Up to 1.4GHz/3.0Gbps		
Memory Depth	Standard 2Mb, Maximum 64Mb		
Probes	All P68xx and P69xx		
iCapture (Analog Mux)	3 GHz		

- Preserve investment in TLA7BBx modules
- Enable higher DDR3 speed support with new interposer

**Tektronix®**

### MagniVu 20ps (50 GS/s) High Speed timing

*Industry Leading Sampling Resolution*

- 50GHz timing analysis on every channel
- Acquired simultaneously and time-correlated with state acquisition data
- Enables acquisition and debug of S/H violations, glitches, and other timing violations
- Reveals fly-by command/address/control bus timing

34 Tektronix

### Analog Mux, iCapture

*Enables Signal Integrity Troubleshooting*

- Unrivaled capability of the TLA that provides single-point digital and analog probing
- No need to separately probe with a scope, as probing done through the interposer
- Walk through all the signals on your DDR bus in less than 15 minutes to review channel behavior and isolate any potential problems
- Quickly perform detailed analog characterization on signals of interest using a scope component interposer

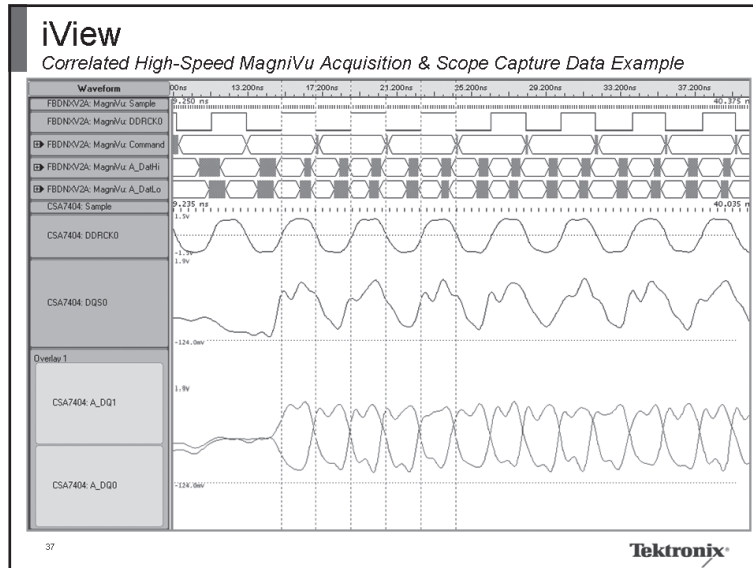
35 Tektronix

### iView

*View Correlated Analog & Digital Characteristics in the Same Display*

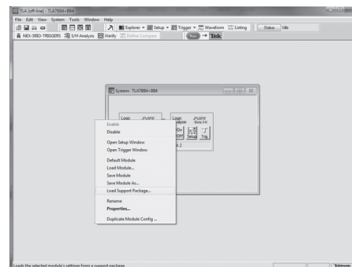
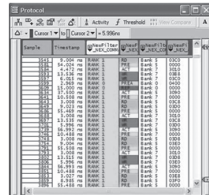
- Unique capability on the TLA that provides time correlated state acquisition, high-speed MagniVu timing acquisition, and analog scope capture results on the same screen.
- Capture events that occur in analog or digital domain through cross triggering
- Enables cross domain analysis by quickly capturing and isolating potential problems

36 Tektronix



### TLA - Initial Setup

- New Fast & Easy Setup
  - Quick and easy connection
  - Fast software setup
  - No calibration needed for CMD/ADDR/CTRL
  - Automated and graphical DQ data calibration
  - Up and running acquiring ALL data in 15-30 minutes!
  - Identify problem channels at the same time!
- Load the TLA Software
- Load the Support Package
- Ready to Acquire CMD / ADDR / CTRL!



38

### iCis Overview

- Goals of iCis
  - Make LA memory tuning easier and quicker
  - Less dependency on platform specific DQ valid regions
  - Less dependency on DQS placement
  - Put more power in the users hands
  - Allow both Vth and sample point to be determined at same time
  - Quick check of signal integrity on the memory bus
  - Allow tuning of address and command signals
  - Simultaneous tuning of Read and Write sample points
  - Double mouse click method to set Vth and sample point for all signals
  - Single tuning tool leveraged for DDR3, DDR4, LPDDR2/3
- User control
  - DDR bus parameters
  - Voltage sweep step size
  - Voltage sweep range
  - Which signals to tune
    - Address bit(s)
    - Command bit(s)
    - DQ-byte lane or individual DQ
      - Read & Write, read only, write only

39

### DDR3 Sweep

100mV Resolution, Full Burst Mode / 8 DQ Eyes, Reads

8 valid DQ eyes

40

Tektronix

### TLA Data Analysis

- State, MagniVu timing, & analog mux at your fingertips
- Compliance analysis tools
  - Fast setup
  - Comprehensive coverage and violation detection

41

Tektronix

### TLA- Example State / MagniVu Display

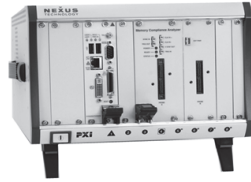
- Command / Address / Control
- DQ Read and Write Data
- Up to 64M-sample state memory
- Simultaneous 50GHz MagniVu timing

42

Tektronix

### Memory Interface Execution Validation

Measure the bus command and control timing sequences, and compare them to a specification or evaluate them as indicators of bus utilization or performance



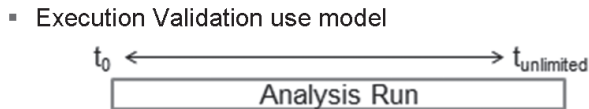
Item	Name	Observed	Validation	Specs	Margin	Margin%	Spec. Unit
1	RD Data Rate/FIFO	0	0	0	0	0	0
2	RD Data Rate	0	0	0	0	0	0
3	RD Data Rate	0	0	0	0	0	0
4	RD Data Rate	0	0	0	0	0	0
5	RD Data Rate	0	0	0	0	0	0
6	RD Data Rate	0	0	0	0	0	0
7	RD Data Rate	0	0	0	0	0	0
8	RD Data Rate	0	0	0	0	0	0
9	RD Data Rate	0	0	0	0	0	0
10	RD Data Rate	0	0	0	0	0	0
11	RD Data Rate	0	0	0	0	0	0
12	RD Data Rate	0	0	0	0	0	0
13	RD Data Rate	0	0	0	0	0	0
14	RD Data Rate	0	0	0	0	0	0
15	RD Data Rate	0	0	0	0	0	0
16	RD Data Rate	0	0	0	0	0	0
17	RD Data Rate	0	0	0	0	0	0
18	RD Data Rate	0	0	0	0	0	0
19	RD Data Rate	0	0	0	0	0	0
20	RD Data Rate	0	0	0	0	0	0
21	RD Data Rate	0	0	0	0	0	0
22	RD Data Rate	0	0	0	0	0	0
23	RD Data Rate	0	0	0	0	0	0
24	RD Data Rate	0	0	0	0	0	0
25	RD Data Rate	0	0	0	0	0	0
26	RD Data Rate	0	0	0	0	0	0
27	RD Data Rate	0	0	0	0	0	0
28	RD Data Rate	0	0	0	0	0	0
29	RD Data Rate	0	0	0	0	0	0
30	RD Data Rate	0	0	0	0	0	0
31	RD Data Rate	0	0	0	0	0	0
32	RD Data Rate	0	0	0	0	0	0
33	RD Data Rate	0	0	0	0	0	0
34	RD Data Rate	0	0	0	0	0	0
35	RD Data Rate	0	0	0	0	0	0
36	RD Data Rate	0	0	0	0	0	0
37	RD Data Rate	0	0	0	0	0	0
38	RD Data Rate	0	0	0	0	0	0
39	RD Data Rate	0	0	0	0	0	0
40	RD Data Rate	0	0	0	0	0	0
41	RD Data Rate	0	0	0	0	0	0
42	RD Data Rate	0	0	0	0	0	0
43	RD Data Rate	0	0	0	0	0	0
44	RD Data Rate	0	0	0	0	0	0
45	RD Data Rate	0	0	0	0	0	0
46	RD Data Rate	0	0	0	0	0	0
47	RD Data Rate	0	0	0	0	0	0
48	RD Data Rate	0	0	0	0	0	0
49	RD Data Rate	0	0	0	0	0	0
50	RD Data Rate	0	0	0	0	0	0
51	RD Data Rate	0	0	0	0	0	0
52	RD Data Rate	0	0	0	0	0	0
53	RD Data Rate	0	0	0	0	0	0
54	RD Data Rate	0	0	0	0	0	0
55	RD Data Rate	0	0	0	0	0	0
56	RD Data Rate	0	0	0	0	0	0
57	RD Data Rate	0	0	0	0	0	0
58	RD Data Rate	0	0	0	0	0	0
59	RD Data Rate	0	0	0	0	0	0
60	RD Data Rate	0	0	0	0	0	0
61	RD Data Rate	0	0	0	0	0	0
62	RD Data Rate	0	0	0	0	0	0
63	RD Data Rate	0	0	0	0	0	0
64	RD Data Rate	0	0	0	0	0	0
65	RD Data Rate	0	0	0	0	0	0
66	RD Data Rate	0	0	0	0	0	0
67	RD Data Rate	0	0	0	0	0	0
68	RD Data Rate	0	0	0	0	0	0
69	RD Data Rate	0	0	0	0	0	0
70	RD Data Rate	0	0	0	0	0	0
71	RD Data Rate	0	0	0	0	0	0
72	RD Data Rate	0	0	0	0	0	0
73	RD Data Rate	0	0	0	0	0	0
74	RD Data Rate	0	0	0	0	0	0
75	RD Data Rate	0	0	0	0	0	0
76	RD Data Rate	0	0	0	0	0	0
77	RD Data Rate	0	0	0	0	0	0
78	RD Data Rate	0	0	0	0	0	0
79	RD Data Rate	0	0	0	0	0	0
80	RD Data Rate	0	0	0	0	0	0
81	RD Data Rate	0	0	0	0	0	0
82	RD Data Rate	0	0	0	0	0	0
83	RD Data Rate	0	0	0	0	0	0
84	RD Data Rate	0	0	0	0	0	0
85	RD Data Rate	0	0	0	0	0	0
86	RD Data Rate	0	0	0	0	0	0
87	RD Data Rate	0	0	0	0	0	0
88	RD Data Rate	0	0	0	0	0	0
89	RD Data Rate	0	0	0	0	0	0
90	RD Data Rate	0	0	0	0	0	0
91	RD Data Rate	0	0	0	0	0	0
92	RD Data Rate	0	0	0	0	0	0
93	RD Data Rate	0	0	0	0	0	0
94	RD Data Rate	0	0	0	0	0	0
95	RD Data Rate	0	0	0	0	0	0
96	RD Data Rate	0	0	0	0	0	0
97	RD Data Rate	0	0	0	0	0	0
98	RD Data Rate	0	0	0	0	0	0
99	RD Data Rate	0	0	0	0	0	0
100	RD Data Rate	0	0	0	0	0	0



43

### What's unique about Execution Validation

- Typical instrument use a post-capture model  
TRIGGER → ACQUIRE → ANALYZE



- Two equipment options
  - Logic Analyzer - S/W automates acquisitions
  - Memory Compliance Analyzer - Real-time Analysis

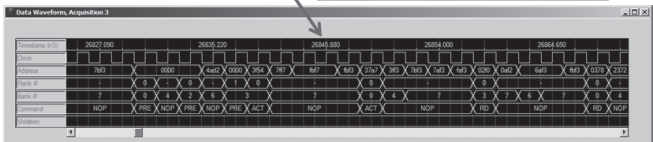


44

### Example Results

Command Timing analysis in both state table and timing views

Address	Command	State	Timing	Validation
14209	26523 960	7d3	-	NOP
14310	26527 080	7d3	-	NOP
14311	26527 720	7d3	-	NOP
14312	26530 840	0000	0	0
14313	26531 480	0000	-	NOP
14314	26534 560	0000	0	0
14315	26535 200	46c2	-	NOP
14316	26538 960	0000	1	0
14317	26538 960	354	0	3
14318	26542 110	7d3	-	NOP
14319	26542 720	6d7	-	NOP
14320	26545 880	6d7	-	NOP
14321	26546 500	6d3	-	NOP
14322	26549 630	3757	0	0
14323	26552 720	6d3	-	NOP
14324	26553 360	7d3	-	NOP
14325	26554 000	6d3	-	NOP
14326	26557 130	6d3	-	NOP
14327	26557 760	030	0	3
14328	26559 800	6d3	-	NOP
14329	26561 520	6d3	-	NOP
14330	26564 560	6d3	-	NOP
14331	26566 270	6d3	-	NOP
14332	26568 440	010	0	0
14333	26569 000	2172	-	NOP
14334	26572 150	6d3	-	NOP
14335	26572 770	7d3	-	NOP
14336	26575 900	0300	0	0



www.newstechnology.com  
877-595-8116



45

### Specifications Published in JEDEC Standards

JEDEC  
STANDARD



DDR3 SDRAM Specification

JESD79-3E

192 Pages  
118 Figures  
80 Tables

46



### What specs are checked?

Test Name	Device Option	Device Option
1. CMD vs SRE/REF Bank	Sequential check. A non-NOP/DEE command can not occur on a self-refreshing rank.	
2. SRE vs ACT Bank	Sequential check. A Self-Refresh Entry (SRE) command can not occur on an active rank.	
3. MRD vs ACT Bank	Sequential check. An Mode Register Set (MRD) command can not occur on an active rank.	
4. RSD(A)/W(R) during MRS	Sequential check. A read (RD) or write (WR) or v(R)A command can not occur during rank MRS cycle.	
5. CMD vs PD Bank	Sequential check. A non-NOP/DEE command can not occur on a powered-down rank.	
6. PRE(A)/REF vs SRE/REF Bank	Sequential check. A read (RD) or write (WR)A command can not occur during rank refresh.	
7. ACT/REF vs ACT Bank	Sequential check. A activate (ACT) or refresh (REF) command can not occur on an active bank.	
8. RD vs ACT Bank	Sequential check. A refresh (REF) command can not occur on an active bank that is reading or writing.	
9. RSD(A)/W(R) vs SRE/REF Bank	Sequential check. A read (RD) or write (WR)A command can not occur during an active (precharged) bank.	
10. sACT	The minimum time between any two activate (ACT) commands to the same rank must meet sACT.	
11. PDRX Exit	Power-Down Exit (PDRX) to any valid command (PRE(A)/REF(ACT)/MRD) must meet PDRX.	
12. sRD Exit	Self-Refresh Exit (sRD) to any command not requiring a locked DLL (PRE(A)/REF(ACT)/MRD) must meet sRD.	
13. dACT	The minimum time between two activate (ACT) commands must meet dACT.	
14. PRE(A) Bank Settle	Minimum time from a PRE(A) command to any valid command on the same rank (MRD/SRD) must meet PREP.	
15. REF Delay SRE	Sequential check. At least one refresh (REF) command is required between self-refreshed (SFX) to SRE.	
16. SRE Separation from PRE(A)	If the last valid command received before a self-refresh entry (SRE) was a precharge (PRE(A)), then the separation between these two commands must meet PREP(SRE).	
17. SRE Separation from REF	If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two commands must meet PREP(SRE).	
18. SRE Separation from ACT	If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two commands must meet sACT(SRE).	
19. SRE Separation from MRD	If the last valid command received before a self-refresh entry (SRE) was a mode register set (MRD), then the separation between these two commands must meet sMRD(SRE).	
20. SRE Separation from WR	If the last valid command received before a self-refresh entry (SRE) was a write (WR), then the separation between these two commands must meet sWR(SRE).	
21. SRE Separation from v(R)A	If the last valid command received before a self-refresh entry (SRE) was a write v(R)A precharge (v(R)A), then the separation between these two commands must meet sVAPEN.	
22. SRE Separation from RD(A)	If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two commands must meet sRD(SRE).	
23. MRS Settle	Minimum time from an mode register set (MRS) command to any other valid command that is not an MRS must meet MRS.	
24. MRD Delay	Minimum time from MRD to the next and subsequent mode register set (MRS) commands must meet MRD.	
25. sSRE Time	The minimum amount of time in self-refresh must meet sSRE.	
26. WR Burn	The minimum amount of time between write (v(R)A) commands must meet sCCD.	
27. RD to MRD Separation	The minimum amount of time between read (RD) and write (v(R)A) commands must meet sDRTV.	
28. PDRX Slow Exit	Power-Down Exit (PDRX) Slow Exit (MRD, A12) to read (RD(A)) command must meet sDPLL.	
29. Rank DLL Reset to PDRX	Read (RD(A)) must wait sDLL after reset.	
30. WR to RD(A) Separation	The minimum amount of time between write (v(R)A) and read (RD(A)) commands must meet sWTR.	
31. RD Burn	The minimum amount of time between read (RD(A)) commands must meet sCCD.	
32. PDRX Time Min	The minimum amount of time in power-down (PDRX) must meet sPDRX.	
33. sPD Time Max	The maximum amount of time a rank can stay in power-down (PDRX) to PDRX must meet sPDRX.	
34. PRE(A) Bank Settle	Minimum time from a PRE(A) command to any valid command on the same bank must meet sRP.	
35. sREF Time	The minimum amount of time in self-refresh must meet sREF.	
36. sACT Time Min	The minimum amount of time a bank must stay active (ACT) to PRE(A) must meet sRActn.	
37. sACT Time Max	The maximum amount of time a bank can stay active (ACT) to PRE(A) must meet sRActn.	
38. ACT to RD(A)/v(R)A	The minimum amount of time from a activate (ACT) command to a read (RD(A)) or write (v(R)A) command must meet sWTR/rd.	
39. RD to PRE(A)	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet sRP.	
40. RD to WR	The minimum amount of time from a read (RD) command to a write (WR) command must meet sWTR.	
41. WR to PRE(A)	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet sWTR.	
42. WR to ACT	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet sWTR.	
43. CCD: Stand-After-DLL Burn	Rank (RD) must remain high sDLL time after sDLL Burn.	

47



### How are the event values set?

The screenshot shows two windows from the JEDEC Compliance Timing Parameters software. The left window, 'JEDEC System Setup', is for 'CORS-1000' and shows configuration for 'DDR System' (CORS-1000), 'DDR Spec.' (DDR3), and various timing parameters like 'Additive Latency', 'CAS Latency (CL)', and 'CAS Write Latency (CWL)'. The right window, 'Compliance Timing Parameters', shows a table of timing parameters for 'CORS-1000' with columns for 'Timing Parameter', 'Value', 'Unit', 'Min', 'Max', and 'Status'. Parameters include tACTPEN, tCCD, tCKESR, tDLK, tFAW\_1b, tFAW\_2b, tMOD, tMRD, tMRSPEN, tPDRX, tPDRX\_HT, tPREPEN, tRASmax, and tRASmax\_HT.

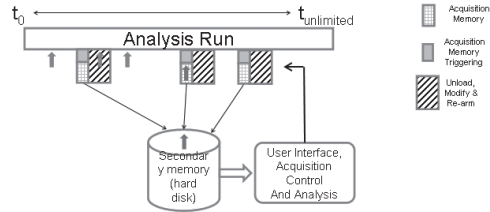
- Standard system setups are provided, and can then be modified
- Once the memory system is setup, any timing parameter can be modified

48





### Post-Capture Protocol Compliance Analysis



- LA Memory Compliance Analysis Package enables automated sweeps of multiple transitions, which would result in violation detection over many acquisitions.
- When violations are occurring frequently the likelihood of capture increases and the analysis time decreases.
- However, near the edge of margin envelopes, intermittency increases, resulting in difficulty to observe and capture the event.

49

### Results per Session & per Acquisition

Compliance Parameters										
Stat. Name	Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)	Spec. Value(ps)
22	SRE Separation from RDCA	00	00	00	00	00	00	00	00	22,488
23	MPS Settle	00	00	00	00	00	00	00	00	22,500
24	MPS Burst	00	00	00	00	00	00	00	00	22,500
25	±SRE# Time	00	00	00	00	00	00	00	00	7,500
26	VR# Time	13,385	00	00	13,385	00	13,385	00	00	7,200
27	RD to MRQA Separation	13,385	00	00	13,385	00	13,385	00	00	13,118
28	FDX Show Exit	00	00	00	00	00	00	00	00	24,000
29	Bank DLL (Reset to RDCA)	00	00	00	00	00	00	00	00	993,700
30	VR to RDCA Separation	22,215	00	00	22,215	00	22,215	00	00	26,236
31	RD Burst	22,215	00	00	22,215	00	22,215	00	00	7,200
32	±RD Time Min.	00	00	00	00	00	00	00	00	5,500
33	±RD Time Max.	00	00	00	00	00	00	00	00	70,200,000
34	PREQA Bank Settle	29,720	00	00	29,720	00	29,720	00	00	13,126
35	±SRE# Time	1,521	00	00	1,521	00	1,521	00	00	110,000
36	±ACT Time Min.	19,419	00	00	19,419	00	19,419	00	00	37,600
37	±ACT Time Max.	19,419	00	00	19,419	00	19,419	00	00	20,000
38	ACT to RDCA(MRQA)	19,419	00	00	19,419	00	19,419	00	00	13,126
39	RD to PREQA	1,521	00	00	1,521	00	1,521	00	00	11,214
40	RD to ACT	1,521	00	00	1,521	00	1,521	00	00	20,000
41	VR to PREQA	1,217	00	00	1,217	00	1,217	00	00	33,717
42	VR to ACT	1,217	00	00	1,217	00	1,217	00	00	33,700
43	CDCA Signal After DLL Reset	00	00	00	00	00	00	00	00	30,000

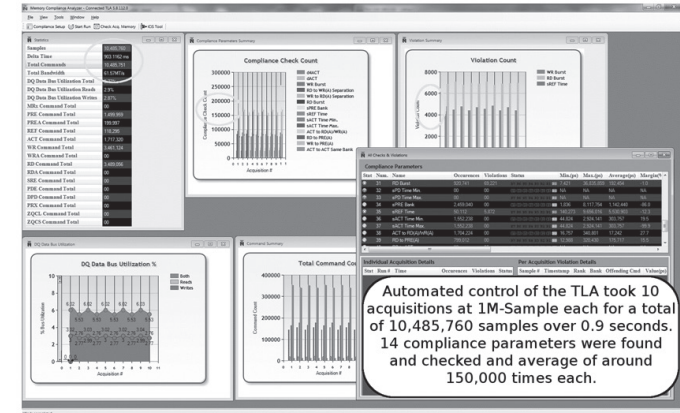
Individual Acquisition Details										
Stat. Name	Time	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)	Spec. Value(ps)
1	10/10/2011 1:30:00 PM	2501	2	00	00	00	00	00	00	1,038,154
2	10/10/2011 1:30:05 PM	2545	3	00	00	00	00	00	00	36,611
3	10/10/2011 1:30:11 PM	2545	3	00	00	00	00	00	00	1,023,172
4	10/10/2011 1:30:16 PM	2552	3	00	00	00	00	00	00	336,695
5	10/10/2011 1:30:21 PM	2620	4	00	00	00	00	00	00	57,402
6	10/10/2011 1:30:26 PM	2630	4	00	00	00	00	00	00	896,874
7	10/10/2011 1:30:31 PM	2543	2	00	00	00	00	00	00	800,650
8	10/10/2011 1:30:36 PM	2646	4	00	00	00	00	00	00	896,811
9	10/10/2011 1:30:41 PM	2637	7	00	00	00	00	00	00	880,706
10	10/10/2011 1:30:46 PM	2666	8	00	00	00	00	00	00	300,000

50

### Individual Event Analysis

51

### Multi-acquisition Automation Session

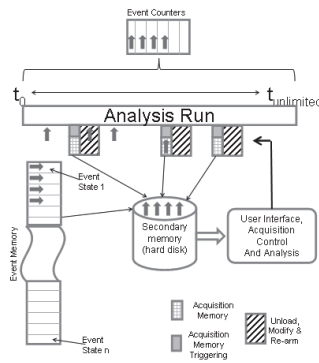


Automated control of the TLA took 10 acquisitions at 1M-Sample each for a total of 10,485,760 samples over 0.9 seconds. 14 compliance parameters were found and checked and average of around 150,000 times each.

52

### Real-time Protocol Compliance Analysis

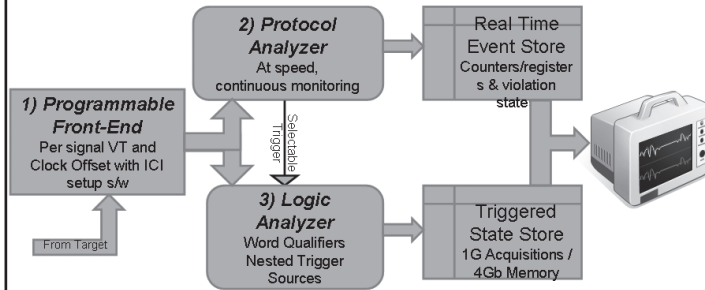
Event Counters and State Memory continue to update **AT-SPEED**, with results displayed in **REAL-TIME**, **While....**



... the Acquisition Memory is unloaded, analyzed and trigger re-armed

53

### Real-time Memory Compliance Analyzer



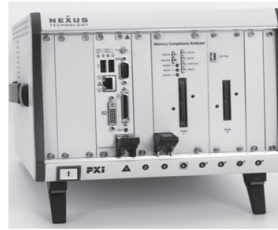
DUAL INSTRUMENT PLUS PROGRAMMABLE FRONT-END

54

## Memory Compliance Analyzer

### REAL-TIME PROTOCOL COMPLIANCE ANALYSIS

- Analysis 160+ categories of JEDEC spec parameters
- Includes Power up/down, self-refresh and auto-precharge (RDA/WRA) analysis
- Timing and State analysis
- HTML reports / XML exporting

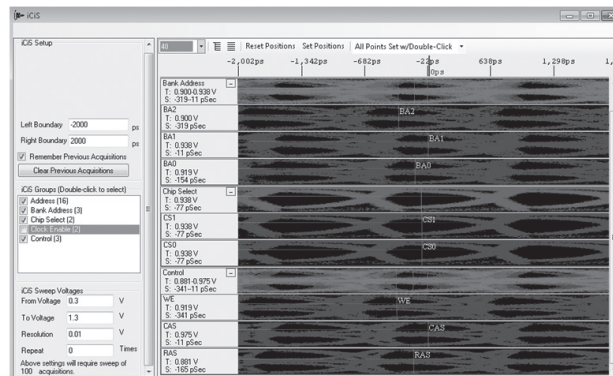


Real-time  
AND  
Post Capture  
Compliance Analysis  
=====  
Command/Address

55

Tektronix®

## Programmable Front-End / High Speed Eye Diagrams



56

Tektronix®

## Automated Analysis Sessions

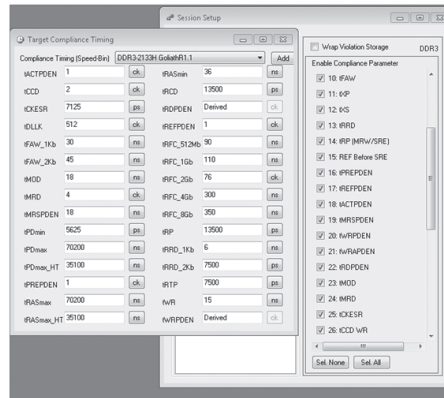
- One or Many Acquisitions / One or Both Analyzers
- Protocol Analysis Session
  - Protocol Analyzer runs until stopped
  - Violations and statistics are reported
- Single Acquisition Session
  - Protocol Analyzer runs until the state analyzer is triggered
  - Violations and statistics are reported.
  - State/Timing data is acquired and available for analysis
- Multi-Acquisition Session
  - Protocol Analyzer runs until the state analyzer is triggered
  - Results are stored in disk memory and analysis is restarted
  - Trigger conditions can be modified mid-session.

57

Tektronix®

### Compliance Timing and Parameter Selection

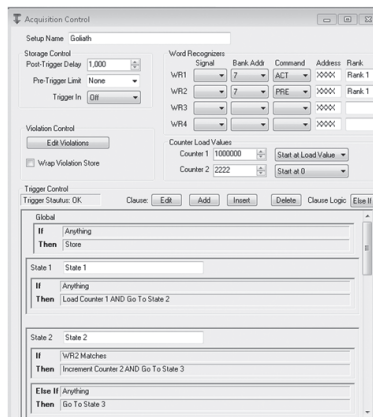
- Spec timing included
- Customize timing per target and margin
- Enable one, some or all violations



58

### Logic Analyzer Acquisition Control

- 8 IF/THEN/ELSE States
- Each State supports multiple AND/OR clauses
- 1 Global Storage qualifier
- 4 Word Recognizers
- 2 Counters



59

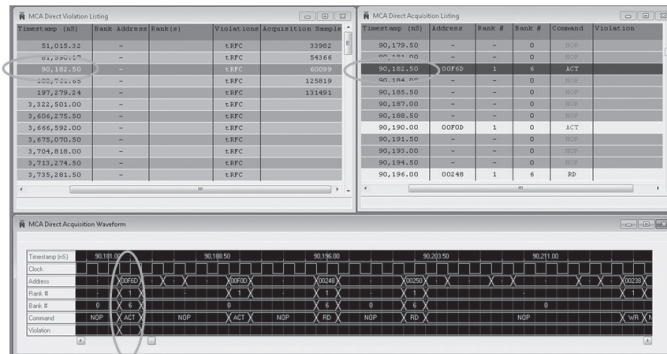
### Real-time Compliance Results

Stat	Name	Occurrences	%Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
22	SRE Separation from RD(A)	00	00	OK	NA	NA	NA	NA	22,488
23	MRS Settle	00	00	OK	NA	NA	NA	NA	22,500
24	MRS Burst	00	00	OK	NA	NA	NA	NA	22,500
25	sSREF Time	00	00	OK	NA	NA	NA	NA	7,500
26	WR Burst	13,386	00	OK	00	168,523	12810238400761000.0	7,200	7,200
27	RD to WR(A) Separation	13,386	00	OK	00	64,028	7031080985578300.0	13,118	13,118
28	PDK Show Exit	00	00	OK	NA	NA	NA	NA	24,000
29	Rank DLL Reset to RD(A)	00	00	OK	NA	NA	NA	NA	858,700
30	WR to RD(A) Separation	22,075	00	OK	00	910,959	3515540420789100.0	26,236	26,236
31	RD Burst	22,075	00	OK	00	164,742	12810238400761000.0	7,200	7,200
32	sPD Time Min.	00	00	OK	NA	NA	NA	NA	5,625
33	sPD Time Max.	00	00	OK	NA	NA	NA	NA	70,200,000
34	PRE(A) Bank Settle	26,236	29	OK	00	947,528	302231015688700.0	13,126	13,126
35	sREF Time	1,527	00	OK	00	5,297,689	838483698867800.0	110,000	110,000
36	sACT Time Min.	19,489	00	OK	00	265,733	249598816484000.0	37,500	37,500
37	sACT Time Max.	19,489	00	OK	00	265,733	13128706057962.0	70,200,000	70,200,000
38	ACT to RD(A)/WR(A)	19,636	00	OK	00	18,969	302231015688700.0	13,126	13,126
39	RD to PRE(A)	15,227	00	OK	00	175,659	82029278164841400.0	11,244	11,244
40	RD to ACT	00	00	OK	NA	NA	NA	NA	29,514
41	WR to PRE(A)	6,217	00	OK	00	154,549	2744082721612700.0	33,722	33,722
42	WR to ACT	00	00	OK	NA	NA	NA	NA	20,614
43	CKEx Signal After DLL Reset	00	00	OK	NA	NA	NA	NA	559,700

Real-time event statistics

60

### Violations and Acquisitions Must Be Time Correlated



61

### Benefits of Real-Time + Post Capture

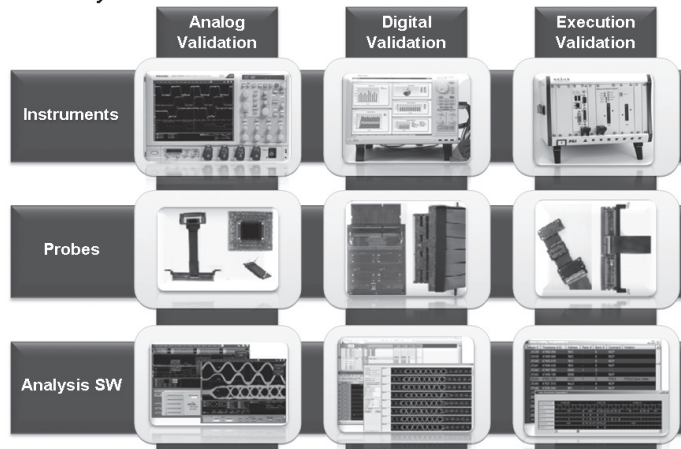
	ACC (Address/Command/Control)	ACC+DQ (Address/Command/Control/Data)
At-Speed / Real-Time	MCA	MCA+LA
Post Capture		LA

MCA Advantages	LA Advantages
Capture Depth 1Gcycles	State Capture of ALL DDR Signals
Cost	20ps High Speed Timing / MagniVu
PA Real Time + LA State Analysis	Analog Mux
	Multi Bus Cross Correlation

62

### Memory Validation Continuum



63