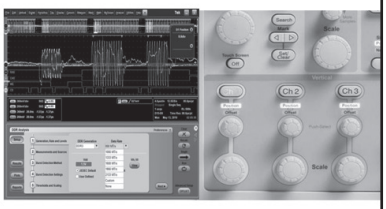
Memory Interface Verification and Debug

Customer Presentation
Version 1.0



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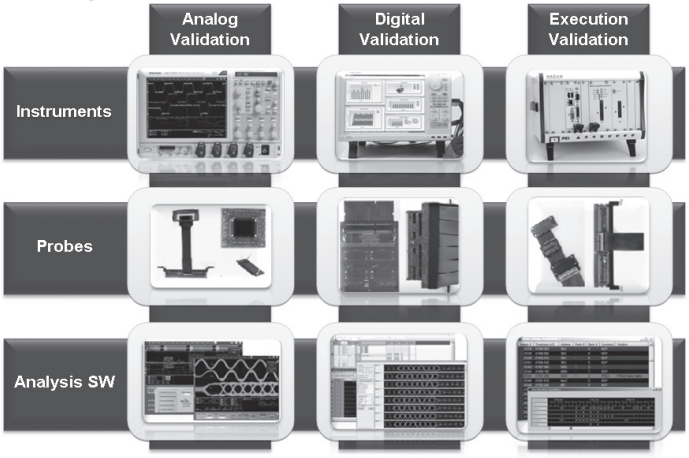
Memory Validation Continuum



2

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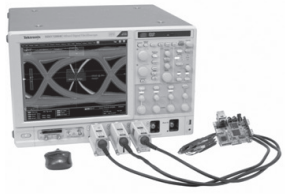
Memory Interface Analog Validation

Measure the analog signal characteristics; trtf, Vmin/max, jitter, eye size, crossover, strobe/clock alignment, etc.



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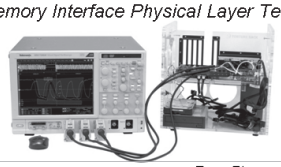
DDRA Features and Benefits

Complete Solution for Memory Interface Physical Layer Test



Feature	Benefits
Memory Validation and Debug	Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3 the newest standards targeted for Server/Computer and Mobile handsets.
Selectable Speed Grades	Support for various JEDEC specification defined speed grades as well as custom speeds
Auto Configuration Wizard	Easily set up the test configuration for performing the analysis.
Qualified Multi-Rank Measurements	Isolate measurements to a rank of interest by using the chip select signal in a multi rank configuration
Cycle Type Identification	Navigate and Timestamp all the READ and WRITE cycles in an acquired record using Search and Mark
Visual Trigger / Pin Point Triggering	Quickly trigger, isolate and capture events of interest with Pin-Point HW Triggering combined with Visual Trigger and Active Search and Mark capabilities in Tektronix Oscilloscopes, making them an indispensable tool for Memory Interface Validation.
De-embedding	De-embed the effects of the Interposers and Probes to provide more accurately representation of the signal.
Test Selection	Provides the ability to select the Memory specification and the Speed Grade against which the analysis needs to be done as well as individual tests or group of tests to perform targeted analysis.
Reporting	Automatically generate consolidated reports that include pass/fail results, statistical measurement information as well as details about the test setup
Conformance and Debug	Quickly switch into debug mode in case a system fails conformance tests and use the DPOJET jitter analysis package
Probing Solutions	P7500 Trimode Probe Family and Micro-Coax Tips combined with Nexus Technology Interposers for various memory standards and packaging types results in a complete probing system that provides easy access to memory interface signals and allows making differential, single-ended, and common mode measurements accurately and definitively
Digital Channels on MSO	Address/Command signals acquired on the digital channels of the Mixed Signal Oscilloscope can be used to precisely qualify bus cycles or events of interest as well as perform timing measurements
Analysis and Debug Tools	Tektronix provides a broad range of tools for Electrical Test, Logic Debug and Execution Validation.

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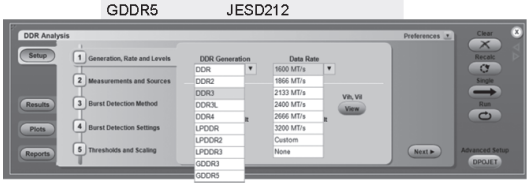
Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings
- JEDEC Standards specify measurements & methods

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212



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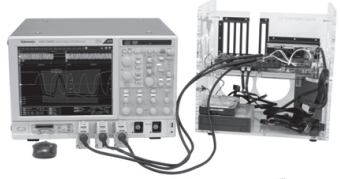
Oscilloscope Bandwidth Requirement

Memory Technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s
Max slew rate	5	5	5	10	12	12	8	16
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8
20-80 risetime (ps)	216	150	150	60	50	45	45	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0
Recommended Scope BW (Max Performance)	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16
Recommended Scope BW (Typ Performance)	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5

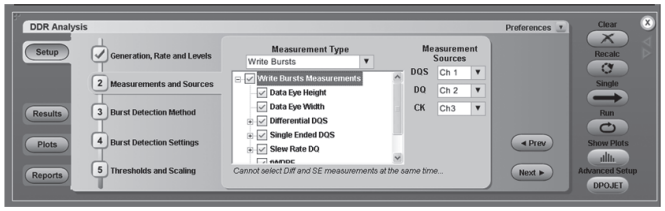
- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 and LPDDR3 is supported only on DSA/MSO/DPO70000C/D models only



6 www.tektronix.com/ddr Tektronix

Test Setup and Configuration

- All the tests are logically grouped based on the input source requirement
  - READ
  - WRITE
  - CLOCK
  - ADDR/CMD
- Quickly set up the test configuration by selecting a complete group or individual tests for targeted analysis.
- Flexible input source requirement, inputs are not hardwired to a particular Oscilloscope channel.



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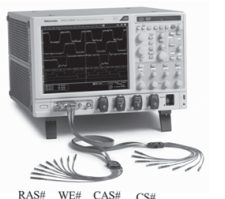
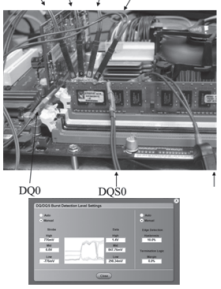
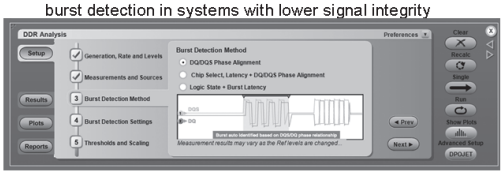
Burst Detection

- Read / Write bursts are automatically detected for analysis purposes
- Several different techniques are used for Read/Write Burst Separation
  - DQ/DQS phase alignment: DQ and DQS have different phase relationship in Read and Write bursts
  - CS, Latency + DQ/DQS Phase Alignment: CS is used to quality the occurrence of a burst, followed by DQ/DS phase relationship to distinguish between Read/Write
  - Logic State + Burst latency: The command bus probed using the digital channels on the MSO is used to identify Read/Write commands on the command bus are quality and distinguish Read and Write bursts
- Options are provided to adjust the levels to improve burst detection in systems with lower signal integrity







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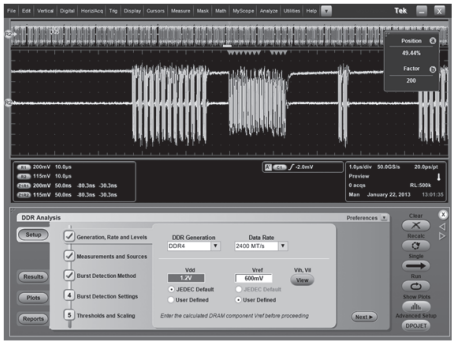
Burst Detection

- Easily Identify, Mark & Measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL Reads/writes within an acquisition



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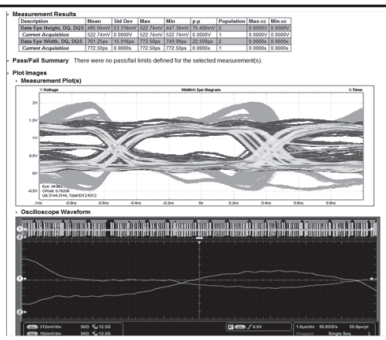
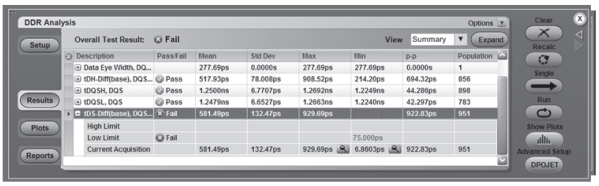
Reports

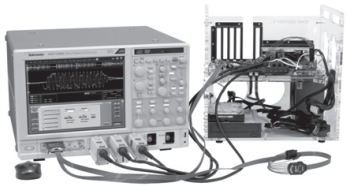
- Analysis results are compiled into an HTML report enabling easy report management and distribution.
- Report includes
  - Measurement results
  - Pass/Fail test results based on specification values
  - Summary and detail plots
  - Oscilloscope screenshots
  - Measurement and Instrument configuration summary
- Report contents are user definable content
  - Provision to append more results later





Beyond DDRA

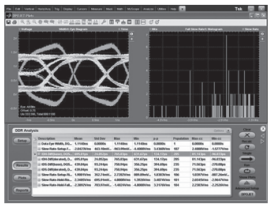
- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
  - DPOJET advanced Jitter analysis toolkit
  - PinPoint Triggering
  - Visual Trigger
  - Mask Testing
  - Advanced Search and Mark



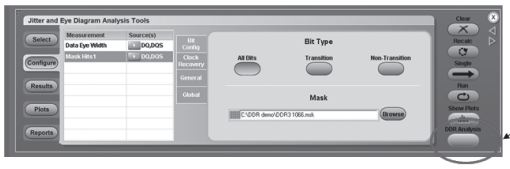
Signal Analysis & Debug

DDRA + DPOJET

- DDRA is not a closed tool – seamlessly links directly to DPOJET for measurement analysis
- Opportunity to change or fine-tune settings, add new measurements as needed



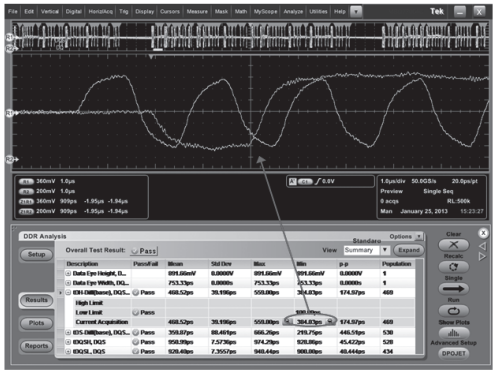
- DPOJET - powerful measurement engine for DDRA
- All settings are explicit – you can see them and change them.



"One Click" access to DPOJET & back

DPOJET Debug Tools

- "Find Worst Case Events" feature
  - Zoom to waveform from Min / Max for each measurement



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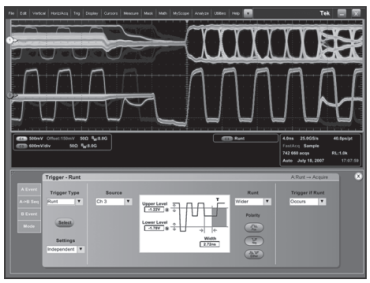
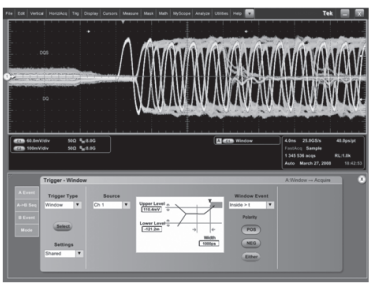
Pinpoint Triggering

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex signaling
  - DPX (FastAcq) and Pinpoint Triggering gives you "the power to see what others can't"
  - FastAcq shows any disparities on signals, like infrequent glitch's





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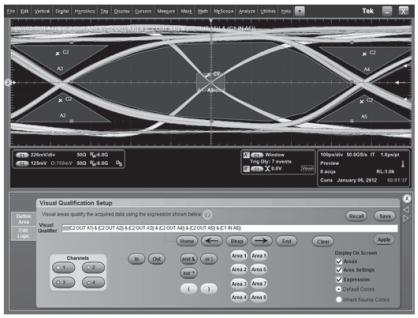
Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 verticies
- Areas are "keep in" or "keep out" and can be applied to either trigA or trigB.
- Can be used to
  - Separate Read / Write Bursts
  - Separate ranks
  - Look for pattern dependencies
  - Enable persistence eye diagrams



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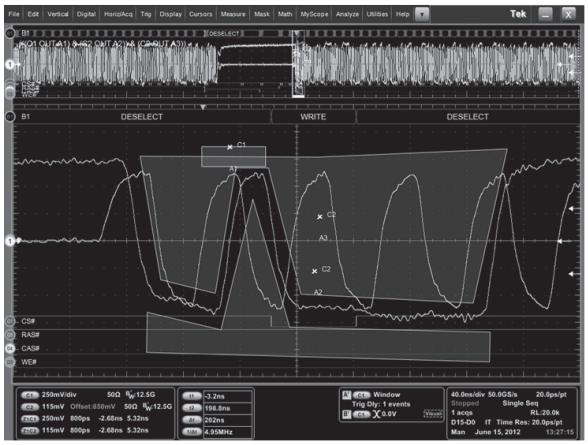
Visual Trigger Used For DQ Pattern Detection

010000X Pattern



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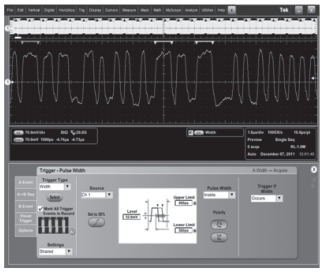
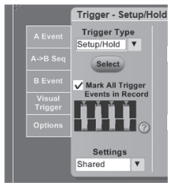
Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
  - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
  - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA





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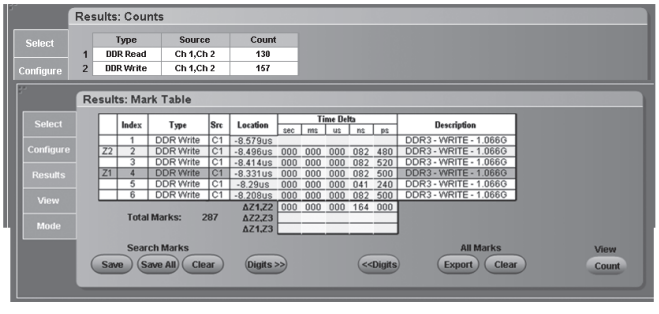
Advanced Search and Mark

- Tabular Results and Navigation
  - Events by Type – read/write or other events
  - Time stamps, delta-times between events
  - Intuitive navigation – Zoom on the burst of interest
- 'Stop on Found' works as a pseudo-trigger mode



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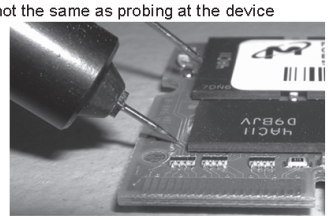
Memory Probing

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- Memory Components use BGA or PoP Packages
  - Reduces the parasitics, enabling performance at higher speeds
  - Mandate from JEDEC
- Probing a BGA or PoP package is Difficult
  - Unable to probe at the Balls of the Device
  - Probing at a connector, trace, or a via is not the same as probing at the device
  - Not a true representation of the signal



*Courtesy Micron Technologies

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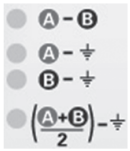
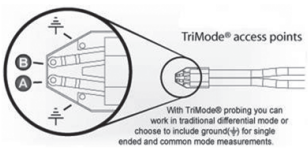
TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements: ((V+) + (V-))/2 with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!





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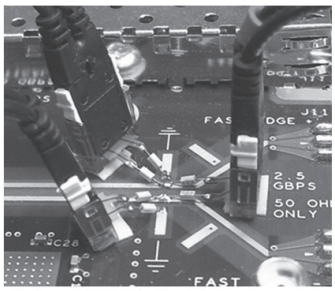
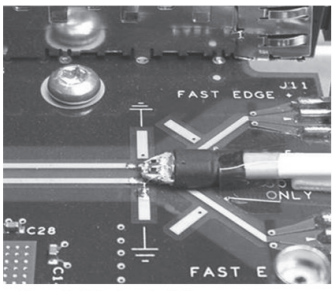
Before and After



Before TriMode Probing
1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode



After TriMode Probing
1 Probe and 1 setup for
Differential, SE and Common Mode

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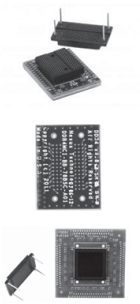
Memory Component Interposers

- Provide easy access to signals of Interest
- Controller Impedance path with embedded resistor for good signal Integrity
- De-embed filters to remove effects of interposer tap trace
- SPICE model available upon request for simulation and analysis

Memory Standard	Supported Form Factors	Interposer Types
DDR2	- BGA	- Socketed Interposer - Direct Attach Interposer
DDR3	- BGA	- Socketed Interposer - Direct Attach Interposer - MSO DIMM Interposer - Instrumented DIMM
DDR4	- BGA	- Socketed Interposer - Direct Attach Perimeter Interposer - MSO DIMM Interposer - Instrumented DIMM
LPDDR2	- BGA - PoP	- Socketed Interposer - PoP Interposer
LPDDR3	- BGA - PoP	- Socketed Interposer - PoP Interposer
GDDR5	- BGA	- Socketed Interposer - Direct Attach Interposer



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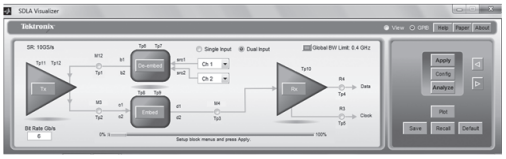
De-embedding

- In order to remove the effects on the Interposer, probe tips and probes de-embedding must be considered.
- De-embedding filters will available for the interposers upon request. These de-embedding filters are developed assuming nominal values
- For more accurate characterization for a particular setup SDLA visualizer for Real time scopes can be used



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Memory Interface Digital Validation

Measure the digital logic state and cycle based timing characteristics for diagnostic and troubleshooting purposes

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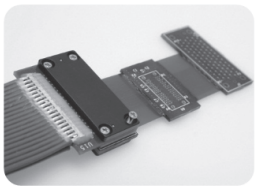
DDR4 Memory Component Interposers

- MCI's are used for probing signals from individual Memory Components
- Comes with a Custom Socket that needs to be soldered to Target system
- Quickly swap TLA & oscilloscope interposers on the same target. Quickly move interposers to different target.
- No special footprints or special routing requirements
- Memory Component Interposer Types
  - Logic Analyzer and Oscilloscope
  - Direct Attach or Socketed interposers
  - x4/x8 and x16 Memory Component types



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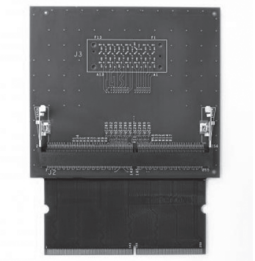
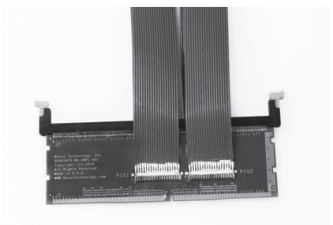
DDR4 ACC Interposers

- Protocol / Execution Validation
  - DIMM and SODIMM Interposers
  - Targeted for protocol compliance analysis
  - Automated Setup
  - Use with Nexus Compliance Analysis S/W
  - Compatible with P6960HCD or NEX-PRB1XL





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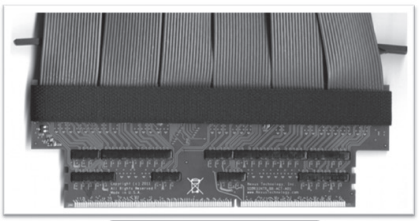
Introducing New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

Gain Unprecedented Visibility Into Your DDR3/4 Signal Activity



DIMM Interposer

SODIMM Interposer

Collaborative design combining years of Logic Analyzer acquisition and DDR3 probing experience between Tektronix and Nexus Technology

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New DDR3/4 High Speed Interposer

Next Generation DDR3/4 Probing Technology

- Provides significant performance improvements to DDR3 probing
  - Integrates Tektronix ultra-high performance SiGe Hybrid ASIC technology
  - Compensation for platform trace loss on writes
- Improved interposer input impedance (5.2k to 0.73V)
  - Reduces load on target with minimal effect on bus
  - Provides an accurate representation of the signal on the target
- Enables probing DDR3/4 speeds at 2400MT/s and beyond
- Enables probing lower voltage signals on LVDDR3/4
- Interposers compatible with UDIMM, RDIMM, LRDIMM

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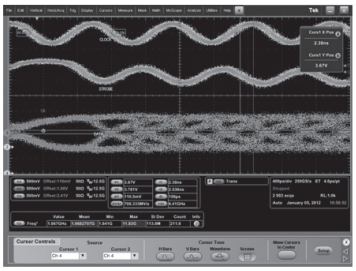
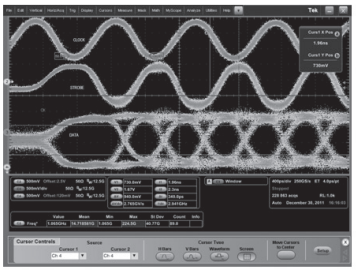
Scope Screenshots at DDR3 2133MT/s – Writes

OLD Interposer

NEW Interposer





ICI's Tool

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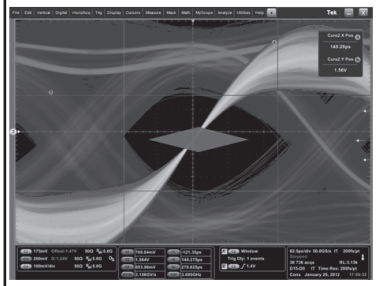
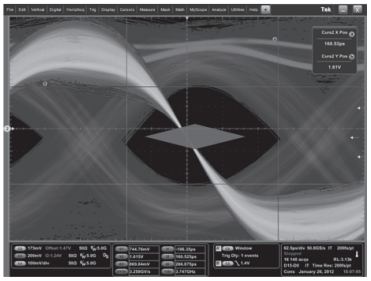
Write Data Eye – DDR3 2400MT/s



Write data eye, rising strobe edge, 853mV x 270ps



Write data eye, falling strobe edge, 869mV x 266ps

Represents minimum TLA7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

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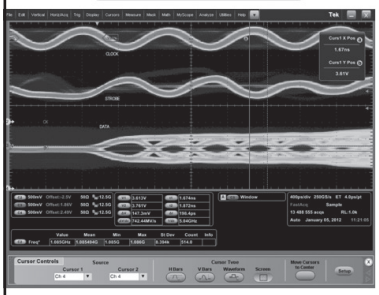
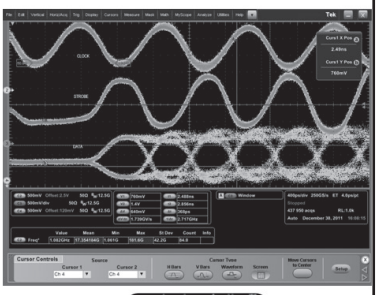
Scope Screenshots at DDR3 2133MT/s – Reads

OLD Interposer

NEW Interposer





ICI's Tool

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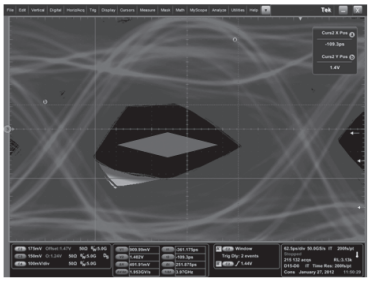
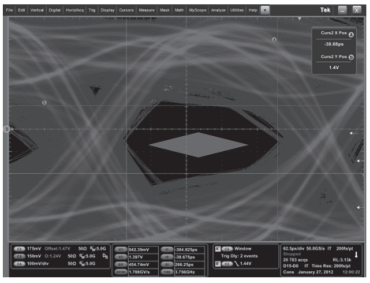
Read Data Eye – DDR3 2400MT/s





Read data eye, rising strobe edge, 492mV x 252ps

Read data eye, falling strobe edge, 454mV x 266ps

Represents minimum 7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

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TLA7BBx Logic Analyzer Modules

Proven Technology for Analyzing DDR3 SDRAM

DIGITAL CHARACTERISTICS	TLA7BB2	TLA7BB3	TLA7BB4
Digital Channels	68	102	136
High Speed Timing (MagniVu)	50GS/s (20ps)		
Deep Memory Timing	Up to 6.4GS/s		
State Speed	Up to 1.4GHz/3.0Gbps		
Memory Depth	Standard 2Mb, Maximum 64Mb		
Probes	All P68xx and P69xx		
iCapture (Analog Mux)	3 GHz		

- Preserve investment in TLA7BBx modules
- Enable higher DDR3 speed support with new interposer

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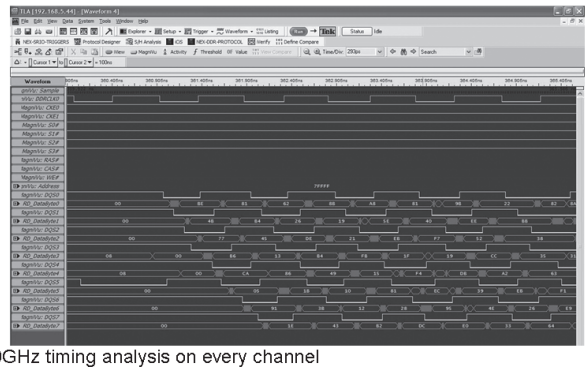
MagniVu 20ps (50 GS/s) High Speed timing

Industry Leading Sampling Resolution



- 50GHz timing analysis on every channel
- Acquired simultaneously and time-correlated with state acquisition data
- Enables acquisition and debug of S/H violations, glitches, and other timing violations
- Reveals fly-by command/address/control bus timing

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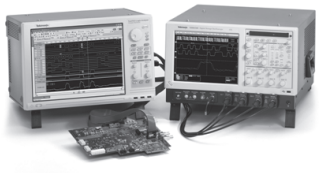
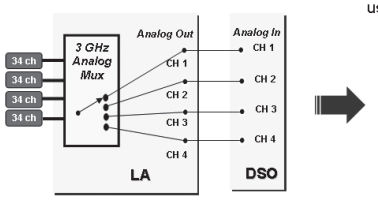
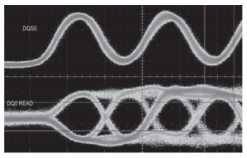
Analog Mux, iCapture

Enables Signal Integrity Troubleshooting



- Unrivaled capability of the TLA that provides single-point digital and analog probing
- No need to separately probe with a scope, as probing done through the interposer
- Walk through all the signals on your DDR bus in less than 15 minutes to review channel behavior and isolate any potential problems
- Quickly perform detailed analog characterization on signals of interest using a scope component interposer





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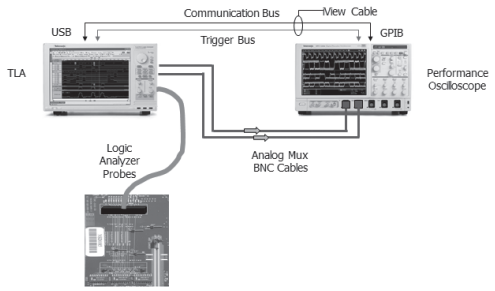
iView

View Correlated Analog & Digital Characteristics in the Same Display

- Unique capability on the TLA that provides time correlated state acquisition, high-speed MagniVu timing acquisition, and analog scope capture results on the same screen.
- Capture events that occur in analog or digital domain through cross triggering
- Enables cross domain analysis by quickly capturing and isolating potential problems



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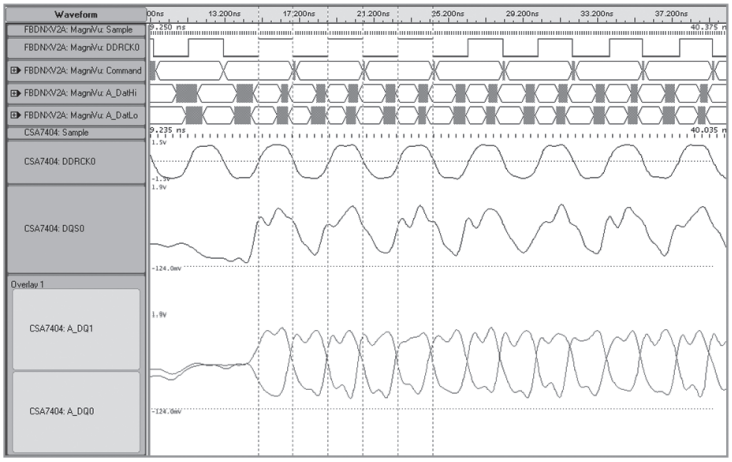
iView

Correlated High-Speed MagniVu Acquisition & Scope Capture Data Example



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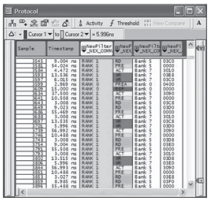
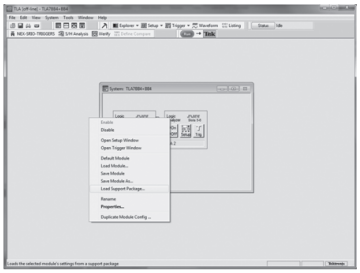
TLA - Initial Setup

- New Fast & Easy Setup
  - Quick and easy connection
  - Fast software setup
  - No calibration needed for CMD/ADDR/CTRL
  - Automated and graphical DQ data calibration
  - Up and running acquiring ALL data in 15-30 minutes!
  - Identify problem channels at the same time!



- Load the TLA Software
- Load the Support Package
- Ready to Acquire CMD / ADDR / CTRL!



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iCis Overview

- Goals of iCiS
  - Make LA memory tuning easier and quicker
  - Less dependency on platform specific DQ valid regions
  - Less dependency on DQS placement
  - Put more power in the users hands
  - Allow both Vth and sample point to be determined at same time
  - Quick check of signal integrity on the memory bus
  - Allow tuning of address and command signals
  - Simultaneous tuning of Read and Write sample points
  - Double mouse click method to set Vth and sample point for all signals
  - Single tuning tool leveraged for DDR3, DDR4, LPDDR2/3
- User control
  - DDR bus parameters
  - Voltage sweep step size
  - Voltage sweep range
  - Which signals to tune
    - Address bit(s)
    - Command bit(s)
    - DQ-byte lane or individual DQ
      - Read & Write, read only, write only

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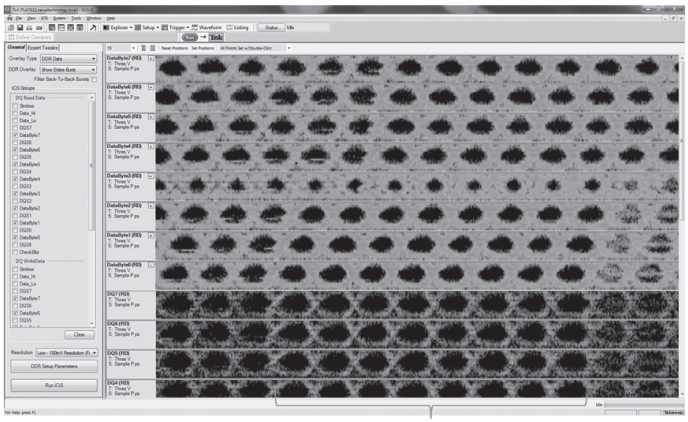
DDR3 Sweep

100mV Resolution, Full Burst Mode / 8 DQ Eyes, Reads



8 valid DQ eyes

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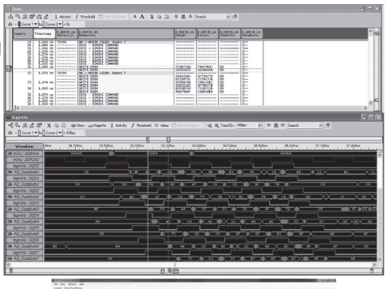
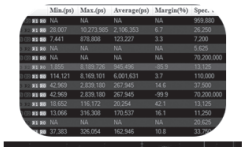
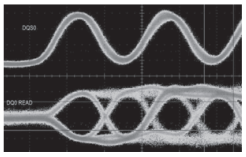
TLA Data Analysis

- State, MagniVu timing, & analog mux at your fingertips
- Compliance analysis tools
  - Fast setup
  - Comprehensive coverage and violation detection







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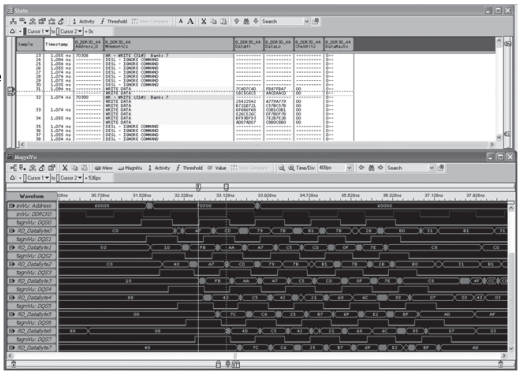
TLA- Example State / MagniVu Display

- Command / Address / Control
- DQ Read and Write Data
- Up to 64M-sample state memory
- Simultaneous 50GHz MagniVu timing



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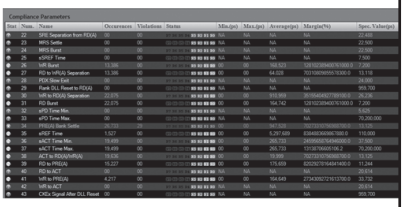
Memory Interface Execution Validation

Measure the bus command and control timing sequences, and compare them to a specification or evaluate them as indicators of bus utilization or performance



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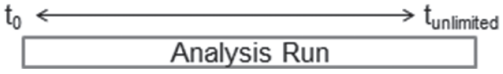
What's unique about Execution Validation

- Typical instrument use a post-capture model

  TRIGGER ➔ ACQUIRE ➔ ANALYZE

- Execution Validation use model



- Two equipment options
  1. Logic Analyzer - S/W automates acquisitions
  2. Memory Compliance Analyzer - Real-time Analysis

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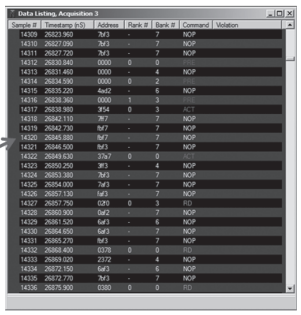
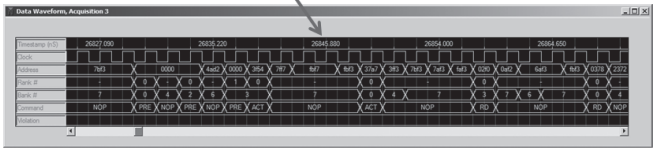
Example Results

Command Timing analysis in both state table and timing views





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Specifications Published in JEDEC Standards

JEDEC STANDARD

JEDEC

DDR3 SDRAM Specification

JESD79-3E

192	Pages
118	Figures
80	Tables

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What specs are checked?

Num.	Name	Description
1	CMD w/oSREF Rank	Sequential check. A non-NOP/DES command can not occur on a self-refreshing rank.
2	SRE w/oACT Rank	Sequential check. A Self-Refresh Entry (SRE) command can not occur on an active rank.
3	MRS w/oACT Rank	Sequential check. An Mode Register Set (MRS) command can not occur on an active rank.
4	RD(A)/WR(A) during MRS	Sequential check. A read (RD or RDA) or write (WR or WRA) command can not occur during rank MRS cycle.
5	CMD w/oPD Rank	Sequential check. A non-NOP/DES command can not occur on a powered-down rank.
6	RD(A)/WR(A) w/oREF Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during bank refresh.
7	ACT/REF w/oACT Bank	Sequential check. A activate (ACT) or refresh (REF) command can not occur on an active bank.
8	REF w/oACT Bank	Sequential check. A refresh (REF) command can not occur on an active bank that is reading or writing.
9	RD(A)/WR(A) to sPRE Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during on an inactive (precharged) bank.
10	d4ACT	The minimum time between any four activate (ACT) commands to the same rank must meet tFAW.
11	PDX Fast Exit	Power-Down Exit (PDX/PR0x) to any valid command (PRE(A)/REF/ACT/MRS) must meet tXP.
12	SRX Exit	Self-Refresh Exit (SRX/PR0x) to any command not requiring a locked DLL (PRE(A)/REF/ACT/MRS/SRE) must meet tXS.
13	dACT	The minimum time between two activate (ACT) commands must meet tRRD.
14	PRE(A) Rank Settle	Minimum time from a PRE(A) command to any valid command on the same rank (MRS/SRE) must meet tRP.
15	REF Before SRE	Sequential check. At least one refresh (REF) command is required between self-refreshed (SRX to SRE).
16	SRE Separation from PRE(A)	If the last valid command received before a self-refresh entry (SRE) was any precharge PRE(A), then the separation between these two commands must meet tRPREPDEN.
17	SRE Separation from REF	If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two commands must meet tREFPDEN.
18	SRE Separation from ACT	If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two commands must meet tACTPDEN.
19	SRE Separation from MRS	If the last valid command received before a self-refresh entry (SRE) was a mode register set(MRS), then the separation between these two commands must meet tMRSPDEN.
20	SRE Separation from tWR	If the last valid command received before a self-refresh entry (SRE) was a write (tWR), then the separation between these two commands must meet tWRPDEN.
21	SRE Separation from tWRA	If the last valid command received before a self-refresh entry (SRE) was a write w/auto-precharge (tWRA), then the separation between these two commands must meet tWRAPDEN.
22	SRE Separation from RD(A)	If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two commands must meet tRDPDEN.
23	MRS Settle	Minimum time from an mode register set (MRS) command to any other valid command that is not an MRS must meet tMOD.
24	MRS Burst	Minimum from the first to the next and subsequent mode register set (MRS) commands must meet tMRD.
25	sSREF Time	The minimum amount of time in self-refresh must meet tCKESR.
26	WR Burst	The minimum amount of time between write (tWR/A) commands must meet tCCD.
27	RD to WR(A) Separation	The minimum amount of time between read (RD) and write (tWR(A)) commands must meet tNRTW.
28	PDX Slow Exit	Power-Down Exit (PDX/PR0x) Slow Exit (MRS_A12 bit low) to read (RD(A) command must meet tXPDLL.
29	Rank DLL Reset to RD(A)	Read (RD(A)) must wait tDLLK after reset.
30	WR to RD(A) Separation	The minimum amount of time between write (tWR) and read (RD(A)) commands must meet tNWTR.
31	RD Burst	The minimum amount of time between read (RD(A)) commands must meet tCCD.
32	sPD Time Min.	The minimum amount of time a rank must stay in power-down (PDE to PDX) must meet tPDmin.
33	sPD Time Max.	The maximum amount of time a rank can stay in power-down (PDE to PDX) must meet tPDmax.
34	PRE(A) Bank Settle	Minimum time from a PRE(A) command to any valid command on the same bank must meet tRP.
35	sREF Time	The minimum amount of time in refresh must meet tRFC.
36	sACT Time Min.	The minimum amount of time a bank must stay active (ACT to PRE(A)) must meet tRASmin.
37	sACT Time Max.	The maximum amount of time a bank can stay active (ACT to PRE(A)) must meet tRASmax.
38	ACT to RD(A)/WR(A)	The minimum amount of time from a activate (ACT) command to a read (RD(A)) or write (WR(A)) command must meet tNARW.
39	RD to PRE(A)	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet tNRP.
40	RD to ACT	The minimum amount of time from a read (RD) command to a activate (ACT) command must meet tNRA.
41	WR to PRE(A)	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet tNWP.
42	WR to ACT	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tNWA.
43	CKEx Signal After DLL Reset	Rank CKEx must remain high tDLLK time after a DLL Reset.

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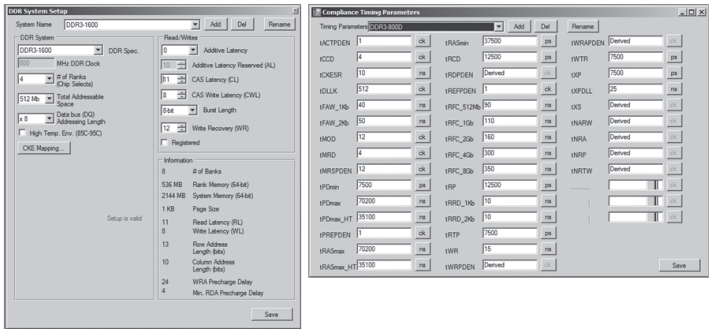
How are the event values set?



- Standard system setups are provided, and can then be modified
- Once the memory system is setup, any timing parameter can be modified

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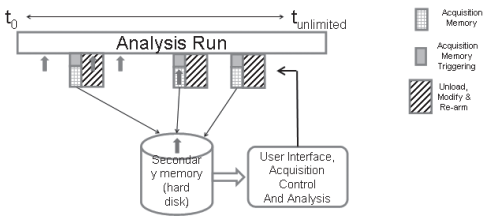
Post-Capture Protocol Compliance Analysis



- LA Memory Compliance Analysis Package enables automated sweeps of multiple transitions, which would result in violation detection over many acquisitions.
- When violations are occurring frequently the likelihood of capture increases and the analysis time decreases.
- However, near the edge of margin envelopes, intermittency increases, resulting in difficulty to observe and capture the event.

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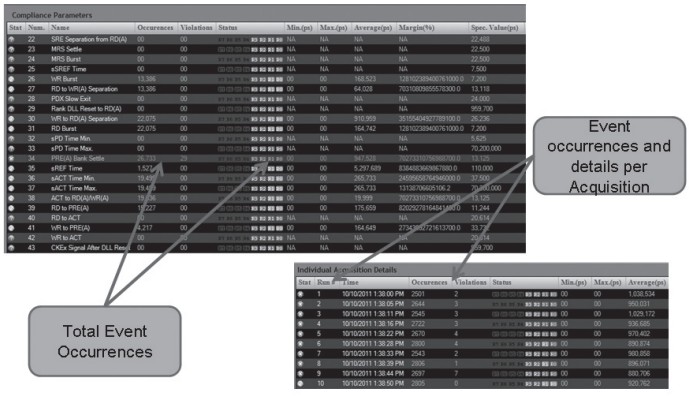
Results per ***Session*** & per ***Acquisition***



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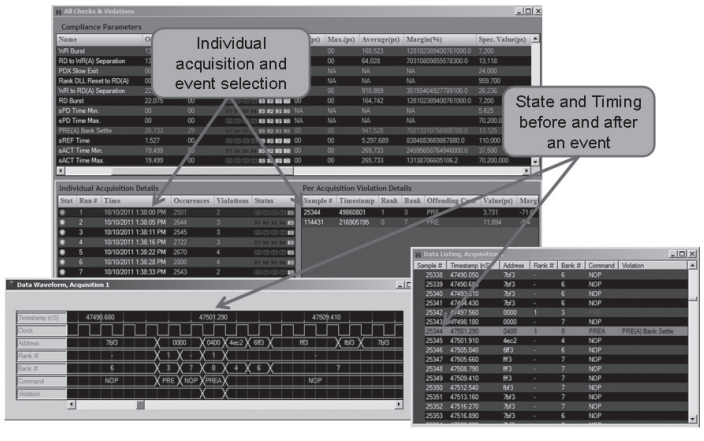
Individual Event Analysis



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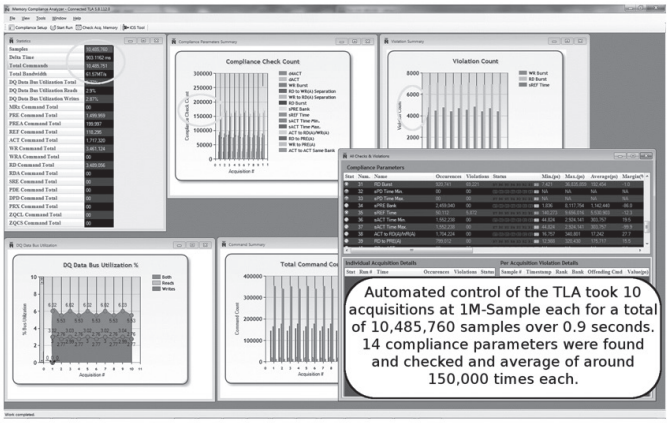
Multi-acquisition Automation Session



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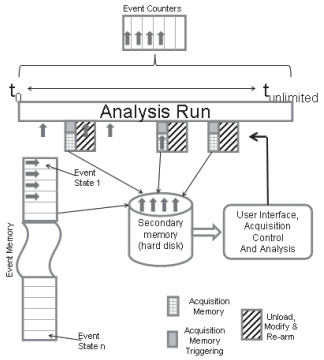
Real-time Protocol Compliance Analysis

Event Counters and State Memory continue to update ***AT-SPEED***, with results displayed in ***REAL-TIME***, ***While….***



…the Acquisition Memory is unloaded, analyzed and trigger re-armed

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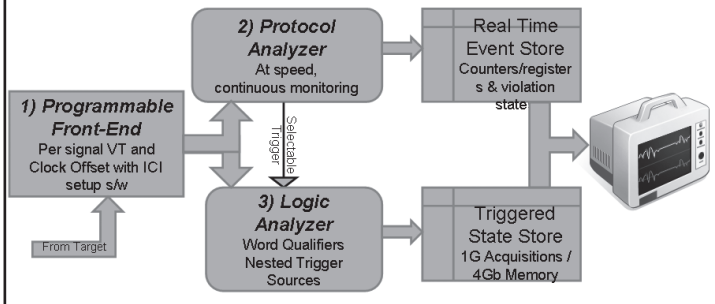
Real-time Memory Compliance Analyzer



DUAL INSTRUMENT PLUS PROGRAMMABLE FRONT-END

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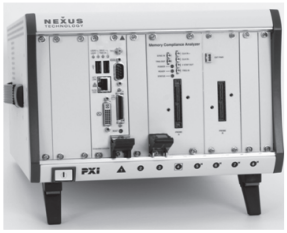
Memory Compliance Analyzer

REAL-TIME PROTOCOL COMPLIANCE ANALYSIS

- Analysis 160+ categories of JEDEC spec parameters
- Includes Power up/down, self-refresh and auto-precharge (RDA/WRA) analysis
- Timing and State analysis
- HTML reports / XML exporting



Real-time
AND
Post Capture
Compliance Analysis

Command/Address

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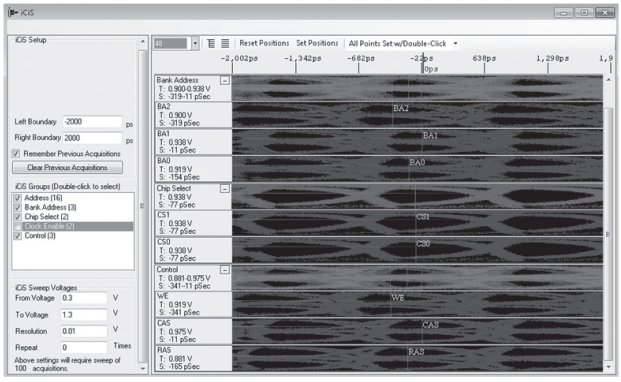
Programmable Front-End / High Speed Eye Diagrams



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Automated Analysis Sessions

- One or Many Acquisitions / One or Both Analyzers
- Protocol Analysis Session
  - Protocol Analyzer runs until stopped
  - Violations and statistics are reported
- Single Acquisition Session
  - Protocol Analyzer runs until the state analyzer is triggered
  - Violations and statistics are reported.
  - State/Timing data is acquired and available for analysis
- Multi-Acquisition Session
  - Protocol Analyzer runs until the state analyzer is triggered
  - Results are stored in disk memory and analysis is restarted
  - Trigger conditions can be modified mid-session.

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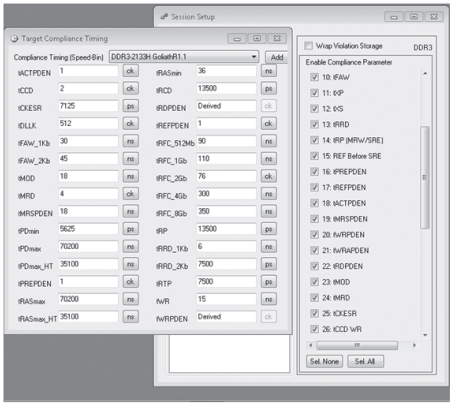
Compliance Timing and Parameter Selection

- Spec timing included
- Customize timing per target and margin
- Enable one, some or all violations



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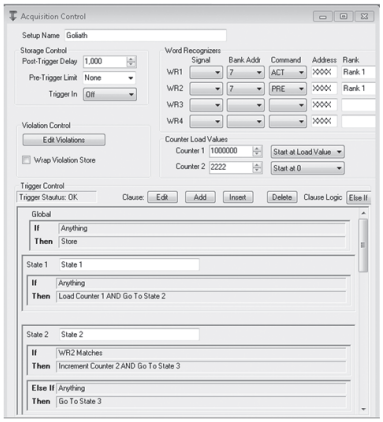
Logic Analyzer Acquisition Control

- 8 IF/THEN/ELSE States
- Each State supports multiple AND/OR clauses
- 1 Global Storage qualifier
- 4 Word Recognizers
- 2 Counters



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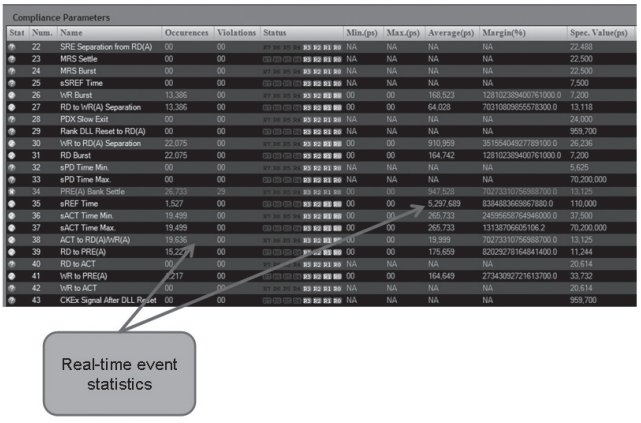
Real-time Compliance Results



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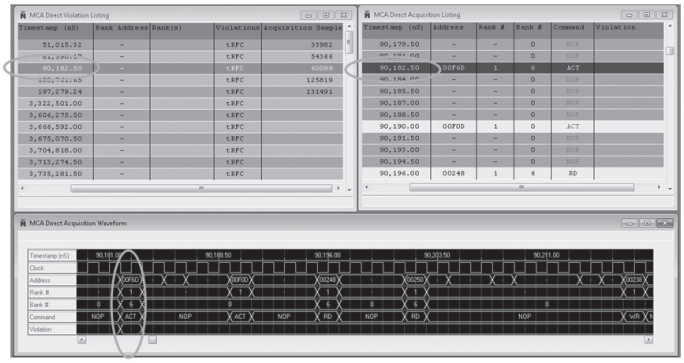
Violations and Acquisitions Must Be Time Correlated



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Benefits of Real-Time + Post Capture

	ACC (Address/Command/Control)	ACC+DQ (Address/Command/Control/Data)
At-Speed / Real-Time	MCA	MCA+LA
Post Capture		LA

MCA Advantages	LA Advantages
Capture Depth 1Gcycles	State Capture of **ALL** DDR Signals
Cost	20ps High Speed Timing / MagniVu
PA Real Time + LA State Analysis	Analog Mux
	Multi Bus Cross Correlation

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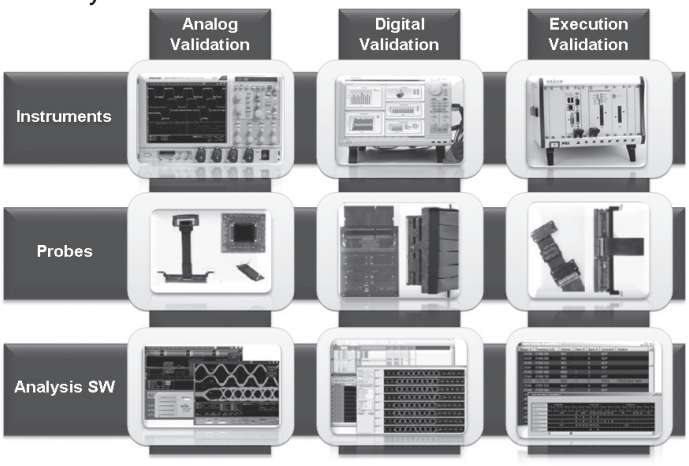
Memory Validation Continuum



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