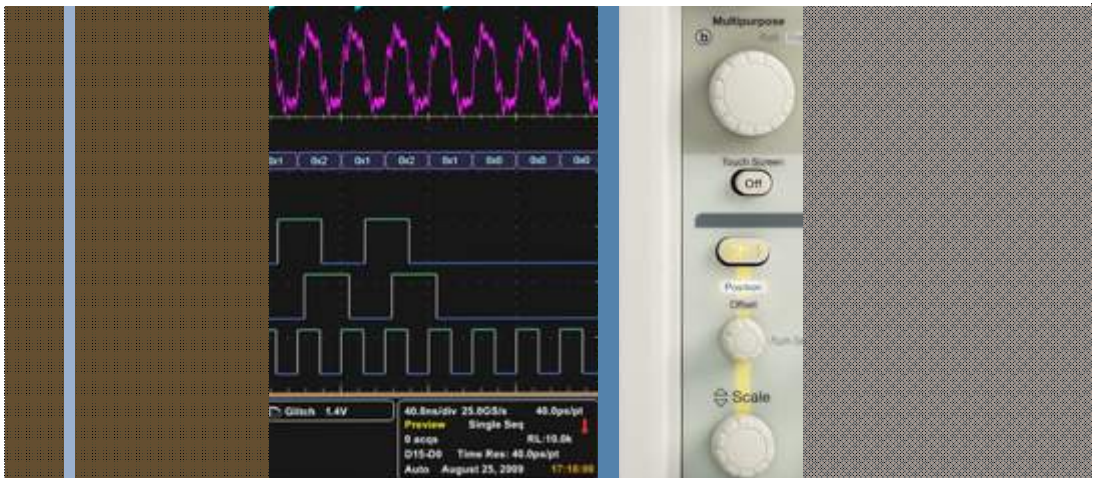
Storage PHY Test Solutions



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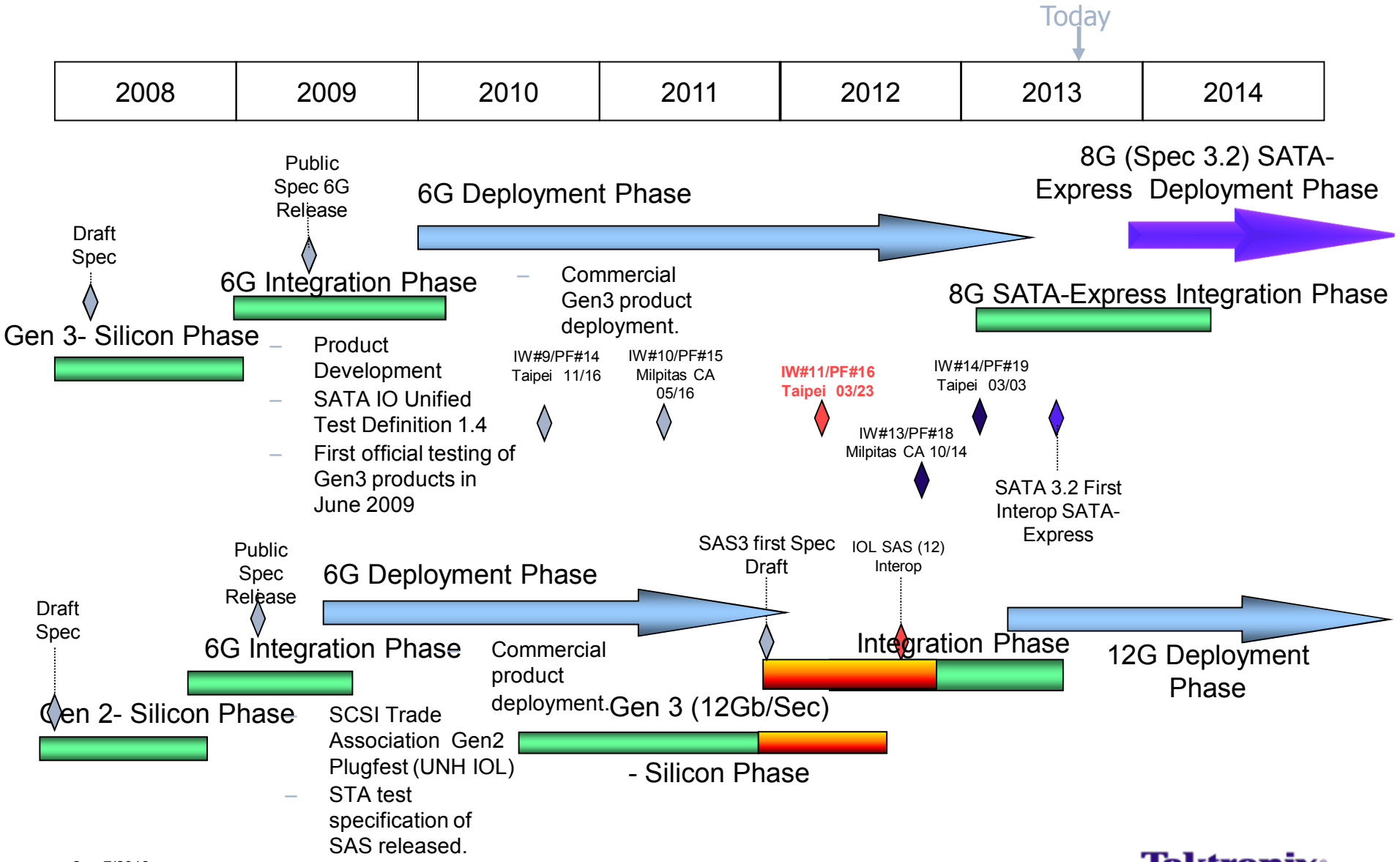
Storage Timelines and Solutions Development



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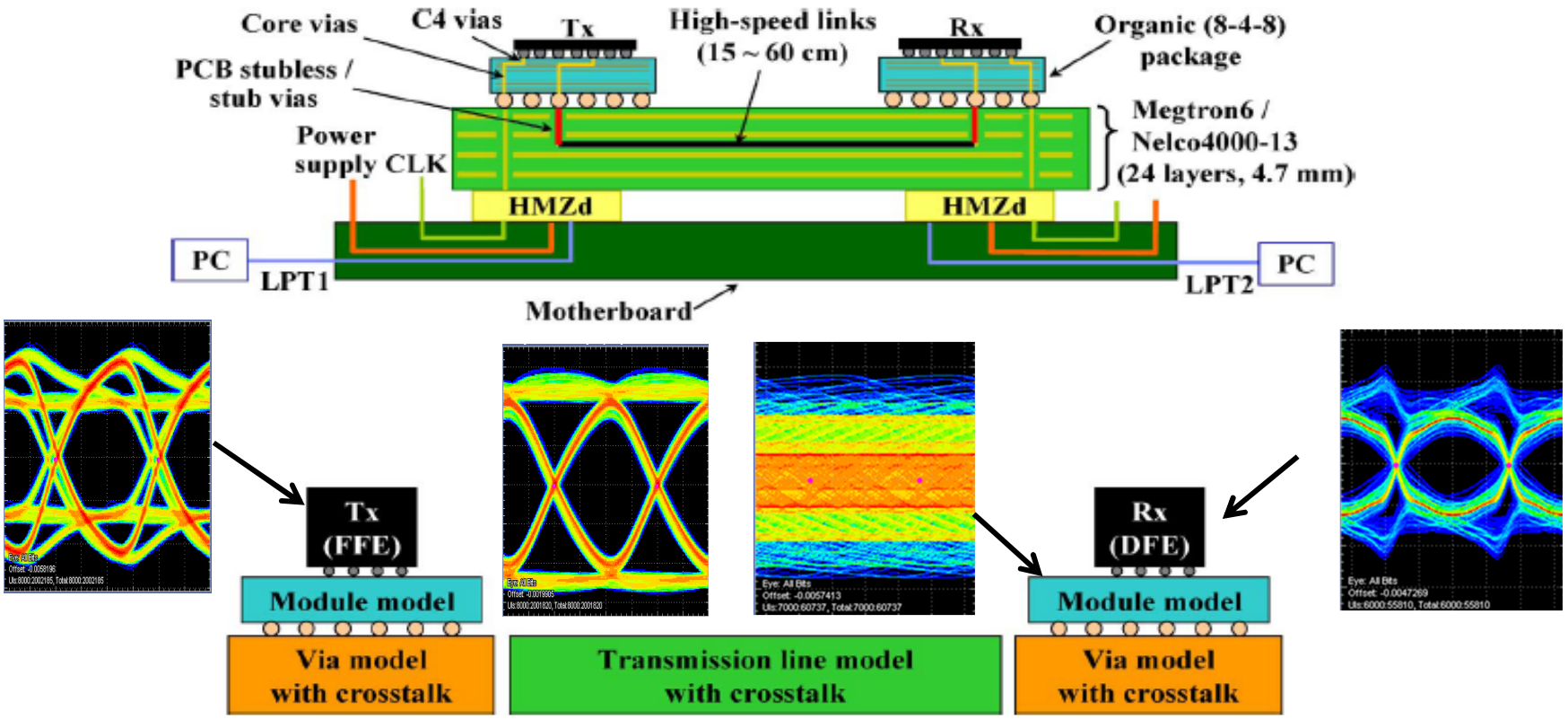
12G+ Design Problem:
1000mV, FFE, Crosstalk, DFE, 50mV

- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.



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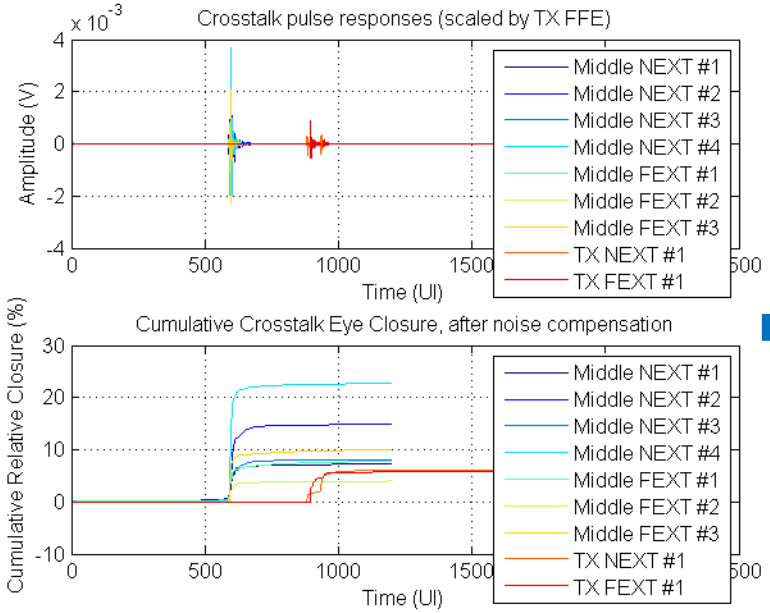
NEW Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization



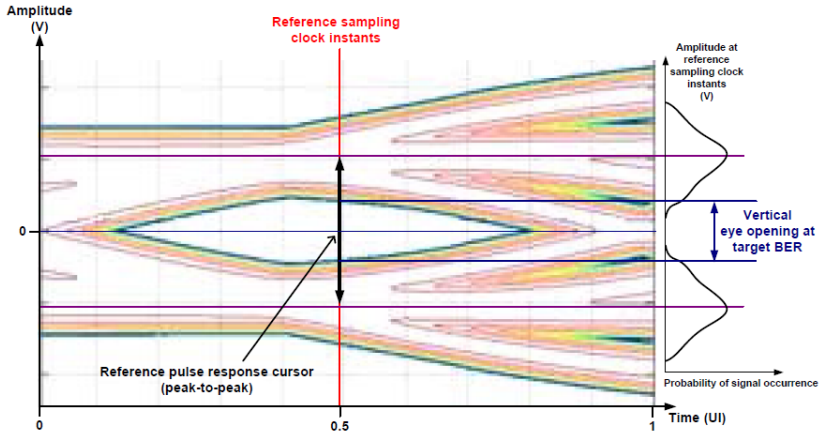


Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

Source: 12-244r3

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

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SAS3_EYEOPENING Provides 4 Different Metrics

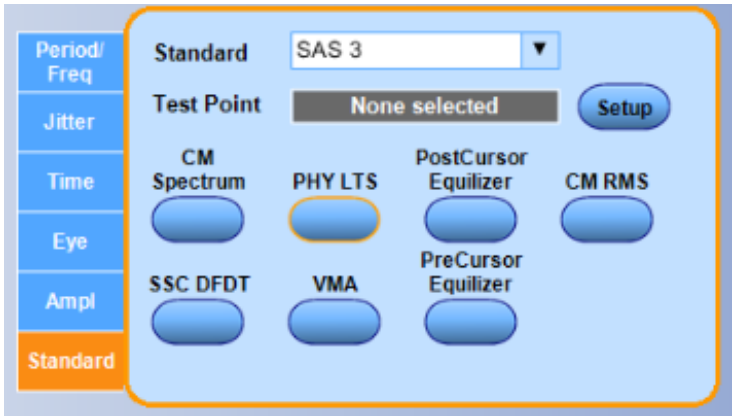
1. **Relative Vertical Eye Opening:** A direct indication of how much margin there is after equalization
   - Takes into account un-compensable ISI and crosstalk
   - ISI and crosstalk broken down in report
2. **Main Cursor Amplitude:** A direct indication of the amplitude after equalization
   - Assumes 800 mVppd max. TX launch amplitude, unless data is captured
3. **Maximal FFE correction**: A direct indication of how much FFE correction is required by the transmitter
   - Max(abs(Cpre/Ccntr,Cpost/Ccntr))
4. **Maximal DFE correction:** A direct indication of how much DFE correction is required by the receiver
   - Max(abs(DFE/Main))

Source: T10/11-234r1

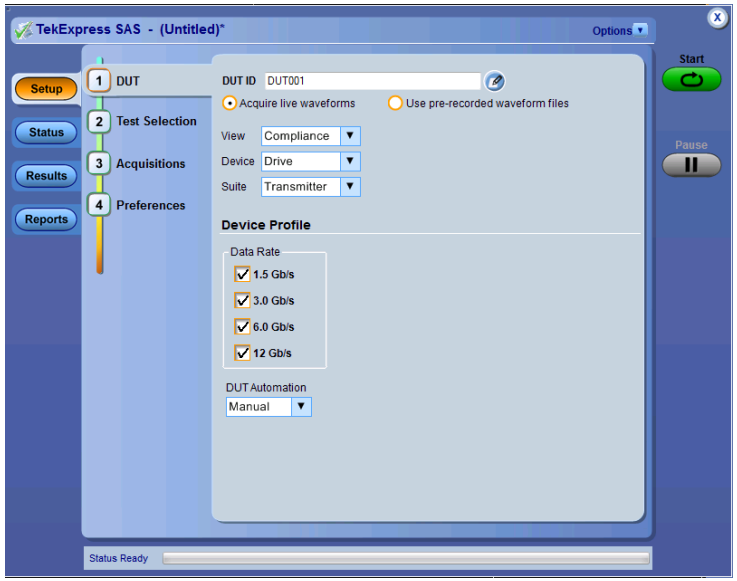
SAS-3 PHY Transmitter Solution – Option SAS3

Group 1 – OOB Signaling	
5.1.1	Maximum Noise During OOB Idle
5.1.2	OOB Burst Amplitude
5.1.3	OOB Offset Delta
5.1.4	OOB Common Mode Delta
Group 2 – Spread Spectrum Clocking (SSC) Requirements	
5.2.1	SSC Modulation Type
5.2.2	SSC Modulation Frequency
5.2.3	SSC Modulation Deviation
5.2.4	SSC Balance
5.2.5	SSC DFDT
Group 3 – NRZ Data Signaling Requirements	
5.3.1	Physical Link Rate Long Term Stability
5.3.2	Common Mode RMS Voltage Limit
5.3.3	Common Mode Spectrum
5.3.4	Peak to Peak Voltage
5.3.5	Voltage Modulation Amplitude (VMA)
5.3.6	Equalization
5.3.7	Rise Time
5.3.8	Fall Time
5.3.9	Random Jitter (RJ)
5.3.10	Total Jitter (TJ)
5.3.11	Waveform Distortion Penalty (WDP)
5.3.12	SAS3_EYEOPENING
5.3.13	Pre Cursor Equalization Ratio
5.3.14	Post Cursor Equalization Ratio
5.3.15	Transition Bit Voltage PK-PK (VHL)
5.3.16	Unit Interval

SAS-3 1.5/3/6/12 Gb/s Tx Test Software



TekExpress SAS3-TSG Automation Software



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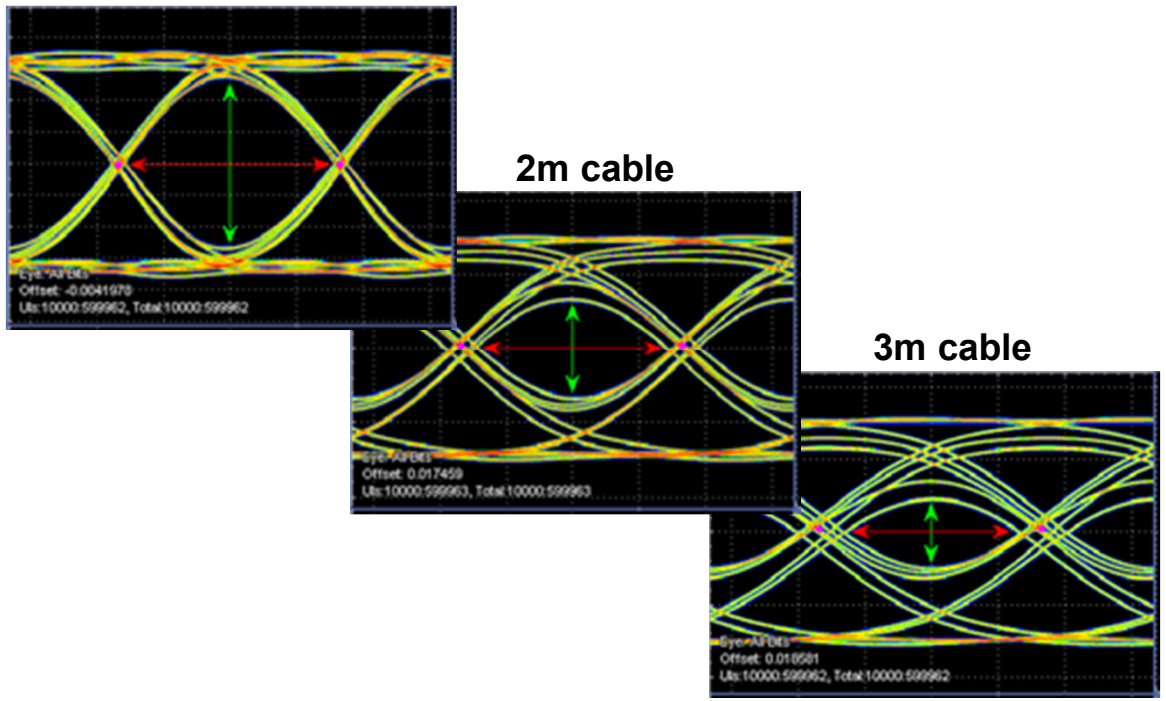
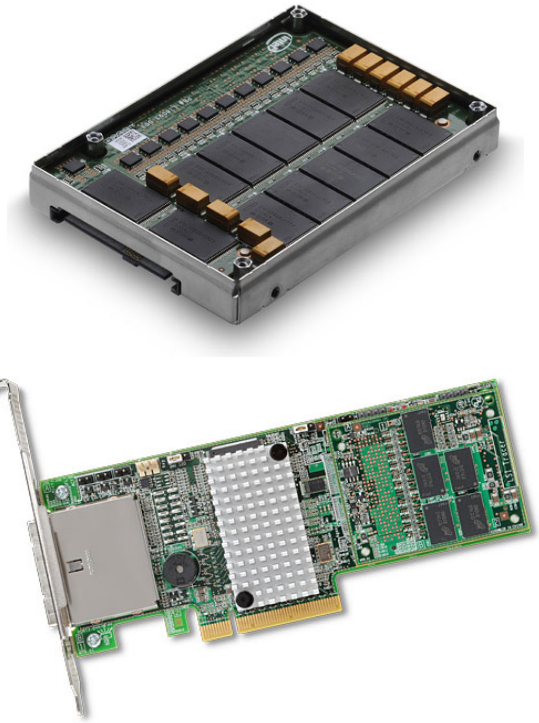
SAS-3 PHY Transmitter Solution – Option SAS3-TSG

- Automated transmitter validation for 1.5, 3, 6 and 12 Gb/s SAS physical layer specification
- Integrated SAS3_EYEOPENING and WDP measurements for accurate analysis of ISI and crosstalk effects and relative vertical eye opening after reference equalization
- Easily reconfigure existing measurements to create user-specified test parameters or test limits
- Multiple plots and measurement configurations provides a quick comparison of the same acquired data with different settings
- Simultaneous two lane testing of primary and secondary ports
- Detailed test reports with screenshots, setup details, and pass/fail limits

Beyond Compliance

- How much margin is there in my design?
- How many DFE/FFE taps are needed to meet the system budget?
- What is longest channel (cable/backplane) the system can tolerate?
- How does process/voltage/temperature affect device performance?





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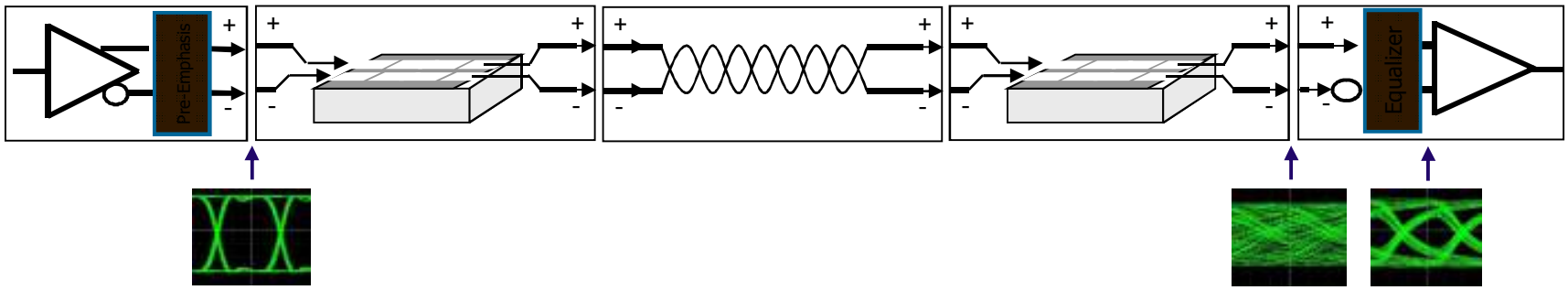
Flexible Link Analysis Tools – option SDLA

- DFE/FFE modeling
  - Reference equalizer vs. vendor-specific
  - Equalizer implementation for PHYs
- Enhanced de-embedding
  - Full four-port network characterization
- Channel emulation for margin analysis



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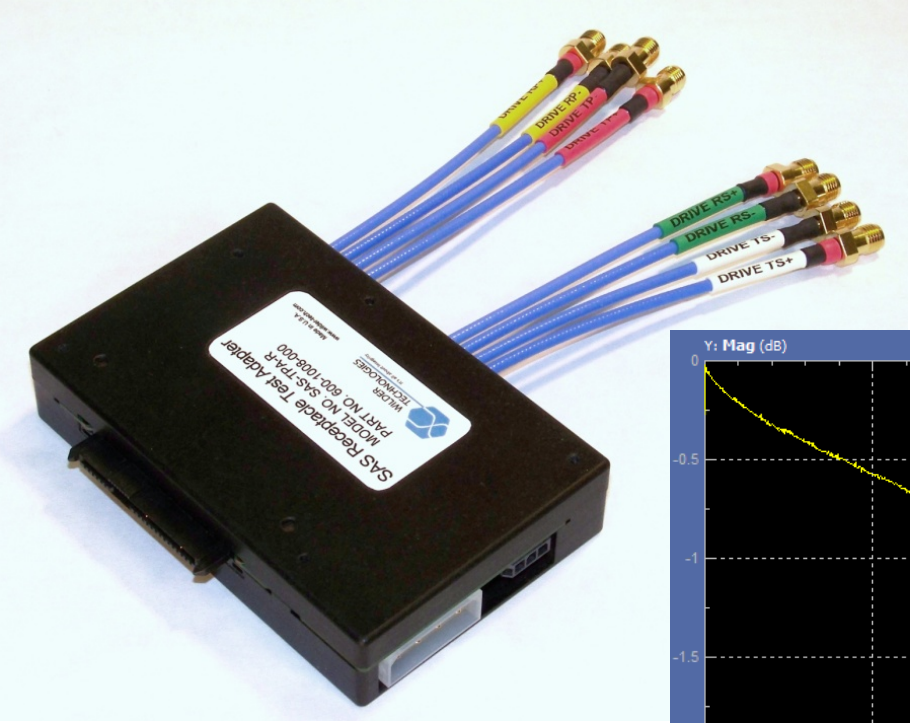
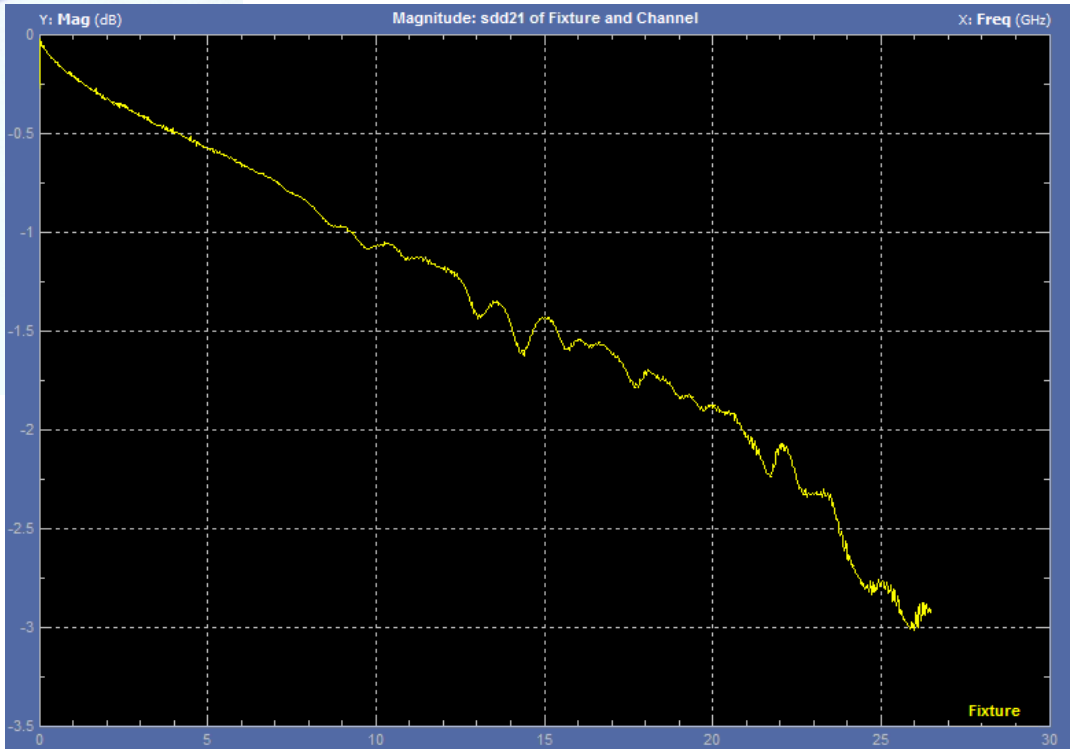
SAS Receptacle Test Adapter



Sdd21 (1x Thru) => -3dB@26 GHz



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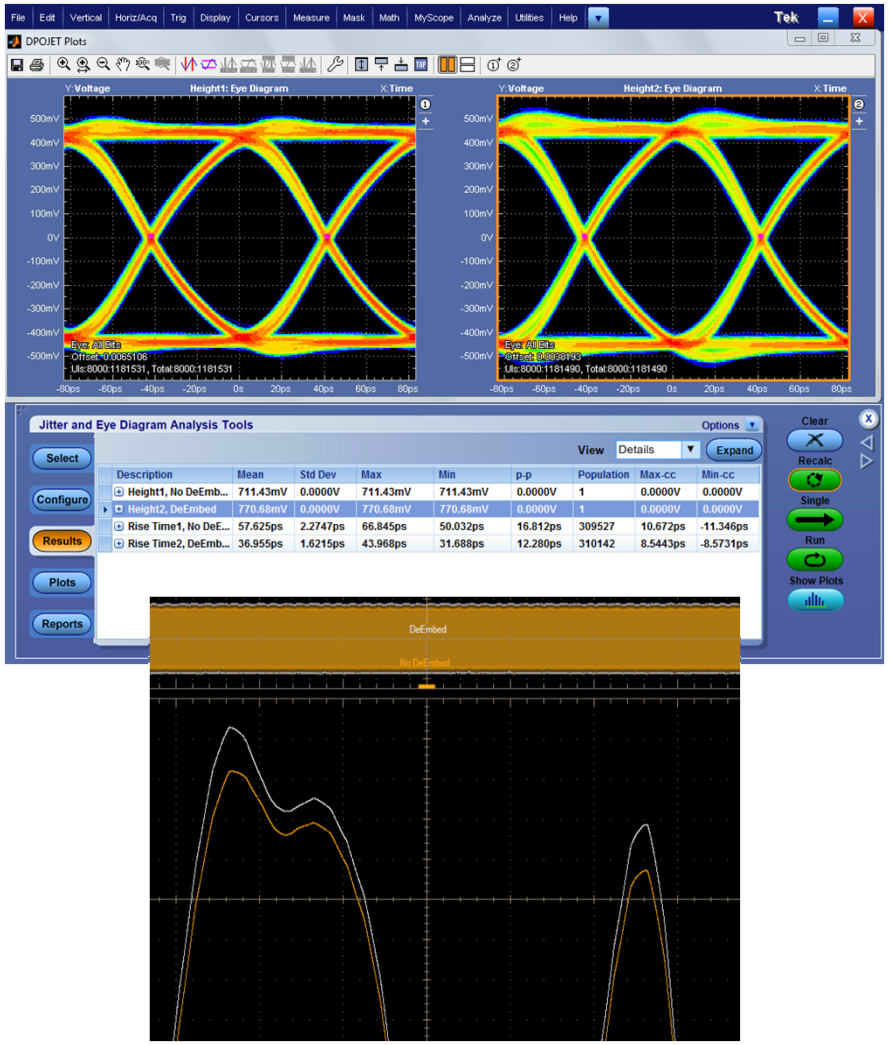
Test Fixture De-embedding

- Why de-embed?
  - Tx measurements referenced to die (ET)
  - Improve margin with removal of fixture effects
- S-Parameters acquired from calibration fixture or model extraction
- Use inverse response to compensate for loss

	Before De-Embed	After De-Embed
Eye Height	711 mV	770 mV
Rise Time	57	37

Before After



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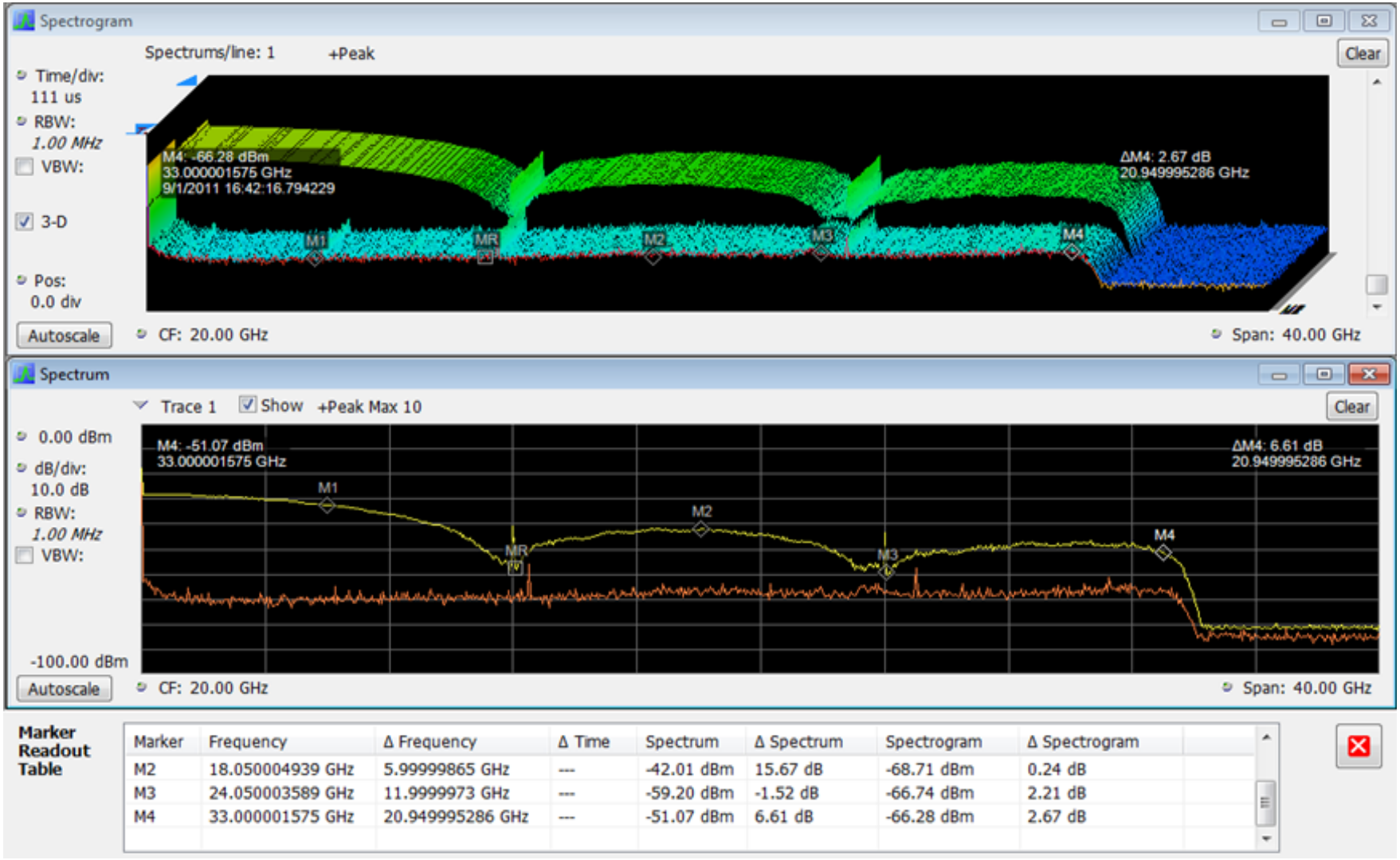
Bandwidth Considerations
SAS PRBS11 12G NRZ Power Spectrum



Marker	Frequency	Δ Frequency	Δ Time	Spectrum	Δ Spectrum	Spectrogram	Δ Spectrogram
M2	18.050004939 GHz	5.99999865 GHz	---	-42.01 dBm	15.67 dB	-68.71 dBm	0.24 dB
M3	24.050003589 GHz	11.9999973 GHz	---	-59.20 dBm	-1.52 dB	-66.74 dBm	2.21 dB
M4	33.000001575 GHz	20.949995286 GHz	---	-51.07 dBm	6.61 dB	-66.28 dBm	2.67 dB

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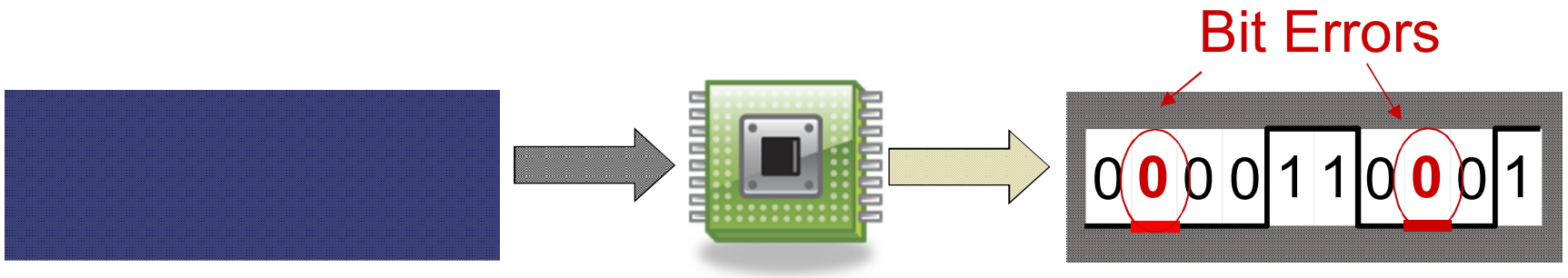
Recommended Equipment

The following components are required for performing SAS12 Tx measurements

- DSA/DPO/MSO70K(C/D) Series Oscilloscope with Opt. 2XL or higher
  - 12.5 GHz or higher recommended for 1.5, 3, or 6 Gb/s
  - 20 GHz or higher recommended for 12 Gb/s
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3-TSG & SAS3-TSGW (required for WDP measurements)
- Test Fixtures:
  - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
  - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
  - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase Matched Cable Set (qty: 2)

SAS Implications for Receiver Testing

- System margins are decreasing, testing the transmitter only does not imply interoperability
- Receiver test requirements are expanding and will include testing with a crosstalk, ISI and Tx/Rx EQ
- Transmitter Equalization requires pre/post-cursor control
- Receiver Equalization is more sophisticated
  - Behavior equalizers (Continuous Time Linear and 5-tap Decision Feedback Equalization) must be used to compensate for channel loss
  - Transmitters must support back channel negotiation to auto-negotiate with Receivers to determine optimal equalization settings for testing



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SAS 12 Gb/s Rx Test Setup

- Similar to SAS 6 Gb/s Rx configuration
- Rx calibration -> CJTPAT -> BER test
- Tektronix Method of Implementation (MOI) provides complete Rx Test procedure

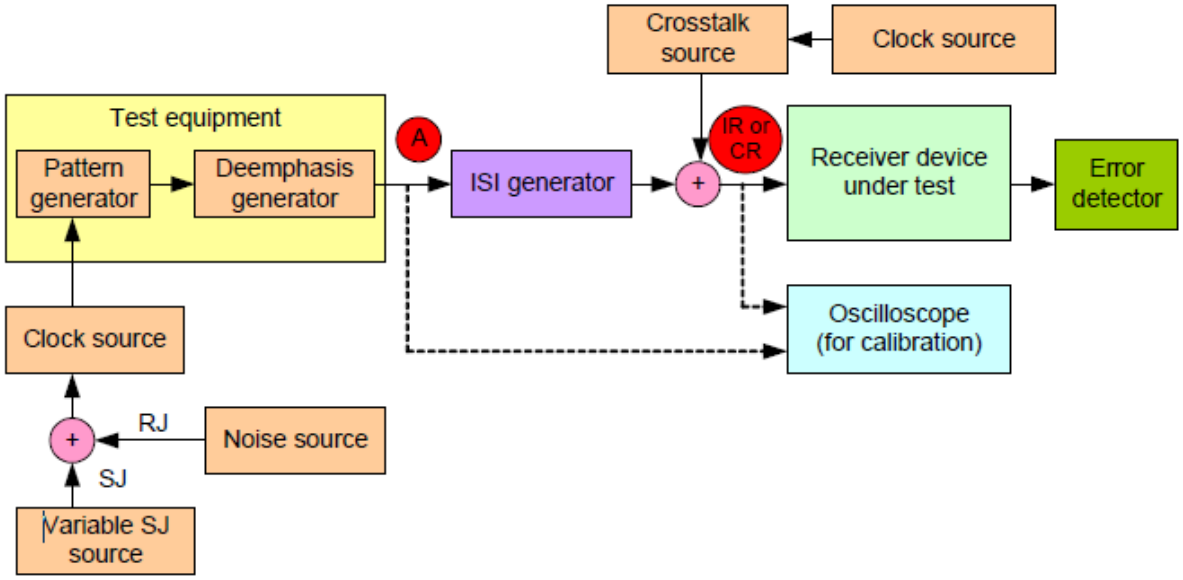
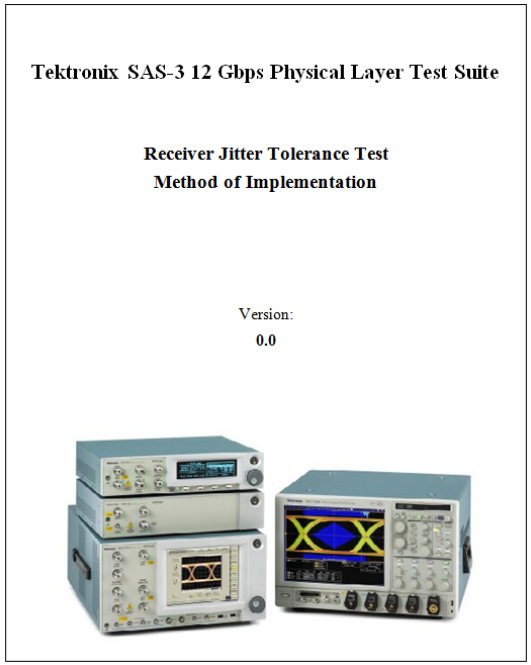


Figure 129 — Stressed receiver device jitter tolerance test block diagram

SAS 12 Gb/s Rx MOI



Source: sas3r03_18Oct2012

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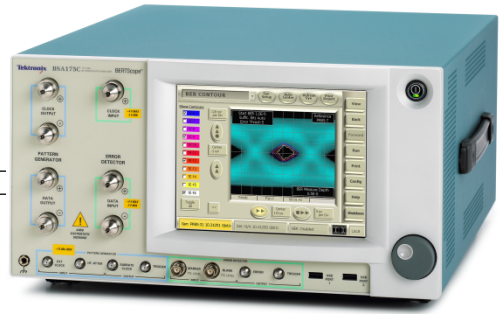
Receiver Test Made Easy with the BERTScope

Stressed Pattern Generator

1

DPP provides pre-emphasis to emulate compliant transmitter



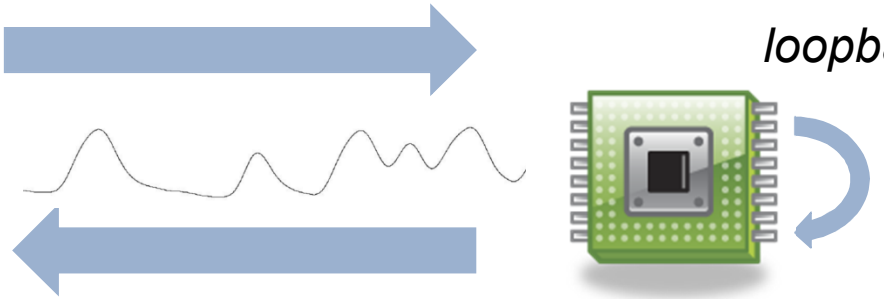
Error Detector

2

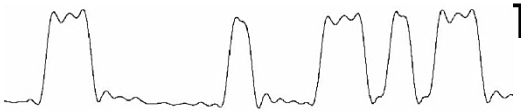
CR recovers a clock from the retransmitted data from the DUT

From Stressed Pattern Generator

loopback



To Error Detector



Device Under Test (DUT)

Bits come back from DUT to **Error Detector** and compared to expected pattern for Bit Error Ratio (BER) measurement

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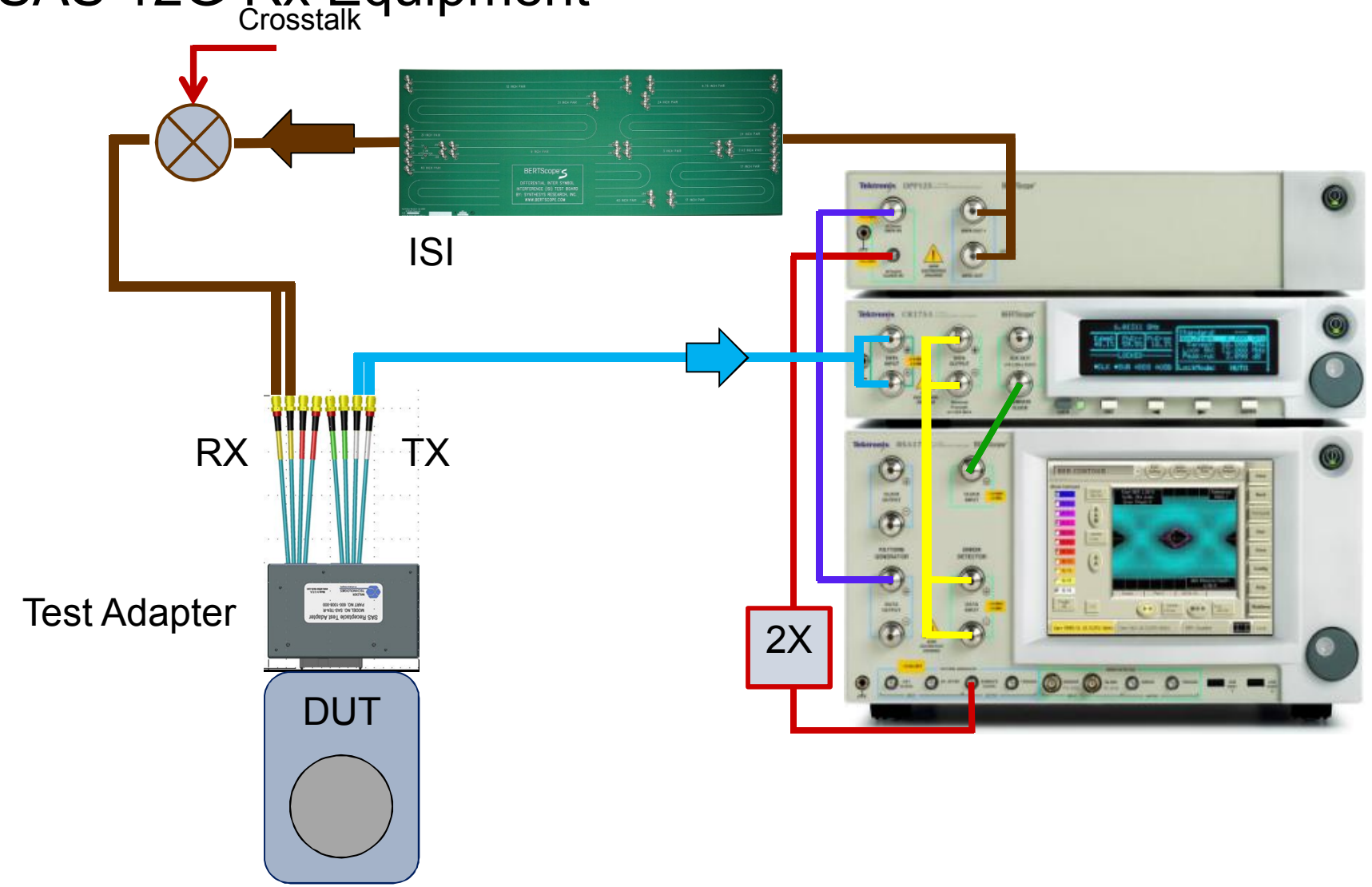
SAS 12G Rx Equipment



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Trained Link for Jitter Tolerance Test

- Complete Rx test exercises both CDR and Tx/Rx EQ capabilities
- Link optimization options
  - Iterate possible Tx/Rx EQ states and apply from 'best' optimized eye
  - Directly apply Preset based on typical configuration for worst case channel

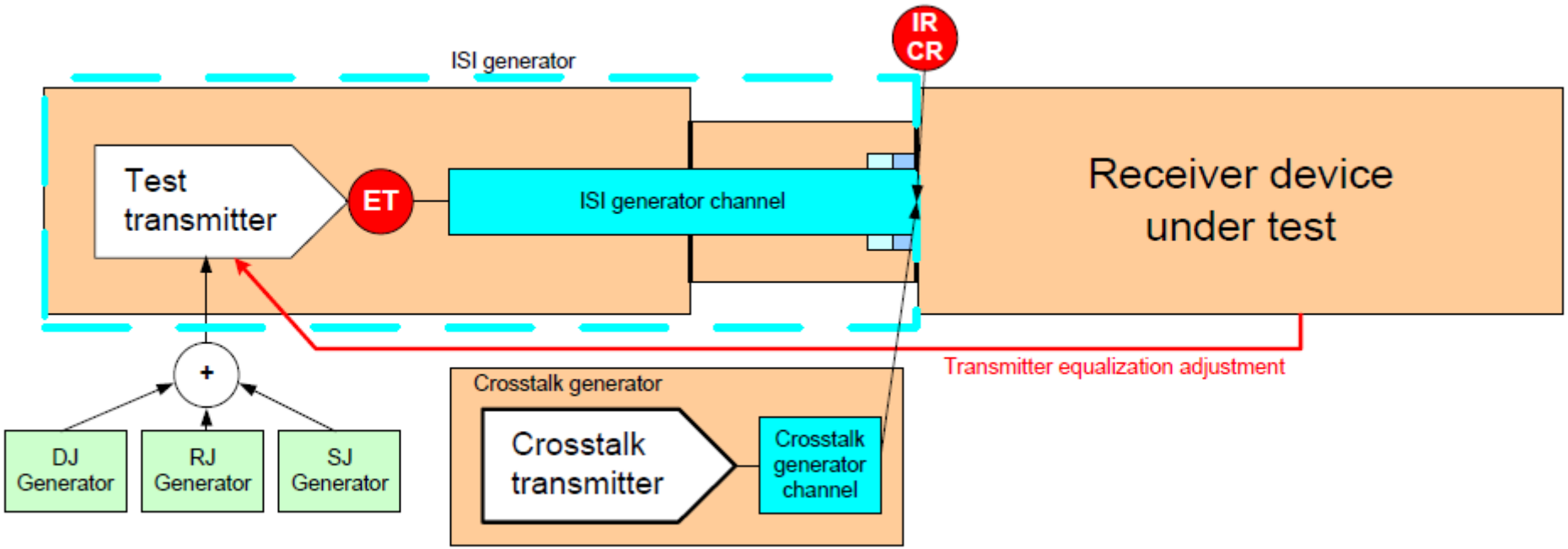

Figure Fh – Stressed receiver transmitter equalization adjustment

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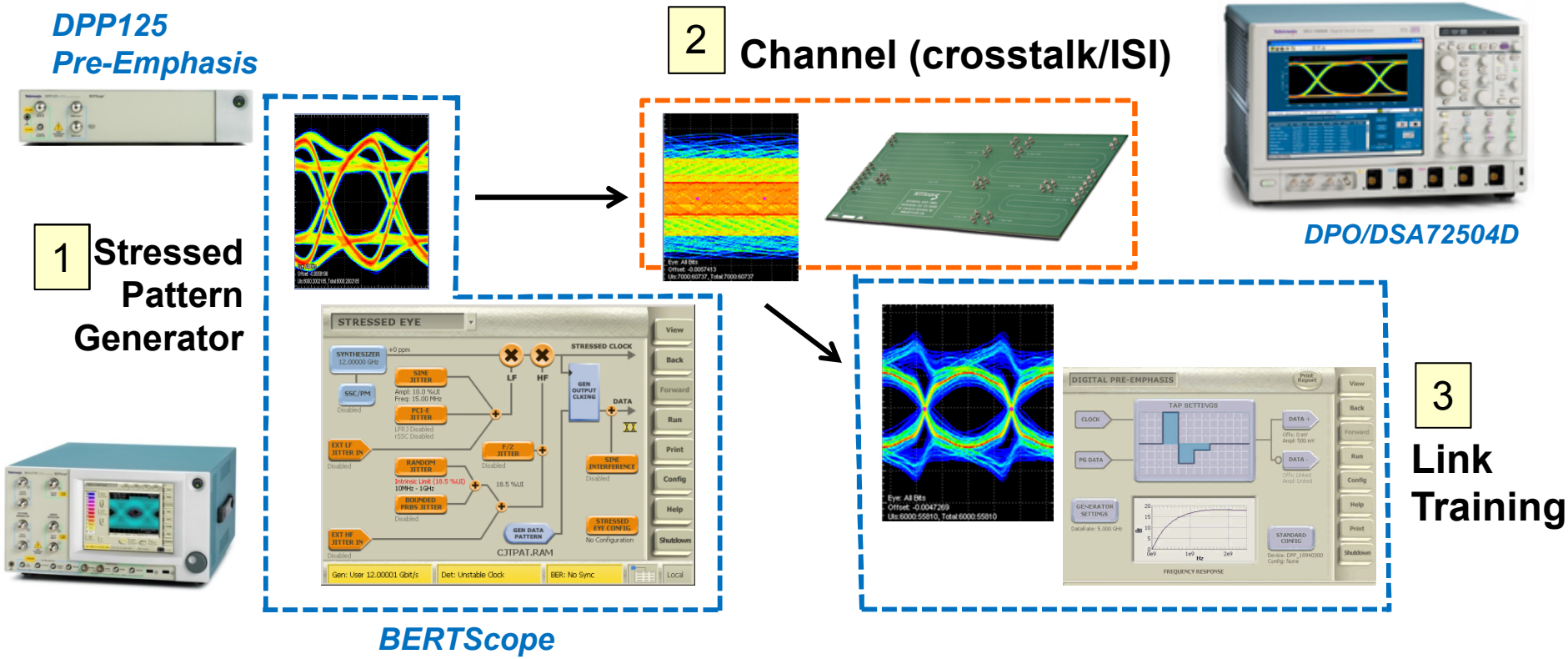
Stressed Pattern Calibration – Putting it Together



Physical Setup → RJ/SJ Calibration → ISI Calibration → Crosstalk Calibration → Tx/Rx Training → RX Testing

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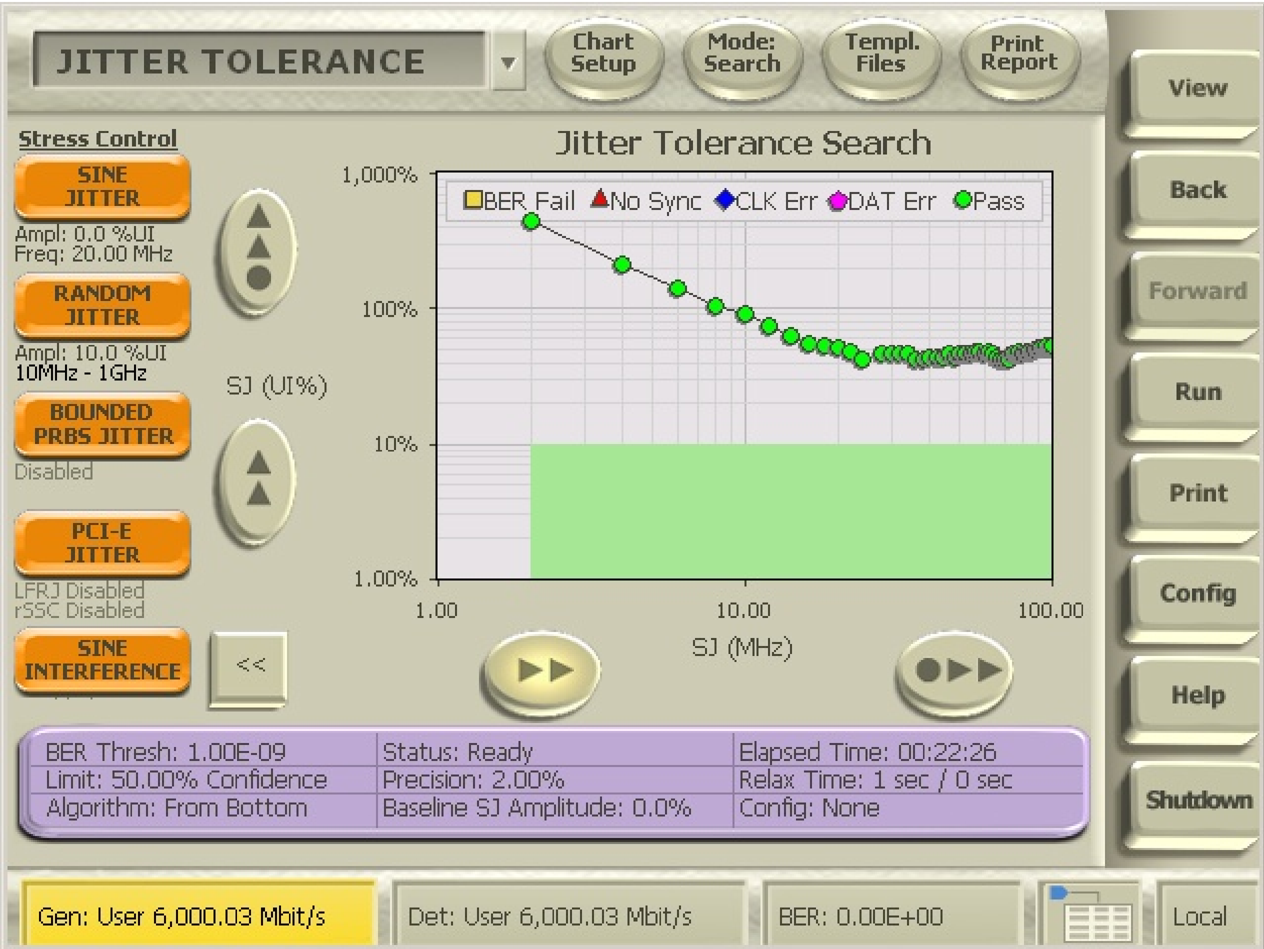
Rx Results (BERTScope)

- Automated Scan from 10 Hz to 100 MHz
- SAS-3 (6/12 Gb/s) spec requires 97, 240 kHz & 2.06, 3.6 and 15 MHz



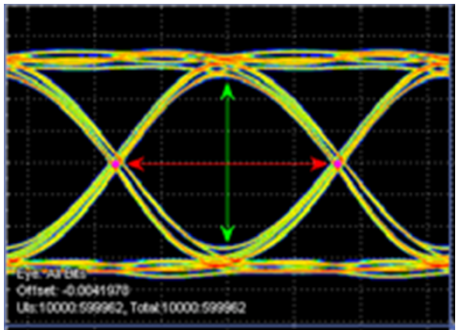
DATA

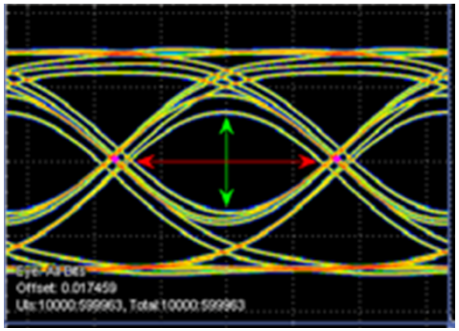
T-MHz	T-SJ	SJ	Bits	Errors	BER	Status	ThreshVX	DelayPS
2	0.1	4.52	6E+08	0	0.00E+00	PASSED	0	267.531
4	0.1	2.1	6E+08	0	0.00E+00	PASSED	0	266.451
6	0.1	1.42	6E+08	0	0.00E+00	PASSED	0	266.451
8	0.1	1.04	6E+08	0	0.00E+00	PASSED	-2	266.451
10	0.1	0.9	6E+08	0	0.00E+00	PASSED	0	266.451
12	0.1	0.74	6E+08	0	0.00E+00	PASSED	0	266.451
14	0.1	0.64	6E+08	0	0.00E+00	PASSED	-2	266.451
16	0.1	0.56	6E+08	0	0.00E+00	PASSED	0	266.451
18	0.1	0.54	6E+08	0	0.00E+00	PASSED	1	266.451
20	0.1	0.52	6E+08	0	0.00E+00	PASSED	0	266.451
22	0.1	0.48	6E+08	0	0.00E+00	PASSED	0	266.451
24	0.1	0.42	6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-2	267.531
			6E+08	0	0.00E+00	PASSED	1	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-2	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-1	267.531
			6E+08	0	0.00E+00	PASSED	-3	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-2	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-1	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-2	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-2	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	PASSED	-1	267.531
			6E+08	0	0.00E+00	PASSED	0	267.531
			6E+08	0	0.00E+00	PASSED	0	266.451
			6E+08	0	0.00E+00	LIMIT REACHED	0	266.451

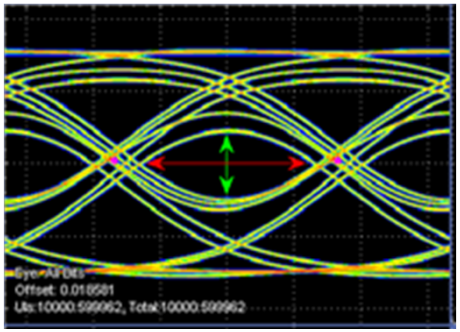
Need for Precise ISI generation

- Device margin testing against variable magnitude sinusoidal test vectors has been foundation of receiver characterization.

- Current PHY designs use sophisticated CTLE and/or DFE architectures, where tolerance and margining against DDJ is more important than SJ.







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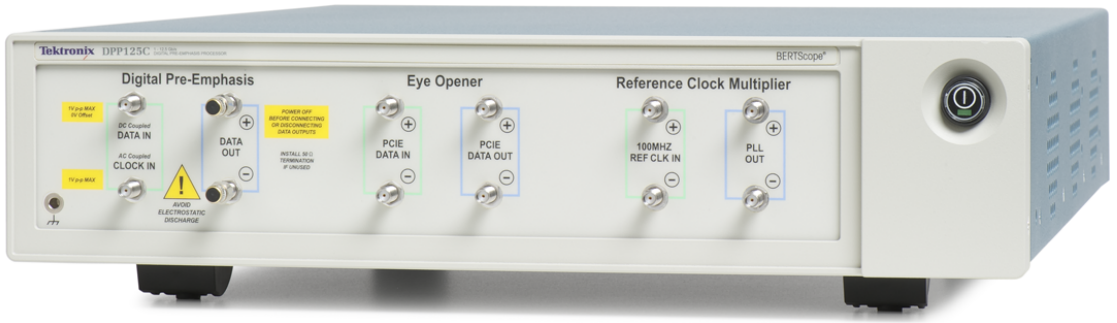
NEW SAS 12 Gb/s Receiver Test Solutions

DPP125C Digital Pre-emphasis Processor

- Integrated eye opener functionality for testing DUTs with long channels
- Integrated clock doubler that enables full rate stress for 12 Gb/s



BSAITS125 Interference Test Set

- Programmable variable ISI for automated testing and precision setting
- Integrated CM and DM interference combiner

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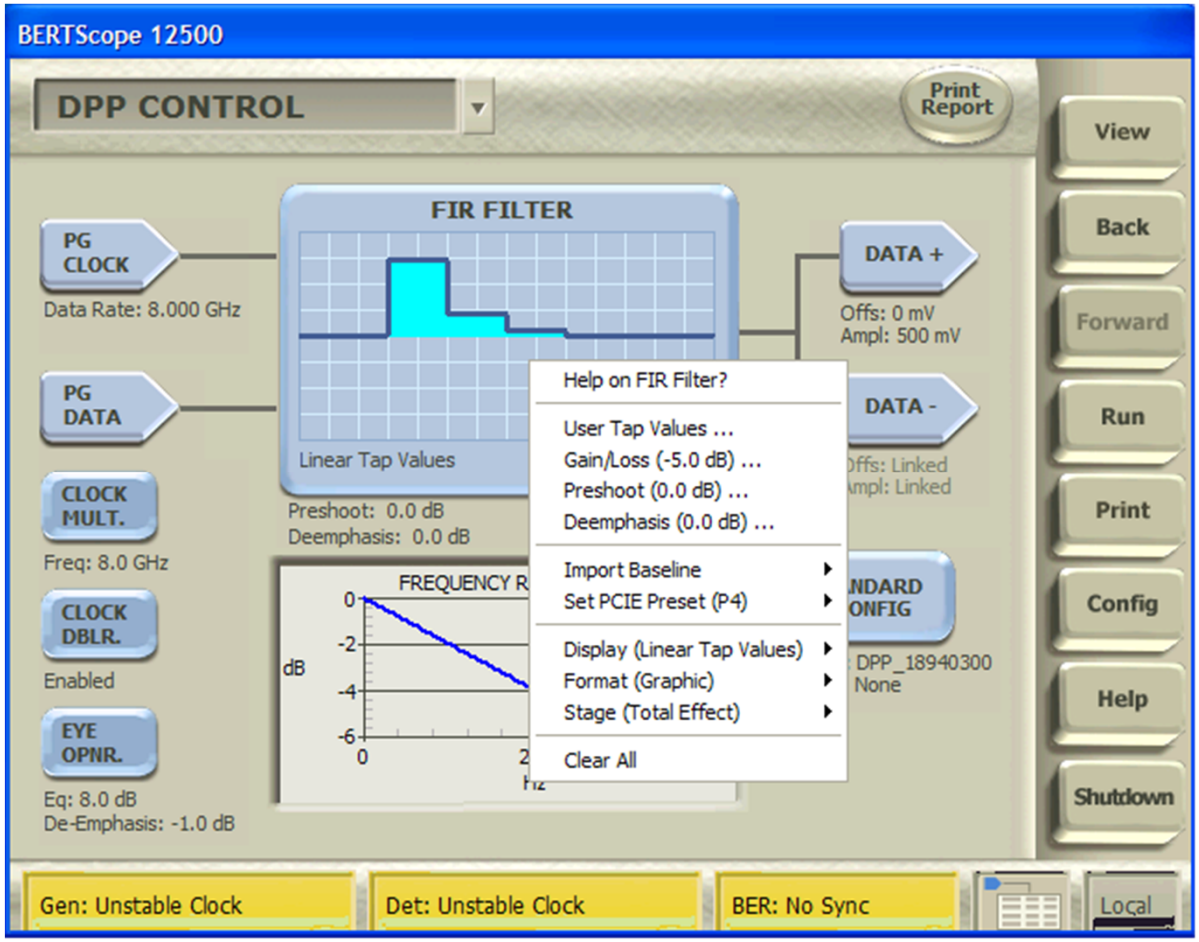
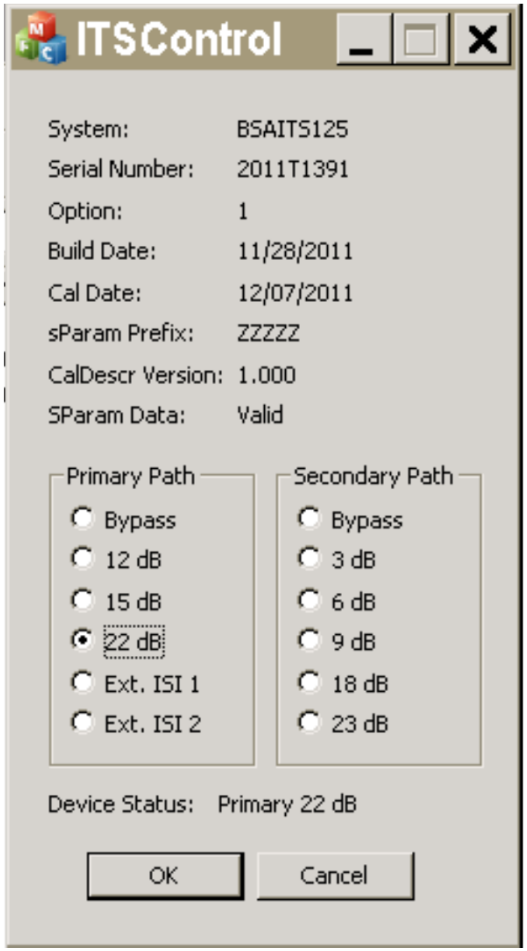
Data Dependent Jitter Variability with BSAITS





BSAITS automates selection of fixed ISI traces with fine (mdB) controls with the DPP FIR filter for a continuously variable high precision ISI source.

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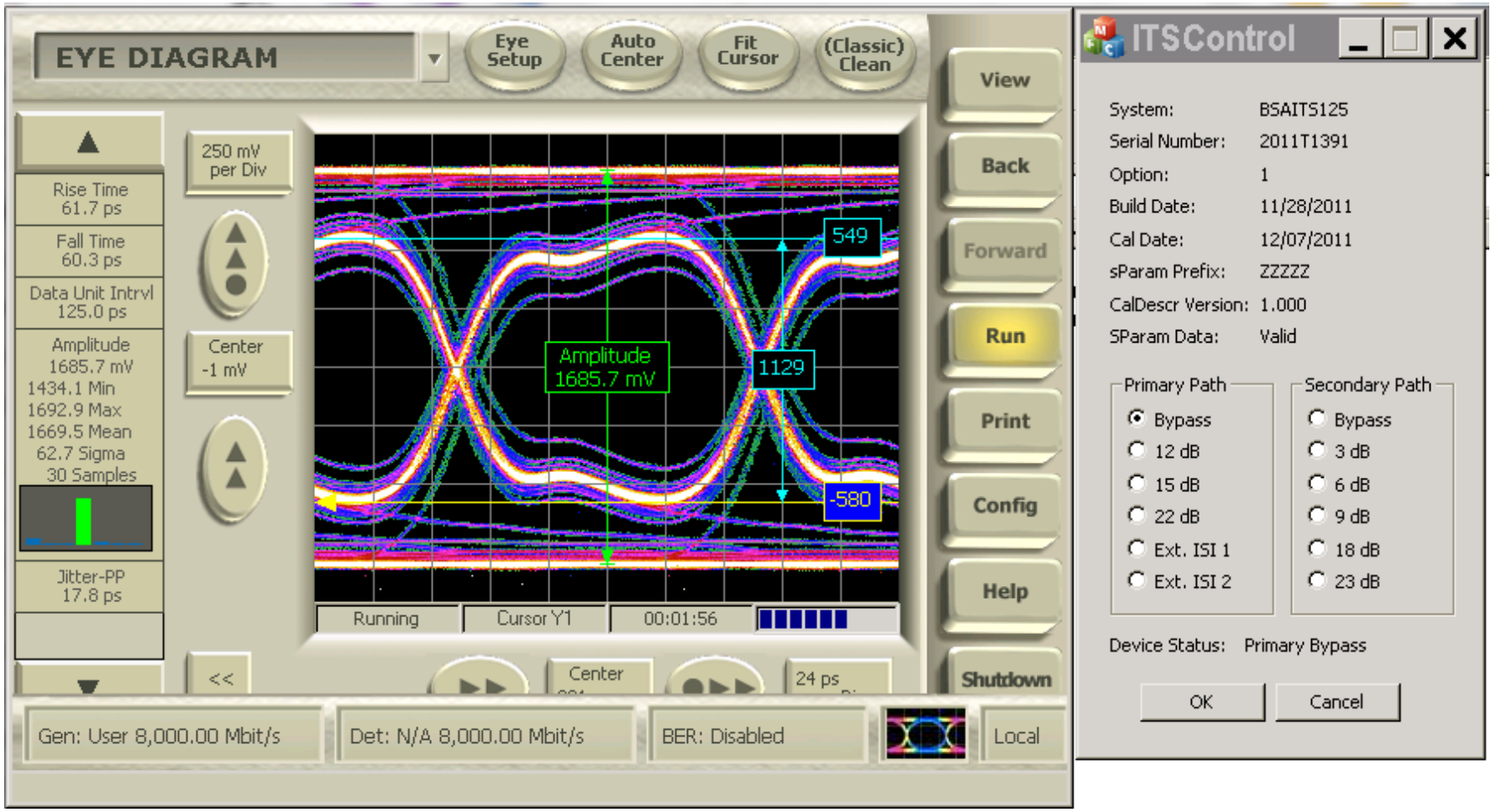
BSAITS Bypass mode



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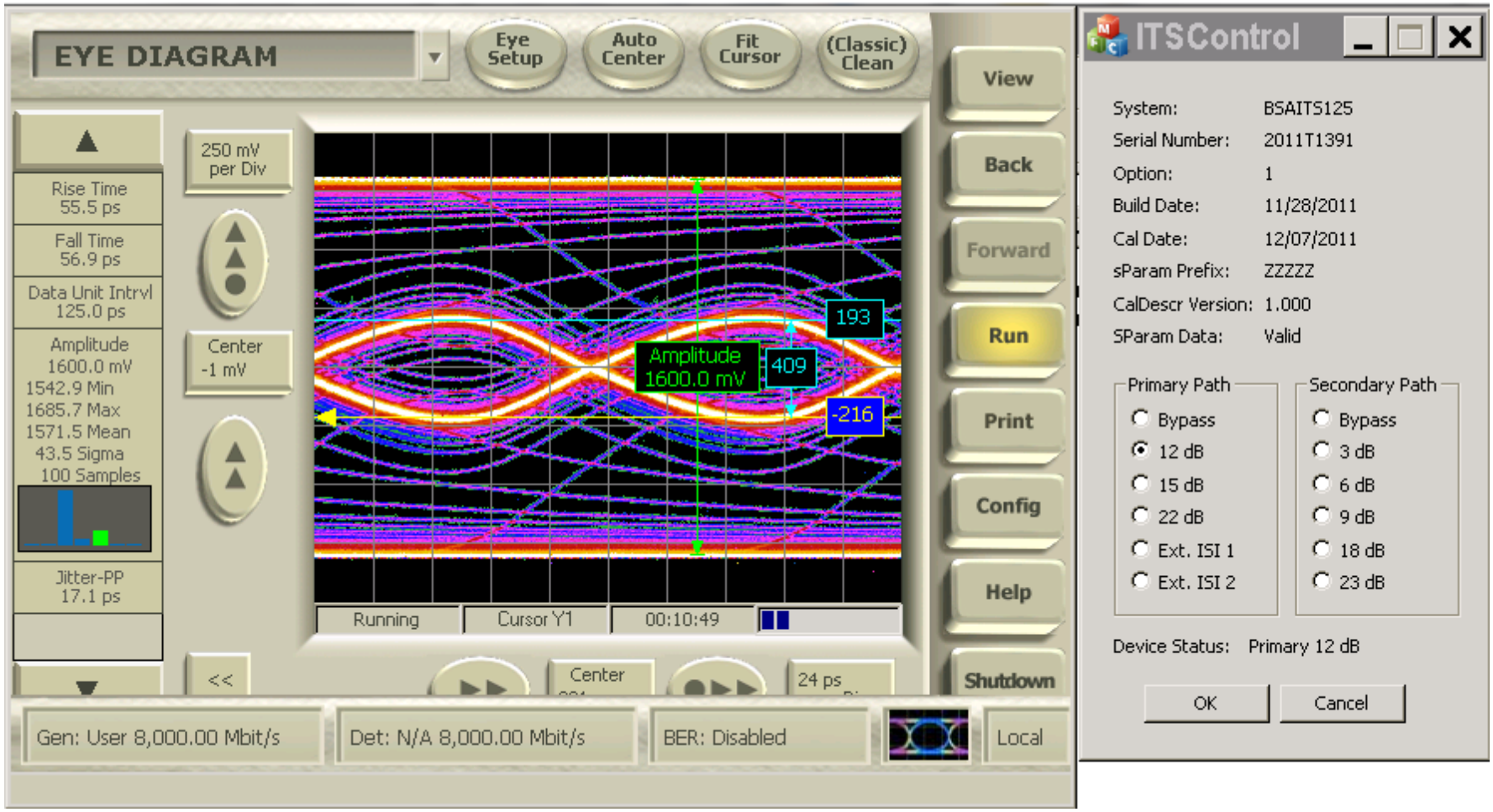
BSAITS 12dB mode



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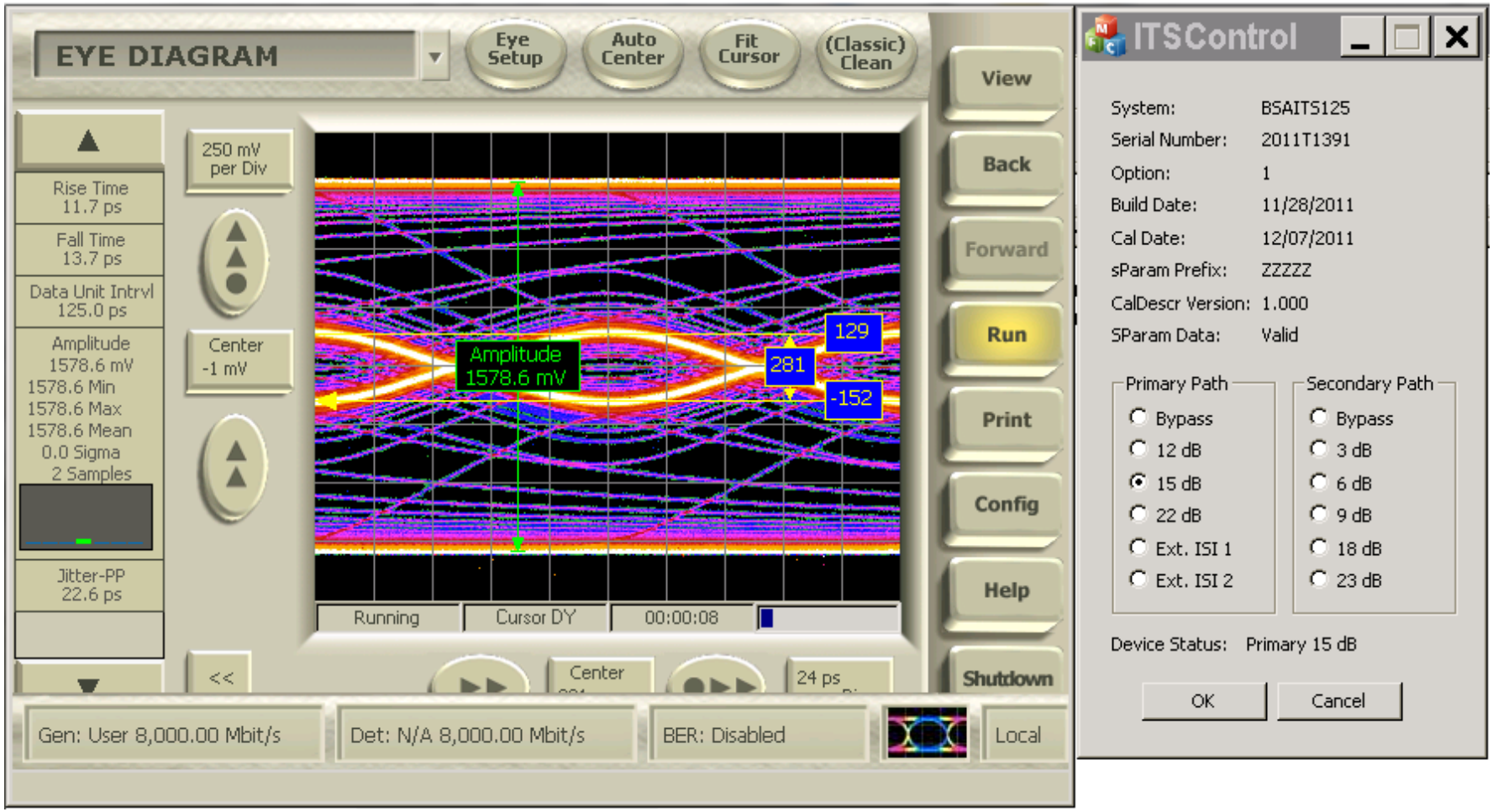
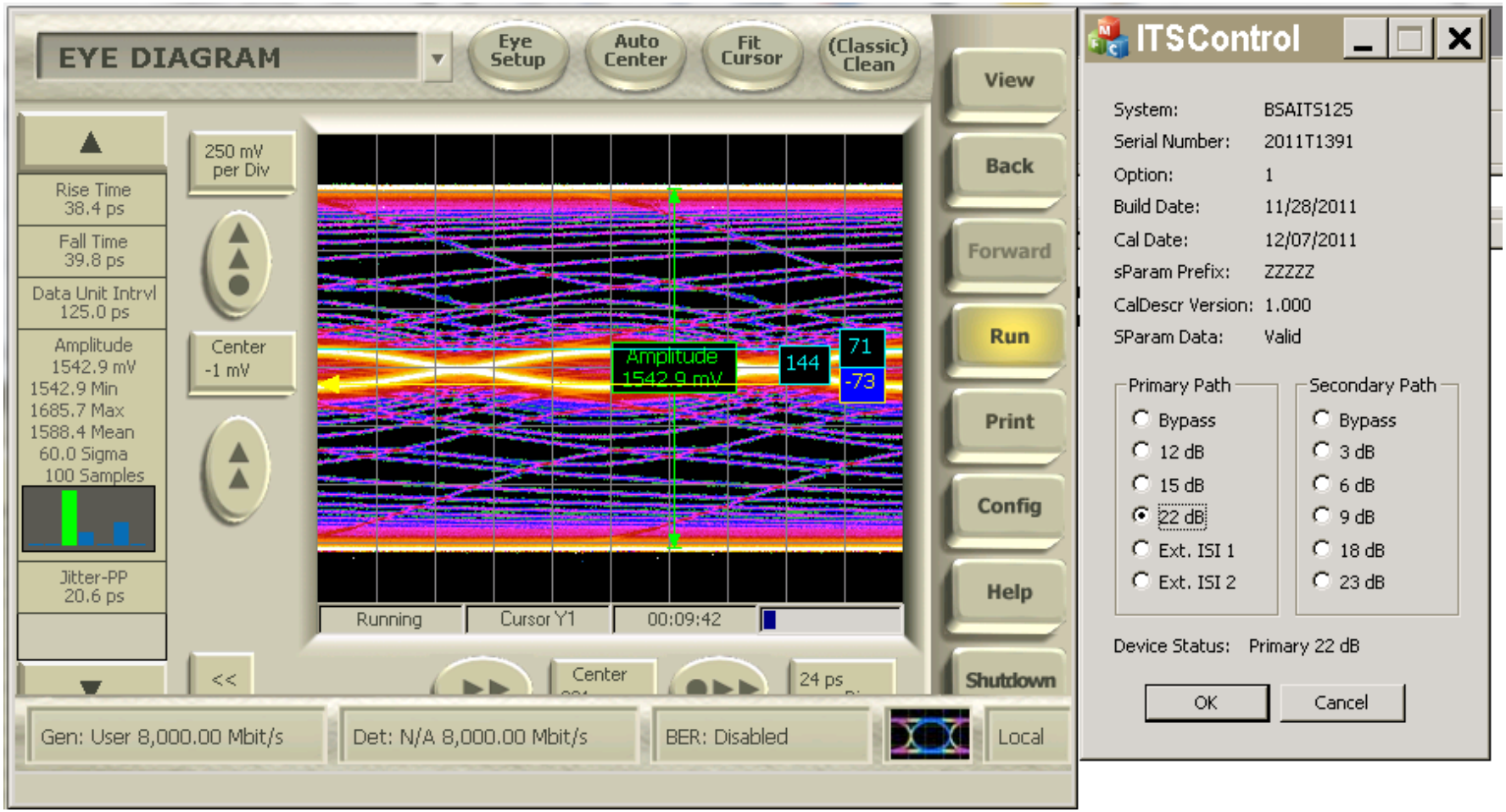
BSAITS 15dB mode



Tektronix

BSAITS 22dB mode



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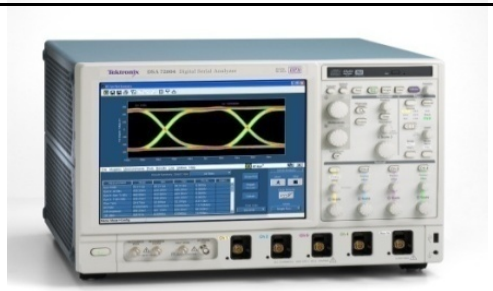
Complete Tektronix SAS Testing

Receiver Tests/Active Cable Tests **RSG/RMT**- Receiver Silicon, Active cable characterization and Compliance testing capability to 26 Gb/s	**BSA125C** with option **JMAP, STR** & **SF** **DPP125C**, **CR125A** and **BSAITS** for Digital Emphasis, Clock recovery and ISI generation	
Channel Tests **ICR**: Insertion Loss/Crosstalk analysis. **Rx/Tx** - Device and Host electrical channel performance, Crosstalk, Impedance and return loss **Passive Cable Tests** Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8300** Sampling Oscilloscope **80E10** TDR Sampling Module for DSA8300 Sampling Oscilloscope **80SICON** S-Parameter Analysis software	
PHY, TSG, and OOB Tests PHY – Signal timing stability and SSC analysis. TSG – Transmitter AC parametric, Jitter, Amplitude. OOB- Out Of Band signal validation	**DSA72504D** Real-Time Oscilloscope **Option SAS3-TSG, SAS3-TSGW,** and **SAS3** 12 Gbps Tx Test Software **DPOJET** Jitter/Eye Analysis software	

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