Tektronix®

On-Oscilloscope De-embedding, Embedding, and Equalization to Remove or Simulate Channel Effects

APPLICATION NOTE

Introduction

As data rates continue to increase, signal integrity challenges compound quickly: channel loss and inter-symbol interference degrade eye opening, impedance discontinuities introduce reflections, and the measurement hardware itself — probes, cables, and fixtures — shifts the effective observation point away from the device pins. Compliance and margin analysis further depend on evaluating the signal as the receiver actually sees it, including CTLE, FFE, and DFE equalization that varies with channel topology and operating conditions. Multi-lane architectures add another layer, requiring coherent cross-channel measurement and correlation to ensure lane-to-lane margin.

Historically, addressing all of this meant exporting data to MATLAB or Python, iterating offline, and reconciling results back to the oscilloscope — adding overhead and increasing the risk of misalignment between measured and modeled results.

This Application Note

- Gives a brief overview of the test challenges in high-speed systems
- Covers compensation methods that shift the reference plane virtually and enable quick "what-if" exploration directly on an oscilloscope
- Demonstrates four practical examples: recovering signal integrity with de-embedding, predicting system performance with embedding, optimizing receiver performance with CTLE equalization, and removing DDR reflections using mid-bus probing
- Includes an Appendix with an explanation of S-parameter fundamentals in relation to system modeling, de-embedding, embedding, and Tx and Rx equalization including CTLE, FFE, and DFE

Tektronix oscilloscopes, with the optional Signal Integrity Modeling software (opt. SIM and SIMA) and Advanced Jitter Analysis (opt. DJA) software, provide an on-oscilloscope solution for detailed signal analysis, design validation, and high-speed digital compliance testing.

Tektronix 5 and 6 Series B MSO and 7 Series DPO oscilloscopes support SIM/SIMA and DJA software. For more information on these and other Tektronix oscilloscopes download the Oscilloscope Selection Guide.

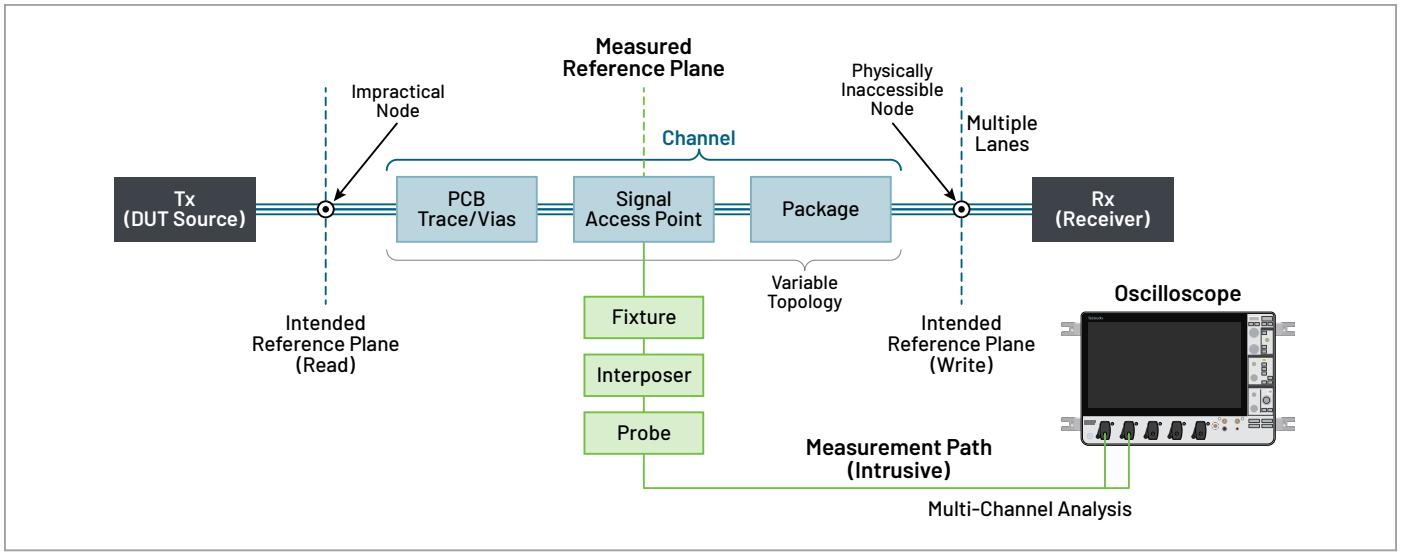


Figure 1. Conceptual overview of key challenges in high-speed measurement and analysis (e.g. DDR System Tx Test). These challenges necessitate engineers de-embed measurement-path effects, embed virtual channel elements, and emulate receiver equalization to test compliance and system performance.

Figure 1 illustrates the key challenges present in a representative high-speed measurement scenario. Tektronix Signal Integrity Modeling software (option SIM) addresses these directly, bringing de-embedding, embedding, and Tx/Rx equalization into a single, integrated on-oscilloscope workflow. Engineers can remove measurement-path effects, insert virtual channel elements, and emulate receiver equalization without leaving the bench — enabling rapid "what-if" exploration and confident reference-plane relocation using virtual test points.

This application note provides practical steps for applying these techniques using SIM. Written for engineers who already understand eye diagrams, jitter, and noise analysis, it focuses on measurement compensation and signal-path transformation. Each of the four examples that follow addresses a specific measurement challenge — reference-plane ambiguity, early channel exploration, receiver equalization, and DDR reflection removal — and walks through the SIM workflow that resolves it. An Appendix provides S-parameter fundamentals for readers who want a deeper background on the underlying theory.

Overview of Key Tools Used in the Examples Below

The comprehensive suite of Tektronix solutions provides engineers with cutting-edge instruments and software essential for detailed signal analysis, design validation, and high-speed digital compliance testing.

- **7 Series DPO Oscilloscope** is fundamental for capturing and analyzing high-frequency signals. This oscilloscope offers advanced functionalities like industry-leading noise performance, measurement throughput, and award-winning usability and flexibility, making it indispensable in R&D and quality control settings.
- **Signal Integrity Modeling Software (options SIM and SIMA)** enable engineers to de-embed and embed probes, cables, fixtures, and equalize data links directly on the oscilloscope, aiding in the design optimization to mitigate integrity issues before and after physical testing.
- **Advanced Jitter Analysis Software (option DJA)** provides detailed jitter analysis and eye diagram generation directly on the oscilloscope, crucial for assessing digital signal timing errors and overall integrity.
  - SIM (Base) provides multi-block de-embedding, embedding, and core analysis tools, and is used in Examples 1, 2, and 4. SIMA (Advanced) includes all SIM capabilities plus transmitter and receiver equalization modeling, and is required for Example 3.

Together, these tools form a robust toolkit, supporting a seamless workflow from design through validation, backed by Tektronix's comprehensive training and support to ensure users can leverage their full potential.

Example 1: How to Recover Signal Integrity with De-Embedding

At high data rates, the act of measurement itself becomes intrusive. Probes, cables, fixtures, and adapters materially alter the electrical behavior of the system under test, shifting the effective observation point away from the device pins and introducing ambiguity in reference-plane definition.

This example shows how Tektronix SIM software uses de-embedding to correct for this, starting from a degraded oscilloscope waveform and recovering the true transmitter output at a virtual reference plane.

What is De-Embedding?

De-embedding mathematically removes the effects of measurement-path elements—recovering the signal at the intended reference plane without moving a single wire.

It enables users to eliminate the influence of fixtures, cables, probes, and interconnects, revealing the true behavior of the device under test. By applying S-parameter models of these elements—typically acquired through VNA measurements or simulation—de-embedding reconstructs what the waveform would look like as if those impairments were never present, improving measurement accuracy and confidence in high-speed signal analysis.

The Setup and Acquired Waveform

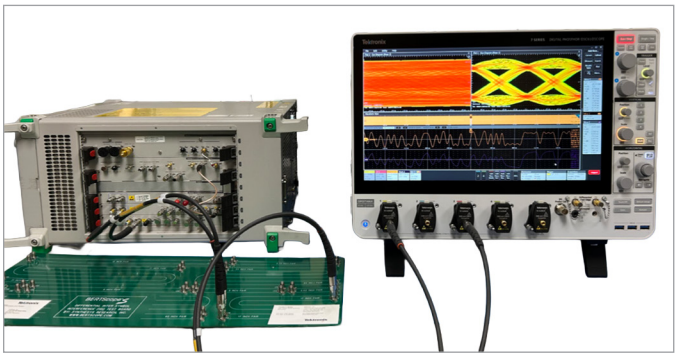


Figure 2: A BERT (left) is used to drive PRBS test signals through PCB traces of 24in length and a pair of 1-meter SMA cables. The 7 Series DPO with Advanced Jitter Analysis software (option DJA) and Signal Integrity Modeling software (option SIM) is used to measure the resulting signal.

The test setup consists of an Anritsu MP1900A Bit Error Rate Tester (BERT), two 1-meter SMA cables, a 24-inch PCB trace pair, and a Tektronix DPO714AX oscilloscope equipped with Advanced Jitter Analysis (option DJA) and Signal Integrity Modeling (option SIM) software.

The BERT transmits a 5 Gb/s, 1 V pk-pk differential NRZ signal with a PRBS11 pattern through the channel — comprising two 1-meter SMA cables carrying the positive and negative legs of the differential pair, a 24-inch PCB trace pair, and two further 1-meter SMA cables — before reaching two single-ended channel inputs on the oscilloscope. The resulting eye diagram is rendered using the Advanced Jitter Analysis software.

The acquired waveform exhibits significant degradation as shown in **Figure 3**. There are rounded transitions, reduced amplitude, and an eye diagram severely impacted by limited rise and fall time performance.

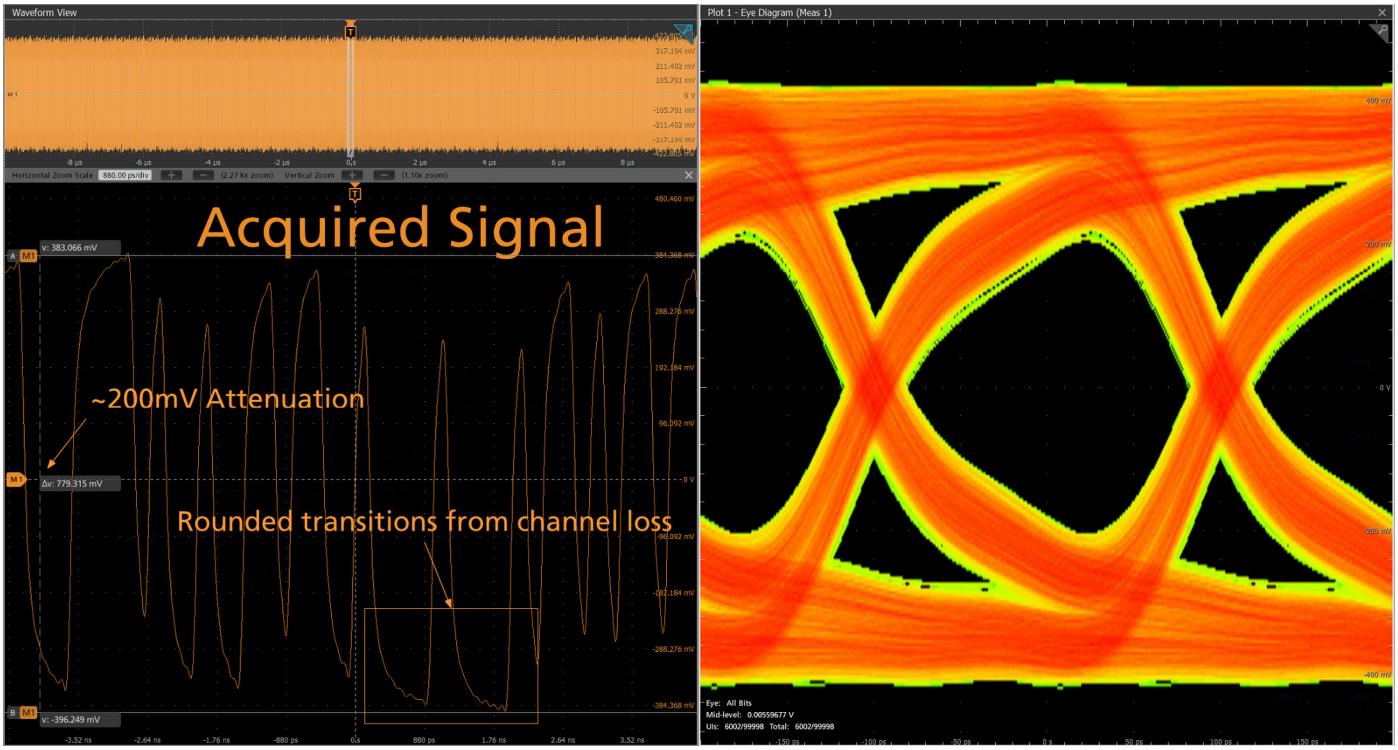


Figure 3. Degraded 5 Gb/s waveform after propagating through 24in PCB trace pair and two 1-meter cables, showing rounded transitions, reduced amplitude, and an eye diagram severely impacted by limited rise and fall time performance.

To see the true performance of the DUT, the effects of the test setup need to be removed. The oscilloscope acquiring the signal using SIM's Simple De-embed Workflow provides the framework needed to easily perform this task. It can also model virtual test points anywhere along the signal path to view the signal without channel impairments. The steps below describe how to do this.

Configure a De-embed to Remove Channel Impairments

To use virtual test points to see the signal without channel impairments, the real-world setup must be defined. The Simple De-Embed workflow provides the framework for this task.

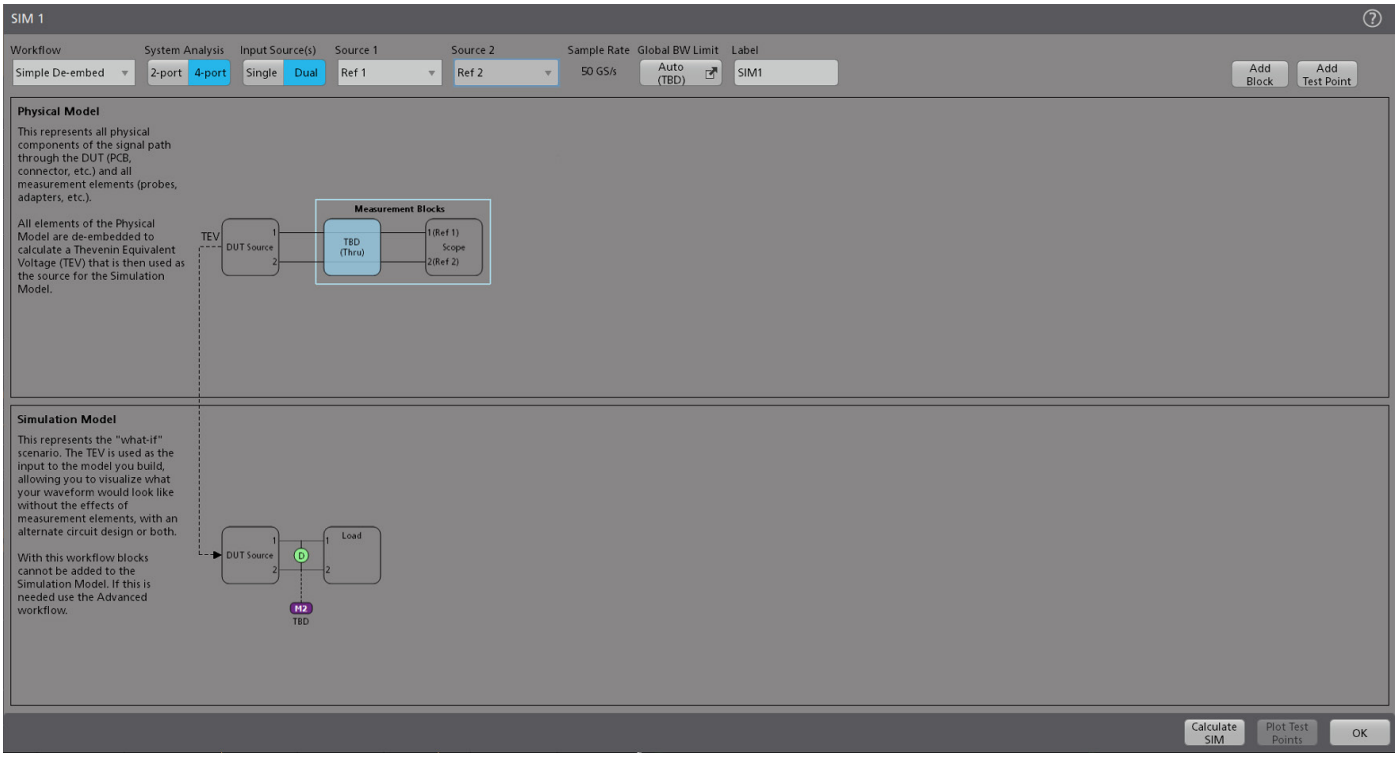


Figure 4. The Simple De-Embed workflow in SIM. Measurement blocks can be added and configured in the Physical Model section to represent the test setup. The Simulation Model represents the "what-if" scenario where virtual test points can be added anywhere along the path to see the signal without channel impairments.

Before configuring the first example, it helps to understand how SIM's two-panel interface works. The Physical Model represents every real element in the measurement path — cables, PCB traces, fixtures, and probes. SIM de-embeds all of these blocks and uses the result to compute a Thevenin Equivalent Voltage (TEV), which represents the true source behavior of the DUT, free from measurement-path effects. This TEV then becomes the input to the Simulation Model, where virtual channel elements can be added and test points placed anywhere along the signal path.

This example uses the Simple De-embed workflow, which streamlines setup for the most common de-embedding scenario by allowing the user to focus solely on defining the measurement path.

First, SIM needs to know what kind of system it will analyze. For a single-ended signal, use 2-port analysis; for a differential signal, use 4-port analysis. 4-port analysis is selected here because the signal is differential — this ensures all four S-parameter terms are used to correctly model cross-coupling between the positive and negative conductors. Two blocks are then defined in the Physical Model to represent the PCB traces and the 1-meter SMA cables, each modeled by a corresponding S-parameter file.

The PCB Traces

To model the differential PCB trace pair, load the specific .s4p S-parameter file for the traces, as seen in **Figure 5**. Clicking the Plot button displays the full S-parameter matrix. The S21 term shows the single-ended forward transmission through the channel, where the high-frequency roll-off responsible for the rounded transitions seen in the acquired waveform is clearly visible.

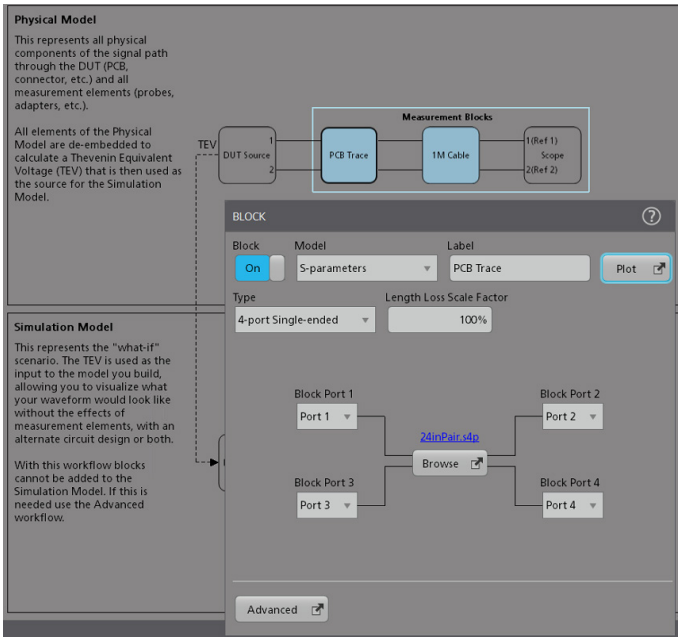


Figure 5. Each block in the Physical Model can be modeled by an S-parameter file that has been generated to accurately model the component. This Configuration menu in SIM software shows a .s4p S-parameter file uploaded to model the 24 in PCB trace pair.

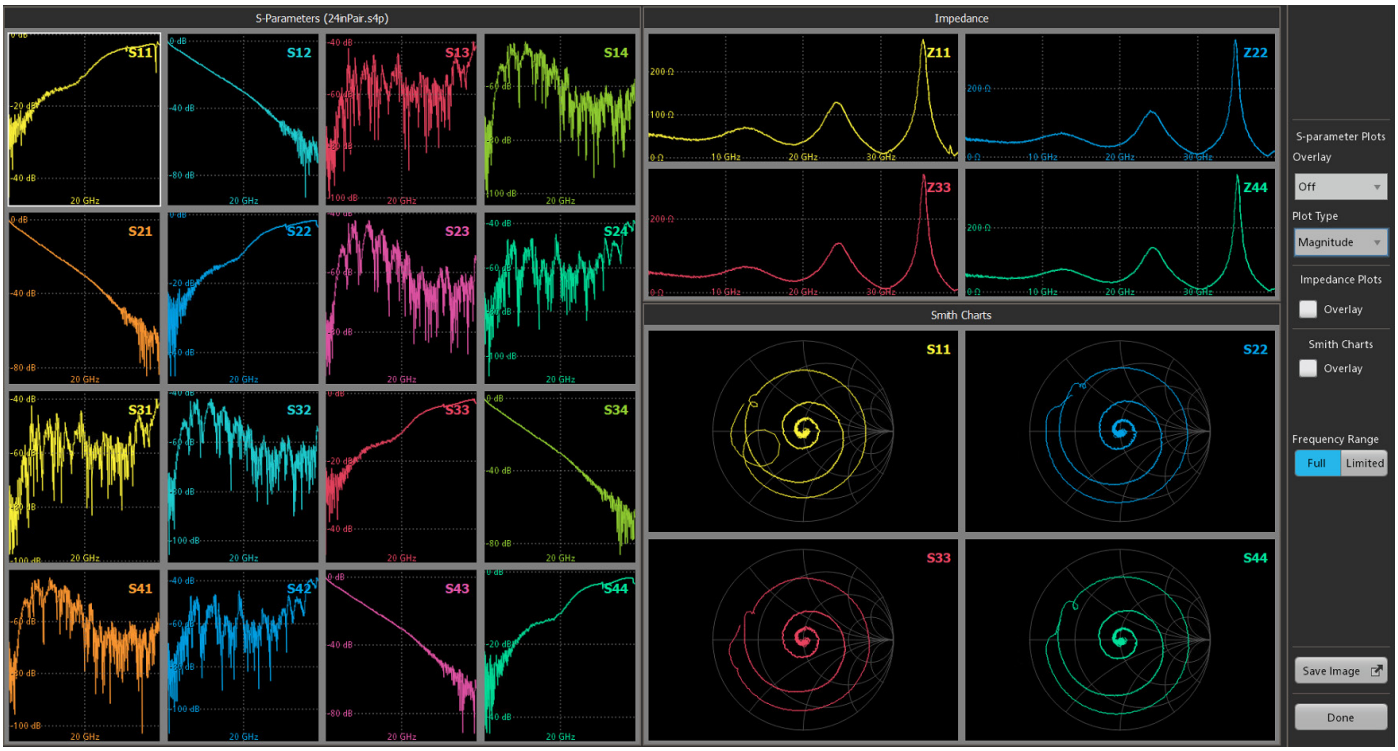


Figure 6. By clicking the Plot button in the block Configuration menu after uploading the S-parameter file, the S21 Insertion Loss can be seen. The high-frequency roll-off that has been "rounding" the signal can be seen.

The 1-meter Cables

Repeat this for the RF cables – the next block in the cascade. By loading their S-parameter file, the software accounts for every bit of the signal's journey before it hits the scope.

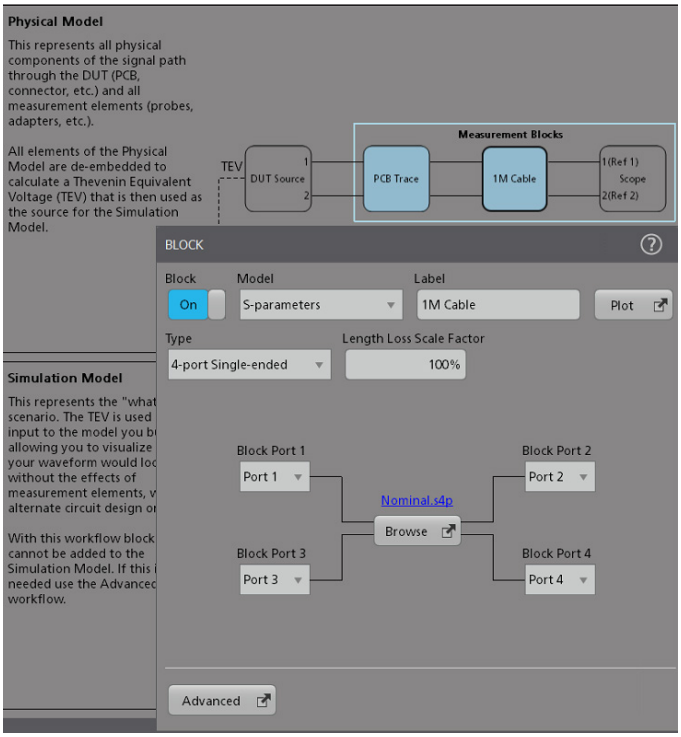


Figure 7. Block Configuration menu in SIM for modeling the 1-meter cables using S-parameters.

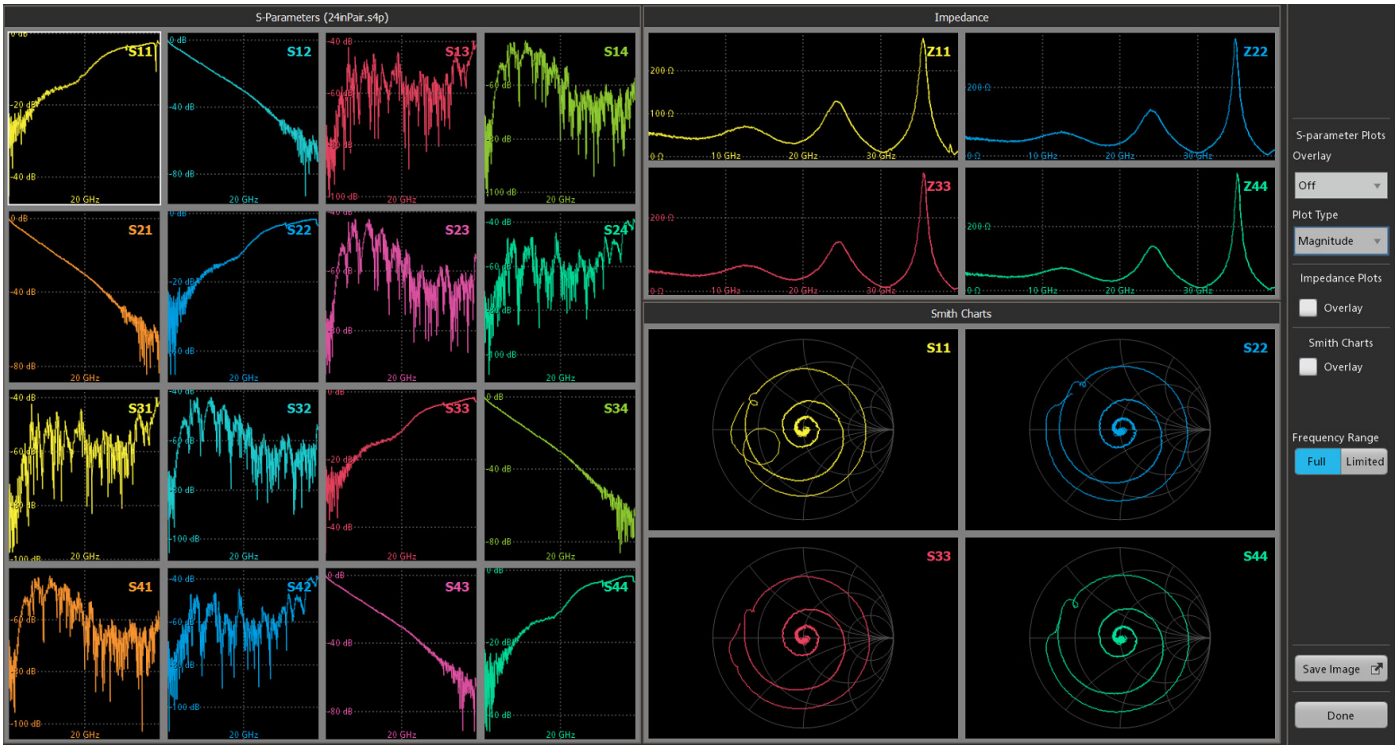


Figure 8. S-parameters for the 1-meter cables plotted.

Shift the Reference Plane

With the Physical Model defined, SIM can be used to move the measurement reference plane. In the Simulation Model, a virtual test point has been placed at the output of the de-embedding cascade. A new Math waveform (M2) is automatically assigned to the signal seen at this test point.

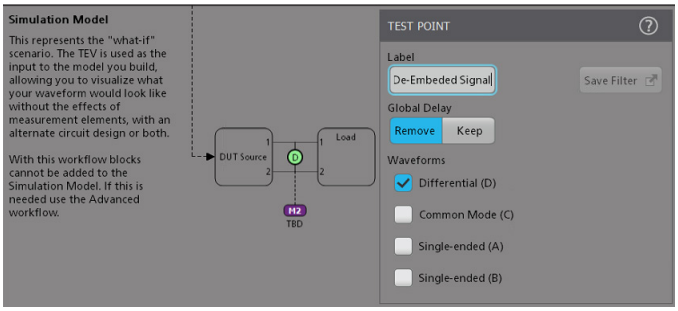


Figure 9. A Simulation Model in SIM with a virtual test point placed at the output of the de-embedding cascade.

To generate the signal at M2, the software is taking the live data from the oscilloscope, working backwards through the physical model cable and PCB trace, and simulating what the signal would look like at that virtual test point, in the absence of the lossy channel.

Easy Analysis of Resulting Waveform Directly on the Oscilloscope

With both the physical model and simulation model defined, SIM will calculate and derive an inverse transfer function from the physical model for a given test point and apply it to the acquired waveform.

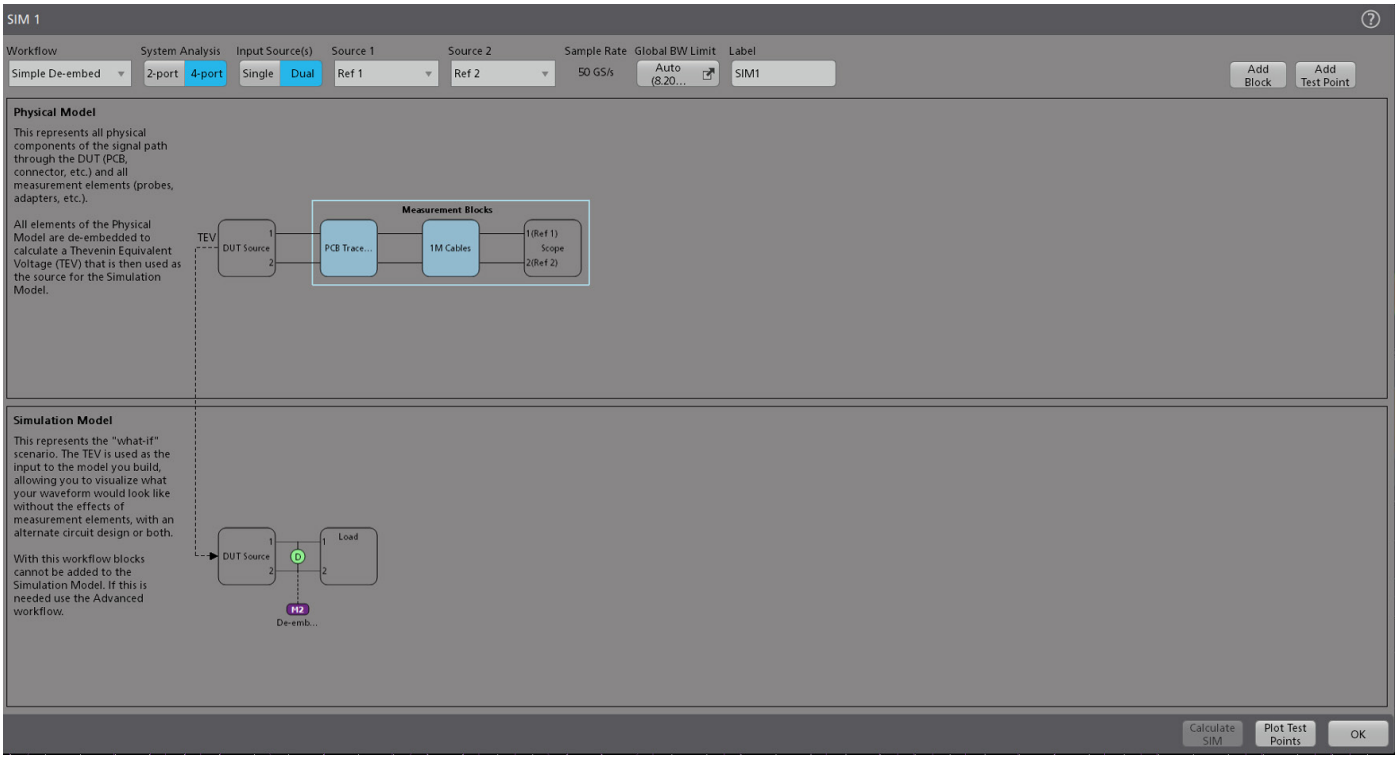


Figure 10. Physical model and simulation model defined in SIM.

During de-embedding, channel loss is compensated by applying increasing gain at higher frequencies. While this restores attenuated signal content, it can also amplify high-frequency noise and measurement uncertainty. It's important to note the Global Bandwidth (BW) Limit setting in the SIM toolbar that controls the highest frequency content passed by the de-embed DSP filter. By default, it is set to Auto as shown in **Figure 11**, which determines the Global BW Limit based on the oscilloscope sample rate and the amount of frequency-dependent gain required by the de-embed filter at the virtual test points.

Increasing the bandwidth limit allows more high-frequency signal content, including higher-order harmonics, to pass through the de-embed filter. This improves edge fidelity and reduces overshoot or ringing that may occur when the bandwidth limit is too restrictive, or the filter transition is too abrupt. However, increasing the limit too far can pass or amplify high-frequency noise, at which point you can simply pull the limit back.

In Auto mode, SIM will not set the Global BW Limit higher than the Nyquist frequency of the acquisitions sample rate, and it may reduce the limit further if the required gain at any test point exceeds thresholds intended to limit noise amplification. While Auto mode works well for this example, Custom mode provides a frequency response plot that visualizes the configured Global Bandwidth Limit filter. After calculation, the Plot Test Points view can be used to examine the filter frequency response and confirm where bandwidth limiting occurs. If the de-embedded result shows excessive high-frequency noise amplification or instability, manually lowering the Global BW Limit can reduce noise by limiting high-frequency gain.

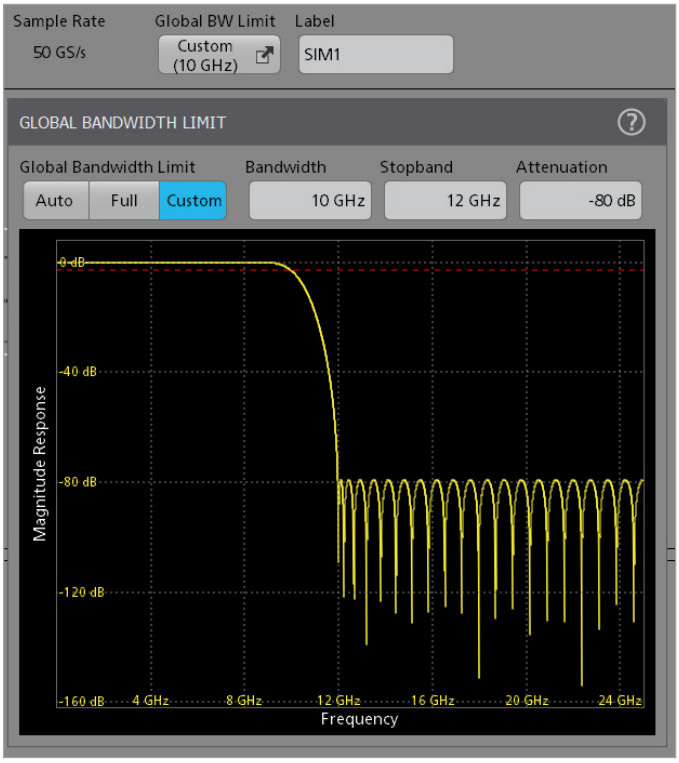


Figure 11. Example Custom Global Bandwidth Limit configuration. The frequency response plot visualizes the bandwidth limit applied to the de-embed DSP filter based on the selected bandwidth, stopband frequency, and stopband attenuation settings.

The waveform transformation is substantial, as shown in **Figure 12**. SIM generates the de-embedded waveform on M2, the new math channel corresponding to the test point defined in the Simulation Model. Comparing the de-embedded waveform to the acquired waveform highlights the recovered signal characteristics — specifically increased amplitude and sharper data transitions.

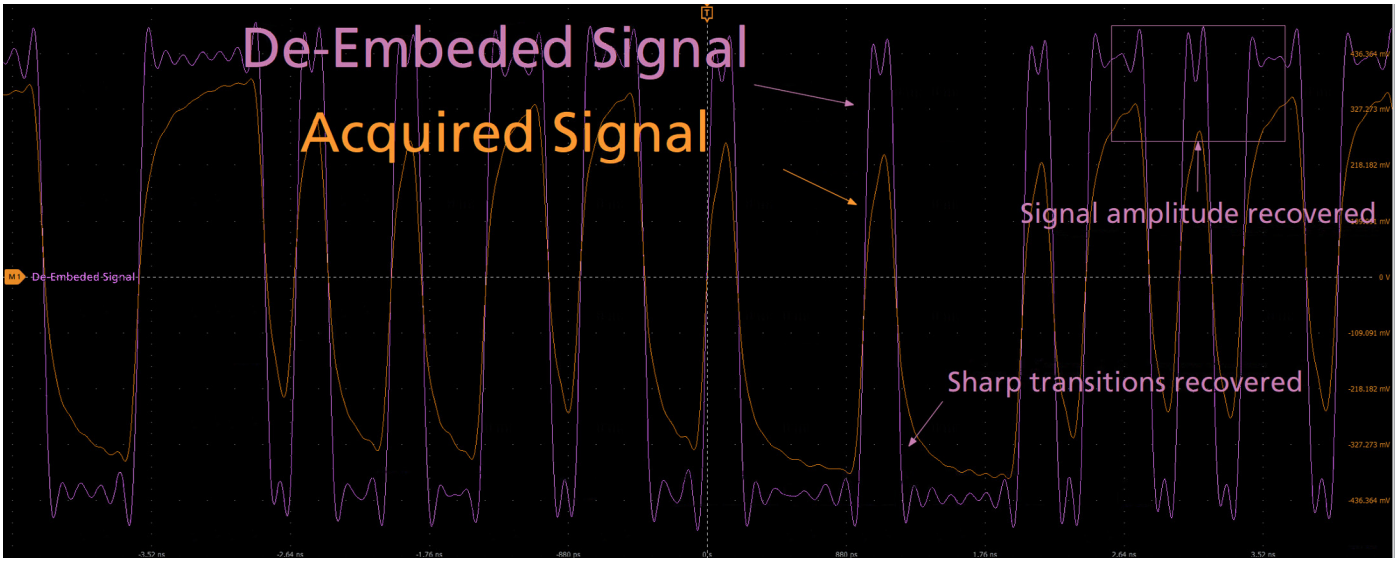


Figure 12. Comparison of acquired and de-embedded signal shows the amplitude recovered and sharp transitions at the edges.

The filter response associated with the test point can also be plotted, as shown in **Figure 13**, displaying the magnitude, phase, impulse response, and step response. The magnitude and phase plots show the high-frequency boost and corresponding phase shift applied to compensate for channel loss, both bounded by the configured bandwidth limit beyond which the correction is no longer valid. The impulse and step responses confirm the filter is well-behaved and causal, evidenced by the sharp, localized impulse spike and clean differential settling in the step response.

If the de-embedded signal shows high-frequency noise amplification — a result of the boost filter amplifying noise alongside the signal — the Global BW Limit can be manually reduced from Auto.

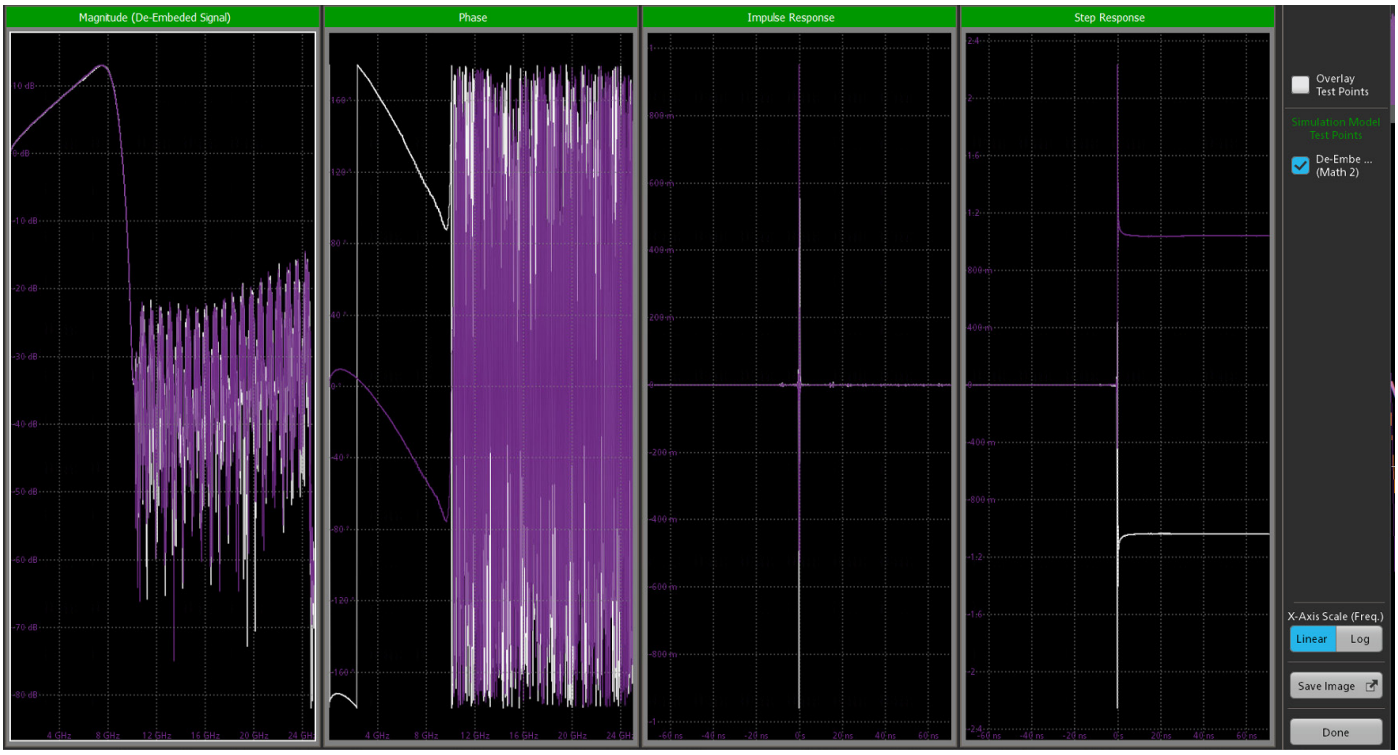


Figure 13. De-embedding filter response at the test point, showing magnitude, phase, impulse response, and step response.

The improvement in signal quality is further demonstrated by comparing the eye diagrams and jitter summary results of the acquired and de-embedded signals. As shown in **Figure 14,** de-embedding the channel-loss effects produces a dramatically improved eye diagram. Compared to the acquired signal, Total Jitter (TJ@BER) is reduced from approximately 44.16 ps to 14.65 ps, eye height increases from 366 mV to 711 mV, and eye width increases from 160.9 ps to 190.0 ps.

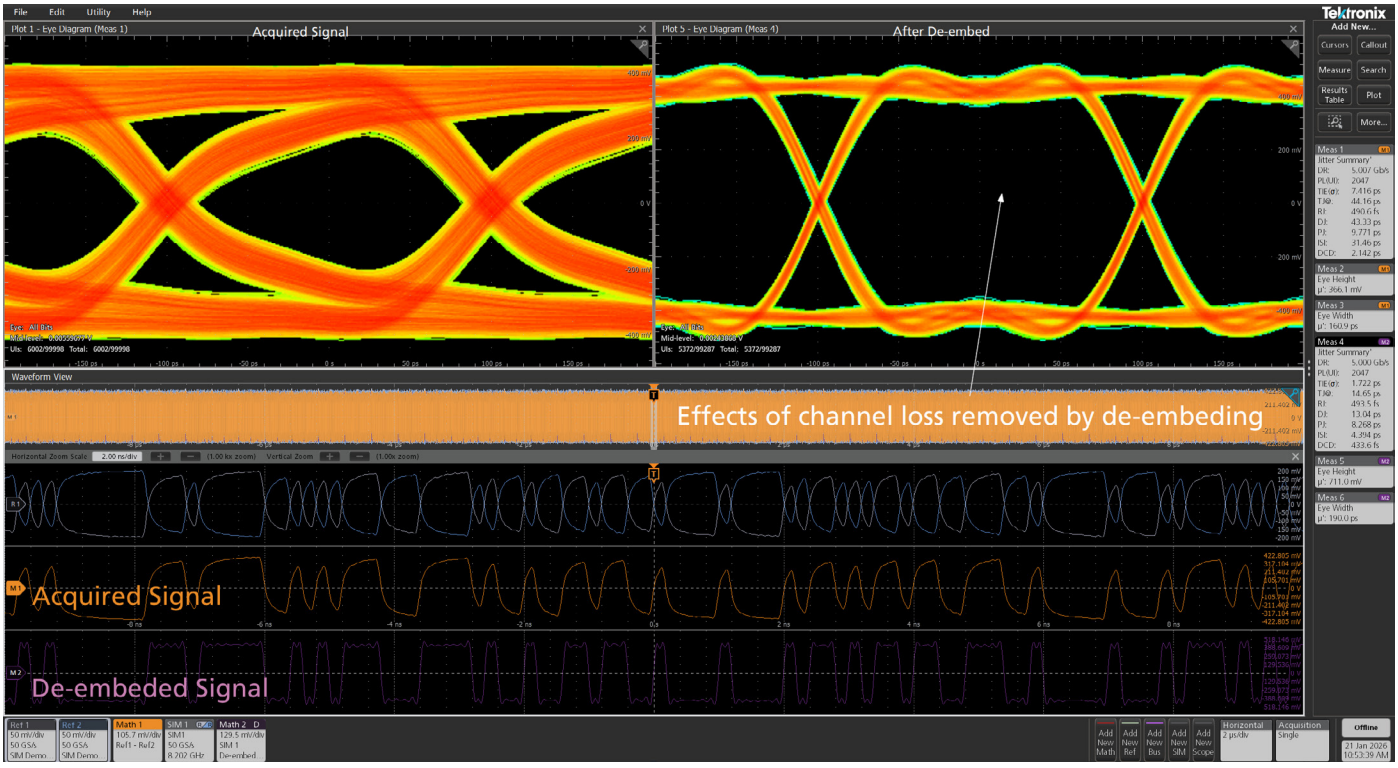


Figure 14. Side-by-side comparison of eye diagrams of the signal before and after de-embedding, showing significant improvement in signal integrity.

Example 2: How to Predict System Performance with Embedding

Validation is often limited to the hardware on the bench, making it impossible to evaluate alternate channel topologies—different trace lengths, materials, or connector variants—until late in the design cycle. This example shows how SIM addresses this challenge with embedding- making exploration of alternate channel topologies fast and repeatable, directly on the oscilloscope, and without needing to spin-up hardware.

What is Embedding?

Embedding is mathematically inserting modeled interconnect elements into the measured signal path, predicting system-level behavior before the hardware exists. Unlike de-embedding, embedding is inherently predictive: it applies a modeled channel or network to a known signal to estimate how the waveform will behave at a future reference plane or under hypothetical system conditions.

The Given Setup and Alternate Topology to Consider

The test setup consists of an Anritsu MP1900A Bit Error Rate Tester (BERT), a pair of 1-meter SMA cables, and a Tektronix DPO714AX oscilloscope equipped with Advanced Jitter Analysis software (option DJA) and Signal Integrity Modeling software (option SIM).

The BERT, acting as a transmitter, outputs a NRZ (non-return to zero) schemed 5 Gb/s 1 Vpk-pk differential signal transmitting a PRBS11 pattern. This signal travels through a pair of 1-meter SMA cables before reaching the front end of the oscilloscope. Using Advanced Jitter Analysis software (option DJA), an eye diagram is rendered, and the signal can be analyzed.

While the evaluation of its standalone performance is crucial, the transmitter will eventually drive the signal through a 40-inch PCB trace not yet available. The Simple Embed workflow in SIM can be used to embed the effects of the 40-inch PCB trace before the board is physically ready.

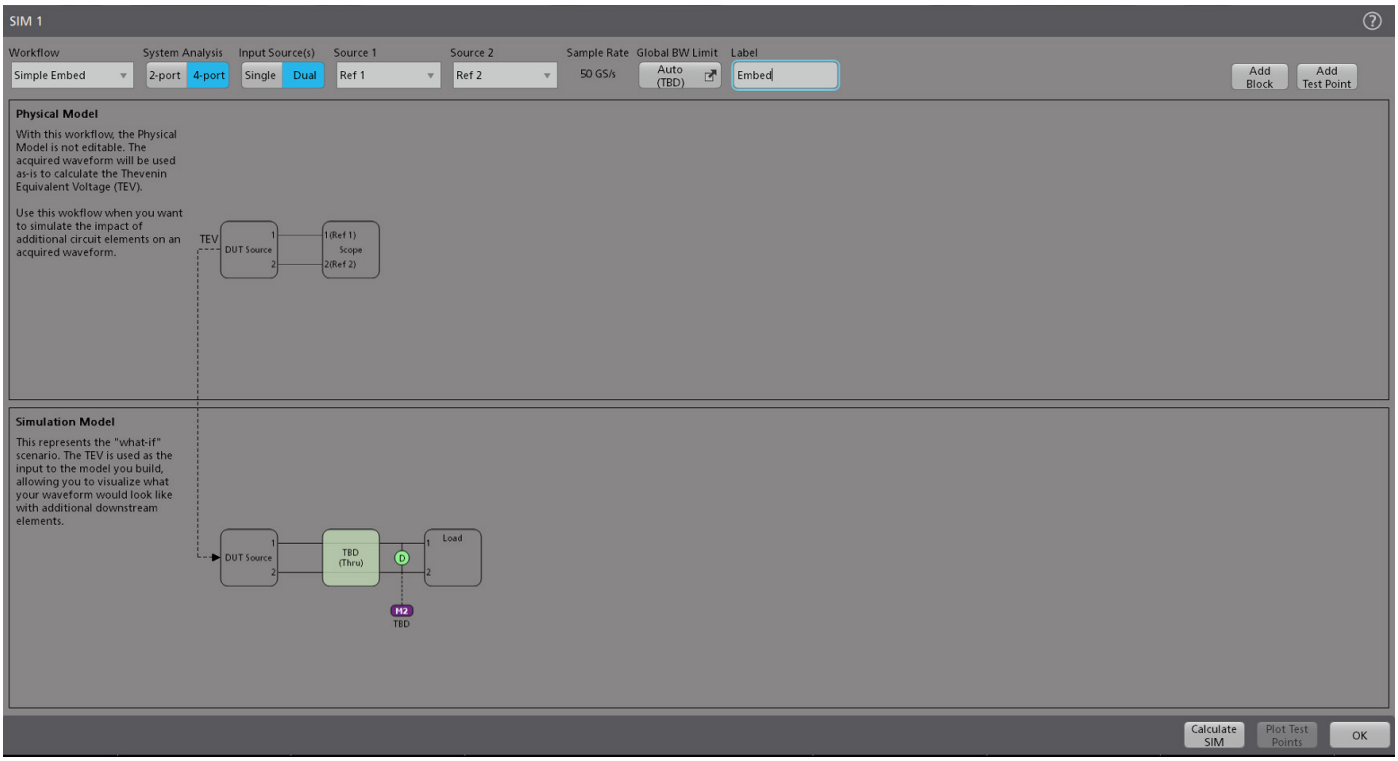


Figure 15. The Simple Embed workflow in SIM used to embed the effects of signal path artifacts for predictive modeling.

Configure the Alternative Signal Path

The Simple Embed workflow assumes that losses between the DUT and oscilloscope are negligible or have already been compensated for. If required, the Advanced workflow should be used to de-embed the measurement path before embedding the virtual channel.

In the Simulation Model, a block has been added between the DUT (transmitter) and load (oscilloscope) to represent the 40-inch PCB trace. The block has been configured to use an .s4p S-parameter to model its expected channel characteristics.

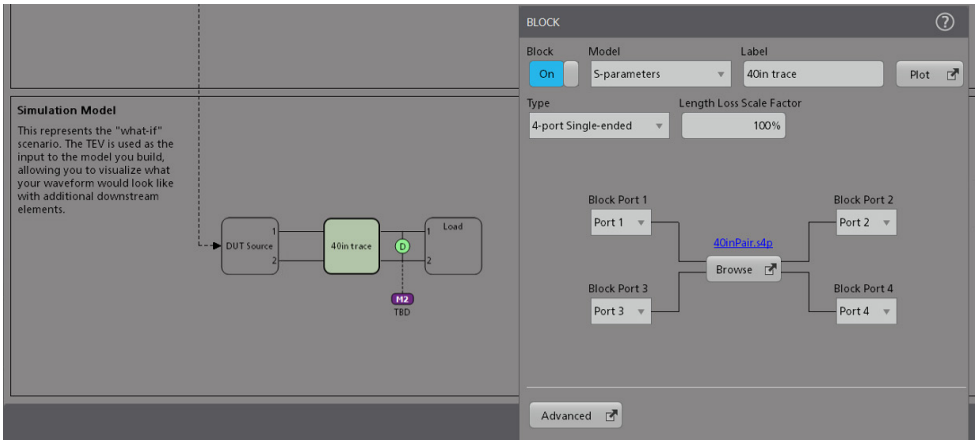


Figure 16. A block added between the DUT (transmitter) and load (oscilloscope) to represent the effects of a 40-inch PCB trace. The block is configured using a .s4p S-parameter to model its expected channel characteristics.

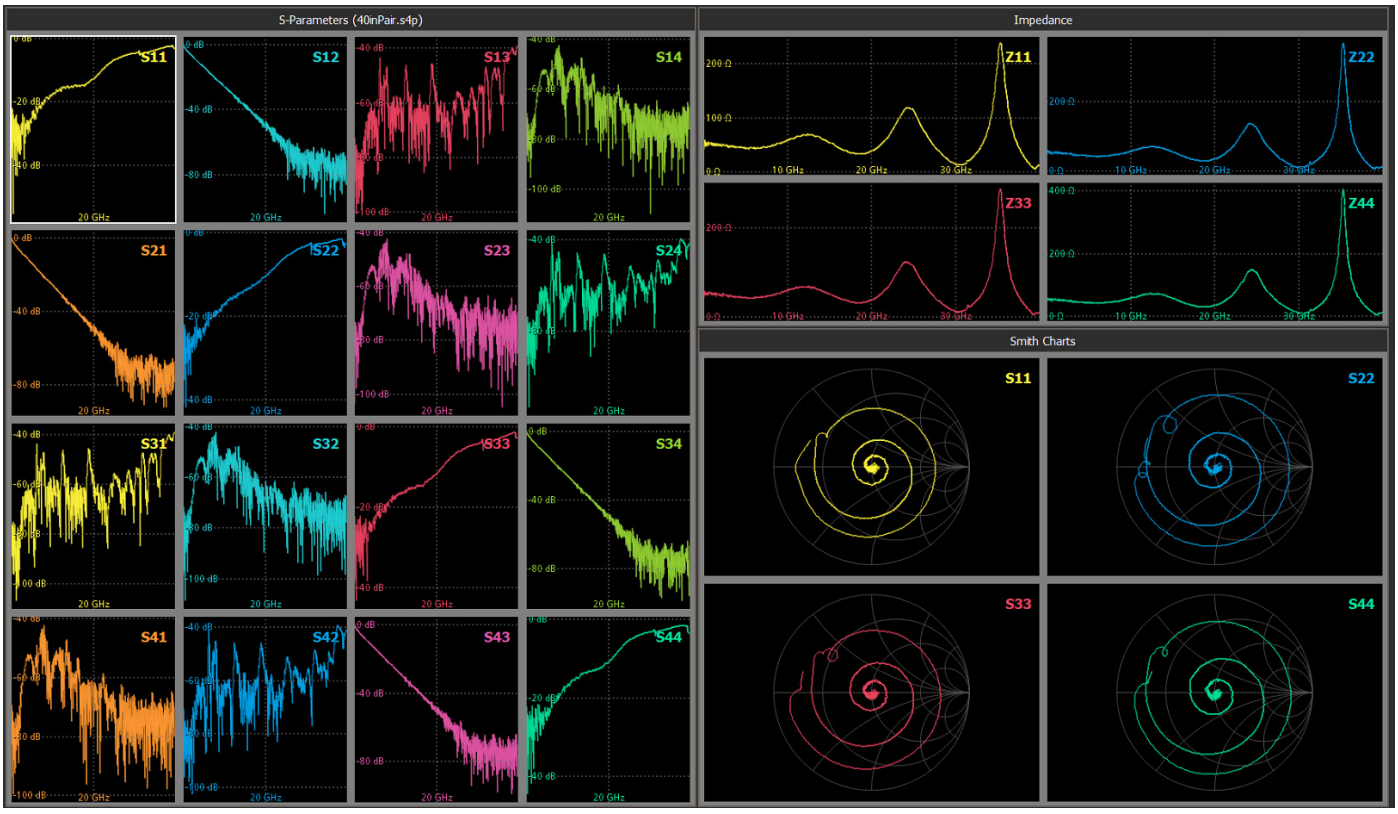


Figure 17. S-parameter plots generated from the block representing the 40-inch PCB trace.

The S-parameters can be plotted to validate its S-parameter quality and response.

Shift the Reference Plane

With the Simulation Model defined, the reference plane has been shifted to the far end of the channel with a virtual test point. This test point was placed after the PCB trace block and assigned to Math2 – the oscilloscope channel the simulated waveform will output to.

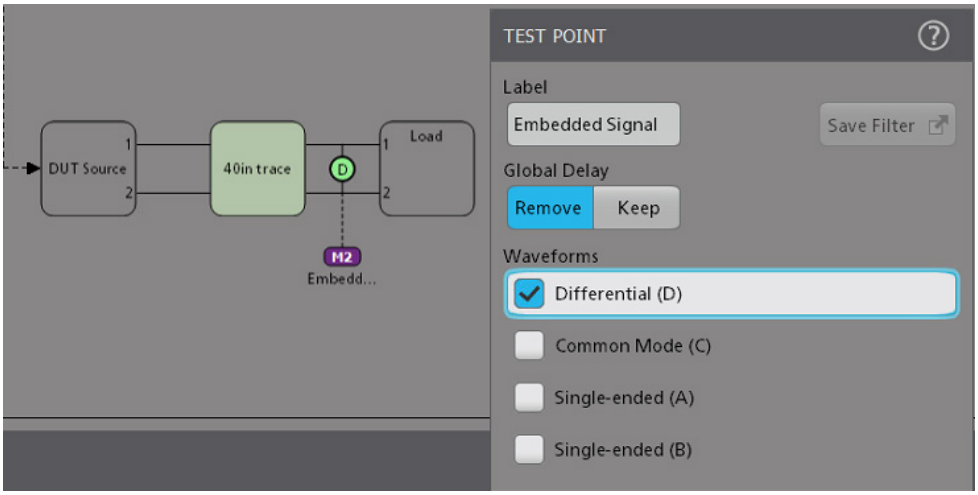


Figure 18. A virtual test point placed after the PCB trace block and assigned to Math2 (M2). M2 shows what the signal would look like at the far end of the channel, terminated into an ideal load.

By doing this, SIM takes the clean real transmitter signal, simulates it traveling through a 40-inch channel, and provides a waveform of what the signal would look like at the far end of the channel, terminated into an ideal load.

View the Waveform at the Desired Test Point

With everything modeled, calculate the SIM to create a filter to view the waveform at the added test point. The software does this by leveraging the S-parameters provided to derive a transfer function for the 40-inch trace.

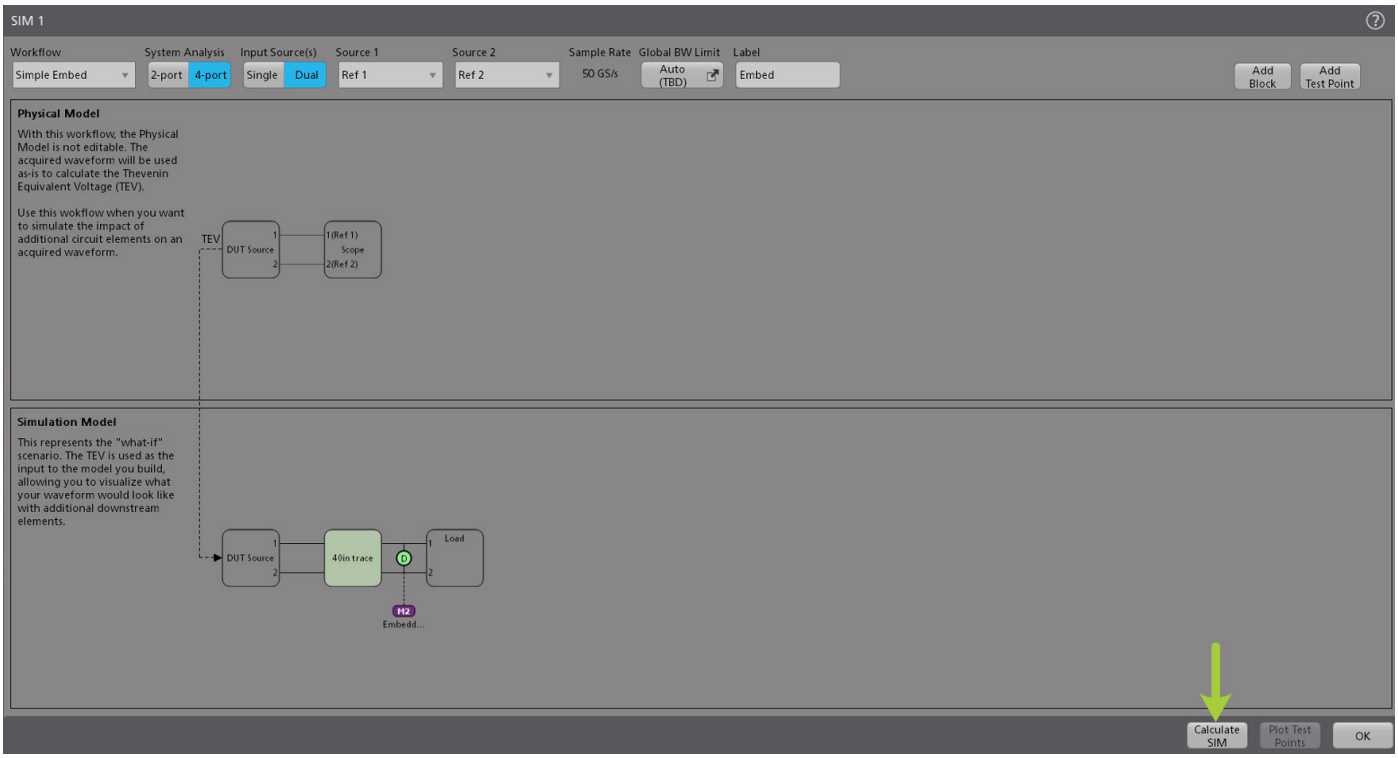


Figure 19. With the Physical Model and Simulation Model defined, Calculate SIM will create a filter to view the waveform at the added test point. The software does this by leveraging the S-parameters provided to derive a transfer function for the 40-inch trace.

After calculation, the embedding filter response can be plotted, as shown in **Figure 20**, and the simulated signal is observed on Math2. Contrast it to the originally acquired signal – which is clean due to its low loss connection directly to the transmitter, as shown in **Figure 21**. The sharp transitions of the original signal are gone, replaced by sluggish rise/fall times and rounded transitions resulting from simulated channel loss and ISI.

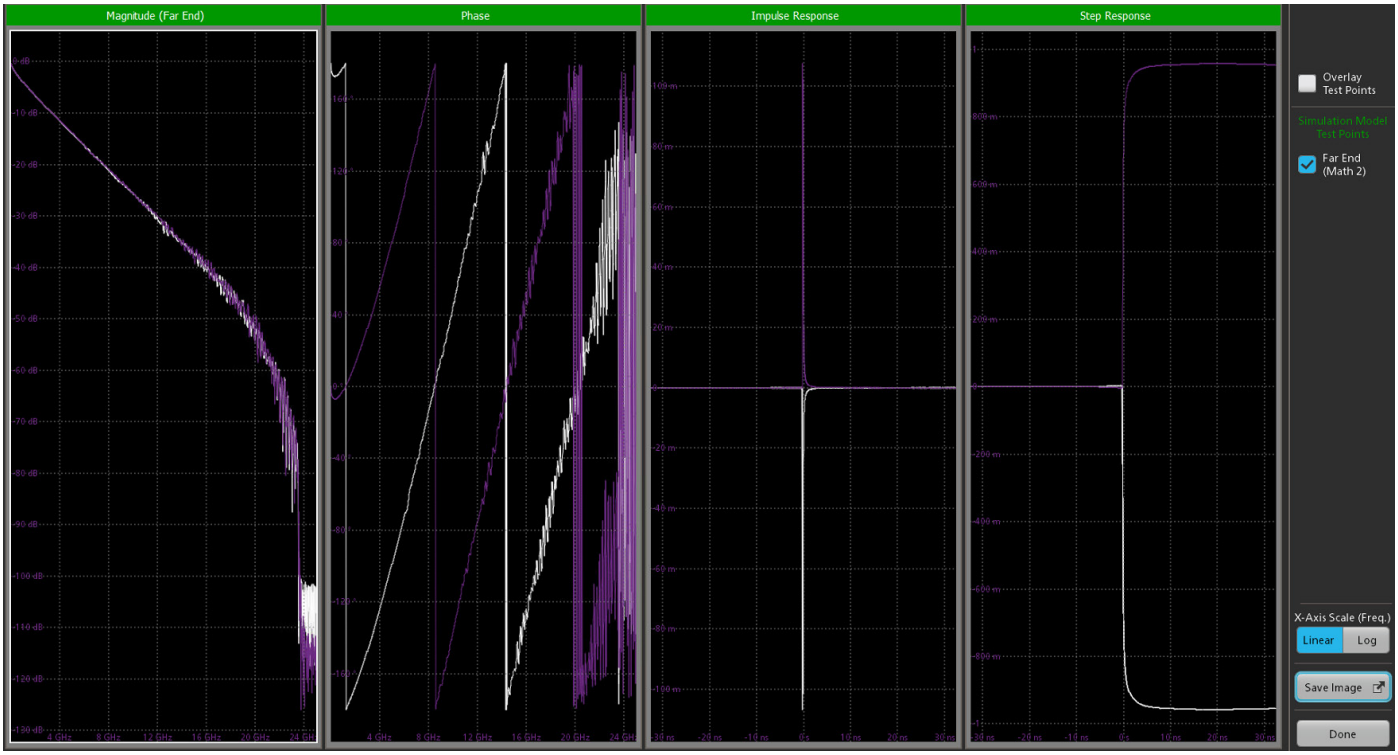


Figure 20. The embedding filter response plotted.

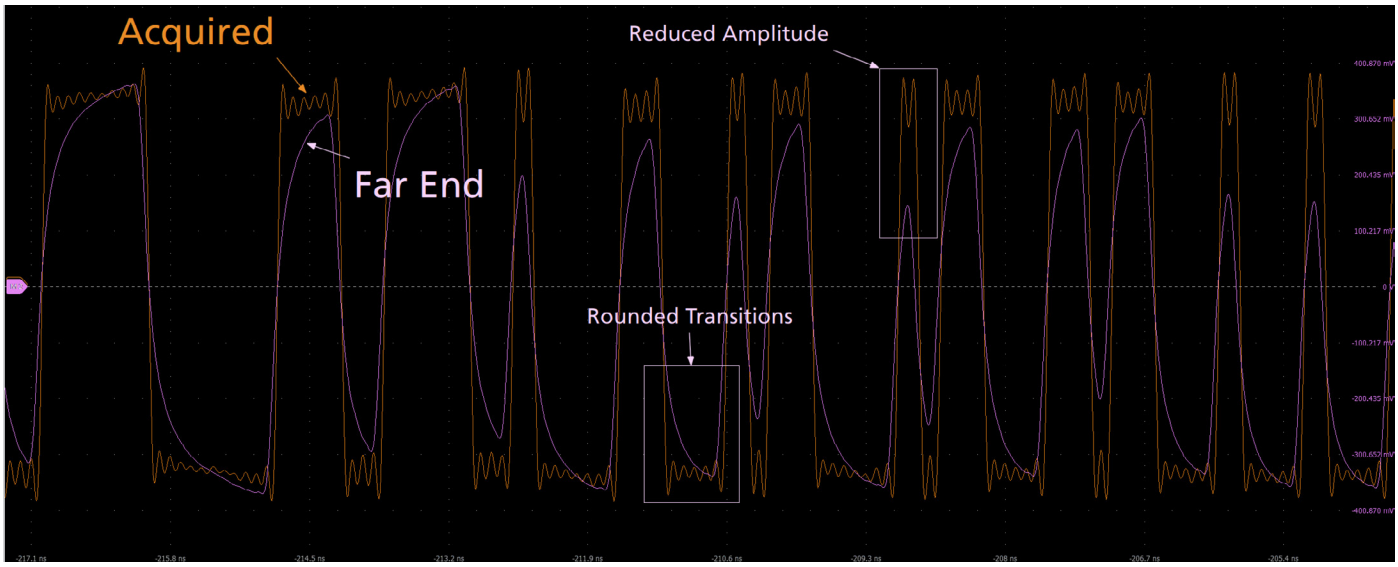


Figure 21. The simulated signal does not have the sharp transitions of the original signal. Instead, it has sluggish rise/fall times and rounded transitions resulting from simulated channel loss and ISI.

The change is extremely apparent when comparing the resulting eye diagrams from both the original and embedded signal. The wide open near end (acquired) eye shrinks significantly after traveling through 40 inches of PCB trace, resulting in the far end (embedded) eye size shrinking. This shows the signal as it would appear at the far end—near the receiver—without needing to manufacture the 40-inch board first.

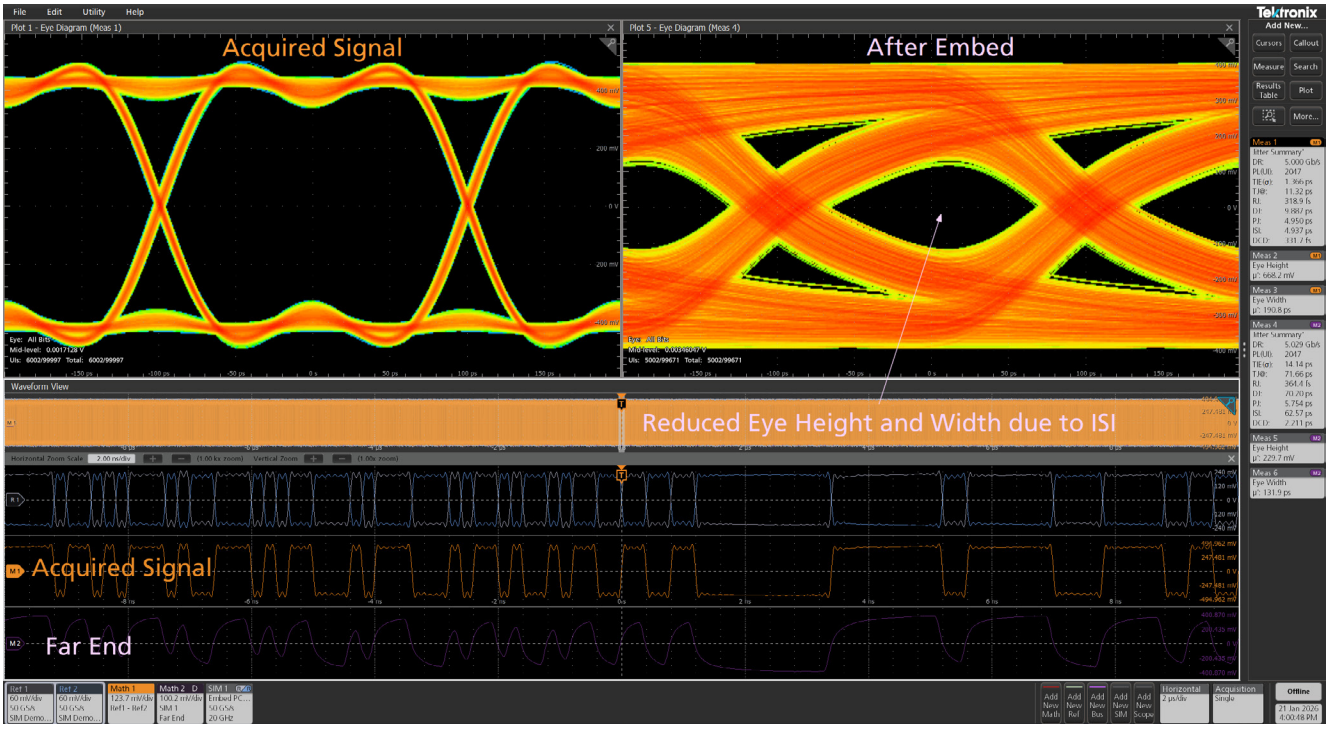


Figure 22. Comparison of the resulting eye diagrams from both the original and embedded signal. The wide open near end (acquired) eye shrinks significantly after traveling through 40 inches of PCB trace, resulting in the far end (embedded) eye size shrinking. This shows the signal as it would appear at the far end—near the receiver—without needing to manufacture the 40-inch board first.

Example 3: Optimizing Receiver Performance: CTLE

With high-speed electrical standards, channel loss is often an unavoidable reality. Higher frequency components are attenuated more severely as the signal travels toward a receiver, resulting in Inter-Symbol Interference (ISI), which can make the data stream difficult or impossible to decode reliably. To counteract these effects, many modern receivers utilize Continuous Time Linear Equalization (CTLE) — a filter that boosts high-frequency signal components to compensate for the channel's frequency-dependent loss. However, the CTLE is part of the receiver integrated circuit and cannot be accessed by test equipment, so it must be modeled.

SIMA's Rx Equalization workflow enables this modeling directly on the oscilloscope, emulating the behavior of a receiver at the far end of the lossy channel — applying the same equalization the receiver would use, and displaying the result as it would appear inside the receiver's silicon

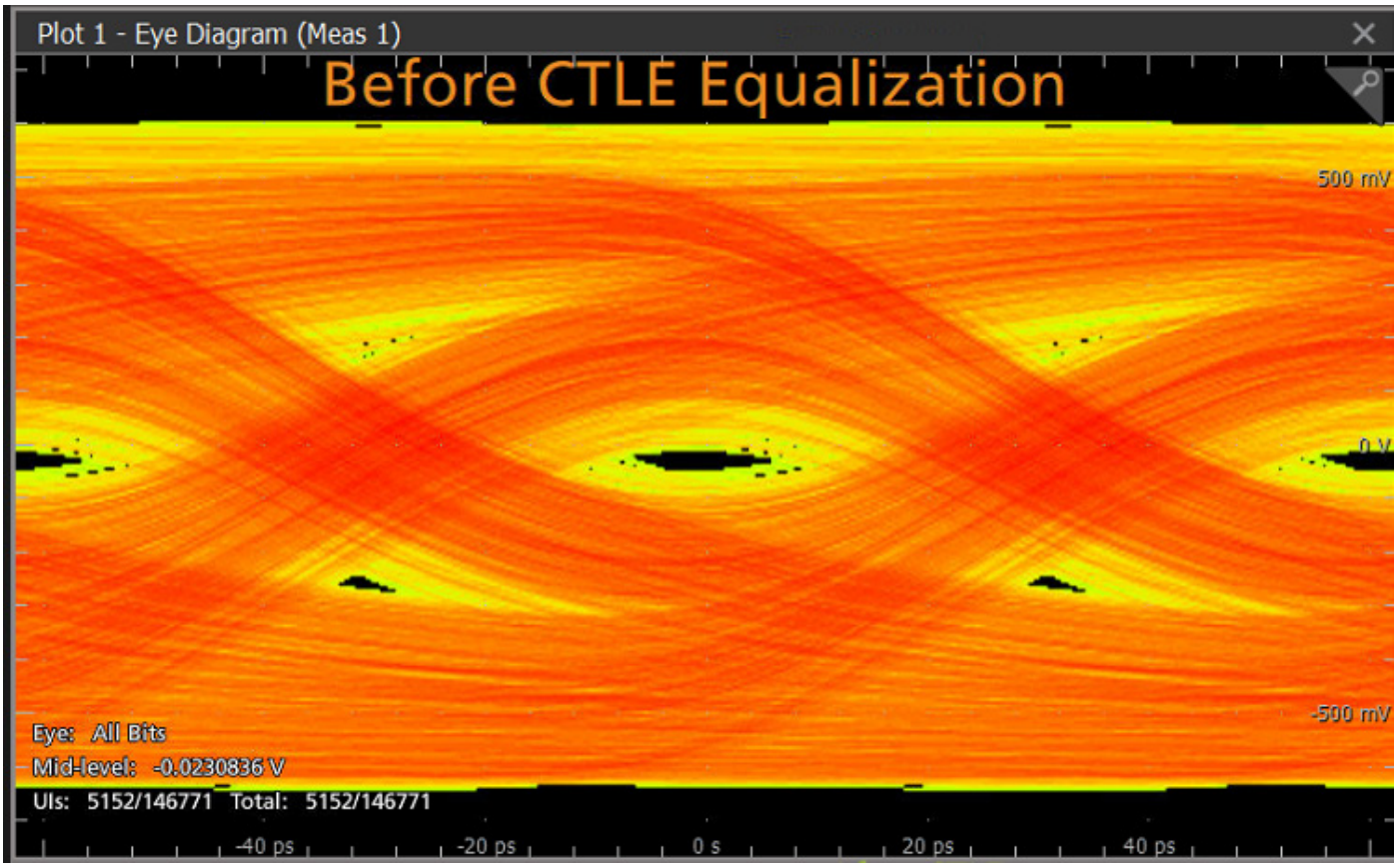
Analyzing the Degraded Signal

An Anritsu MP1900A BERT is outputting a 16 Gb/s differential data signal using NRZ signaling with a PRBS15 pattern. The data signal is transmitted through a 17-inch differential PCB trace, into a pair of 1-meter SMA cables, and finally into two channels of a Tektronix DPO714AX oscilloscope equipped with Advanced Jitter Analysis software (option DJA) and Signal Integrity Modeling Advanced software (option SIMA).

As shown in **Figure 23**, the baseline eye performance before equalization is extremely poor. The eye is nearly closed and in a bathtub plot, the eye width at the target Bit Error Rate (BER) of 1E-12 is only 14.8 ps.

Constructing the Equalization Model

SIMA's Rx Equalization workflow simulates the receiver portion of a serial data link, restoring data stream integrity and recovering the embedded clock. This provides everything needed to evaluate the post-equalization signal at any stage of the receiver chain.



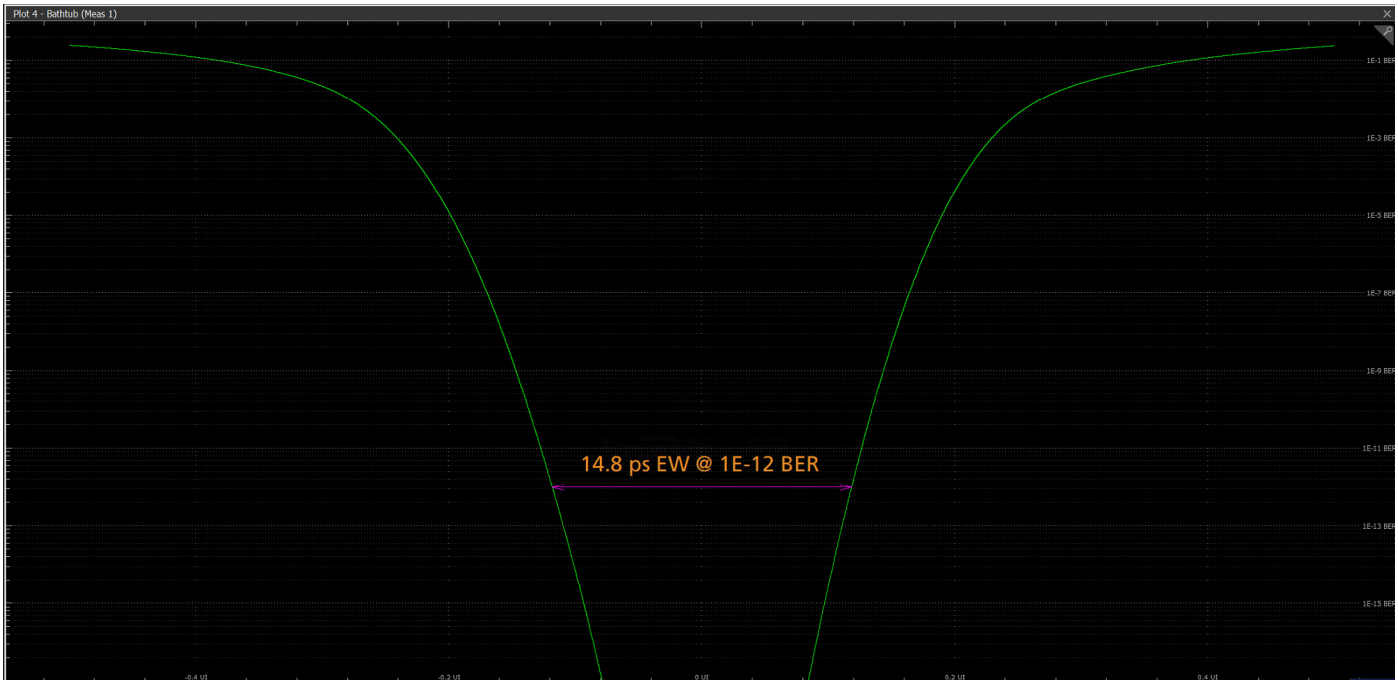


Figure 23. An eye diagram of the signal before equalization. The eye is nearly closed with no corrective measures applied. The degradation is also evident in a bathtub plot, where the eye width at the target Bit Error Rate (BER) of 1E-12 is only 14.8 ps wide.

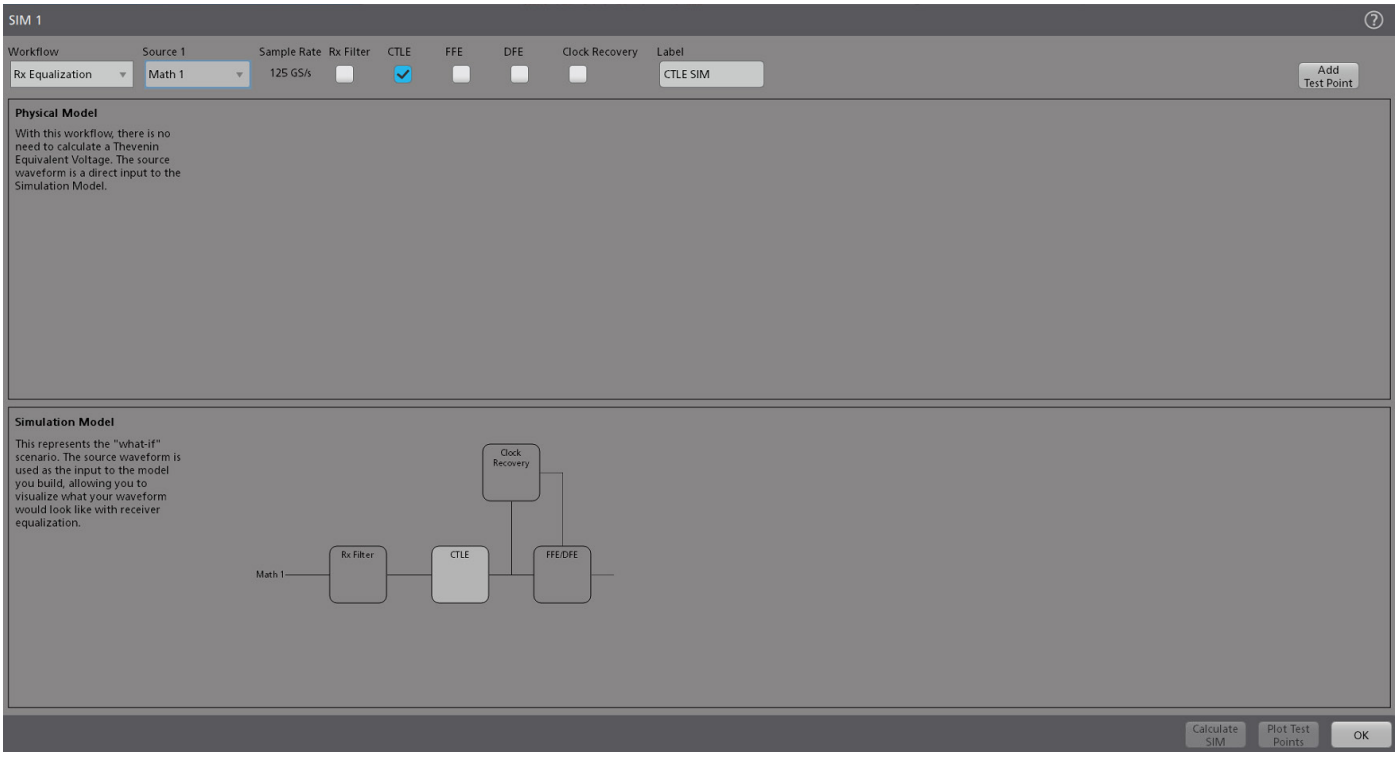


Figure 24. The Rx Equalization Workflow, available with SIM Advanced, being configured for quick evaluation of the signal as it would appear inside the receiver's silicon.

With CTLE enabled on the top ribbon, as shown in **Figure 24**, the Simulation Model allows configuration of the CTLE block. A .json file can be uploaded directly to model the CTLE, or a custom definition of the filter can be configured. The receiver uses a 6 dB CTLE as defined in the PCI Express Gen 4 specification, which defines one zero at 1 GHz and poles at 2 GHz and 16 GHz, with a DC gain (Adc) of 0.5. These parameters produce the characteristic high-frequency peaking needed to counteract channel loss. A CTLE configuration can be easily plotted to view its response and how the signal will be affected (see Appendix: CTLE).

Additional receiver equalization blocks, including the Rx Filter, FFE, DFE, and Clock Recovery, can also be configured if needed. For this example, only the CTLE block is enabled.

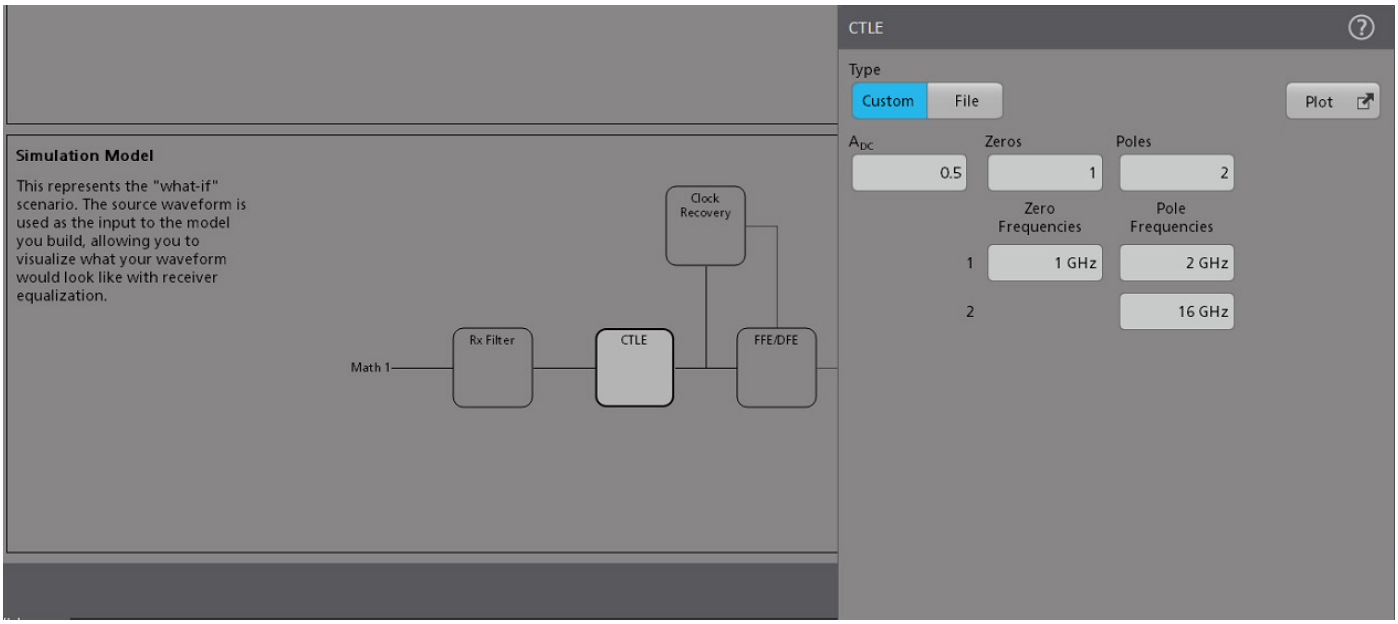


Figure 25. The Simulation Model allows configuration of the CTLE block. A .json file can be uploaded directly to model the CTLE, or a custom definition of the filter can be configured. The receiver uses a 6 dB CTLE as defined in the PCI-Express Gen 4 specification, so this CTLE block is modeled to match.

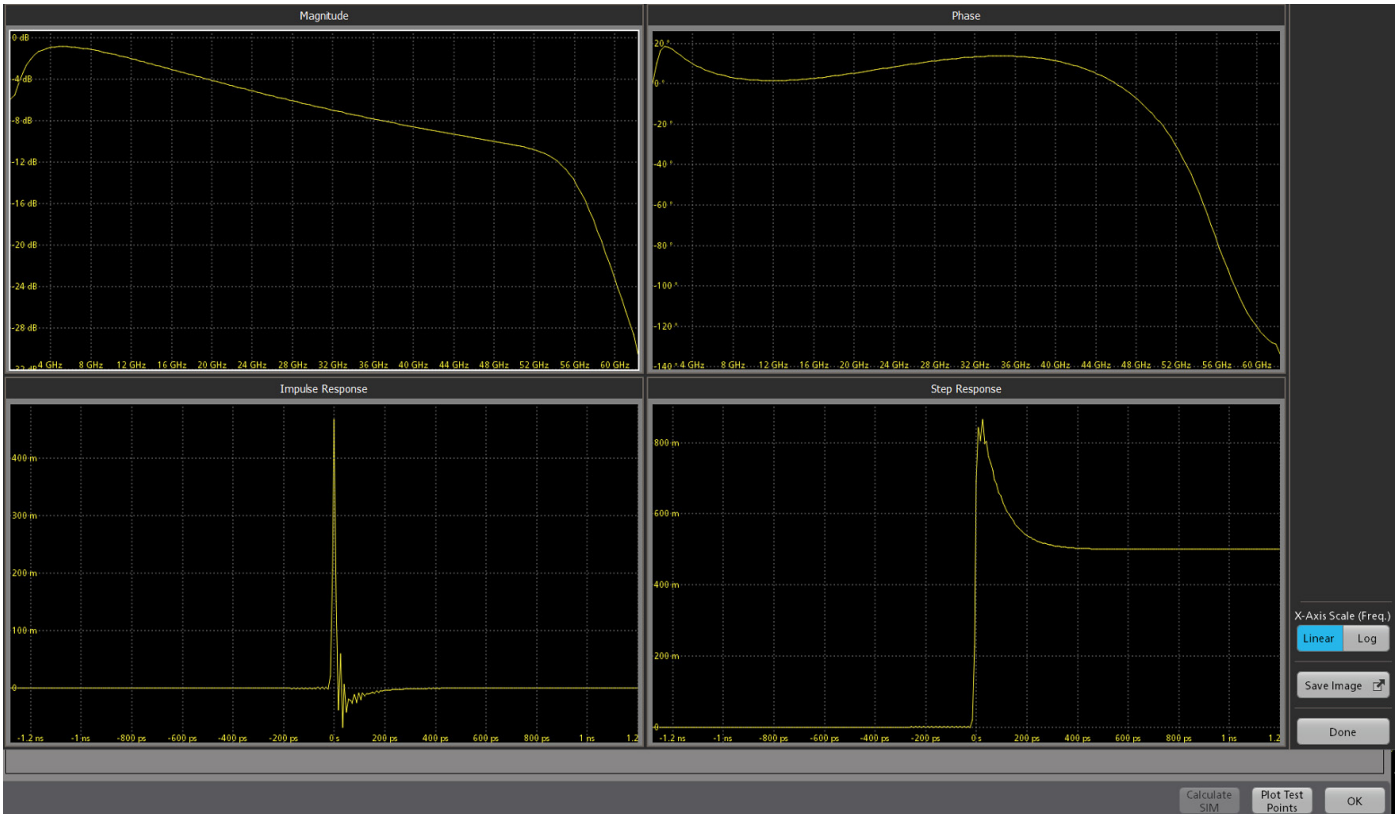


Figure 26. The CTLE Configuration plotted to view its response and how the signal will be affected.

Moving the Reference Plane

With the equalization model defined, the measurement reference plane must be shifted from the physical input of the receiver to the internal output of the CTLE filter – an inaccessible location. In the Simulation Model, a virtual test point is established at the output of the CTLE block and assigned to a new math channel, M2.

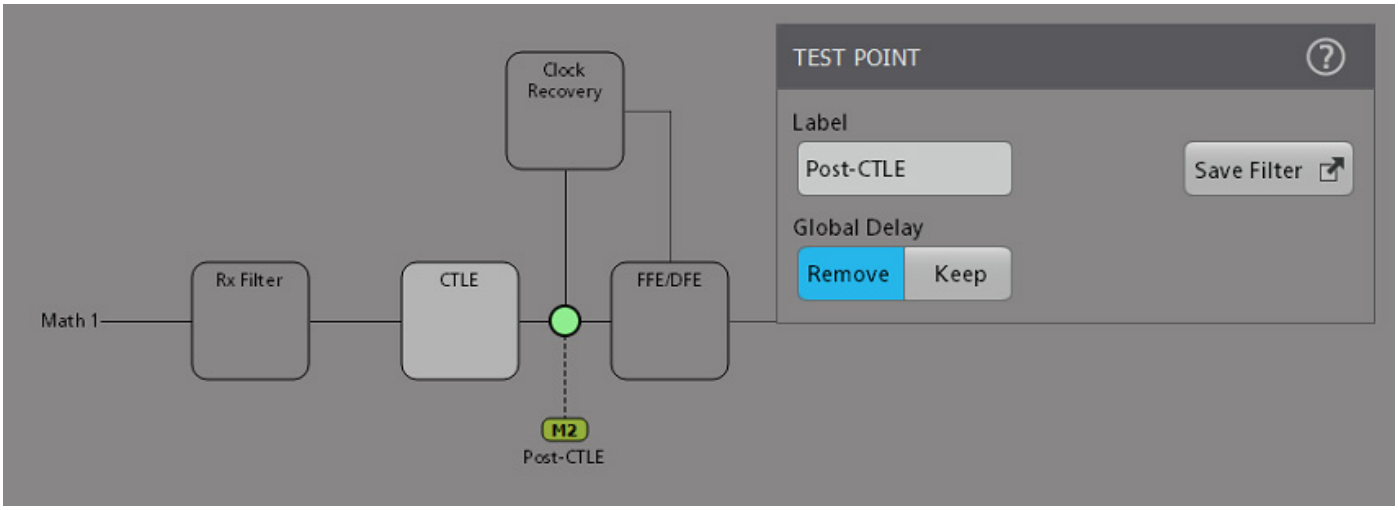


Figure 27. A virtual test point is established at the output of the CTLE block and assigned to a new math channel, M2.

This placement takes the degraded far-end signal and simulates the results of the receiver equalization. The resulting waveform represents the state of the data just before it reaches the decision-making circuitry of the receiver.

Applying the CTLE Transfer Function to the Acquired Waveform

Pressing the 'Calculate SIM' button computes the CTLE transfer function, generates a corresponding FIR filter for each test point, and applies it to the source waveform resulting in the M2 waveform. The impact of equalization is immediately visible in the resulting eye diagram. CTLE has greatly opened up the eye. A significant reduction is seen in ISI and jitter in the post-CTLE waveform. The eye width at a BER of 1E-12 has dramatically increased to 48.9 ps.

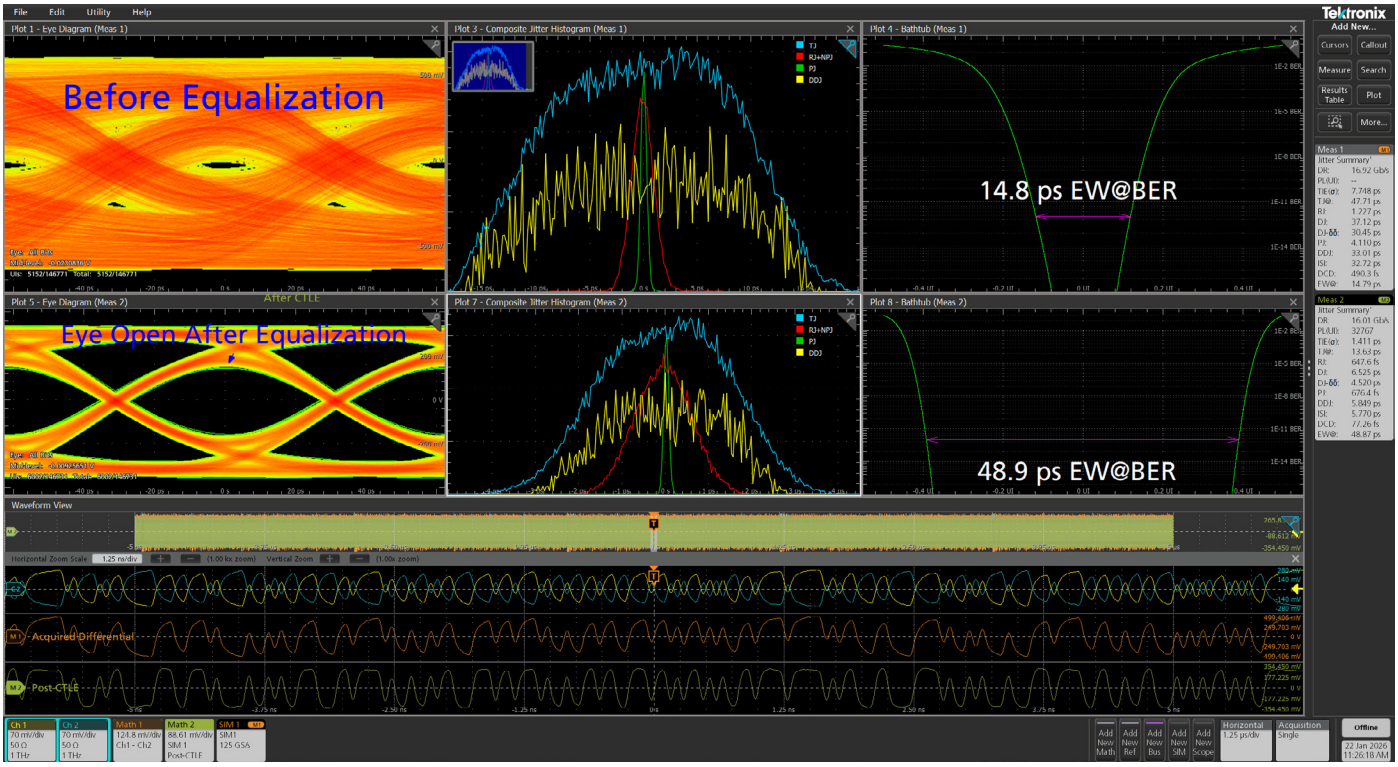


Figure 28. CTLE has greatly opened up the eye. We see a significant reduction in ISI and jitter in the post-CTLE waveform. The eye width at a BER of 1E-12 has dramatically increased to 48.9 ps.

These results indicate strong receiver performance with this CTLE configuration. The SIM results show that the receiver can successfully interpret the data despite the losses incurred during transmission, providing confidence in the system's overall performance.

Example 4: Recovering Signal Integrity: DDR Reflection Removal

In DDR memory applications, the physical topology of the system creates a challenging environment for signal integrity. The future channels that DRAM will sit at the far end of are often unknown until system integration testing begins. The most common way to access DDR signals is through an interposer utilizing mid-bus probing. The overall channel consists of multiple impedance discontinuities at the DIMM connectors, the DRAM package, the probing hardware, and the termination points.

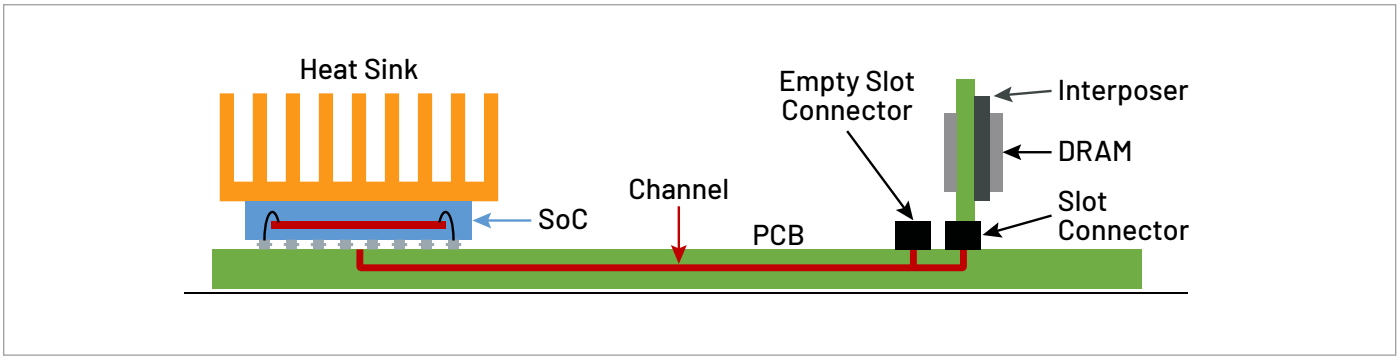


Figure 29. DDR memory applications are a challenging environment for signal integrity. The future channels that DRAM will sit at the far end of are often unknown until system integration testing begins. The most common way to access DDR signals is through an interposer utilizing mid-bus probing.

These discontinuities manifest waveform reflections traveling throughout the channel. These reflections often appear as step-like anomalies in the waveform, which can lead to poor measurement results.

To overcome these challenges, SIM has an Advanced Workflow that can be used for such topologies where mid-bus probe de-embedding is required. The Mid-Circuit setting provides access to a mid-bus block diagram to accurately model the physical set up and generate a corrected signal free of reflected imperfections. The following example demonstrates this.

Analyzing a Mid-bus Waveform with Reflections

A DRAM module on a consumer ready UDIMM is being evaluated in a system and has a Nexus Interposer attached. Soldered to the interposer pads is a Tektronix P77STFLXB solder-down probe tip being used in combination with a P7720 TriMode performance probe and DPO714AX oscilloscope. The connected differential data strobe (DQS) signal has been acquired from this DDR system in a mid-bus setup. A single burst has been isolated in the acquisition for clarity — note in **Figure 30** the stepwise response on both the rising and falling edges of the DQS signal, muddying up what would otherwise be a clean signal. These are caused by reflections traveling through the channel because of impedance discontinuities in the test setup.

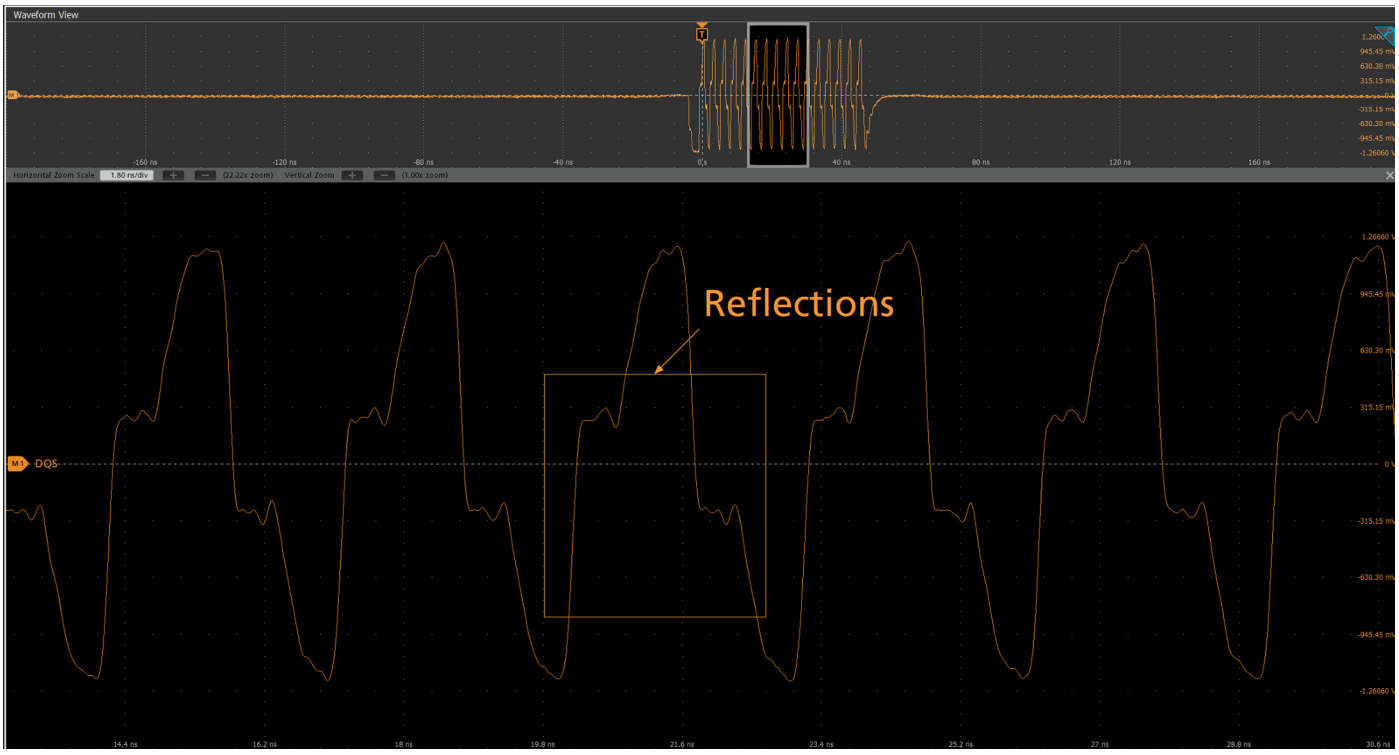


Figure 30. A single burst from the acquired differential data strobe (DQS) signal. The stepwise response on both the rising and falling edges of the DQS signal is muddying up what would otherwise be a clean signal. These are caused by reflections traveling through the channel because of impedance discontinuities in the test setup.

To correct this behavior, SIM can accurately model the system and generate a corrected signal free of reflected imperfections.

Model the Physical System

The Advanced Workflow in SIM best models the setup of this DDR system. The signal access point is set to Mid-Circuit, which provides access to a mid-bus block diagram matching the physical setup on the bench, where the Signal Access Point (SAP) block represents the mid-bus probe connection—the physical location where the interposer taps into the signal path.

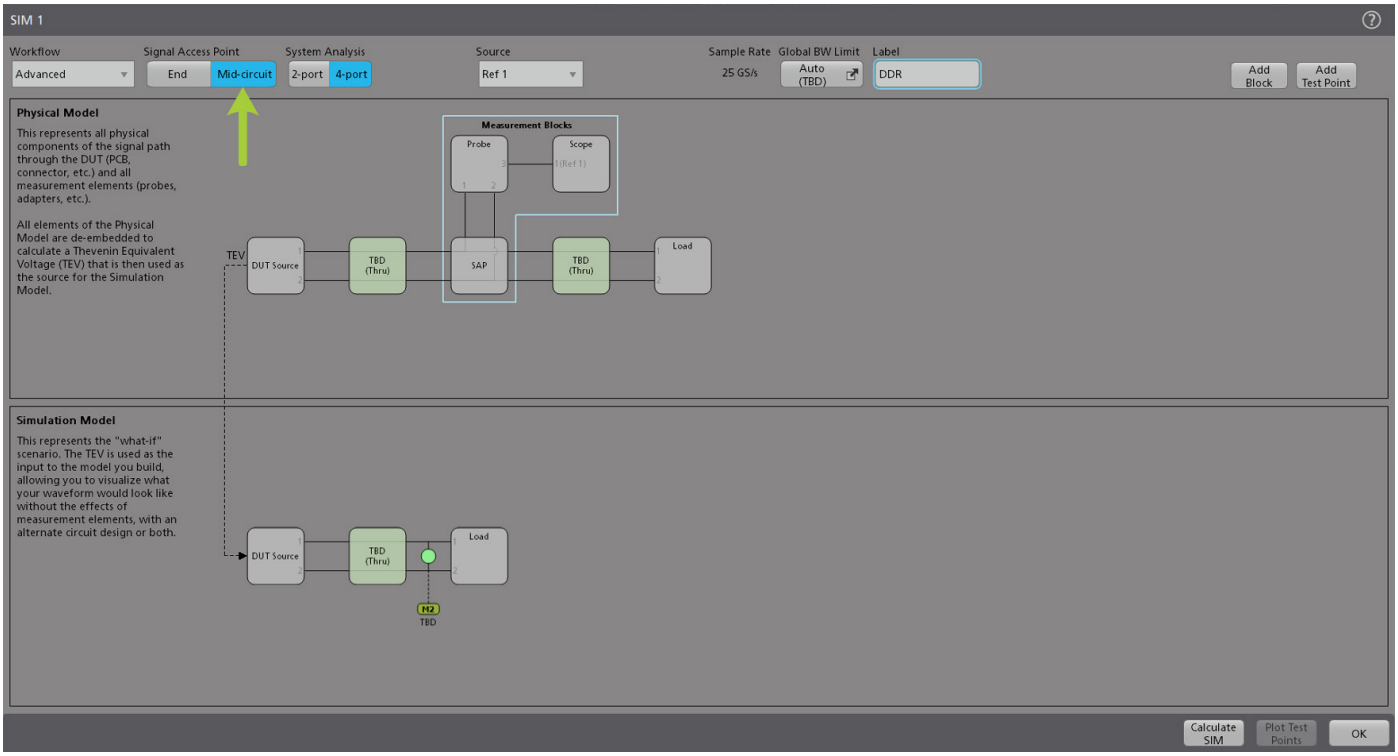


Figure 31. The Advanced Workflow in SIM, useful for modeling the setup of a DDR system. The signal access point is set to Mid-Circuit, which provides access to a mid-bus block diagram matching the physical setup on the bench.

Each block represents an element in the real test setup and must be configured accordingly. Circuit components can be best characterized in a block by either loading an S-parameter file directly, or by manually configuring its characteristics, such as with a transmission line model.

Modeling the DRAM

The Load block is used to characterize the DRAM termination impedance and for this device is set to 200 Ω as shown in the figure below.

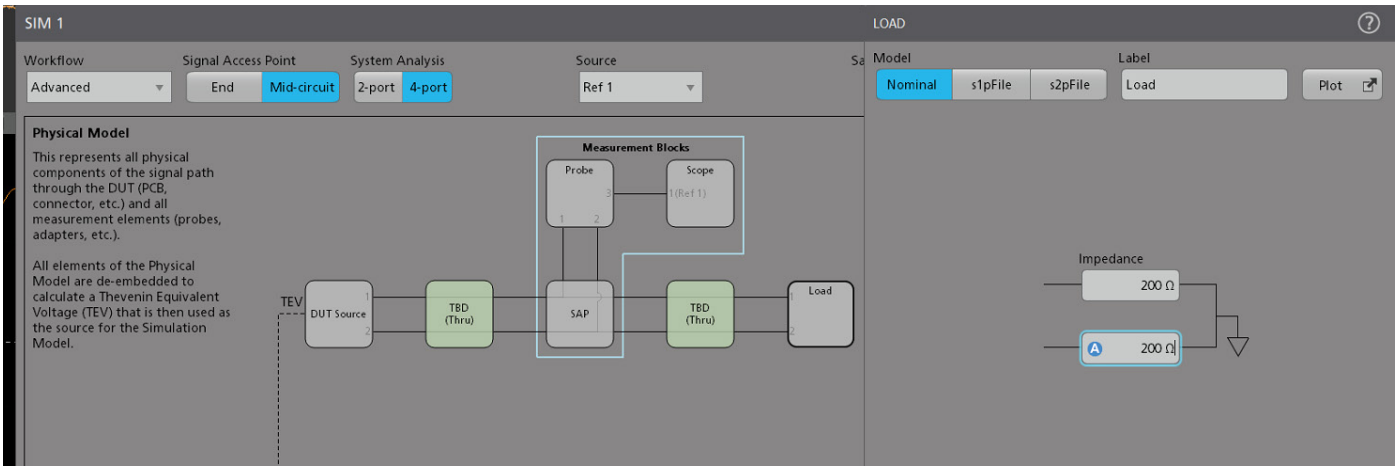


Figure 32. Each block represents an element in the real test setup. Blocks are configured by either loading an S-parameter file directly, or by manually configuring its characteristics, such as with a transmission line model.

A block labeled "PKG" has been added to model the DRAM package loss. This loss is internal to the DRAM before the signal reaches the receiver and is represented by an s4p file as shown in the figure below.

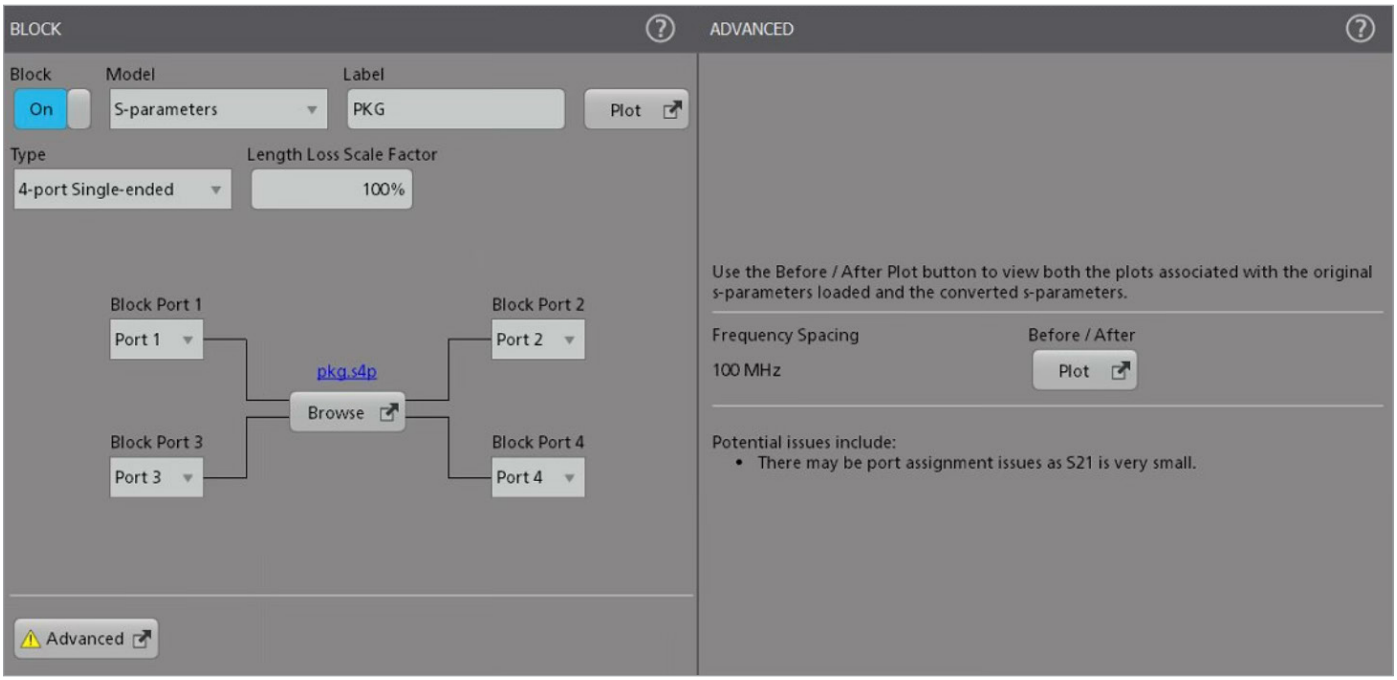


Figure 33. The Load block, labeled "PKG", is used to model the DRAM termination. A warning is flagged saying "There may be port assignment issues as S21 is very small". The Plot button can be used to easily plot S-parameters.

After loading the PKG .s4p file, SIM flags a warning as seen in the image above. Clicking the "Advanced" button reveals the warning: 'There may be port assignment issues as S21 is very small.' This is a useful prompt to inspect the S-parameters before proceeding. SIM's S-parameter plots can be used to quickly spot oddities. Clicking Plot reveals the issue seen in **Figure 34**: the transmission parameters S21, S12, S34, and S43 show a non-monotonic profile, peaking mid-band rather than increasing smoothly with frequency as expected for a passive package interconnect. This indicates a port assignment mismatch. It's important to note that correctly setting the port inputs and outputs of an S-parameter model is crucial to accurate representation..

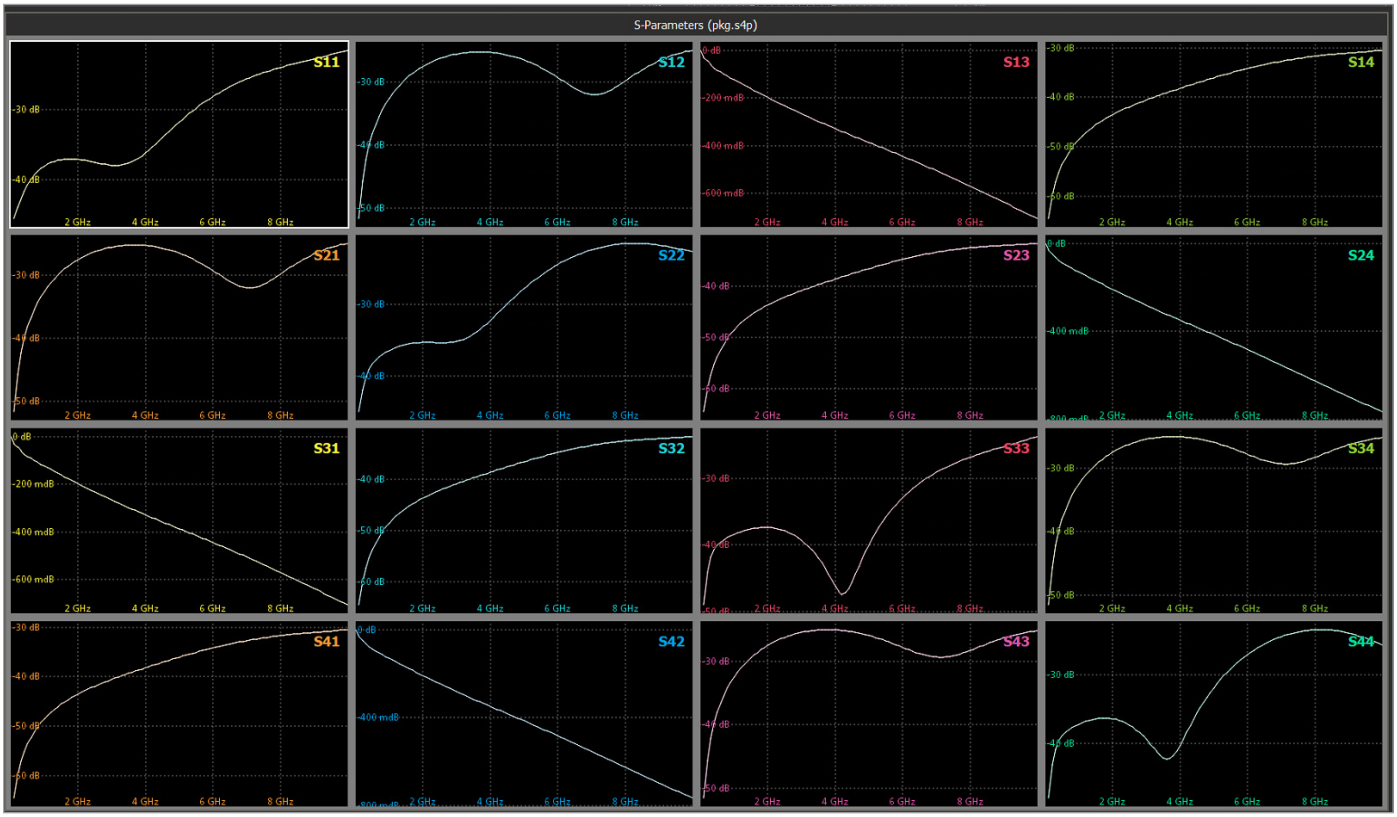


Figure 34. S-parameter plots allow for rapid visual inspection and validation of block component behavior.

The port assignments for specific S-parameter models are dependent on how they were defined when the S-parameter file was generated, which can sometimes vary across tools. Rather than manually modifying the S-parameter file, port assignments can easily be adjusted in SIM to ensure that the S-parameter is modeled correctly in the system. Swapping the port assignments for "Block Port 2" and "Block Port 3" fixes the issue.

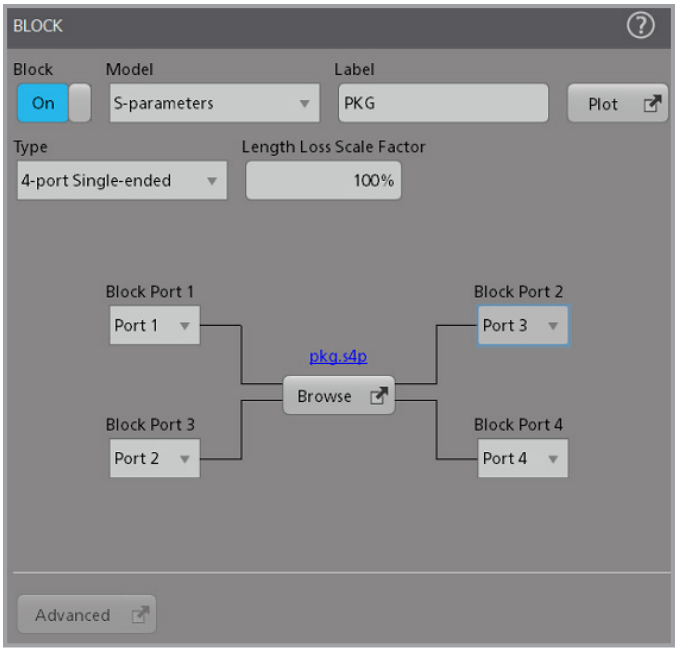


Figure 35. Ports can be easily remapped in the block configuration menu. No need to manually edit and reupload the .s4p file.

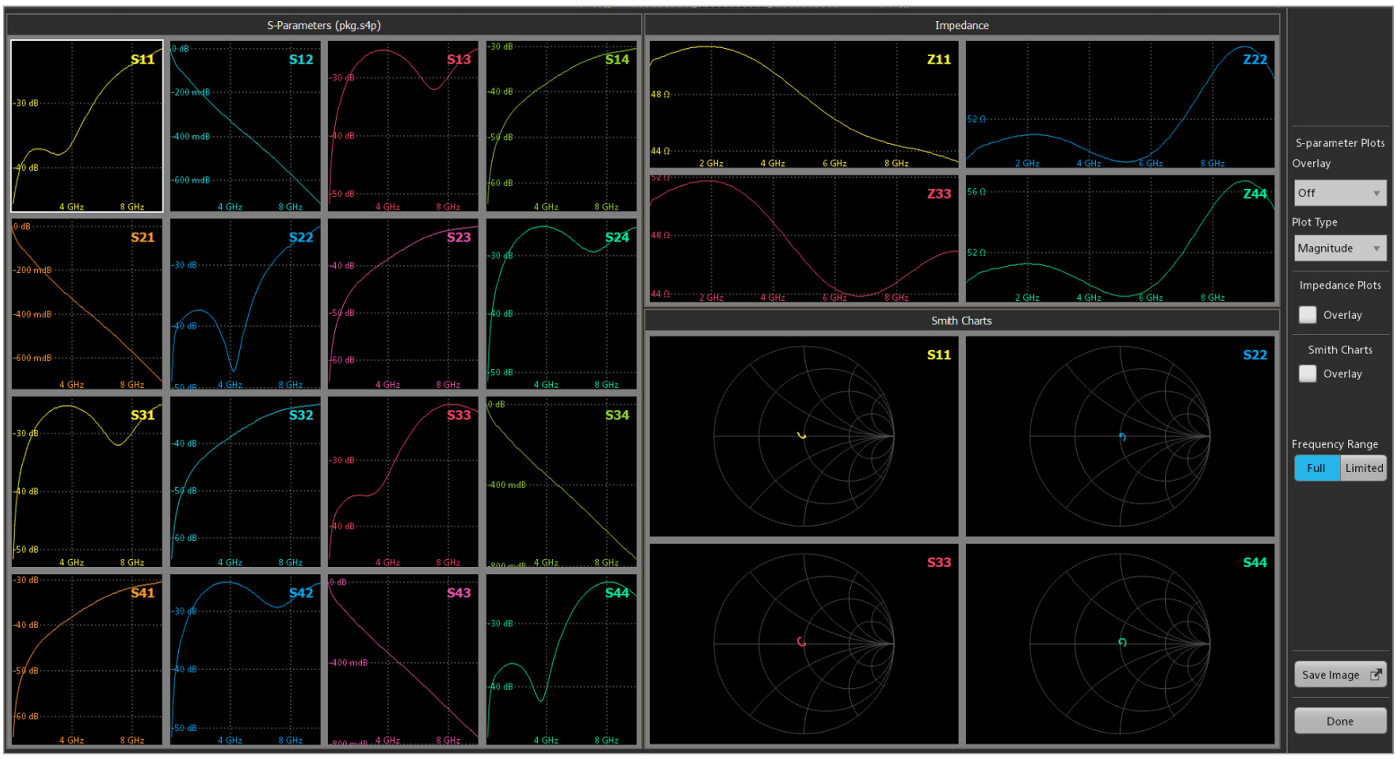


Figure 36. Replotting the S-parameters after correcting the port configuration reveals an expected response.

Replotting the S-parameters after correcting the port mapping reveals an expected response as seen in **Figure 36**.

Model the PCB Traces

The PCB traces leading to the DRAM itself are modeled by a block configured as a transmission line as shown in **Figure 37**. The round trip delay, if unknown, can be observed in a pronounced incident waveform reflection on the oscilloscope shown in **Figure 38**. Half the round trip delay is attributed to the T-line model in SIM.

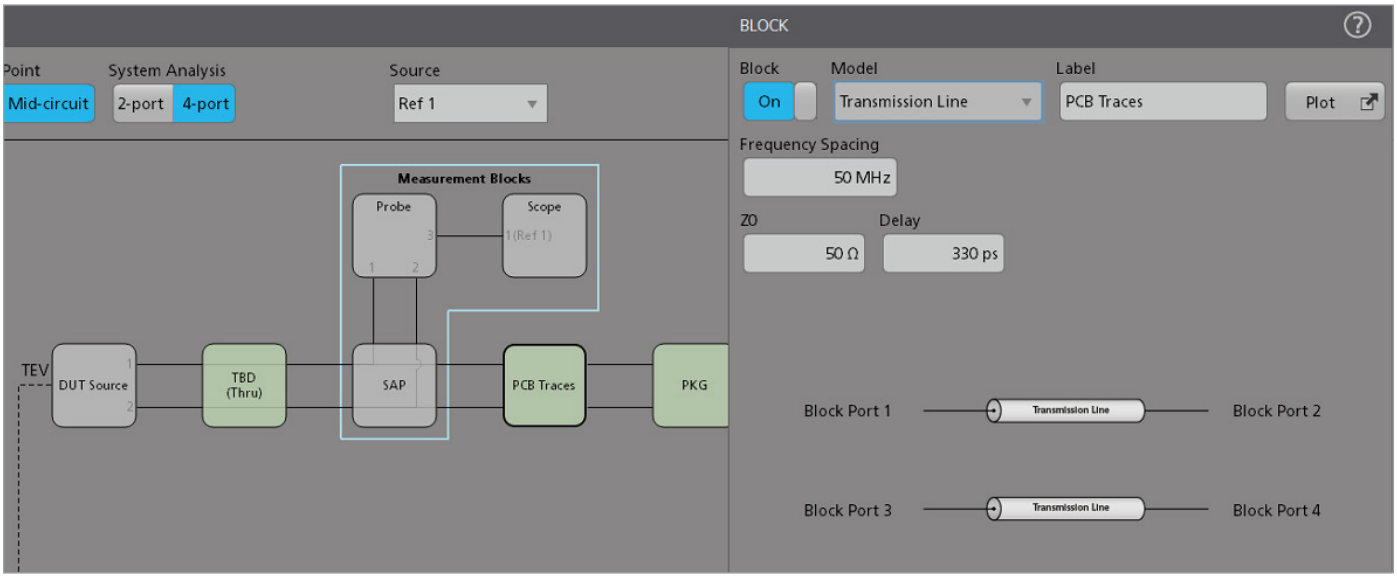


Figure 37. The PCB traces leading to the DRAM itself are modeled by a block configured as a transmission line.

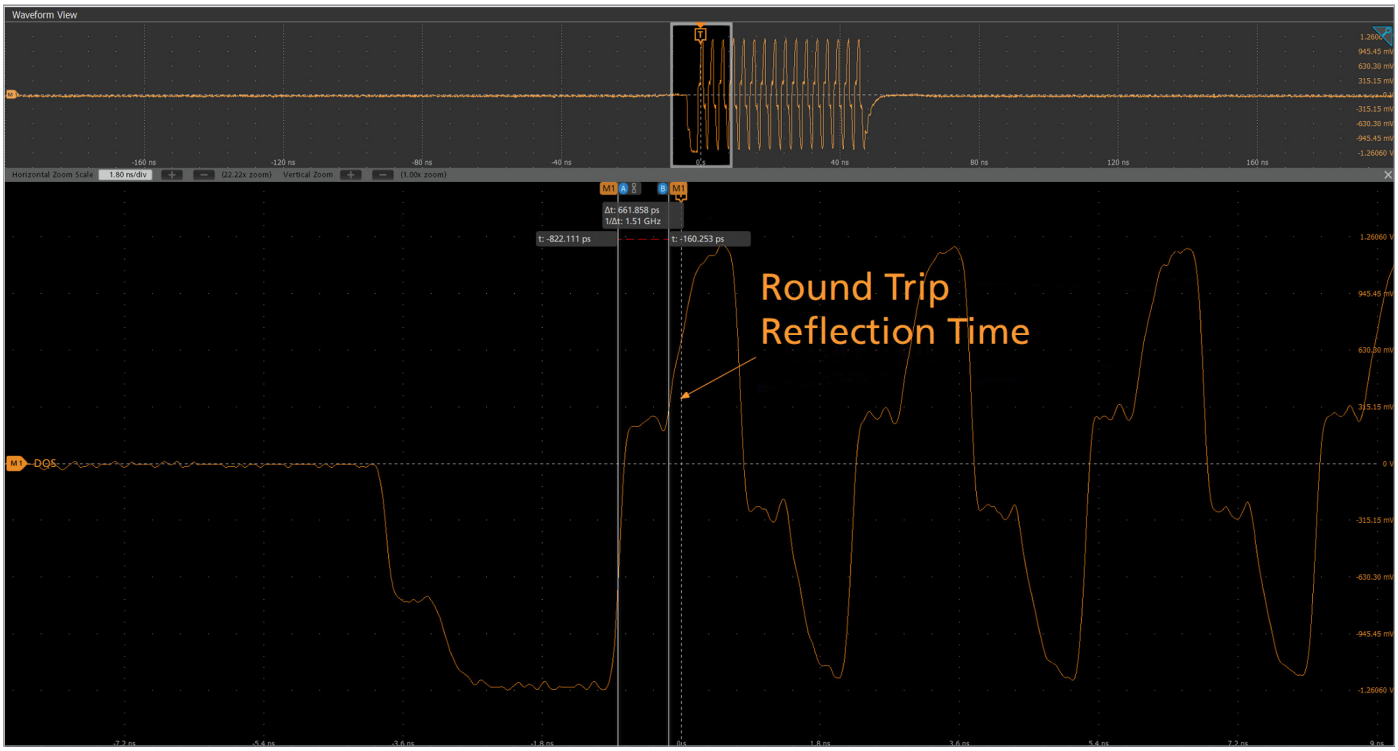


Figure 38: The round trip delay observed in a pronounced incident waveform reflection.

Model the Probe Block

The Probe block represents the electrical loading and frequency response of the probing hardware used to access the DDR signal. In a mid-bus configuration, the probe introduces its own impedance discontinuities, parasitic capacitance, and bandwidth limitations, all of which contribute to reflections and amplitude distortion. Accurately modeling the probe is essential to separating true DUT behavior from measurement artifacts.

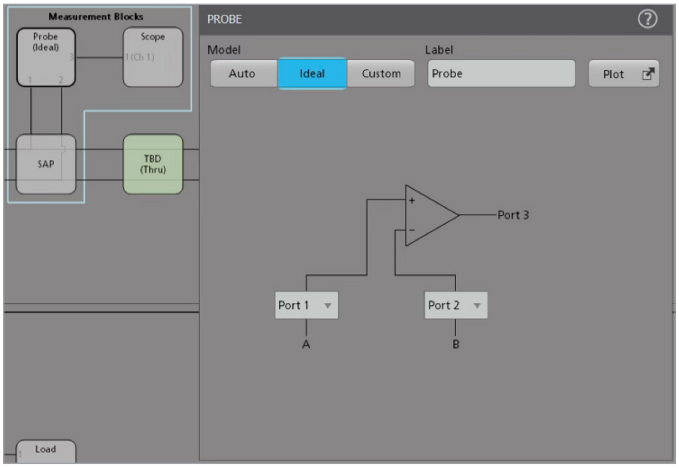


Figure 39. The Probe block configured using ideal mode. This mode represents an idealized probe with negligible loading and flat frequency response across the analysis bandwidth.

The Probe block can be configured using three modeling modes: Auto, Ideal, and Custom.

Auto mode applies a pre-characterized S-parameter model for supported Tektronix probes connected to the oscilloscope. This simplifies setup, reduces modeling errors, and ensures that the probe's bandwidth, loading, and differential behavior are accurately represented without requiring manual file management. Auto mode is recommended when using supported Tektronix probing hardware and when rapid setup and repeatability are priorities.

Ideal mode represents an idealized probe with negligible loading and flat frequency response across the analysis bandwidth. Refer to the SIM datasheet for a list of supported probes. This mode is useful for conceptual exploration, debugging model configuration, or isolating the impact of other blocks in the cascade. Because Ideal mode does not represent real probe behavior, it should not be used for compliance or correlation analysis, but it can be valuable for quickly understanding sensitivity to measurement intrusiveness. For this example, Ideal mode is used.

Custom mode allows the user to load a measured S-parameter file—typically obtained from a VNA characterization of the probe, tip, and any adapters—to precisely model the probe's real-world response. This is particularly important in DDR mid-bus environments, where probe capacitance and stub effects can significantly influence reflections and eye quality. In Custom mode, correct port mapping and verification of passivity and causality are critical to ensure physically meaningful results.

Once defined, the Probe block becomes part of the overall cascade, allowing SIM to mathematically remove its effects during de-embedding or evaluate its contribution when analyzing signal fidelity at various virtual test points.

Generate the Corrected Signal

With the physical environment modeled, the goal is to look at the signal without the artifacts introduced by the test setup. This is achieved by shifting the measurement reference plane to the virtual test point location.

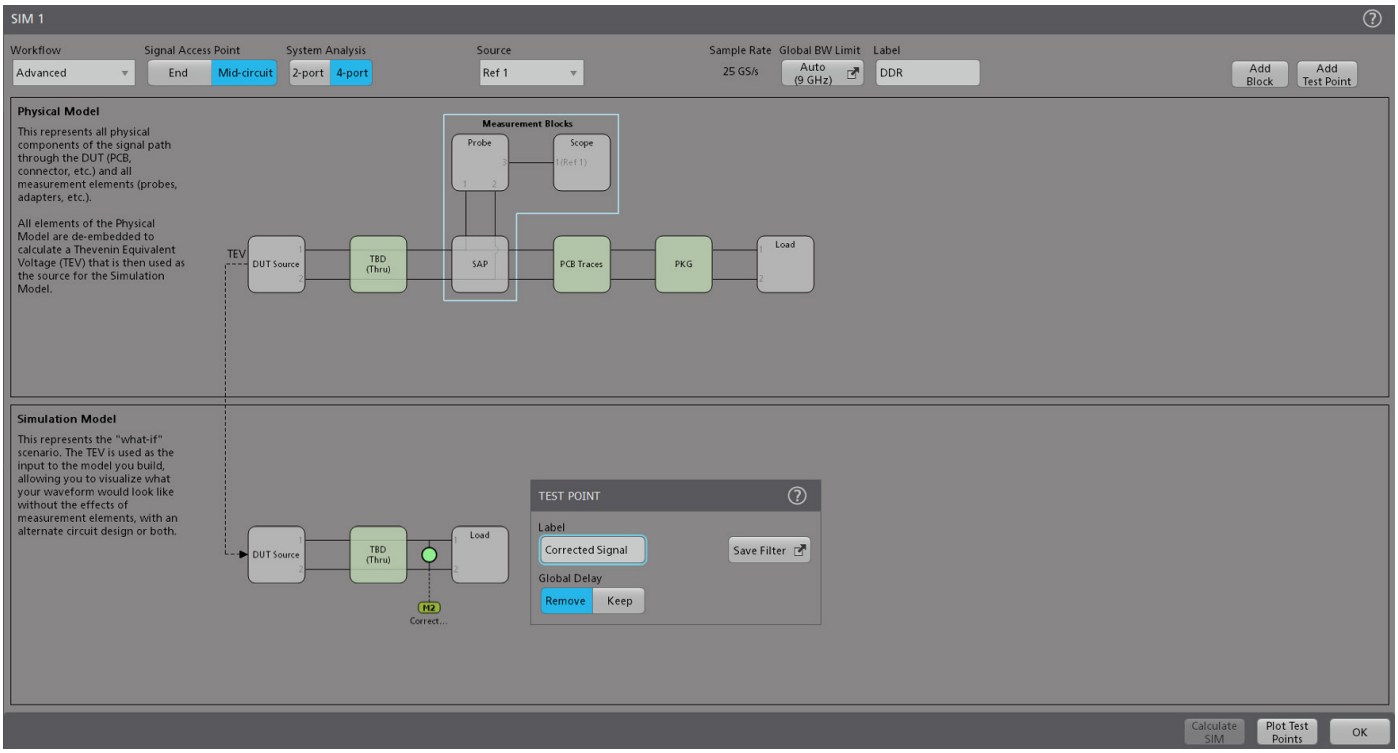


Figure 40. A virtual test point is established at the input of the Load block in the Simulation Model to see the signal as it was before it was distorted by the test setup.

In the Simulation Model, a virtual test point is established at the input of the Load block. This point is assigned to a new math channel, M2. To generate the corrected signal, the software derives an inverse transfer function of what the signal would look like at the virtual test point without the discontinuous effects of the components (Probe, PCB Trace, DRAM PKG) in the physical model. The corrected signal is shown in the figure below.

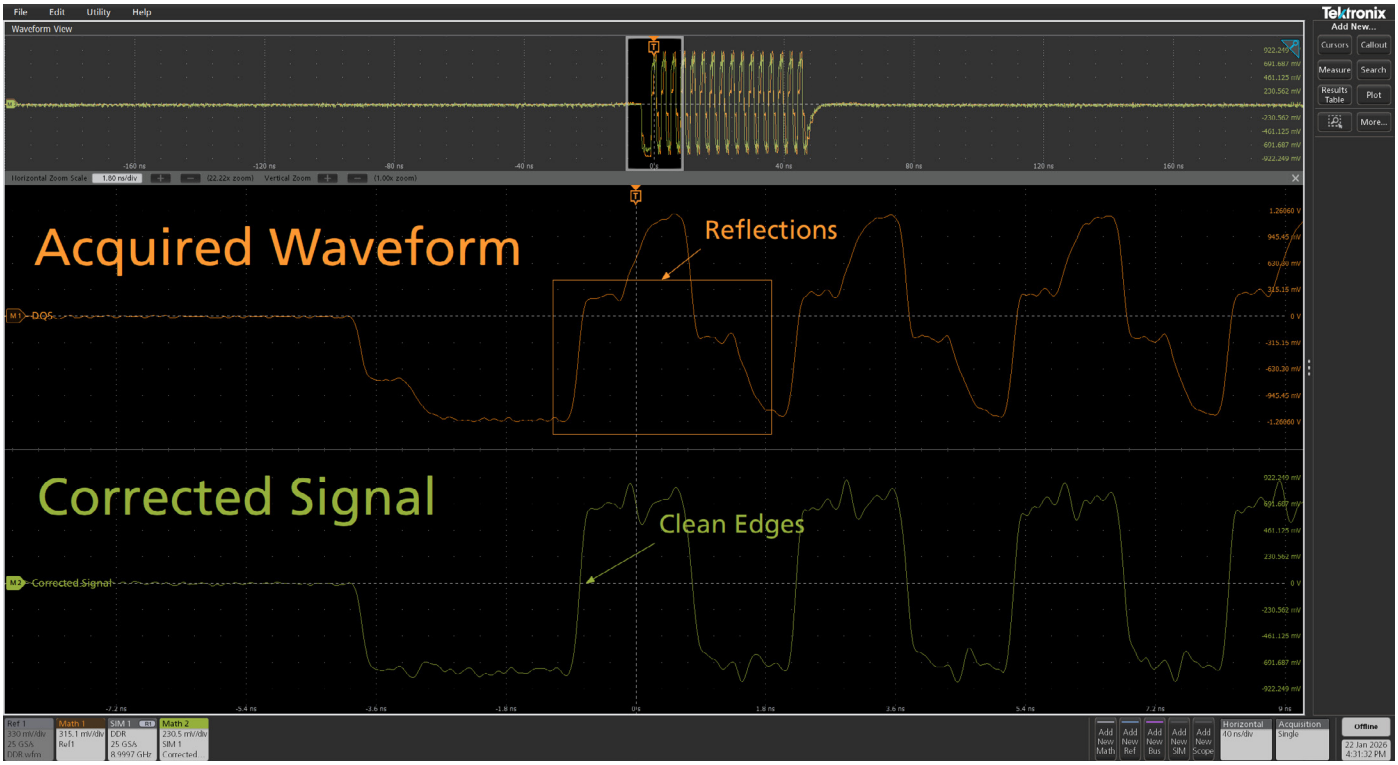


Figure 41. The corrected signal compared to the acquired signal, showing cleaner edges. To generate the corrected signal, the software derives an inverse transfer function of what the signal would look like at the virtual test point without the discontinuous effects of the components (Probe, PCB Trace, DRAM PKG) in the physical model.

Conclusion

High-speed serial validation demands accurate measurements and confident insight into true DUT behavior under real-world channel conditions. Tektronix oscilloscopes, combined with SIM and DJA software, deliver an integrated, on-oscilloscope workflow that lets you de-embed measurement effects, embed realistic channels, and apply Tx/Rx equalization without leaving the bench. The result is faster setup, fewer iterations, and clearer decisions from early design through final compliance. SIM's coherent multi-channel support extends these same de-embedding and equalization workflows to parallel lanes, enabling lane-to-lane margin assessment across multi-lane architectures without additional tooling. By integrating the full modeling workflow directly onto the oscilloscope, SIM eliminates the need for offline tools like MATLAB or Python scripts—keeping measured waveforms and modeled results in sync throughout the validation cycle.

For more information on how to accelerate your high-speed serial design and compliance testing today visit the Signal De-Embedding, Embedding, and Equalization and Jitter, Eye Diagram, and Timing Analysis pages.

Appendix A: S-parameter Fundamentals and Measurement Techniques

S-parameter Fundamentals

Scattering parameters (commonly known as S-parameters) are complex, frequency-dependent coefficients that describe how signals behave at network ports in a linear system. They enable engineers to describe how waveforms reflect and transmit power at each port. They can be used to quantify an incident wave that is reflected or transmitted when it encounters a component or interconnect.

Each S-parameter is a complex number representing both magnitude and phase, commonly expressed in linear+j, polar, and matrix forms.

- Magnitude: Represents the gain or loss (attenuation) in signal amplitude. It is often expressed in decibels (dB)
- Phase: Represents the phase shift or time delay experienced by the signal as it travels between ports or reflects back.

A S-parameter file representing a physical component in a circuit is commonly used to model complex systems, which means that the measurement and creation of S-parameters must be accurate representations of the components they model.

S-parameter Measurement Techniques

S-parameters are most commonly measured using a Vector Network Analyzer (VNA). A VNA is an electronic test instrument used by engineers to measure S-parameters of components and networks in the frequency domain. This is achieved by injecting a known test signal (a vector) into a device at a specified point and then measuring the magnitude and phase of the reflected and transmitted signals that result.

A VNA will perform a continuous sweep across a wide range of frequencies that are selected by the user and bounded by instrumentation hardware. At each frequency step point within the sweep range, the magnitude and phase of the reflected and transmitted waves are measured. A VNA uses this data to compute the S-parameters of the network. The raw data acquired is a set of complex numbers matched to frequency and represented as the S-parameter matrix. While this characterizes the network in the frequency domain, engineers often need to see the network response in the time domain.

The time domain is another useful view for analyzing the S-parameter data for correctness or troubleshoot problems that can occur. The Inverse Fast Fourier Transform (IFFT) can be used to make this conversion; however, several mathematical steps must be performed before the IFFT function can be applied.

1. Extrapolate the S-parameter from the start frequency of the selected sweep to DC. Since S-parameters are commonly obtained from a VNA measurement, the data set will not contain DC unless it was measured independently and added to the file.
2. Extrapolate or truncate to set the stop frequency to the Nyquist point at ½ the sample rate of the VNA.
3. Create the data set for frequencies from Nyquist to the sample rate by copying the complex conjugate of the data from the first point after DC to Nyquist in reverse order.
4. Compute the IFFT of the resulting S-parameter data. If this step is performed correctly, then the IFFT of the S-parameter data will result in time domain data that is real only, with the imaginary part equal to zero.

The IFFT conversion allows simulation of a Time Domain Reflectometry (TDR) or measurement. The resulting output can be used to create an Impedance plot along the transmission path, revealing the location and magnitude of discontinuities (like connectors, vias, and impedance mismatches) that cause reflections, or other systemic behavior.

A Time Domain Reflectometer (TDR) is an alternate tool that can be used to measure S-parameters directly in the time domain. Instead of sweeping across a frequency range, a TDR characterizes a network by launching a fast-rising voltage step or pulse into the transmission line as an incident waveform. The instrument then measures the voltage of the reflected wave against elapsed time. This reflected signal is a function of the change in impedance encountered by the incident as it travels. The TDR's core strength is its ability to provide an immediate, intuitive plot of impedance versus time (or equivalent distance). While the TDR directly yields the time-domain reflection coefficient (equivalent to S11), acquiring the full frequency-domain S-parameter data is an indirect process. This requires applying the Fast Fourier Transform (FFT) to the time-domain data. The accuracy and bandwidth of the

resulting frequency-domain S-parameters are critically dependent on the rise time of the TDR's stimulus pulse and the instrument's sampling rate, meaning a VNA is generally preferred for the most precise frequency-domain characterization, particularly for low-loss transmission measurements.

Instrument	Measured Domain	Strength	Weakness
Vector Network Analyzer (VNA)	Frequency	Direct S-parameter data acquisition. Multiport analysis	Time-domain analysis (TDR-like) is indirect (requires IFFT) and limited by the frequency span
Time Domain Reflectometer (TDR)	Time	Excellent for quickly locating shorts, opens, and impedance mismatches.	Frequency-domain analysis is indirect (requires FFT). Primarily a one-port tool for reflection measurements.

Table 1. Strengths and weakness of using TDR vs a VNA to measure S-parameters.

S-parameter Modeling Concepts

A basic two-port S-parameter model for a network is shown. Z_S is the source impedance of the generator that drives the network, and Z_L is the load impedance attached to the output of the network. The signals traveling into the ports are represented by a, and the signals travelling out of the ports are represented by b.

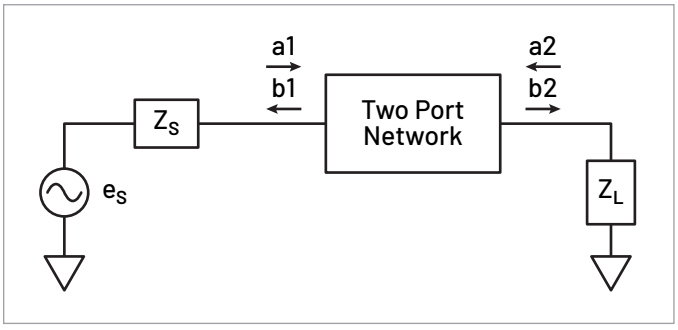


Figure 42. A two-port S-parameter model showing source impedance (ZS), load impedance (ZL), incident waves (a), and reflected waves (b).

a_1 is the incident signal traveling into port one of the network from the source. It is a sine wave signal having a specific frequency. b_1 is the reflected signal leaving port one and returning towards the source. b_1 is reflected towards the source due to an impedance mismatch when port two is terminated with $Z_L = Z_0$.

The value of Z_0 is the reference impedance used during the measurement process of the S-parameters; it is most commonly 50 Ohms.

Similarly, if port one is instead terminated with Z_0 and port two is driven by a generator, then a_2 becomes the incident into port two, and b_2 would be the reflected signal. When considering transmission through the network, a1 into port one may result in energy contribution to b_2 out of port two. The same can be true in reverse - a_2 into port two may result in contribution to b_1 out of port one.

Assume E_{a1} is a wave traveling into port 1, and E_{b1} is a reflection leaving port one. Likewise, assume E_{a2} is a wave traveling into port two and that E_{b2} is a reflected wave from port two. This system can be characterized as:

$$a_1 = \frac{E_{a1}}{\sqrt{Z_0}} \qquad a_2 = \frac{E_{a2}}{\sqrt{Z_0}} \qquad b_1 = \frac{E_{b1}}{\sqrt{Z_0}} \qquad b_2 = \frac{E_{b2}}{\sqrt{Z_0}}$$

The S-parameters relate to these four waves (a_1, b_1, a_2, b_2) in scattering matrix as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

Where the S-parameters are then defined as:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

- a_1 is zero when the input of port one is terminated with Z_0, and port two is driven with a test signal.
- a_2 is zero when the load impedance equals the reference impedance (Z_L=Z_0), and one is driven with a test signal.

These are the conditions of the network that are fulfilled when using a VNA or TDR measurement system to measure S-parameters. The S-parameters are each a vector of complex numbers that are a function of frequency. The values of S_{11} and S_{22} are called reflection coefficients, and S_{21} and S_{12} are called transmission coefficients.

Parameter	Name	Meaning	Interpretation	Example (Waveform)
S11	Input Reflection Coefficient	Portion of the wave incident at port 1 that is reflected back when port 2 is terminated in Z0	Measures input match of port 1 (return loss)	A sine wave enters port 1 → part reflects back toward the source
S22	Output Reflection Coefficient	Portion of the wave incident at port 2 that is reflected back when port 1 is terminated in Z0	Measures output match of port 2	A sine wave enters port 2 → part reflects back toward the source
S21	Forward Transmission Coefficient	Portion of the wave incident at port 1 that exits from port 2	Forward gain or insertion loss	A sine wave enters port 1 → appears at port 2 (possibly attenuated)
S12	Reverse Transmission Coefficient	Portion of the wave incident at port 2 that exits from port 1	Reverse isolation or reverse gain	A sine wave enters port 2 → appears at port 1 (usually small)

Table 2. Explanation of two-port S-parameters.

Mixed-Mode S-parameters

While standard S-parameters describe the behavior of single-ended ports, most high-speed interfaces utilize differential signaling to improve noise immunity. To analyze these systems, single-ended multi-port data (such as a 4-port measurement of a differential pair) is mathematically transformed into Mixed-Mode S-parameters. This transformation describes how signals behave in differential modes (the intended signal) and common mode (often associated with noise or EMI).

Differential and Common Mode Transformation

For a 4-port network representing a differential input and output, the ports are treated as pairs. The signals are no longer viewed as individual voltages at ports 1, 2, 3, and 4, but as composite waves:

- Differential Mode (Sdd): The difference between the signals on two conductors.
- Common Mode (Scc): The average of the signals on two conductors.

The resulting mixed-mode matrix allows engineers to quantify not only how a differential signal travels through the channel but also how it might inadvertently convert into a common-mode signal due to physical asymmetries.

Defining Mixed-Mode Parameters

Mixed-mode parameters use a four-character notation (e.g., Sdd21) where the first two subscripts indicate the mode (differential or common) and the last two indicate the port relationship

- Sdd (Differential-to-Differential): Describes how differential signals reflect (Sdd11) or transmit (Sdd21).
- Scc (Common-to-Common): Describes the behavior of common-mode noise within the system.
- Sdc and Scd (Mode Conversion): Quantify how much energy is converted from one mode to another (e.g., a differential signal becoming common-mode noise due to skew or imbalance).

Parameter	Decriptor	Meaning	Interpretation
Sdd21	Differential Insertion Loss	Portion of differential wave incident at the input that reaches the output.	Measures the primary signal bandwidth and attenuation of the channel.
Sdd11	Differential Return Loss	Portion of differential wave reflected back toward the source.	Assesses impedance matching and the impact of discontinuities like connectors.
Sdc21	Differential-to-Common Conversion	Portion of the differential signal that converts to common-mode.	Measures system imbalance; high conversion often leads to EMI issues.
Scc11	Common-Mode Reflection	Portion of common-mode noise reflected back at the input.	Useful for analyzing how noise or interference interacts with the network.

Table 3. Explanation of mixed-mode S-parameters.

Plotting and Evaluating S-parameters

Plotting S-parameters is a critical step in validating model quality before using them for de-embedding, embedding, or cascade operations. Visual inspection often reveals modeling errors, measurement artifacts, or configuration issues that may not be obvious from raw data alone.

Magnitude Plots

Magnitude plots are typically displayed in decibels (dB) and are used to evaluate:

- **Insertion Loss (e.g., S21)** – Indicates signal attenuation versus frequency. Excessive roll-off at high frequency directly impacts rise time and eye opening.
- **Return Loss (e.g., S11, S22)** – Indicates impedance matching. Poor return loss suggests reflections that may cause ringing or eye closure.
- **Isolation (e.g., S12)** – Indicates reverse transmission behavior.

A smooth, physically reasonable magnitude response is expected for passive interconnects. Unexpected gain in passive structures, abrupt discontinuities, or non-monotonic behavior at high frequency may indicate measurement noise or data corruption.

Phase and Group Delay

Phase plots reveal propagation characteristics and can indicate causality issues or excessive dispersion. For many interconnects, phase should decrease approximately linearly with frequency. Non-linear phase behavior may correspond to dispersion or measurement artifacts.

Group delay, provides insight into signal transit time through a circuit. Sudden discontinuities or oscillations in group delay can indicate poor S-parameter quality or insufficient frequency resolution.

Low-Frequency and DC Behavior

Accurate low-frequency behavior is essential for time-domain conversion. Because many S-parameter measurements do not include DC, extrapolation is required. Errors at low frequency—particularly magnitude or phase inconsistencies—can introduce tilt or distortion in the resulting step or impulse response.

When plotting near DC:

- Reflection coefficients should approach physically reasonable limits.
- Passive structures should not exhibit gain.
- Phase behavior should be continuous and stable.

Model Validation Before Cascading

Before using an S-parameter block in a cascade:

- Confirm consistent reference impedance across connected ports.
- Verify frequency range and spacing compatibility with other blocks.
- Check passivity and causality.
- Inspect magnitude and phase plots for physically realistic behavior.

Careful plotting and validation of S-parameters ensures stable, accurate simulation results and prevents error propagation when combining multiple blocks in a system-level model.

Cascading S-parameter Networks

The process of combining multiple 2-port networks, each described by its own S-parameter matrix, into a single equivalent representation, is known as a S-parameter Cascade. This allows for the modeling of signals passing through a chain of components in a transmission path. Cascading is important in describing complex networks in real systems with many elements.

Each component in a cascade can be represented as a 'block.' Each block is characterized by its own set of S-parameters, and each block can only interact with the greater network through its connecting ports. To observe the effect all components in series have on a traveling waveform, we must describe the contribution from each block of the cascade to a signal. To understand how these blocks interact and several of the issues involved, consider the following cascade.

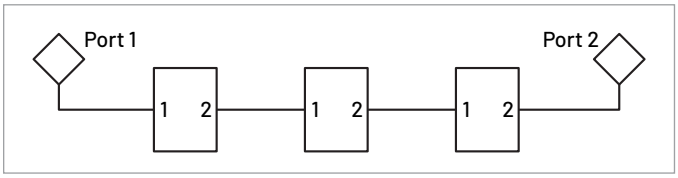


Figure 43. An S-parameter cascade where each component in the cascade is represented by a block characterized by it's own set of S-parameters. This allows for the modeling of signals passing through a chain of components in a transmission path.

The model in each block is represented by a set of 2-port S-parameters. In order to compute transfer functions for the system test points, it is necessary to combine several cascaded blocks into a single block.

These blocks may be converted to T-parameter matrices. Then they may be multiplied together to obtain a single T-parameter matrix, TT , for the total system. The TT matrix may then be converted back to an S-parameter set. In order to combine the matrix sets they must be consistent.

Note: SIM does not use T-parameters for cascading in order to avoid divide by zero issues that might arise. T-parameters are mentioned because they represent a more intuitive way to cascade by multiplying the matrices for each block together.

Some important considerations when evaluating a cascade:

- Frequency spacing must be the same, thus time interval represented must be the same.
- Start and stop frequencies must be the same.
- Reference impedance must be the same for any two ports connected together.
- The final combined matrix will cover the same time interval of each block matrix. Thus if the system delay of the cascaded blocks is greater than the time interval covered by the individual block S-parameters then aliasing will occur.
- In the time domain the aliasing results in pulse response features occurring in the wrong time position and they may be reversed in time order. This is the result of phase aliasing in the frequency domain where there are less than 2 samples per revolution

The resulting S-parameter models the entire system, capturing the combined reflections, transmission behavior, and interactions of all blocks in the cascade. This final description now represents the entire cascaded system as if it were a single 2-port network.

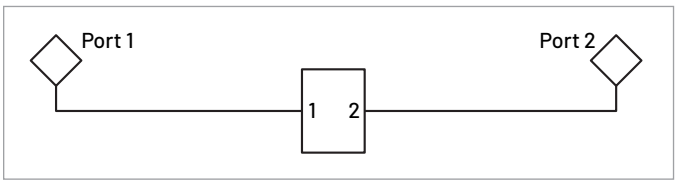


Figure 44: A single 2-port network representation of a cascaded system

Time-Domain Considerations and Modeling Risks

Managing Time Delay, Aliasing

A crucial consideration when cascading channel elements is the total delay of the system. If the combined system delay exceeds the time interval covered by the S-parameter data, a phenomenon called aliasing or time domain wrapping occurs. This shifts features of the impulse response to incorrect time positions. SIM automatically manages this risk by intelligently resampling the S-parameter data to ensure the time window is sufficiently large to contain the full impulse response, preserving causality and accuracy.

Filter Causality

For time-domain analysis, SIM applies filters (such as for bandwidth limiting) in the frequency domain. To prevent signal distortion (specifically, non-linear phase distortion which causes eye diagram tilting), the software often utilizes linear phase symmetrical filters. While mathematically non-causal, these filters are necessary to achieve clean bandwidth limiting without introducing unwanted phase noise, which is critical for accurate Eye Diagram measurements.

S-parameter Quality and Extrapolation Risks

The accuracy of S-parameter files, particularly at low frequencies, is paramount. SIM uses data extrapolation to extend the S-parameters down to 0 Hz (DC). Even seemingly minor errors—such as a magnitude error or a phase error—in this extrapolated DC point can be highly detrimental. These small errors in the frequency domain translate to significant tilt and large errors in the final computed time-domain step or pulse response, corrupting the overall simulation accuracy. Proper S-parameter measurement is therefore critical.

High-Speed Measurement and Simulation Techniques

In the domain of high-speed engineering, obtaining representative data for a device under test can be complicated by the effects of the measurement setup or the intended operating environment. To move beyond the limitations of physical measurement boundaries, engineers employ two crucial mathematical techniques based on S-parameters: de-embedding and embedding. These processes allow us to either surgically remove unwanted effects from a measurement or predict performance when circuit characteristics change into a complex simulated system.

The capabilities to de-embed and embed are critical in high-speed design because measurement path artifacts often dominate test results. There are many measurement challenges where an engineer might employ de-embedding and embedding techniques.

Measurement Path Artifacts Dominate: At high data rates, passive elements (cables, probes, fixtures) introduce loss and delay that can overshadow the Device Under Test's (DUT) true behavior, leading to inaccurate results.

Physical Access is Limited: De-embedding virtually moves the measurement reference plane to the DUT pin using S-parameter models, recovering the signal at the precise location of interest despite physical constraints.

Compliance Requires Accuracy: Standards specify signal behavior at the transmitter/receiver pins. De-embedding corrects for the measurement setup, mitigating the risk of failing compliance due to system errors rather than DUT design flaws.

Design Exploration with Embedding: Embedding allows engineers to test the DUT with different interconnect models (cables, backplanes) without building new hardware. This validates system margins across various use cases and avoids costly hardware re-spins.

De-Embedding

When modeling high frequency signaling networks, signals are often impacted by connectors, PCB traces, adaptors, or connected test equipment. These components can introduce reflections, phase shifts, and losses. De-Embedding is the process of removing the effects of unwanted components from the signal of interest.

De-embedding can be achieved through the use of measured S-parameters. Components in the network characterized by a S-parameter can be mathematically removed from the measurement. This allows for a new description of how the waveform would behave without the removed component present in the signal path.

Mathematically, de-embedding treats the measurement system as a cascade of two networks. Each of the following elements is first characterized by its own S-parameter description.

- F = fixture or undesired network (probes, connectors, PCB traces, etc.)
- DUT = device under test
- M = measured response of fixture + DUT

In two-port form:

$$M = F \circ DUT$$

Cascading two-port networks is simplest in T-parameters (chain matrices), where:

$$T_M = T_F \cdot T_{DUT}$$

To isolate the DUT, the fixture's effect is inverted and removed:

$$T_{DUT} = T_F^{-1} \cdot T_M$$

Once computed, the DUT matrix is converted back to S-parameters:

$$S_{DUT} = f(T_{DUT})$$

This yields S-parameters representing only the DUT's intrinsic behavior, free from fixture-induced reflections, loss, and phase distortion.

One of the most common use cases for the De-Embedding procedure is to remove the loading effects of test equipment (such as a probe, cables, connectors, etc) that has been attached to a circuit of interest – such that the acquired data is representative of the system without the additional test equipment in place. De-embedded data is essential for precise modeling, simulation, and design verification, particularly in high-frequency applications where even small parasitic effects can significantly impact performance.

Embedding

Engineers often need to predict the impact of integrating a device into a larger system containing specific connectors, PCB traces, adaptors, or surrounding circuitry. These components will introduce their own reflections, phase

shifts, and losses. Embedding, the reverse of de-embedding, is the process of mathematically adding the simulated or desired effects of these networks to the performance data of a device.

Embedding can be achieved through the use of S-parameters. Components that are characterized by an S-parameter can be mathematically cascaded such that the measurement made includes these additional characteristics. A new waveform with the effects of the embedded components can be used as a basis for measurement.

Embedding uses the same network cascade mathematics as de-embedding, but applies it in the forward direction. Given:

- D = S-parameters of the DUT
- E = S-parameters of the environment to embed (connectors, traces, packaging, etc.)
- R = resulting embedded network

Convert each S-parameter matrix to a T-parameter matrix:

$$T_D = f(S_D),\ T_E = f(S_E)$$

Embedding is accomplished by cascading the environment with the DUT:

$$T_R = T_E \cdot T_D$$

Then convert the cascaded result back to S-parameters:

$$S_R = f(T_R)$$

The resulting S-parameters represent how the DUT behaves when placed inside the embedded environment, including the added reflections, phase delay, loss, and frequency-dependent effects of the added structures.

Some of the most common use cases for the Embedding procedure is to virtually move a component into a modeled environment (such as a different variant of connector, different losses from PCB material, differing designs, etc.) — such that the acquired data is representative of what the system's performance would be with these changes in place without physically modifying physical assembly – or to virtually move where the signal access (probe) point is located, to acquire waveform data throughout various test points within the system. Embedded data is essential for system-level performance prediction, "what-if" analysis, and early design validation, particularly in high-frequency applications.

Emulating Tx and Rx Equalization

As data rates continue to climb, the physical interconnect (PCB traces, cables, and connectors) introduces high channel losses, severely attenuating and hampering high-frequency signal fidelity. This frequency-dependent loss leads to the spreading of pulses, a phenomenon known as Intersymbol Interference (ISI). ISI causes bit boundaries to become corrupted, resulting in a closed or highly distorted eye diagram and an unacceptable Bit Error Rate (BER).

Equalization is a critical technique used at the receiver (Rx) and/or transmitter (Tx) to compensate for channel loss and restore signal integrity. These techniques selectively boost the high-frequency components of the signal, thereby opening the eye and improving BER. The choice of equalization techniques depends on the severity of channel loss, power budget, and acceptable latency. Modern high-speed receivers often use a hybrid approach to maximize performance:

Continuous Time Linear Equalization (CTLE)

Continuous Time Linear Equalization (CTLE) is the simplest and often the first stage of equalization in a receiver. CTLE functions as an analog, tunable high-pass filter that provides frequency-dependent peaking to counteract the channel's low-pass loss. It actively boosts the high-frequency content (the signal edges) relative to the DC content, effectively compensating for the frequency-dependent loss. The CTLE's compensation level is typically configured to achieve the best results, either by using specific presets defined by the applicable standard, or by the engineer selecting a specific boost or peaking level to match the channel loss.

Feed Forward Equalizer (FFE)

The Feed Forward Equalizer (FFE) is a linear digital filter typically implemented using a tapped delay line. It can be used both at the Transmitter (as a pre-emphasis or de-emphasis filter) and the Receiver.

An N-tap FFE consists of:

- Taps: Digital samples of the incoming signal delayed by one unit interval (UI) per tap.
- Coefficients: Each tap is multiplied by a weighted coefficient (Cn).
- Summation: The resulting weighted signals are summed to produce the output.

The coefficients are adjusted to inject energy before (pre-cursor taps) and subtract energy after (post-cursor taps) the main data bit, effectively canceling ISI. This is a linear process, meaning the output is a linear combination of the weighted input samples.

Decision Feedback Equalizer (DFE)

The Decision Feedback Equalizer (DFE) is a non-linear digital filter designed specifically to cancel post-cursor ISI (ISI caused by the current bit affecting subsequent bits).

The DFE is split into two sections:

- Feed-Forward Section (FF): Often includes a short FFE or CTLE stage to handle pre-cursor ISI and general high-frequency boost.
- Feedback Section (FB): This is the core non-linear element. It takes the previously decided data bits and feeds them back through weighted taps. Since the decisions are (ideally) correct, this section subtracts the known post-cursor ISI component from the incoming analog signal before the final decision is made.

Technique	Primary Function	Best Application Scenario
CTLE	Initial high-frequency gain and wide-band compensation.	Channels with low-to-moderate loss where power is a major constraint.
FFE	Precise, linear cancellation of both pre-cursor and post-cursor ISI.	Use at the TX (pre-emphasis) to compensate for predictable channel loss, or at the RX where linear noise amplification is tolerable.
DFE	Non-linear cancellation of only post-cursor ISI.	High-loss channels where SNR improvement is critical. Always used in conjunction with a linear element (CTLE/FFE) to handle pre-cursor ISI.

Table 4. Summary of CTLE, FFE, and DFE.

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Rev. 02.2022

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