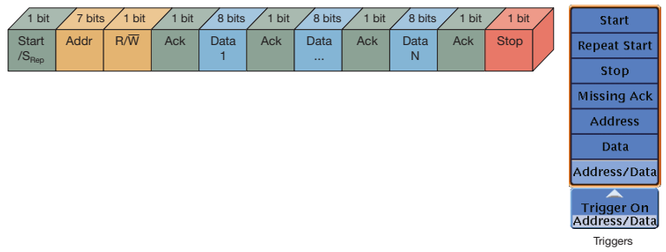
Debugging Low-Speed Serial Buses in Embedded System Design

All low-speed serial buses were developed to communicate data between digital devices with minimum wiring, optimum speed, low cost, and maximum integrity. Serial buses are becoming more and more successful because they effectively and economically solve data communications problems both between chips on the same circuit board and between “black-boxes” distributed around a vehicle.

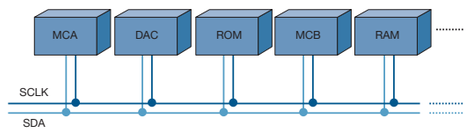
I²C (Inter-IC bus)

The I²C (Inter-IC bus), developed in the early 1980s by Philips, has become a worldwide standard for communications between integrated circuits in a system. The simple 2-wire design has found its way into a wide variety of chips like I/O, A/Ds, D/As, temperature sensors, and microprocessors. Any I²C device can be attached to the bus allowing any master device to exchange information with a slave device. I²C also saves cost and reduces the overall space.

With the Serial Triggering and Analysis Module option (DPO4EMBD), packets are decoded automatically for you, eliminating manually counting bits and saving you valuable time.

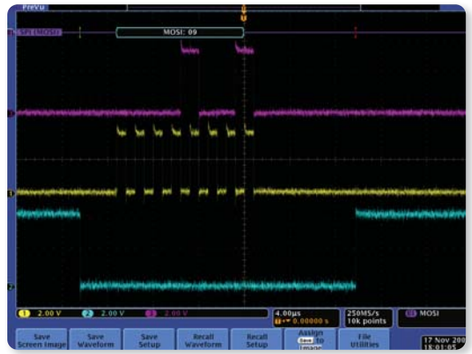


Data transfer on the I²C bus.



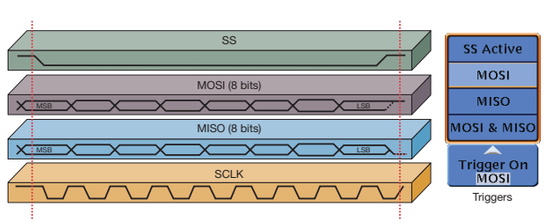
Example of an I²C bus configuration using two microcontrollers.

SPI (Serial Peripheral Interface)

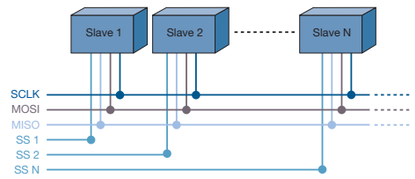


The SPI (Serial Peripheral Interface) bus is a 4-wire interface used primarily in synchronous serial communication for both processors and peripherals. SPI uses a synchronous clock which shifts serial data into and out of the microcontroller in blocks of 8 bits. SPI bus is a master/slave interface. The master drives the serial clock. When using SPI, data is simultaneously transmitted and received, making it a full-duplexed protocol.

The Serial Triggering and Analysis Module (option DPO4EMBD) bridges the gap between software and hardware design triggering and decoding on SPI traffic showing your code execute in hardware, while at the same time, hardware engineers can see the analog packet detail.



Single master, multiple slave SPI implementation. The single master drives data out its SCLK and MOSI pins to the SCK and MOSI pins of the slaves.

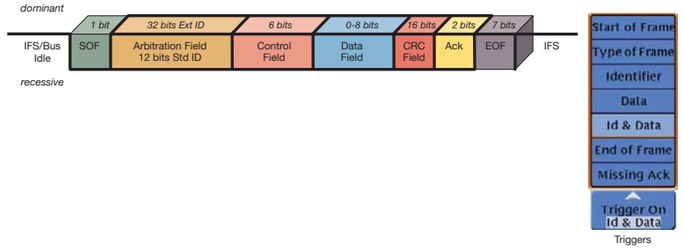


Data transfer on the SPI bus with CPHA=0. When an SPI data transfer occurs, an 8-bit data word is shifted out of MOSI, while a different 8-bit data word is being shifted in on MISO.

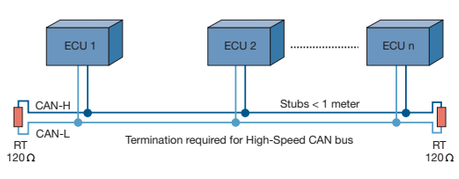
CAN (Controller Area Network)

The CAN (Controller Area Network) bus is a layered serial data communication protocol developed in the 1980s by Bosch GmbH, specifically to control and communicate with electronic devices in electrically noisy environments. In 1992, Mercedes-Benz became the first automobile manufacturer in 1992 to employ CAN in their automotive systems. Today, the CAN domain continues to expand into other systems (marine, industrial, medical, aerospace, and more) that require electrical noise tolerance, reduced wires, error checking, and high-speed transfer rates (up to 1 Mbps @ 40 M).

Use the Search and Mark capability to quickly mark and decode packet into Hex for analysis.



The CAN Data Frame fields. Transmission is asynchronous and controlled by start and stop bits at the beginning and end of each character in a binary format: Logic 0 represents dominant bits and logic 1 recessive bits.



CAN High-Speed Signal Network.

DPO4000 Series

Serial buses pose some significant challenges. It’s harder to isolate events and difficult to interpret what is displayed on the screen. Manually decoding is time-consuming and error-prone. The DPO4000 Series—with bandwidth ranging from 350 MHz to 1 GHz and a minimum of 5x oversampling—captures and accurately displays even the fastest transient events. The standard 10 M record length on all channels enables you to capture long windows of signal activity while maintaining fine timing resolution.

With the DPO4000 Series’ powerful trigger, decode, and search capabilities, design engineers can solve embedded system design issues with exceptional efficiency.

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