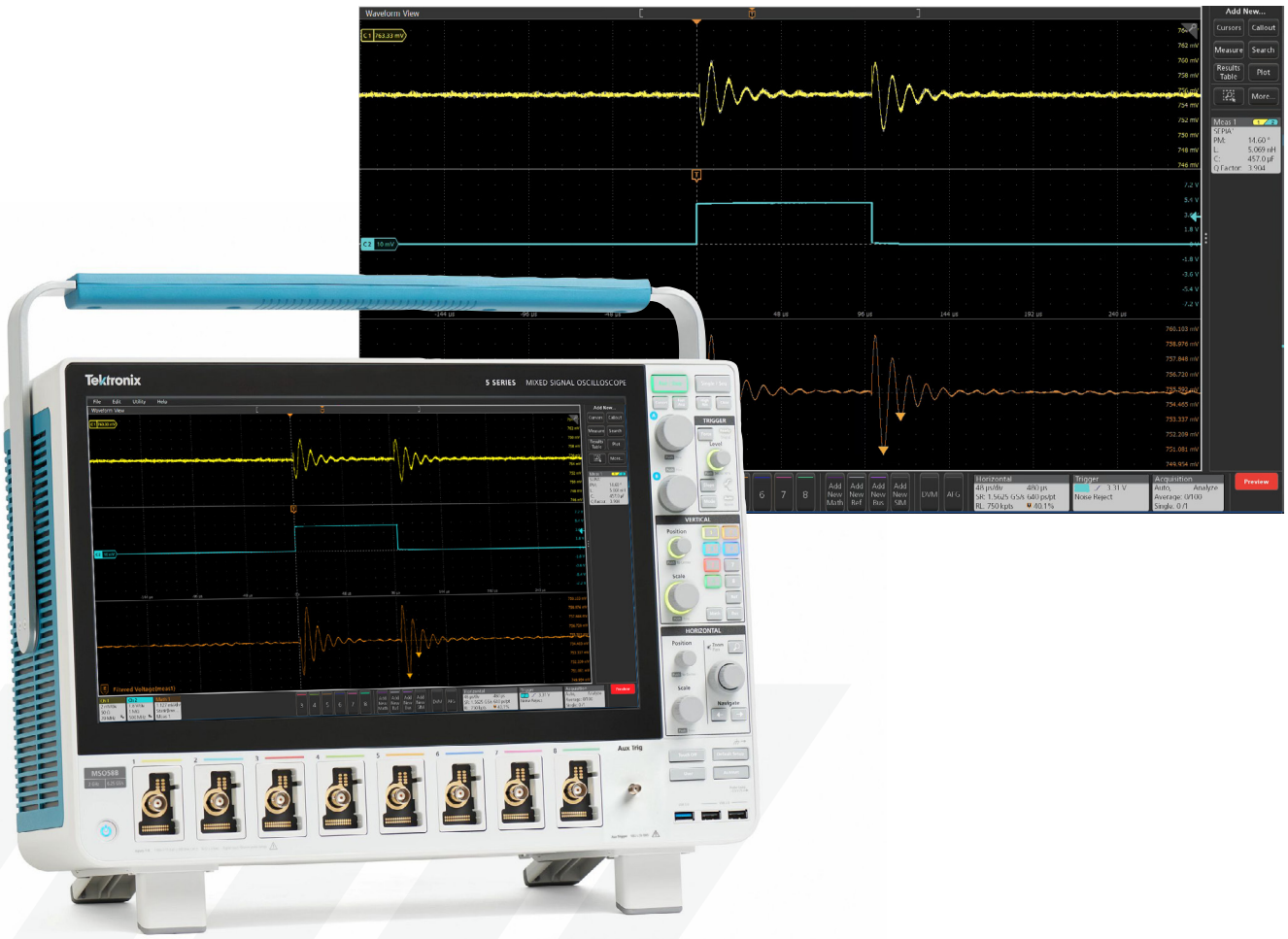
Tektronix®

Using Step Load Response to Evaluate VRM Stability

Scope Embedded Power Integrity Analysis (SEPIA)

APPLICATION NOTE



Introduction

Bode plots have long been the traditional method for determining the stability of power converters. However, integrated voltage regulator modules (VRMs) with no loop injection points and multiple internal loops have made the use of this analytical tool impractical in many cases.

Unlike Bode plot analysis, the Scope Embedded Power Integrity Analysis (SEPIA) technique, developed by Picotest, enables evaluation of loop stability without breaking into the control loop. SEPIA, which has also been called Stability Evaluation for Power Integrity Analysis, relies on the fact that if the loop is stable or unstable one can tell from how the output voltage rings in the time domain in response to a step change in the load current. Since the step load response is part of the power distribution network (PDN) designers' normal workflow, SEPIA measurements are a natural extension.

The measurement is integrated into 4 Series B, 5 Series B and 6 Series B MSOs equipped with Power Distribution Network Analysis Software (Options 4-PDN, 5-PDN and 6-PDN, respectively) [1]. The SEPIA measurements can be invoked directly from the front panel Measure control, enabling the user to capture the rail's response to a fast load step and derive the loop's effective Q factor and equivalent phase margin—without cutting traces or inserting injection resistors. One can also extract an equivalent RLC circuit to help with modeling.

This application note

- Describes the challenges driving this new approach to evaluating the stability of power distribution networks using traditional methods.
- Explains the theoretical basis for SEPIA, and how it works.
- Illustrates the test setup.
- Explains how to perform the analysis.

SEPIA was developed by Picotest and is integrated into Tektronix 4, 5 and 6 Series B MSO oscilloscopes equipped with optional Power Distribution Network (PDN) analysis software.

Measurements in this application note were made on a 5 Series B MSO equipped with Option 5-PDN. Although the measurements are shown on a 5 Series B, they operate practically identically on the 4 and 6 Series B MSOs when they are equipped with options 4-PDN or 6-PDN, respectively.

Challenges in Evaluating State-of-the-Art PDNs and VRMs

The traditional approach to evaluating power converter stability is to:

- Break the control loop and insert a small resistor into the feedback path of the loop
- Use an injection transformer to couple a perturbing signal into the loop
- Sweep a small AC signal with a vector network analyzer (VNA) or oscilloscope (**Figure 1**) and read gain and phase margin from a Bode plot

This approach is invasive and can be difficult or impossible to set up. However, it is effective when it is possible and small signal behavior is of interest.

Bode plot stability analysis of VRM control systems assumes that the system is linear and time-invariant (LTI). However, these assumptions may not be applicable to today's power converters [2]. For regulators that feed GPUs, FPGAs and AI accelerators today, several factors make the use of Bode plots impractical or inappropriate:

- Multiphase controllers have nonlinear responses
- The behaviors of rail currents in amps or hundreds of amps are not accurately reflected in small injected signals
- Many VRMs and converters do not provide loop access
- Wideband frequency sweeps take time and may cause heat and stress issues

The Bode plot can be difficult or impossible to set up and it should not be applied to non-LTI control systems; however, it is effective when it is possible and small signal behavior is of interest. Broader PDN stability can be evaluated by using 2-port shunt-through impedance measurements and studying the impedance of the PDN over frequency. This analysis does not require access to the control loop of the PDN, but it is performed using relatively small, swept signals. So, it shares some of the same limitations as Bode plot analysis.

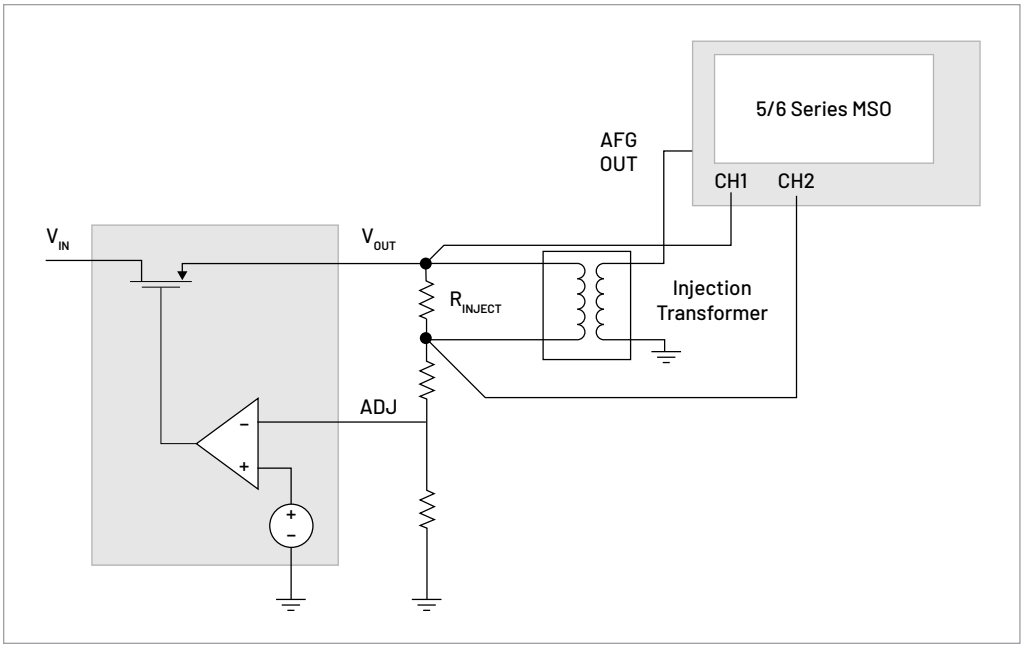


Figure 1. Bode plot analysis relies on an injection point in the control loop of the VRM. If these nodes are internal to a VRM, probing and signal injection are impossible.

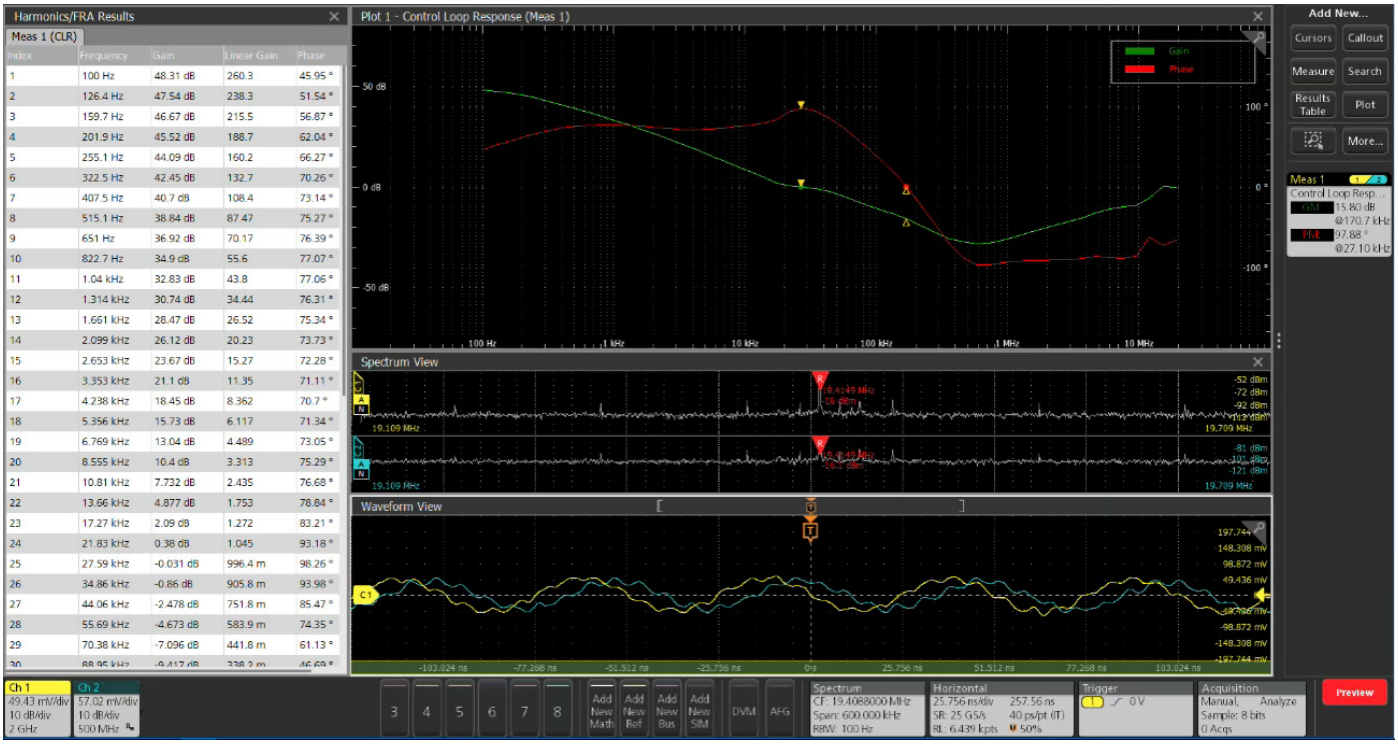


Figure 2. Bode plot analysis provides phase margin and gain margin measurements [4].

While Bode plots and 2-port impedance measurements are traditionally performed using vector network analyzers, these measurements can also be performed using Tektronix oscilloscopes with function generators, signal injectors, PDN Analysis or Advanced Power Analysis software [4]. This measurement is shown in **Figure 2**.

Time domain testing, in contrast, is relatively simple: one applies a realistic current step at the regulator's output and measures the results (**Figure 3**). The relationships between time domain and frequency domain measurements are well-established [5]. But even though step load testing has

been standard practice, it was impossible to go from the qualitative observations of ringing behavior to quantitative figures of merit — SEPIA analysis provides this bridge.

While SEPIA is not intended to replace swept measurement techniques such as the Bode plot and 2-port shunt-through impedance, it fills the gap where these measurements are impossible or inaccurate.

SEPIA Measurement Theory

SEPIA is a time-domain analysis technique, developed by Steve Sandler of Picotest [3], for assessing VRM, power converter or PDN stability without requiring direct loop access or a frequency sweep.

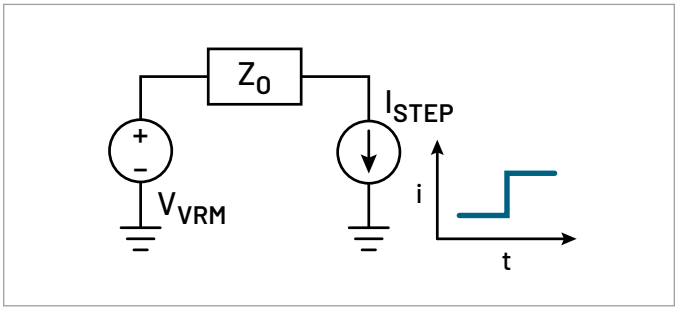
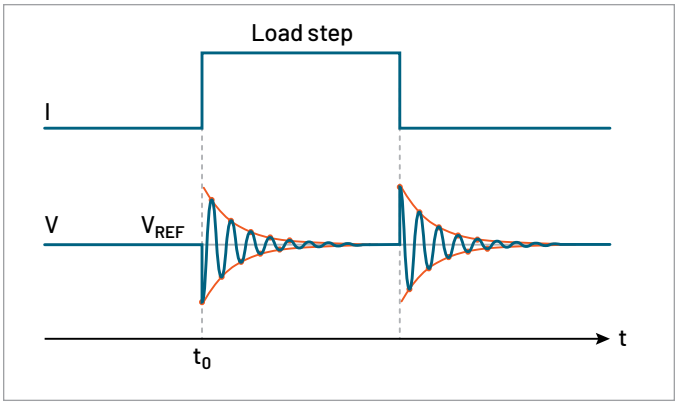


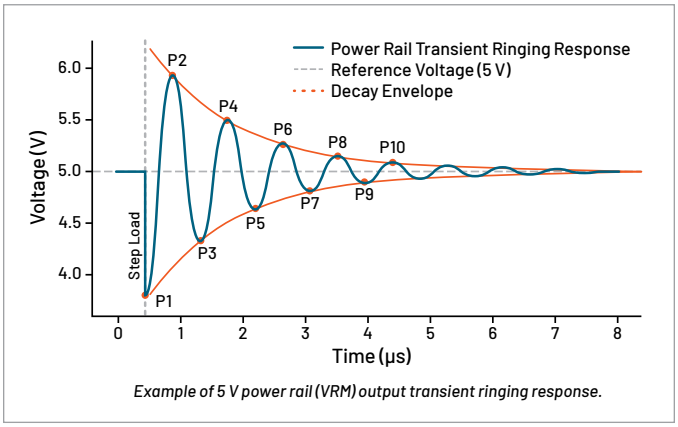
Figure 3. Applying a step load to the output of the VRM enables one to gain an understanding of its output impedance and that of the surrounding PDN. [5]

At a high level, the SEPIA measurement involves:

- Subjecting a VRM or power system to a step change in load current and capturing the resulting output voltage waveform, that is, the transient response. (Note that SEPIA can also be applied in simulations [6].)
- Processing and measuring the ringing on the time domain waveform
- Calculating quality factor (Q) of the dominant resonance, and an equivalent phase margin inferred from the resonance shape and peak location relative to crossover.

The step load is useful to evaluate the large signal, non-linear, and time-variant aspects of the transient response with regards to the PDN voltage limits. Around its dominant resonance, an underdamped loop behaves like a second order system that produces a ringing waveform, like the simple example shown in **Figure 4**. The decay rate and number of peaks can be represented by the quality factor, Q. Thus, for a given response waveform the Q may be determined and used to calculate an equivalent phase margin.





Figures 4a and 4b. SEPIA uses the response of a voltage regulator to a step load to indicate the stability of the regulator and surrounding downstream PDN. The rate of decay detailed in Figure 4b is measured to derive Q.

Core Assumptions

The SEPIA analysis built into the PDN Analysis package relies on several assumptions:

- The closed-loop power converter does not have to be linear, but it should exhibit second order ringing in response to a load step.
- Although the Picotest SEPIA analysis can be applied to overdamped responses, the current implementation in Tektronix oscilloscopes requires an underdamped response with at least two discernible ringing cycles.
- The step load has a rise- or fall-time faster than 35% of maximum measurement bandwidth or at least five times faster than the DUT control loop bandwidth [6].
- The off-time must be long enough for the ringing to settle until the voltage response is flat (< 5° slope). A good rule of thumb is to set off-time greater than 5 times the ring period.

The algorithm uses the real and imaginary terms to determine stability margin. The stability margin is then mapped to a 2nd order system response. The ringing will always correspond with stability margin which is a better metric than phase margin and gain margin.

Some specific topologies, SEPIC for example, have a 5th order step response, not 2nd order. Even so, the SEPIA algorithm will correctly align with stability margin. When the response is fitted to a 2nd order response, the equivalent phase margin accurately represents stability. Note that even though the equivalent phase margin is an accurate indicator of stability, it will be different from the phase margin observed on a small signal Bode plot. In these cases, SEPIA is a better indication of quantitative stability.

We can use this model to determine the quality factor and equivalent phase margin of the voltage regulator [6].

Mathematical Basis for SEPIA

Given these assumptions and conditions, the transient ringing envelope can be modeled as:

$$v(t) = Ae^{-\zeta\omega_n t}\sin(\omega_d t + \phi) \quad \text{Equation 1}$$

where the damped natural frequency, $\omega_d = \omega_n\sqrt{1-\zeta^2}$

The algorithm analyzes the filtered voltage waveform produced in response to a step load and identifies successive ringing peak amplitudes (positive or absolute-value peaks) p_1, p_2, p_3, ...

The logarithmic decrement represents the drop between the amplitude of the first two peaks (Equation 2) and then the damping ratio (Equation 3):

$$\delta = ln\left(\frac{|p_1|}{|p_2|}\right) \quad \text{Equation 2}$$

$$\zeta = \frac{\delta}{\sqrt{(2\pi)^2 + \delta^2}} \quad \text{Equation 3}$$

This enables one to find quality factor, which is an output of the SEPIA analysis:

$$Q = \frac{1}{2\zeta} \quad \text{Equation 4}$$

Measuring the ringing period T_d between peaks provides the damped natural frequency:

$$\omega_d = \frac{2\pi}{T_d} \quad \text{Equation 5}$$

Then the natural frequency:

$$\omega_n = \frac{\omega_d}{\sqrt{1-\zeta^2}} \quad \text{Equation 6}$$

An equivalent phase margin is calculated from the damping ratio, ζ, or quality factor, Q, using a linear second-order approximation derived from control-loop theory.

The SEPIA analysis performs a least-squares parameter fit to obtain an equivalent RLC model that represents the measured ringing frequency, damping, and change in steady-state impedance associated with the load step. The damping resistance may be represented using either a series-loss model or a parallel-damping model.

Equivalent RLC Models and Resistance Extraction

For both models, the characteristic impedance of the equivalent LC network is defined as:

$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{Equation 7}$$

where: L is the equivalent inductance
C is the equivalent capacitance
Z_0 is the characteristic impedance

Series-Loss Model

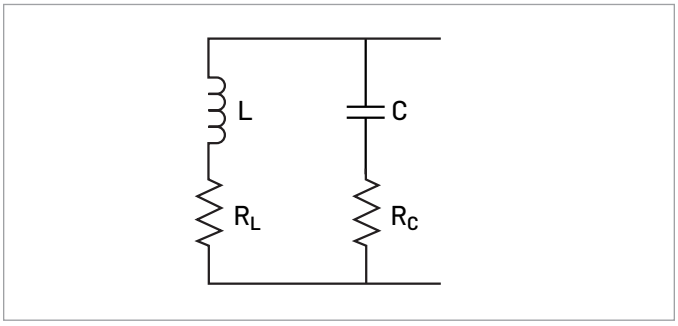


Figure 5. A circuit model representing the output impedance of a VRM with resistors in series with reactive components.

The model in **Figure 5** represents the resistive losses in series with the reactive components. The total series resistance is calculated from the fitted *L*, *C*, and *Q* values:

$$R_{SERIES} = \frac{Z_0}{Q}$$ Equation 8

The total series resistance consists of two components:

$$R_{SERIES} = R_L + R_C$$ Equation 9

In the steady-state regions before and after the load step, the capacitor carries no DC current and its branch behaves as an open circuit. The measured steady-state voltage change associated with the current step is therefore used to estimate R_L:

$$R_L = \frac{\Delta V_{SS}}{\Delta I}$$ Equation 10

where ΔV_{SS} is the change in steady-state output voltage and ΔI is the applied current step.

After R_L is determined, the remaining series resistance is assigned to R_C:

$$R_C = R_{SERIES} - R_L$$ Equation 11

Parallel-Damping Model

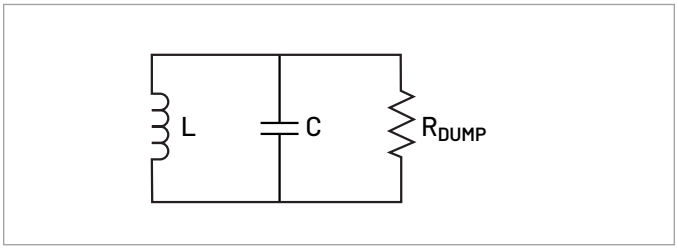


Figure 6. A circuit model that assigns resistance in parallel with reactive components.

Figure 6 shows an alternative equivalent model in which the damping resistance is placed in parallel with the reactive components. For this model, the equivalent parallel damping resistance is:

$$R_{DUMP} = Z_0 Q$$ Equation 12

In the parallel-damping representation, the fitted damping is represented by a single resistance. Therefore, separate R_L and R_C values cannot be extracted from this model.

Relationship Between the Models

Both representations can model the same fitted second-order dynamic response. The extracted *L* and *C* values are identical for the two models, while the equivalent resistance changes according to whether the damping is represented in series or in parallel with the reactive network.

In the current release of SEPIA analysis on Tektronix oscilloscopes, the series resistance model shown in **Figure 5** is available as a net list for impedance simulations. Net list output will be described in more detail toward the end of this application note.

How to Make the Measurement

The Measurement Setup

To make the measurement, a high-speed step-load must be applied to the output of the VRM. **Figure 7** shows a typical setup. This requires a pulse loading device such as the browser probe-based Picotest S50 or P2105A S10 Load Steppers. Picotest also offers other Load Stepper products. These devices are designed to apply a fast-switching load very close to the node under test, thus reducing parasitic capacitance and inductance associated with benchtop electronic loads. The Picotest load steppers require an external pulse generator to switch in the load.

To measure the response, a voltage probe must be connected to the output of the VRM, in parallel with the load stepper (**Figure 8**). For the best stability assessment, the response should be monitored at, or close to, the voltage regulator sense point of the VRM.

Since the SEPIA measurement observes the voltage response in detail, it is critical to select an appropriate voltage probe. The goal is to minimize ringing introduced by the probe. Ideal probing systems will have 50 Ω input impedance, short tip and isolation. A power rail probe or isolated current probe are effective options. A power rail probe, like the Tektronix TPR1000/TPR4000, with high bandwidth, low noise and DC offset range is a good choice. The TPR's ±60 V offset capability is useful for low noise power rail measurements up to 60 V, but its single-ended nature will introduce ground bounce errors in measurement results. To prevent this a ground loop isolator such as the Picotest J2115A is recommended. Picotest offers 50 Ω cables and browsers (P2104A or P2105A) that can be used to connect to the DUT. This configuration was used to make the measurements in this application note.

Tektronix IsoVu Isolated Current Probes can also be used as differential power rail probes. These probes are galvanically isolated from the scope inputs, so ground loop errors are eliminated. These probes are superior for core voltage measurements below 1.2 V but the TICP's advantage over the TPR power rail probes diminishes at higher rail voltages. This is due to the TICP's lower offset range and the need to use attenuating tips which raise the noise floor in proportion to the increased tip attenuation. The Picotest P2104A and P2105A browser probes are also compatible with the TICP system.

Although the actual measurement is made using the output voltage, the current step signal plays a critical role as a trigger signal. A high bandwidth current probe, such as a current shunt probe, a Rogowski probe, or AC/DC clamp-on probe can be used to capture the current step, depending upon the constraints of the DUT. This may not be feasible in all cases. While it can be useful to see the digitized current step waveform, a pulse signal concurrent with the step may be substituted for an actual current probe to simplify the setup and reduce parasitics. The pulse amplitude and scale factors on the scope can be set to mimic the current step. For example, a 5 V pulse from an AFG, with 1 V/A scaling on the scope will mimic a 5 A step load. This will be illustrated in the case below.

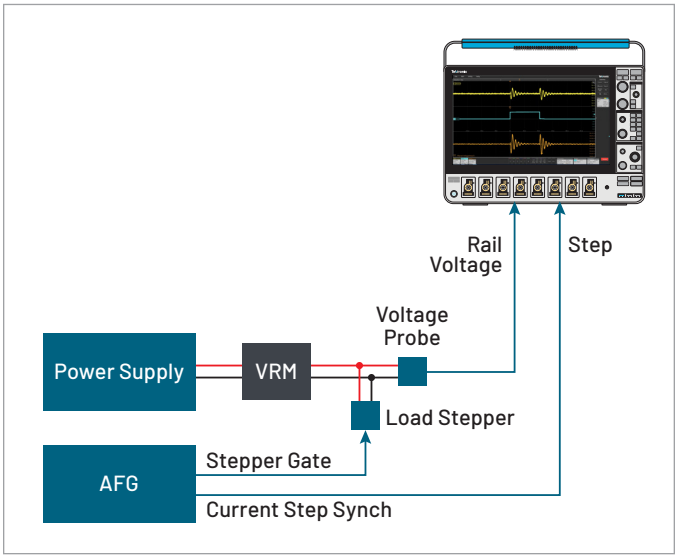


Figure 7. A typical setup for making SEPIA measurements. The measurement requires the application of a fast step load and voltage measurement close to the node being studied. Instead of using a current probe, a synch signal in phase with the load stepper drive signal may also be used to trigger the measurement.

In the measurements that follow, the DUT is a Picotest evaluation board including a Monolithic Power Systems MPQ2286. The MPQ2286 is a high-frequency, 6 V maximum input, 12 A maximum output programmable synchronous buck regulator with integrated MOSFETs and digital interface. This VRM is extremely flexible and control loop parameters can be programmed using the manufacturer's configuration software. This programmability enables designers to build highly stable PDNs. For this application note, **the loop is intentionally detuned to produce ringing to demonstrate SEPIA analysis.**

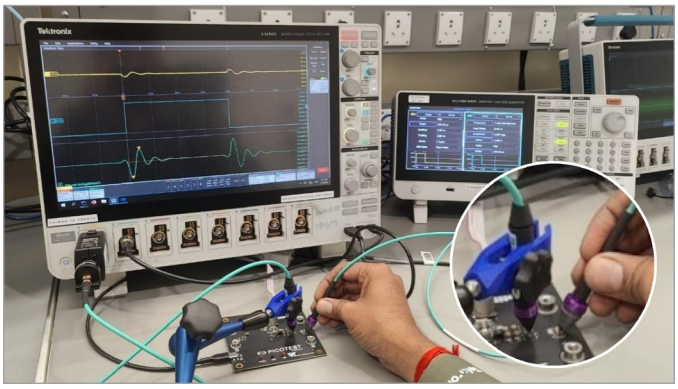


Figure 8. A test setup for performing SEPIA analysis. A TPR4000 Power Rail Probe is connected to the VRM output through a Picotest J2115A Probe Coaxial Isolator and P2105A 1-Port 50 Ω Browser probe.

In addition to the DUT, the following instruments and probes were used to create the measurements:

- 5 Series B MSO Oscilloscope equipped with Option 5-PDN Power Distribution Network Measurement and Stability Analysis was used to acquire signals and make measurements
- Instead of a traditional differential probe, a low-noise power rail probe system was used. A Picotest ground isolator was used to prevent ground currents.
  - Browser: Picotest P2105A 1-Port 50 Ohm Voltage Browser Probe
  - Isolation: Picotest J2115A Probe Coaxial Isolator to isolate the DUT ground from earth
  - Probe: Tektronix TPR4000 Power Rail Probe measures DC to 4 GHz with low noise contribution
- Picotest P2105A (S10 Version) 1 Ω load (customizable) stepper was used to generate the step load
- AFG31000 Arbitrary/Function Generator delivers turn-on pulses to the load stepper and provides a 5 V pulse, concurrent with the gate signal, to emulate a 5 A step through a 1 Ω load
- Linear bench power supply to provide a 5 V DC input to the DUT
- Picotest VRM test board, described above

The measurements were made with no load on the DUT and as noted above, the DUT was intentionally tuned to produce an "interesting" step response.

The Measurement Procedure

The measurements are included in the optional Power Distribution Network Measurement and Stability Analysis (PDN) measurements on the oscilloscope.

Preparing for the Measurement

The SEPIA measurement is added from the Add Measurements dialog, as shown in **Figure 9**.

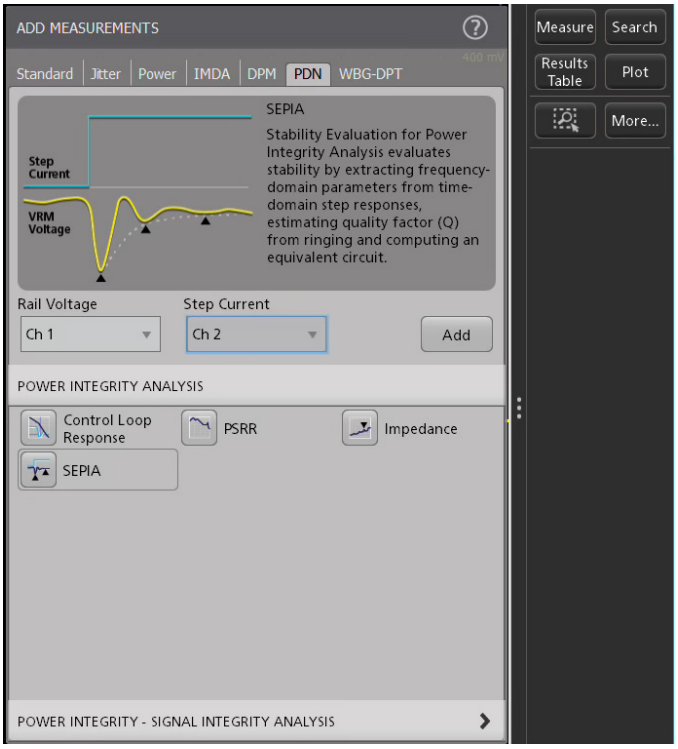


Figure 9. The SEPIA measurement is activated from the PDN tab.

Double-clicking on the SEPIA measurement badge opens the setup window shown in **Figure 10**. The settings for this example are:

- Rail Voltage is set to 0.75 V. This is used by the PDN Preset to set scaling for the main voltage signal.
- Step Current is set to 5 A. This is used by the PDN Preset to establish a trigger point and set the vertical scale for the current signal. In this example, this is not an actual current measurement. It is a scaled (1 V/A), phase-aligned TTL trigger signal from the function generator.
- Max Step Duration is set to 100 µs. This is used by PDN Preset to set the horizontal scale. In this example it is the width of the load on-time as determined by the function generator.

To ensure good measurements it is important to provide a step load pulse such that the SEPIA ringing is completely captured and the power rail output voltage settles to a final value.

The voltage channel should be properly scaled to view the power rail ripple. For many power measurements it is common practice to use a 20 MHz bandwidth limit on the scope's input channel in order to constrain noise to a predictable bandwidth. This example has the 20 MHz bandwidth limit activated.

The ringing may be buried in noise, and using waveform averaging on the scope can average multiple acquisitions to remove ripple and noise from waveforms. In this example, 100 waveforms are averaged to reduce switching ripple and random noise. Note that while waveform averaging will clean up noise, it will also average out any actual time variance in the response. Real-time sampled measurements, without averaging, will capture any time variance. Quantifying this variation can be helpful, and real-time sampling is ideal. However, in this example, switching noise amplitude is very close to the voltage response amplitude, so averaging is used to reduce the switching noise.

Capturing the Acquisitions and Making the SEPIA Measurements

After the initial configuration, the scope was ready to acquire the step response from the DUT. As noted above, the scope was placed in average mode and set for 100 waveform averages. A single acquisition may be used, but applying waveform averaging reduces random noise. Since the step is asynchronous with respect to the VRM switching, averaging removes the switching ripple. (As noted above, it also averages out any time variance, which is not recommended unless noise levels demand it.) The value used in this case (100) pulls the voltage response out of the switching noise without significantly impacting test time. The scope was put in normal trigger mode and the trigger pulse was generated from the AFG31000. The scope triggers on the load step as shown in **Figure 11**. Ringing observed in the step region of the signal on Channel 1 indicates the step response of the VRM. The display was zoomed in to completely show the ringing on the signal.

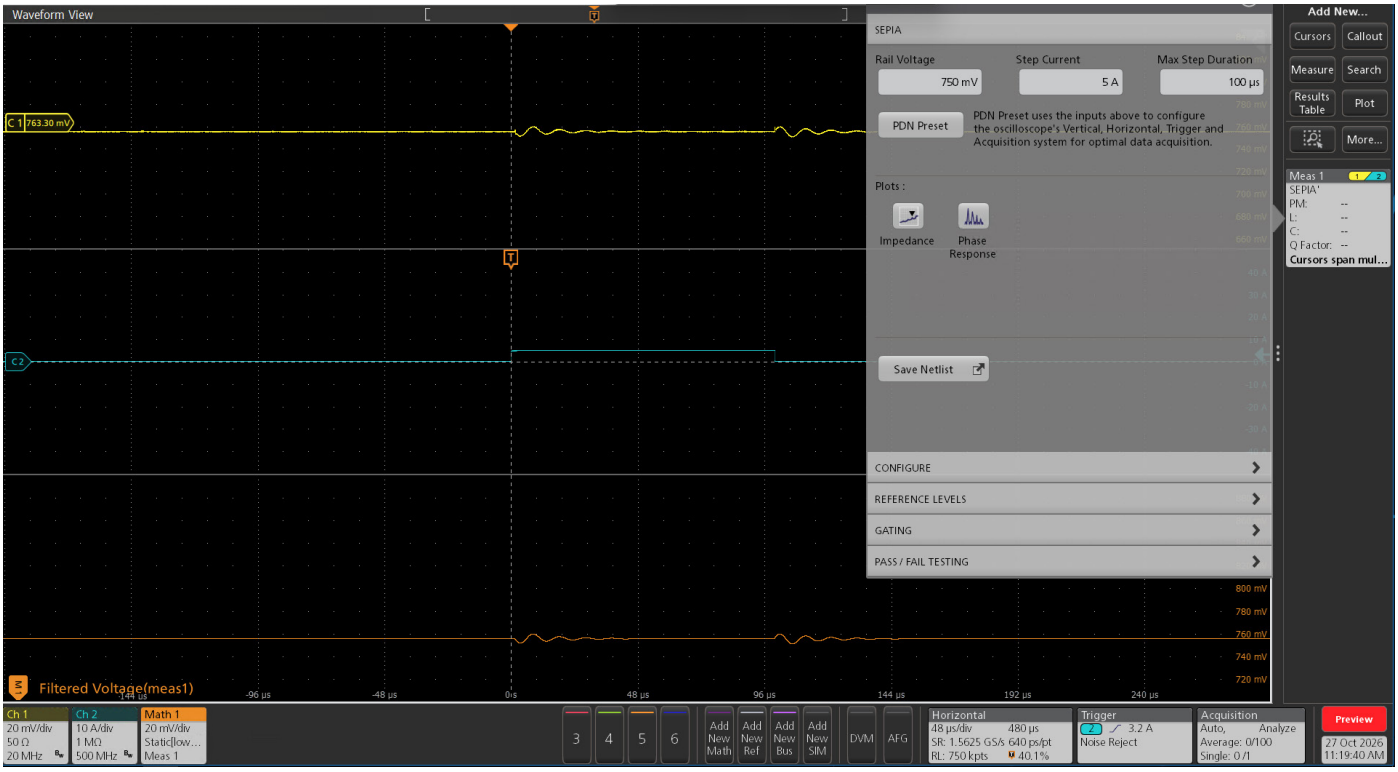


Figure 10. The SEPIA setup window gives variables used by the PDN Preset function to set vertical and horizontal scales, as well as establishing a trigger.

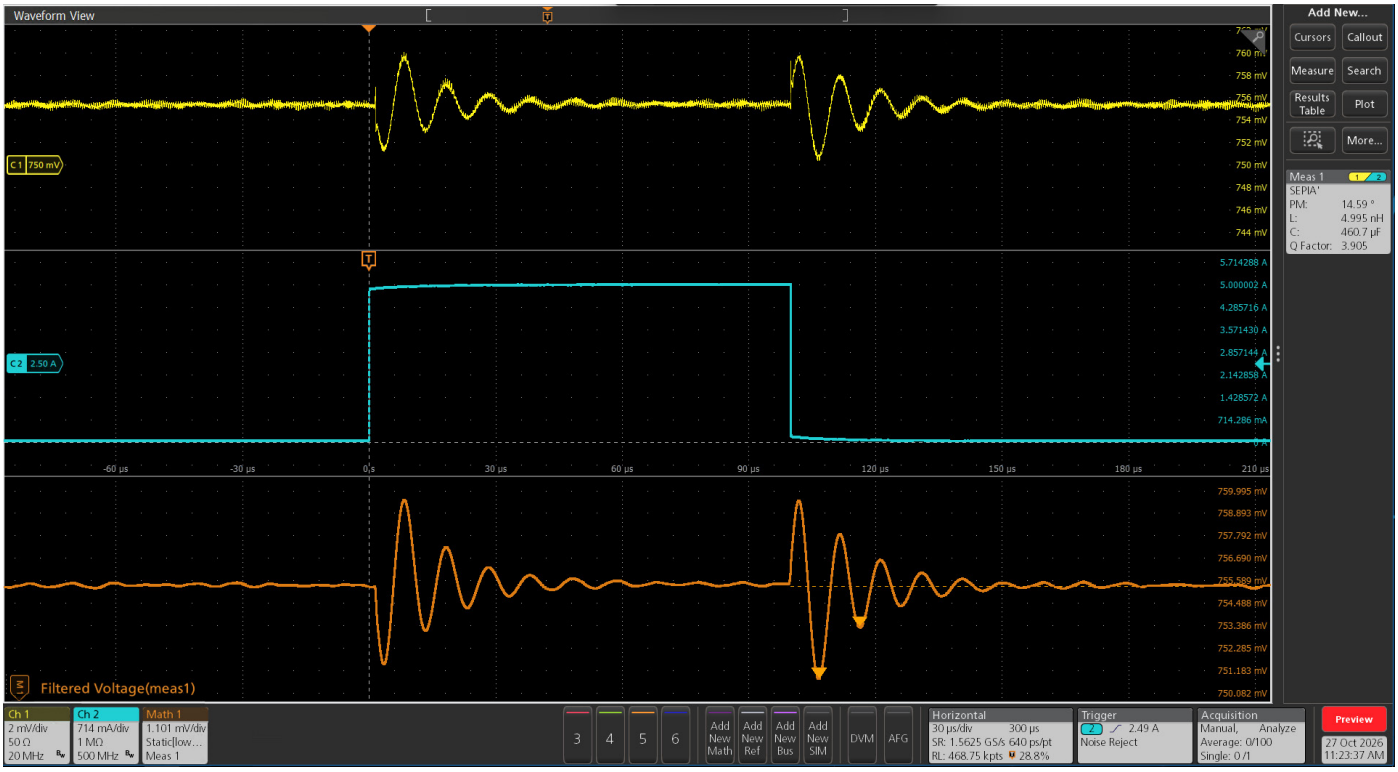


Figure 11. The timing signal on Channel 2 (cyan) shows the timing of the load step. Scaling is applied on the oscilloscope input to display the signal in amps. The voltage response on Channel 1 (yellow) is conditioned on the Math 1 waveform (orange).



Figure 12. The same capture as the previous figure, zoomed in to show ringing at the trailing edge of the load step. The configuration settings for the SEPIA analysis are shown and the resulting filtered voltage waveform is shown as Math 1. Note that the VRM has been intentionally detuned for this example.

The Configure window, shown in **Figure 12**, includes settings for channel assignments, filter specifications and reference voltage. As explained in the measurement theory above, the algorithm identifies the 2nd order ringing from the voltage response. The voltage signal is filtered to remove high-frequency noise and isolate valid peaks and valleys. The algorithm uses the steady state voltage as a reference.

In Auto mode, the measurement algorithm determines the reference voltage used to find peaks and valleys. Higher order effects, if present, are removed in DSP, and a voltage histogram is used to set the reference. In Custom mode, the user defines the steady state reference voltage.

Note that if the decay ratio between consecutive same-polarity peaks is not constant — if Vpk3/Vpk2 is not equal to Vpk2/Vpk1 – the response has multiple modes and the response is not 2nd order. Beat patterns (amplitude growing and shrinking) or varying peak spacing also indicate non-2nd-order behavior. In these cases, Custom mode may be used to manually select two peaks from the same oscillation mode, with the understanding that results represent an approximation of a single resonance. Even in Custom mode, the current algorithm requires at least one pair of edges within the ringing.

In this example, Custom mode is used. The settled power rail voltage on Channel 1 was measured using cursors to be 755.3 mV, and the Reference Voltage was set to this value.

The Voltage Filter order (1st Order through 3rd Order) determines how fast the FIR filter rolls off. (Note that specifying a very low cutoff frequency may eliminate the ringing altogether. It is better to start with a higher value and work down.) The filtered signal is shown in Math1 in **Figures 11** and **12**.

Finally, the cursors were placed at two valleys, and the the SEPIA analysis measurement is performed between those points. The results are shown in the Meas 1 measurement badge in **Figure 12**.

In typical power-distribution applications, lower Q values are generally associated with higher damping and greater stability margin. The phase margin in this example measures around 14° with a Q factor of 3.9. This indicates that the system has poor stability and needs attention. This result is expected since the VRM has been purposely tuned poorly for demonstration purposes.

```
* Tektronix
* SEPIA PDN SPICE netlist
* Measurement: Meas 1
* Phase Margin: 1.45958468e+01 deg
* Quality Factor: 3.90370820e+00
*
* ===== AC Impedance Testbench =====
* 1 A AC current injected at VOUT.
* V(VOUT) = PDN impedance |Z(f)| in ohms.
* Plot V(VOUT) after simulation to view impedance and phase.
* Open in HSPICE/PSpice; plot V(vout) vs frequency from the .ac0/.dat output.
I1  0    VOUT  AC 1
X1  VOUT 0     PDN_SEPIA
.ac dec 200 1 1G
*
* ===== Auto-measure PDN parameters =====
.meas AC RL_lowF    FIND V(vout) AT=1
.meas AC Rcap_highF FIND V(vout) AT=1G
*
* ===== PDN subcircuit =====
.SUBCKT PDN_SEPIA VOUT GND
* Inductive branch (RL1 + L)
L1  VOUT N1   5.06942162e-09
RL1 N1   GND  2.44745565e-05
* Capacitive branch (Rcap + C)
C1  VOUT N2   4.56979689e-04
RC1 N2   GND  8.28730480e-04
.ENDS PDN_SEPIA
.end
```

Figure 13. An example net list for an RLC equivalent circuit based on a SEPIA analysis. The PDN Analysis software can automatically produce this file, which can be directly loaded into SPICE simulators to run AC (impedance and phase) analysis.

The measurement also outputs L and C values which are equivalent circuit parameters when the circuit is viewed as a simple RLC circuit. The PDN analysis software in the oscilloscope can generate a net list file, such as the one shown in **Figure 13**. The Save Netlist button, shown in **Figure 10**, is used to generate this file. This net list can be imported into SPICE to perform AC impedance and phase analysis of the RLC circuit produced by the SEPIA analysis.

It is also possible to add phase response and impedance plots versus frequency for reference, as shown in **Figure 14**. The displayed plots are a simulated response across frequencies based on the RLC circuit parameters extracted from the step response. They are not measured frequency response curves.

The C and L values determined by SEPIA analysis may also be used to simulate transient response. This is outside the scope of this application note, but Reference 6 gives excellent examples of using QSPICE to simulate transient response.

Variations in Measurements

Some variation across runs may be due to the normal operation of the DUT. As noted above, VRM response is often time-variant. For example, part of the transient response depends on the energy stored in VRM output inductors. This energy is proportional to I^2 and the current ramps during the switching cycle. Thus, both the current and energy vary over time, and the response depends on the state of the system at the instant the step is applied. SEPIA will track these responses, delivering measurements corresponding to each point.

However, measurement system effects may also contribute to variations. To eliminate measurement system effects, switch from Auto mode to Custom mode. Custom mode is recommended for noisy waveforms, in the case of an unsettled reference voltage, and when there are multiple resonances in the response waveform. In these cases, use manual peak detection by selecting Custom mode.

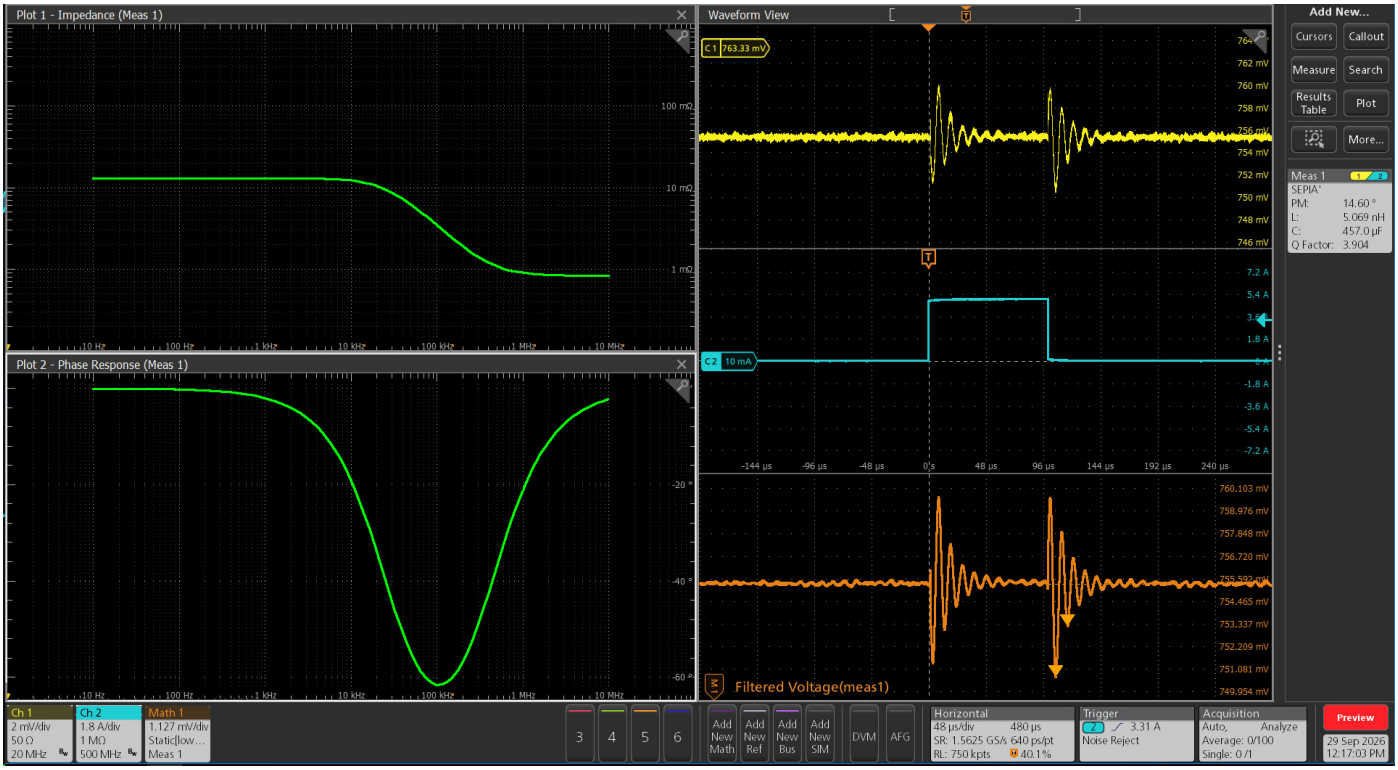


Figure 14. Phase versus frequency and impedance versus frequency plots can be displayed. These are not measured response curves but are modeled based on the second order circuit defined by the RLC values.

Adjusting the low-pass filter parameters for a faster rolloff and lower cutoff frequency will reduce noise in the math waveform. As in the example above, waveform averaging may be used to reduce switching noise and random noise, as well as time variance.

Conclusion

SEPIA extends conventional step-load testing by turning time-domain ringing into practical stability metrics for modern VRMs and PDNs. It provides an alternative to small-signal, swept sine Bode plot analysis which may be impossible due to lack of loop access and risk of thermal overstress during frequency sweeps. By using a fast load step, an oscilloscope, and Power Distribution Network analysis software, one can determine a Q factor, phase margin, and RLC parameters to quantify step response without loop injection or frequency sweeps. Lower phase margin is associated with more ringing and longer settling time and is an indication of system instability. This knowledge enables designers to identify instability and adjust compensation, output capacitance or other control loop parameters.

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