

# Tektronix and FS2 Answer Debug Challenges for Xilinx FPGAs



## Real-Time Logic Debug of Xilinx FPGAs

The FS2 FPGAView software, when used with a Tektronix TLA Series logic analyzer, provides a complete solution for debugging your Xilinx FPGA and surrounding hardware. This combination enables you to gain complete visibility and allows you to:

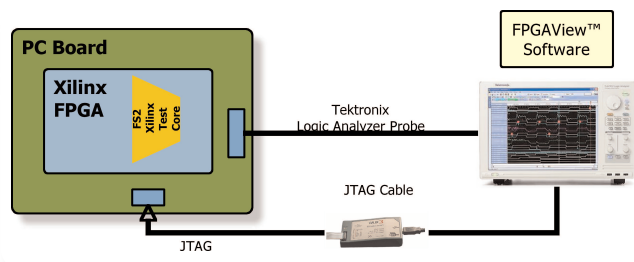
- View internal activity and external activity
- Quickly change your probe points without recompiling your design
- Monitor multiple internal signals per pin

## Debug Your Xilinx® FPGA Design At Full Speed

Advances in design tools and electronic design automation (EDA) software allow design teams to tackle more complex designs while maintaining, or shrinking, the required design time.

With gate counts over 1 million, effective design tools, and time-to-market advantages, FPGAs are used in many of today's systems to implement much of the functionality. Advances in design tools allow designs to be done at higher levels of abstraction, synthesize complex designs quicker, and complete place and route cycles in less time. As FPGA designs grow in sophistication and complexity, similar advances need to occur in debugging FPGAs. To keep pace with the increased debug needs of FPGAs, new tools are needed to optimize real-time FPGA debug.

The First Silicon Solutions (FS2®) FPGAView™ software is a PC Windows-based program designed for use with Tektronix® TLA Series Logic Analyzers to enable real-time debugging of Xilinx FPGAs. Using FPGAView, design engineers can quickly and easily measure signals inside their Xilinx FPGA design and select different internal signals to probe without having to recompile their design. FPGAView also simplifies logic analyzer use by automatically updating channel names with the internal signal names selected.



Solutions	
Multiplexer	FS2 Xilinx TestCore
Control Software	FS2 FPGAView™
Logic Analyzer	Tektronix TLA Series Logic Analyzer, running v4.3 or later
JTAG Cable	Xilinx Platform Cable USB

## FS2 FPGAView Simplifies Xilinx FPGA Debug

Step 1. Configure and insert the appropriate test core into your design

- Use FS2 On-Chip-Instrument Generator (OCIGEN) to define and insert FS2 Xilinx Test Core
- Specify number of debug pins
- Specify number of banks
- Specify mode
- Specify clock
- Power-up mode

Step 2. Configure FPGAView for your debug environment

- Specify JTAG interface
- Specify TLA interface

Step 3. Establish the mapping of FPGA pins to TLA logic analyzer channels

- Use FPGAView to “connect” FPGA pins to logic analyzer
- Enables automatic channel name updating with simple drag & drop operation
- Supports multiple LAIs / FPGAs / TLA modules

Step 4. Make your measurement

- Use Bank pull-down list to select Bank to measure, then FPGAView sets up LAI via JTAG and programs the TLA with the proper signal names
- Easily switch internal probe points by selecting a different Bank, thus eliminating the need to recompile your design
- Correlate FPGA signals with other signals in your system

## Supported Xilinx® Quartus® II FPGA Families

- Virtex,
- Virtex2,
- Virtex4,
- Spartan,
- Spartan3,
- Spartan3E

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Our most up-to-date product information is available at: [www.tektronix.com](http://www.tektronix.com)



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