Suggested Clocking Modes for Acquiring Flash and DRAM Memories with a TLA Series Logic Analyzer

James Mauck
Tektronix, Inc.
Beaverton, Oregon, USA

I. Introduction

An analysis of ST Microelectronics' M58WR064EB Flash memory and Micron Technology's MT48H4M16LF Synchronous DRAM shows that a fairly fast sampling speed will be required to capture all the signals of interest with adequate resolution. The obvious drawback to sampling at higher speeds is that it dramatically shortens the acquisition time window.

The best approach to use when the desire for larger acquisition time windows conflicts with the need for higher resolution is to acquire the data transitionally. This form of logic analyzer clocking samples the data at high speed (500MHz for the TLA) and stores data only when it detects that one of the signals has changed. This clocking mode provides high resolution without wasting acquisition memory by storing static signal states.

To obtain the maximum acquisition time window three capabilities must be present in the logic analyzer. The first is having a separate timestamp memory. Next is being able to mask signals from causing storage. And finally is a transition detector that is fast enough to look at single samples.

II. Timestamping Stored Data

Timestamping (or time tagging) memory is required when storing data only when signal transitions occur. In order to recreate an accurate waveform display the logic analyzer must know exactly how far apart two adjacent stored samples are in time. If one change causes us to store a data sample, and then after 100 analyzer clocks the next change is stored, we have no method of knowing how many analyzer clocks occurred between the two samples. This is the role of the timestamp data. It tells us how far apart the samples are so that the waveform display can be scaled correctly.

However, simply having the ability to timestamp data isn't enough. Some logic analyzers use a portion of the data storage memory to store timestamps. If ½ of the available data storage memory is consumed by timestamp data it can be difficult to obtain a significant increase in the acquisition time window since you start out with an immediate 50% reduction.

III. Masking Signal Transitions from Causing Storage

In some applications storing the state changes on some signals doesn't add any significant value. An example is the address and data busses of SDRAMs when we are interested in data flow to and from the devices. The points of interest usually occur when signals such as Chip Select, RAS, CAS, and Write Enable occur. Being able to mask signals from storage allows us to limit data storage to when those particular signals change. Figures 1 and 2 provide examples for how to mask signals for the two devices mentioned at the beginning of this brief.

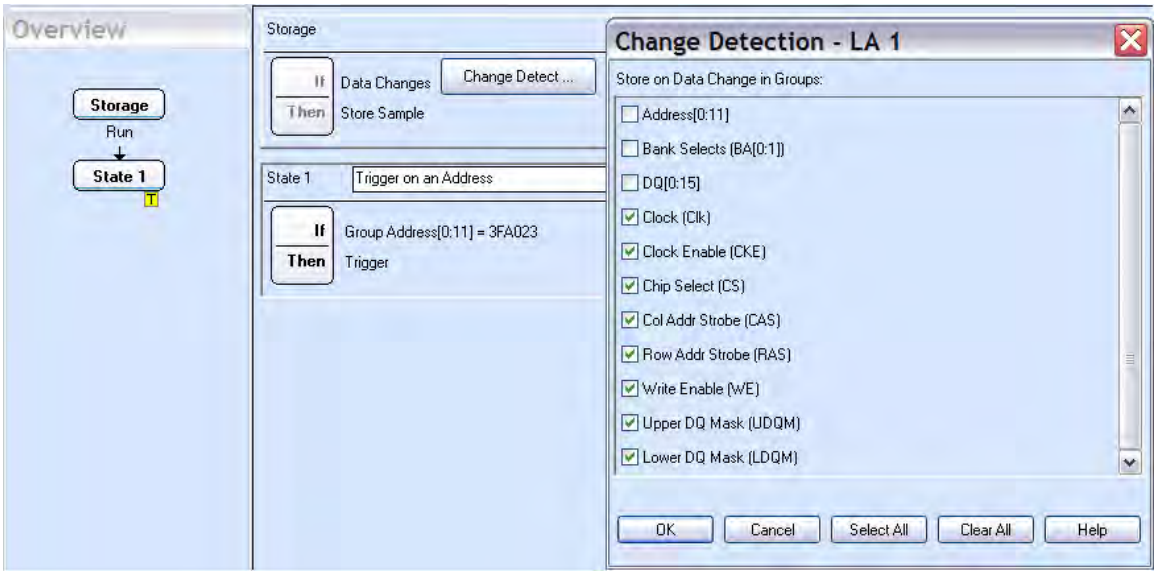

Figure 1. Transitional masking of signals for Micron's MT48H4M16LF Synchronous DRAM

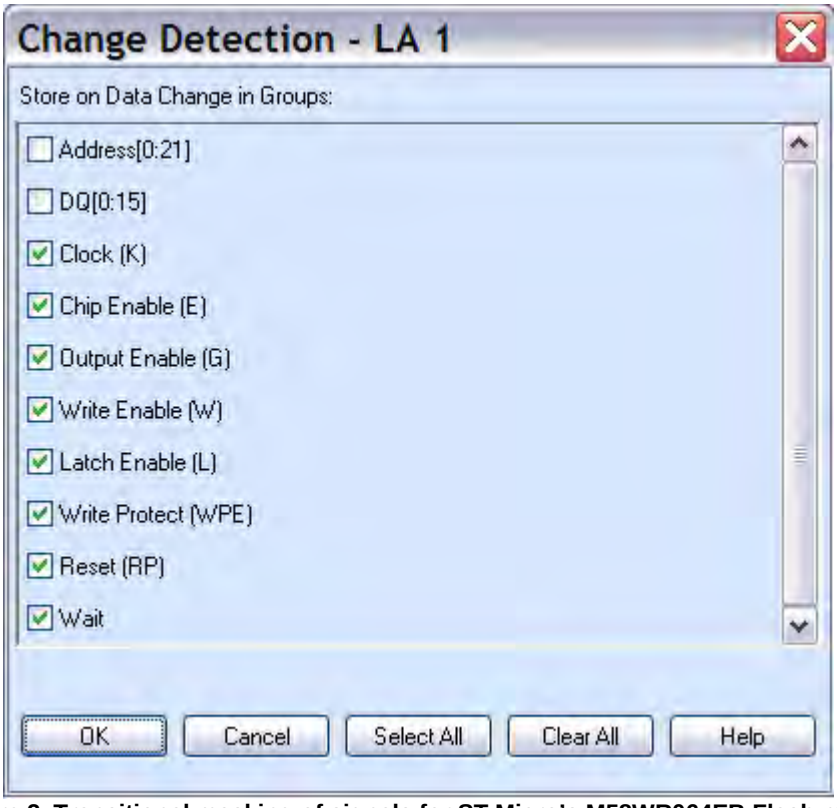

Figure 2. Transitional masking of signals for ST Micro's M58WR064EB Flash memory.

IV. Single Sample Transition Detection

Some logic analyzer designs don't have transition detectors that are fast enough to examine each sample as they are taken. A sample in logic analyzer terms is the logic state for one tick of the analyzers timing clock for all of the signals connected to the probes. If we are using a 500MHz timing clock then the transition detector would need to be able to complete the check for signal changes in under 2ns in order to keep up with the rest of the analyzer.

If the transition detector can't keep up with the timing clock a technique of looking at two, or more, successive samples at the same time can be used. While this is a clever work-around for a design limitation it can have a severe impact on the size of the acquisition time window that isn't immediately obvious.

When two samples are checked for changes at the same time, and a change is detected, then two memory samples must be stored. Instead of storing the single memory location as the fast detector would, the slow one must store two. The number of transitions that a slow detector can store will never be greater than ½ the memory depth.

If the analyzer with the slow detector also lacks a separate timestamp memory then the greatest number of transitions stored will be ½ of ½ of the memory. Being able to store only ¼ the number of transitions compared to the memory depth means that a analyzer with 2M of trace depth per pin provide a shallow 512k transitions when used in this very convenient sampling mode.

V. Conclusion

Tektronix's TLA Series Logic Analyzers excel at providing the maximum resolution along with large acquisition time windows which are useful when debugging data flow into and out of Flash and SDRAM memories. The combination of high timing clock rates for transitional timing (500MHz), a separate timestamp memory, user definable signal masking, and fast transition detectors that look for changes at the full speed of the analyzer add together to provide the best value in hardware debug.