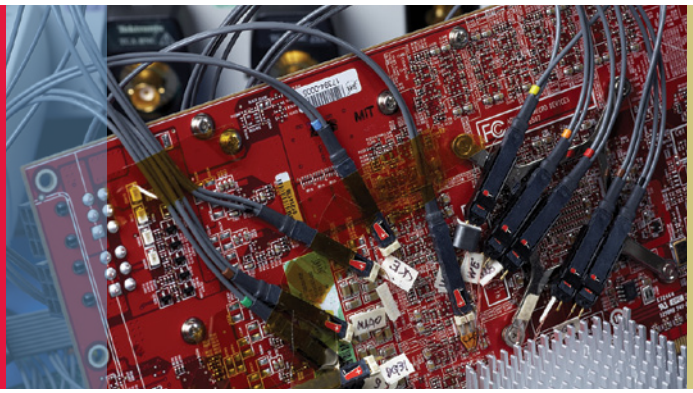
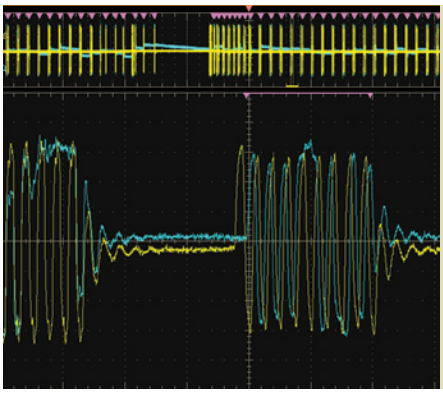




Electrical Verification of DDR Memory

Application Note

Virtually every electronic device, from consumer electronics, smart phones to server farms, uses some form of memory. SDRAM is the dominant memory technology in most types of computers and computer-based products, offering a good combination of speed and storage capacity for relatively low cost per bit. DDR, or double-data- rate SDRAM, has become today's memory technology of choice, and the technology continues to evolve as companies strive to increase speed and capacity while reducing cost, power budget, and physical size of memory devices in order to cater to newer more complex application needs.

As clock rates and data transfer speeds continue to increase with each advance in performance, analog signal integrity of the memory subsystem has become an increasing area of focus for designers who must guarantee system performance margins, or ensure interoperability of memory and memory-control devices within a system. Many performance problems, even some of the ones found at the protocol layer, can be traced back to signal integrity issues. So the importance of doing analog verification on memory devices has grown to become a critical step in validating many electronic designs.

The jitter, timing, and electrical signal-quality tests required to validate memory devices have been specified in detail by JEDEC Solid State Technology Association. Parameters such as clock jitter, setup and hold timing, signal overshoot, undershoot, transition voltages etc are included in the comprehensive set of tests described in the JEDEC specifications for each memory technology. But performing these tests in conformance with the spec presents a host of challenges that can be a complex and time-consuming task. Having the right tools and techniques can significantly reduce test time and ensure the most accurate results. In the balance of this application note, we will discuss several elements of the Tektronix solution 'toolkit' for memory test that can help overcome the inherent challenges and simplify the validation process.

Tektronix®

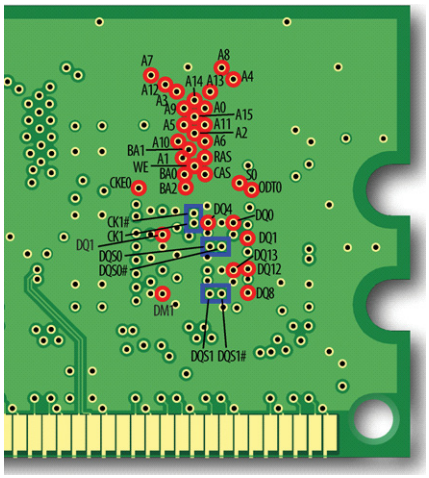


Figure 1. Test points on "back side" vias of DDR3 DIMM.

Signal Access and Probing

One of the first obstacles to overcome in memory validation is the issue of accessing and acquiring the necessary signals for analysis. The JEDEC standards specify that measurements should be made at the BGA ballouts of the memory component. Since FBGA components include an array of solder ball connections that are, for practical purposes, inaccessible, how can this be accomplished?

One solution is to design for test during PCB layout and include vias directly beneath the memory components that can be probed on the back side of the board. Although these test points are not strictly "at the component ballouts," for practical purposes the trace length through the PCB is generally short enough that signal degradation effects are minor. When this approach can be used, signal integrity is usually quite good and electrical validation can be performed with acceptable test margins.

Although it is possible to use handheld probes for this type of application, maintaining good electrical contact between multiple probe tips and test points simultaneously can be difficult. Considering that some JEDEC measurements require three or more test points, plus other signals such as Chip Select, RAS, and CAS that may be needed to qualify the memory state, the option of using solder-down probe connections quickly becomes an attractive alternative for many engineers.

Tektronix has developed a selection of probing solutions that are designed specially for this type of application. The P7500 series probes, with bandwidths from 4 GHz to 20 GHz, are the models of choice for memory applications. Figure 2 illustrates one of several available P7500 probe tips that are well-suited to memory applications. These "micro-coax" tips provide a cost-effective solution for situations where multiple tips must be soldered and left in place, while offering excellent signal fidelity for testing the latest set of SDRAM memory interface specifications.

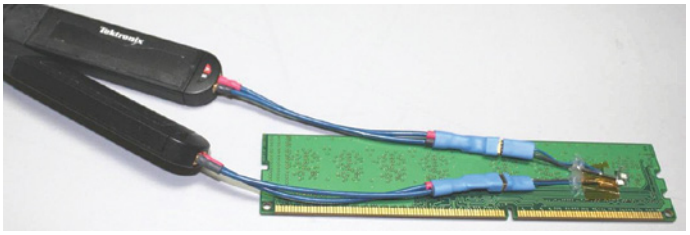


Figure 2. P7500 Micro-Coax probe tips soldered to DIMM.

Figure 3. P7500 probe and accessories.

Technology	JEDEC Specification
DDR	JESD79F
DDR2	JESD79-2F
DDR3	JESD79-3F
DDR3L	JESD79-3-1A
DDR4	JESD79-4
LPDDR	JESD209B
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
GDDR5	JESD212A

Table 1. JEDEC Specifications for DDR Technologies.

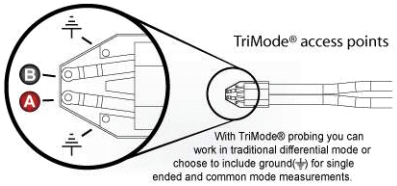


Figure 4. P7500 TriMode tip connections.

Another advantage of the P7500 probes for memory applications is their patented TriMode® feature. This unique feature allows the probe to measure either differentially between + and - , or single-ended between signal and ground. Using three solder connections at the probe tip, the user then has the ability to switch between differential and single-ended modes using control buttons on the probe or menu commands on the oscilloscope. One example of how this can be useful for memory applications is the technique of soldering the probe's + connection to a single-ended data or address line, and soldering the probe's – connection to another adjacent line. The user can then easily measure either of these two signals using one probe, by switching the probe between its two single-ended measurement modes.

There are, however, many situations where signal access through back-side vias may not be an option. Designs using embedded memory or package on package configurations used in many of the consumer applications as well as smart phone may not provide the the luxury of available board space on the back side opposite the memory components. Even many standard DIMM's now have memory components back-to-back on both sides of the board, to increase storage density. How can the test engineer get access to test points in this scenario?

Fortunately, there are now probing solutions for even these situations. Tektronix has partnered with Nexus Technology, to develop memory component interposers for all popular memory standards and package types Interposers are available in different form factors targeted for specific applications. Based on the form factor the interposers can be grouped into the following types (Table 2).

These interposers use a socket that solders down onto the target device in place of the memory component. The interposer, which has test points for probing, then snaps into place on the socket. The memory component then attaches to the top of the interposer.

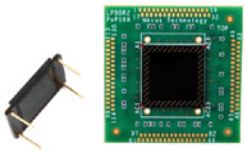
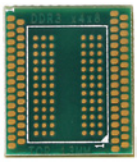
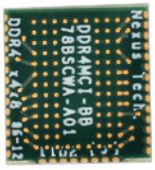
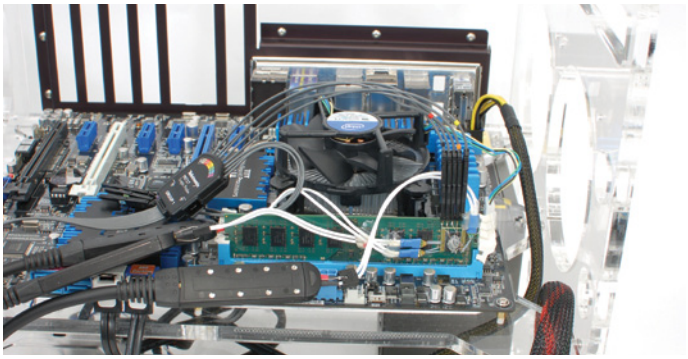
Interposer Type	Description
Socketed Interposer 	■ Comes with a Custom BGA Socket that needs to be soldered to Target ■ Allows snap-in/snap-out of components using micro socket ■ Full BGA visibility ■ No Special design or routing requirements needed ■ Quickly swap TLA & oscilloscope interposers on the same target. ■ Quickly Swap Memory Components on the Target
PoP Interposer 	■ Comes with a Custom BGA Socket that needs to be soldered to Application Processor ■ Allows snap-in/snap-out of components using micro socket ■ Full BGA visibility ■ No Special design or routing requirements needed ■ Quickly swap TLA & oscilloscope interposers on the same target. ■ Quickly Swap Memory Components on the Target
Direct Attach Interposer 	■ Interposer is soldered to Target ■ Memory Component is soldered to Interposer ■ Full BGA visibility ■ No Special design or routing requirements needed
Edge Interposer 	■ Interposer is soldered to the Target ■ Memory component is soldered to Interposer ■ Signals are brought to pads on edge of the Interposer ■ KoV of the interposer is the same size as the BGA component ■ Because of limited space around the edge not all signals can be probed ■ Choose between wide / narrow Address or data
MSO Interposer 	■ Provides a quick and easy access of the Addr/CMD signals to MSO digital channel ■ Allows the Addr/cmd triggers to correlate Analog Inputs ■ Combine with Component Interposers for high fidelity analog analysis

Table 2.



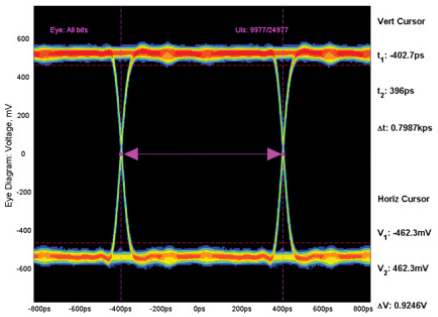


Figure 5. Component Interposer with solder tips; eye diagram of probed signal.

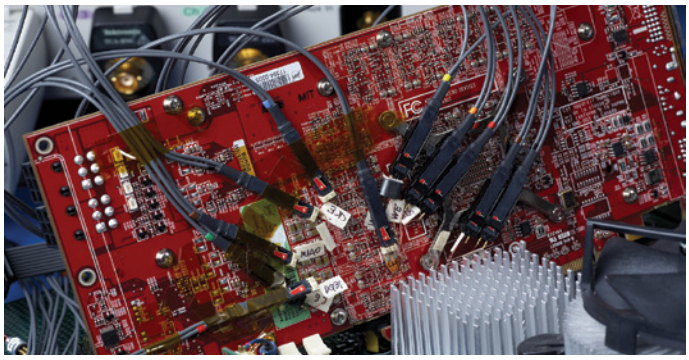


Figure 6. P6780 digital probe tips soldered onto GDDR5 PCB.

Figure 8. MSO Interposer.

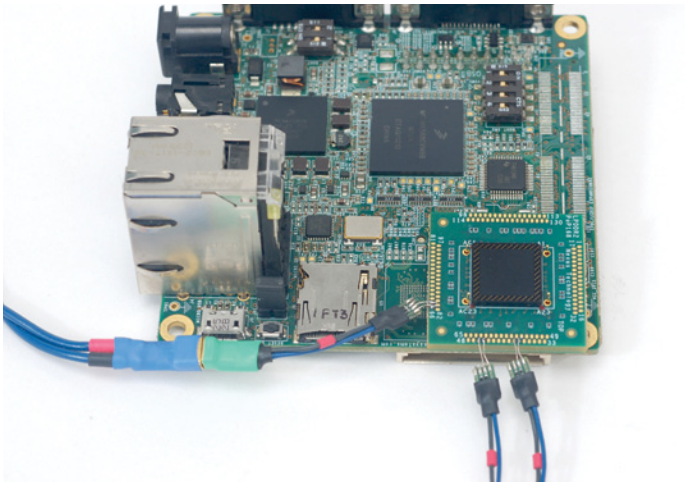


Figure 7. P7500 probe connected to LPDDR2 using PoP Interposer.

Small isolation resistors are embedded within the interposer, as close as possible to the BGA pads of the memory component. These resistors are matched to the P7500 probe tip's electrical network, ensuring excellent signal fidelity.

Digital Probing

The Tektronix MSO70000 Series Mixed-Signal Oscilloscopes combine four analog channels with up to sixteen digital channels. In addition to connecting to 1 or 2 data and clock lines, it's often useful to connect to the DDR command bus signals and subsequent address lines. The P6780 differential probe enables high-bandwidth performance with wide bus signal access for use on the MSO70000 Series. Because of high-density layout and constrained packaging, signal access continues to be challenging for those validating DDR memory.

Probing a full spectrum of connectors, pins, device leads, traces, and vias is simplified with these high performance P6780 logic probes that include a range of solder-in accessories. With solder-in probe tips for the P6780, designers can add test points as necessary without the need to include a dedicated probe footprint. As with any measurement setup, care should be taken to minimize test equipment impact on the measurements. The P6780 solder-in tips include ferrite cores to reduce reflections on the line. Keeping wire length to the minimum required for connectivity will ensure better signal fidelity.

The MSO interposers for the slot connectors provide another option to get access to the signals on the command bus with the ability to probe the data and the strobes using the analog channels on the MSO.

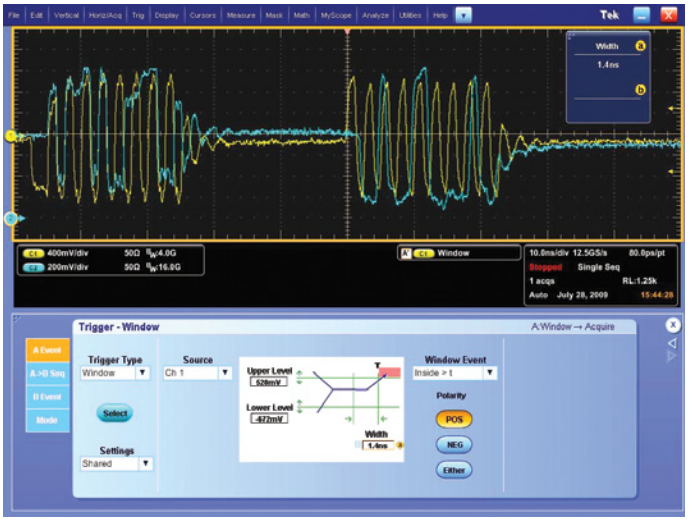


Figure 9. Using « Window » trigger to identify DQS Write Preamble.

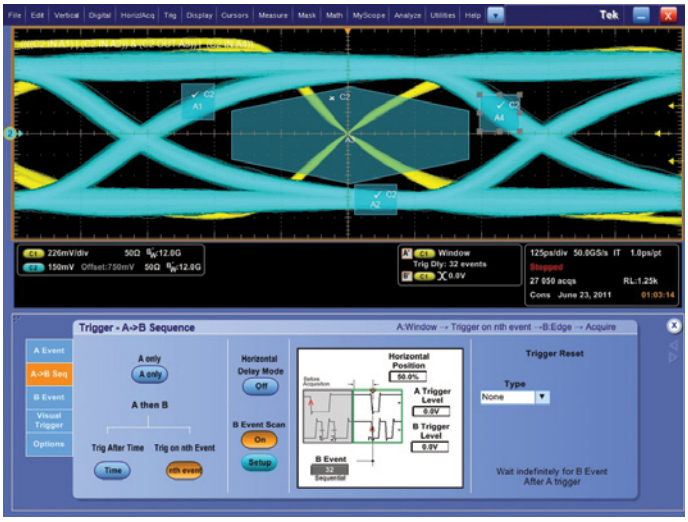


Figure 10. Visual trigger on a DQ Signal Eye.

Signal Capture

Once the signal lines have been successfully probed, the next step is to isolate the events of interest on the memory bus. If performing JEDEC conformance measurements, you may need to perform certain measurements only on qualified portions of the data stream such as read or write bursts. For debug it may be necessary to further isolate certain events by a particular rank or bank, or to isolate certain data patterns for analysis of signal-integrity issues such as data-dependent jitter, timing, or noise problems.

There are several methods that can be used to identify and isolate read- and write bursts or other bus conditions. One of the simplest methods is to use the DQS or Data Strobe signal to identify the start of a read or write burst. For example, DDR3 always asserts DQS high at the start of a write, or low at the start of a read. Hardware triggering capabilities in the oscilloscope can trigger on this preamble portion of the burst and assure that only reads or writes are captured at the beginning of the acquired waveform. Figure 9 shows both read & write bursts, with the trigger point at center-screen on a write burst.

The Visual Trigger option on the DPO/MSO70000 Series Oscilloscope enables additional flexibility in utilizing custom-designed shapes to complement traditional edge triggers for more versatile DQS burst capture capability (see Figure 10). Visual trigger lets users place custom-designed shapes directly on the scope's display where the boundaries of the shape define trigger events for a DQS or Data Strobe being acquired. These shapes can be moved, rotated and modified into one of 4 different (e.g., triangle, trapezoid) on the scope graticule and can be combined with traditional scope trigger functions to enable a more comprehensive and accurate signal capture.

Command	SO#	RAS#	CAS#	WE#
Mode Register	0	0	0	0
Refresh	0	0	0	1
Precharge	0	0	1	0
Activate Row	0	0	1	1
Write Column	0	1	0	0
Read Column	0	1	0	1
No Operation	0	1	1	1
Deselect	1	x	x	x

Table 3. SDRAM Commands.

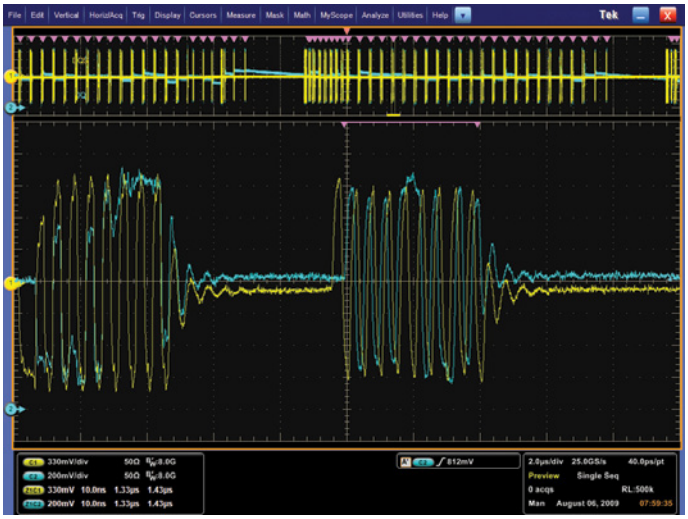


Figure 11. Using Advanced Search & Mark to identify all write bursts.

Qualifying Reads & Writes with Advanced Search & Mark

Another tool available in the DPO/MSO70000 series oscilloscopes is a utility called Advanced Search & Mark (Option ASM). ASM can scan through an entire waveform acquisition and search for a variety of user-configurable conditions. One of these conditions available to the user is DDR Read/Write identification; ASM will find all read bursts or write bursts in an acquired waveform record and mark each burst with a visible marker on-screen. In addition to using these marks for visual analysis, the oscilloscope can apply the marks as qualifiers for DDR-specific measurements, so that measurement occurs only on the appropriate portion of the data stream. In the case of DDR, the search algorithms in ASM make use of the fact that phase relationships are different for read and write bursts; DQ and DQS are in-phase for reads, and 90 degrees out of phase for writes. In Figure 11, ASM has marked all write bursts with pink triangle symbols shown above the waveform, and a single write burst magnified in the zoom window in Figure 11.

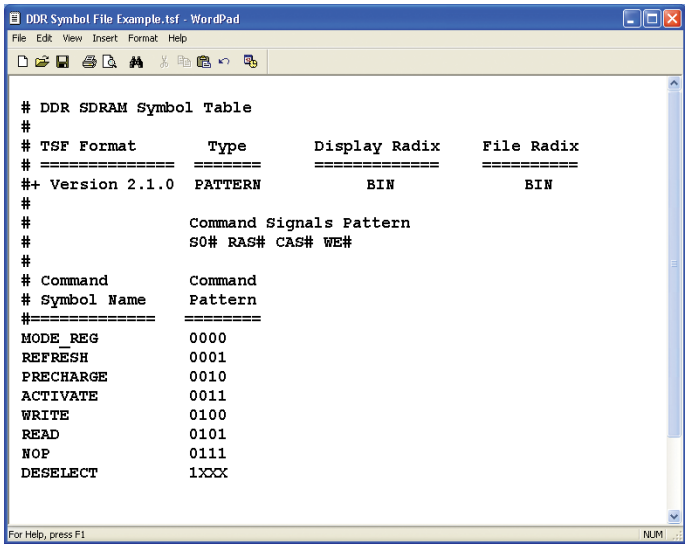


Figure 12. DDR Symbol File Example.

Bus-Qualified Triggering

A performance mixed-signal oscilloscope provides many options to qualify signal capture using the state of command and control lines on the memory bus.

SDRAM memory commands are synchronized to the rising edge of the memory clock (CK). The four command signals are chip select (S0# or CS#), row address select (RAS#), column address select (CAS#) and write enable (WE#). The # symbol indicates these are active low signals (see Table 3). The verification of memory commands requires the MSO to probe five signals, CK, S0#, RAS#, CAS# and WE#, in addition to acquiring the appropriate data (DQ) and strobe (DQS) signals. In the MSO digital channel menu the five command signals – CK, S0#, RAS#, CAS# and WE# – are assigned to probe channels.

The Activate Row command is the first command of a write or read command sequence. To trigger the MSO on the Activate Row command, configure the MSO to trigger on a Command group equal to 0011. This is S0#=0, RAS#=0, CAS#=1 and WE#=1, as shown in Table 3.

Dealing with binary values like 0011 can be error prone. The MSO works with data in several formats: binary, hex, and symbolic. Pattern symbol files are used when a group of signals define a logical state such as the SDRAM command group. Based on the SDRAM command table, as shown in Table 3, a Tektronix Symbol File (.tfs) was created with Microsoft Notepad (see Figure 12).

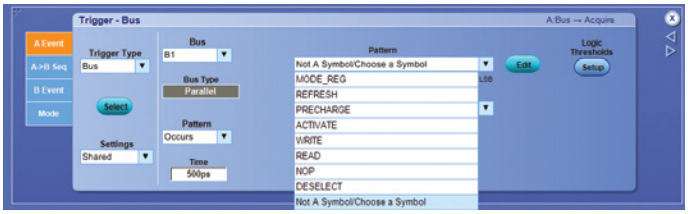


Figure 13. MSO70000 Symbol Trigger menu with DDR commands.

Figure 14. DDR3 Command Bus decoding on MSO70000.

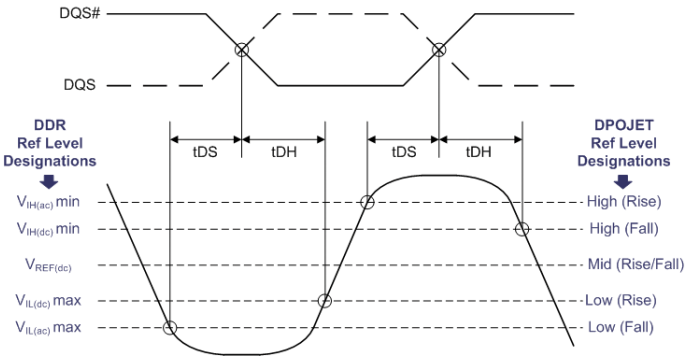


Figure 15. Measurement reference levels.

The MSO uses these pattern symbols when setting up the MSO to trigger on the Activate command (see Figure 13). To use pattern symbols in the MSO bus trigger menu, the Bus Radix is changed to Symbolic and the symbols become available for selection. When used along with Visual Trigger capability, the time spent performing DQS, Data Strobe and Pattern verification can be greatly improved.

Performing JEDEC - Compliant Measurements

As mentioned earlier, the JEDEC specifications for each memory technology specify an array of conformance measurements specific to the technology. These include parameters such as clock jitter, setup and hold timing, transition voltages, signal overshoot & undershoot, slew rate and other electrical-quality tests. These specified tests are not only numerous but can also be complex to measure using general-purpose tools.

An example is measurement reference levels. JEDEC specifies certain voltage reference levels that must be used when making timing measurements. Figure 15 shows a graphic representation of the Vih and Vil levels (both AC and DC) that are used for timing measurements on data signals. Note that levels for rising and falling edges are defined differently.

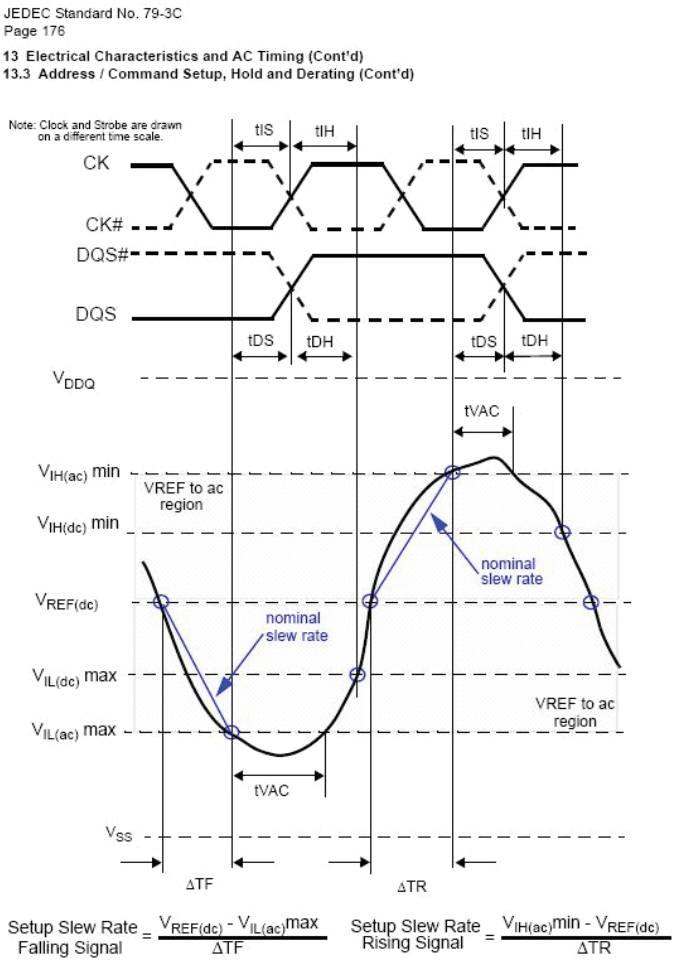


Figure 16. Slew Rate measurement - "Nominal" method for DDR3.

Another example is slew rate measurements. Slew rate must be measured on data, strobe, and control signals and is then used to calculate adjustments to the pass/fail limits for timing measurements such as Setup and Hold. But the details of how the slew rate measurement is performed varies depending on which signal is being measured. See Figure 16: the 'nominal' method is used for one set of measurements, while a different 'tangent' method must be used for another set.

Because of the complexity inherent in the JEDEC-specified measurement methods, reference levels, pass/fail limits, etc. it can be extremely valuable to have an application-specific measurement utility for DDR test. Using such a utility ensures that your measurements are configured properly and eliminates many hours of setup that would be required using general-purpose tools alone.

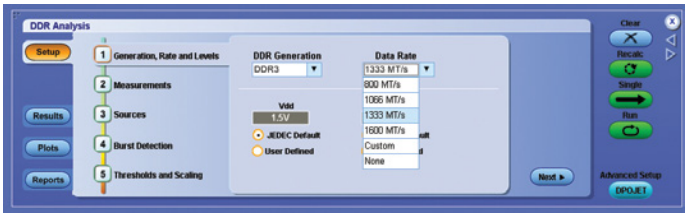


Figure 17a. DDRA setup screen - Step 1.

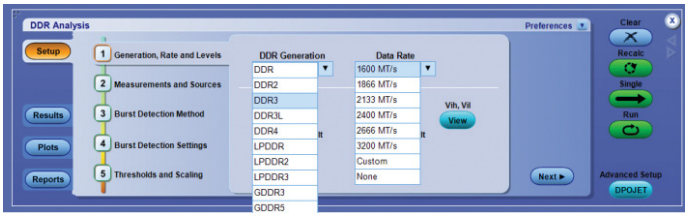


Figure 17b. DDRA Analysis.

DDR Analysis Software

Option DDRA for Tektronix real-time oscilloscopes (DPO / MSO70000 Series, DPO7000 Series and DPO/MSO5000 Series) is a software utility dedicated to automation and setup of measurements for testing DDR devices. The broad set of Measurements available in DDRA all conform to the JEDEC specs, but the user also has the option to customize many settings for measurement tasks on non-standard devices or system implementations. This software option currently supports DDR, DDR2, DDR3, DDR3L, DDR4, LPDDR, LPDDR2, LPDDR3, GDDR3, GDDR5.

Option DDRA works in conjunction with two other software packages on the Tektronix oscilloscope; Advanced Search & Mark (Option ASM, described above) and DPOJET Jitter and Eye Diagram Analysis Tools. These three utilities work together to create a powerful, flexible yet easy-to-use suite for DDR testing and debug.

The menu interface for DDRA has five steps which guide the user through a selection process. Step one of the interface is shown in Figure 15. Here the user selects the DDR generation to be tested and the speed grade of the memory. The drop-down selection box in this example shows all the commercially-available speed grades for DDR3. In addition to the default choices, the user can enter a custom speed setting, making the software easily adaptable to future technology advances, overclocking applications, etc. Once the generation and data rate have been selected, DDRA automatically configures the proper voltage references for measurements. Here again there is

a “User Defined” setting, allowing the user to override the JEDEC defaults and enter custom values for Vdd and Vref if desired.

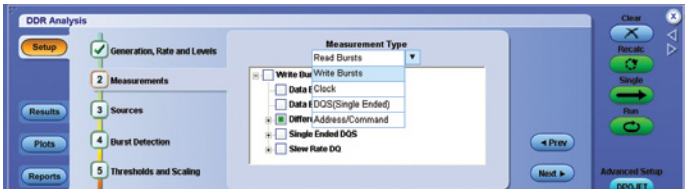


Figure 18. DDRA setup screen - Step 2 (measurement selection).

Step 2 allows the user to select which measurements to perform. The available measurements are grouped into drop-down menu selections according to which signals and probing connections are required. For example, measurements made on the Clock line are all grouped under a “Clock” drop-down menu. Read measurements, Write measurements and Address/Command measurements are similarly grouped into their own drop-down menus so that all measurements requiring a particular probing setup can be easily selected for a single test run.

The remaining steps 3, 4, and 5 in the DDRA menu interface guide you as to how the needed signals should be probed and offer additional opportunities for customizing or adjusting parameters such as measurement reference levels.

Once the setup is complete and the user selects <Run> (or <Single>) the oscilloscope will acquire the signals of interest, identify and mark data bursts if needed, and make the selected measurements. Using the default record length, the oscilloscope will typically acquire around 1000 unit intervals, taking measurements on all valid edges in the acquisition. When measuring data bursts, the software automatically generates an eye diagram showing both DQ and DQS overlaid to show relative timing. The DDRA “Results” panel shows all measurement results with their statistical population, spec limits, pass/fail results and other data. If desired, a printed report can be generated, with an option to also save the waveform data that was used to make the measurements.

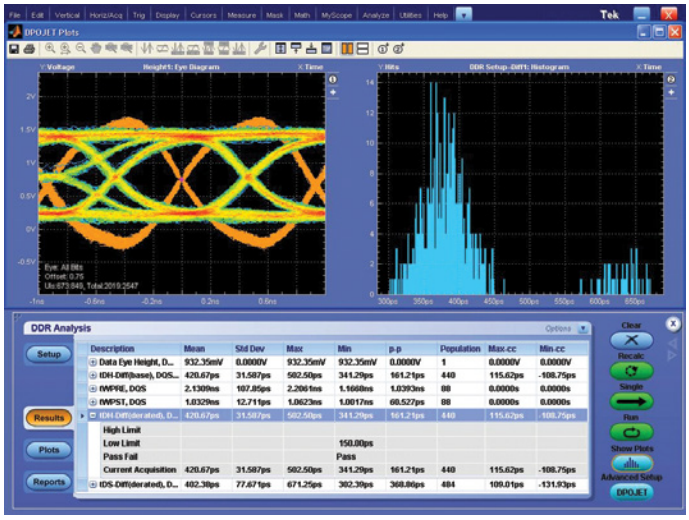


Figure 19. DDRA “Results” Screen showing two of the available plots.

Failure Analysis and Debug

Because all of the captured waveform data is available behind the measurement results, many options are available to the user beyond the results themselves. If a measurement fails the spec limits, it is possible to identify exactly where in the waveform record the failure occurred, then zoom in on the region of interest to investigate the exact signal details and characteristics at the time of failure. Several tools available in the software make it easy to analyze the captured data and to pinpoint regions of interest. For example, the Histogram plot shown in Figure 19, can be applied to any measurement of interest, showing worst-case measured values (in this example it has been applied to a Setup measurement.) Several other plot types are available. Tools such as “Cursor Sync” make it easy to link any data point in the plot back to its corresponding event in the original waveform record, making it simple to move back and forth between different views of the data for in-depth analysis.

Figure 20. Back-to-back DDR3 Write operations.

Verifying Command and Protocol Operations

The protocol sequence for a SDRAM Write operation starts with the Activate command followed by one or more Write commands. The Activate command with its row and bank addresses opens a specific row in a specific bank for writes and reads. The Write command with its column and bank addresses opens a specific column in the opened row in a specific bank for writes. It would be a protocol error for the Write command to access a bank that has no open rows. After the Write command, the memory expects at a defined memory cycle that the memory controller hub will write data to it. The row needs to be closed or deactivated with a Precharge command when the writing is completed for the open row and another row is to be accessed. The simplest DDR2 SDRAM command protocol sequence is Activate, Write and Precharge. A consecutive write-to-write sequence is Activate, multiple Writes and Precharge. A write-to-read sequence is Activate, Write, Read, and Precharge. You can have any order of Writes and Reads on an open row. It would be a DDR2 DRAM protocol error if the memory controller hub sent two Write commands in a row without the Deselect command between them. The DDR2 DRAM will respond to the Write command by reading in data that is strobed by the memory controller hub.

Another key DRAM specification is the minimum tRP time after the Precharge command is sent and before the Activate command is sent to open a row. This can be easily verified by changing the MSO to trigger on the Precharge command and measuring the tRP time between the Precharge and Activate commands to the same bank.

The same protocol and timing verification techniques are applied to DDR3 DRAM read/write operations. Note however with DDR3 multiple back-to-back write operations are supported in the specification. When performing write burst isolation a continuous strobe may cause a write cycle to merge two back-to-back writes if care is not taken to match the termination logic of the strobe signal while analyzing bus traffic.

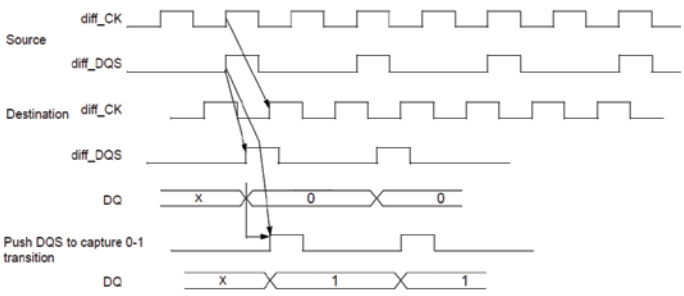


Figure 21. DDR3 Write leveling to deskew DQS and CK lines (source: JEDEC DDR3 SDRAM Standard, JESD79-3C).

In addition to verifying complete read or write cycle operations other important verification tasks that should be performed include:

Basic Functional Testing

During prototype system initialization a quick check of clock, reset and PLL lines helps to identify any key issues that may propagate into other subsystems. Browser or handheld probes are useful in moving from point to point while checking "vital signs".

Another basic test check would be verification of trace impedances. Since SDRAM memory systems use single-ended signals and differential signals, the traces for these signals have different impedances. As a result, one can perform verification using a DSA8300 Series sampling oscilloscope and time domain reflectometer (TDR) sampling module. Trace impedance flaws and trace termination flaws can cause poor quality edge transitions with non monotomic rising and falling edges. Poor quality edge transitions take longer, reducing the data valid window of clocked signals.

Power Management and Other Special Operating Modes

As the bus enters and exits power states certain lines may become inactive or turn back on. Careful attention is needed as these additional states add complexity in system interoperability. In Low Power DDR3 (LPDDR3), for example, devices incorporate advanced power management techniques such as Partial Array Self Refresh, allowing only necessary parts of the memory array to be used thus improving its efficiency and power consumption.

Write/Read Leveling

Increasing bandwidth of source synchronous buses can be difficult if only data rate scaling is used. However higher bandwidths can be achieved with innovative physical layer design techniques. DDR3 supports a fly-by topology in which signals from the memory controller arrive at each memory component in a sequential manner, thus reducing loading and improving overall signal integrity. Because of the electrical delays between each component the memory controller needs to perform a delay calibration to realign the clock (CK) with the data strobe (DQS) for each component. Ensuring this operation functions properly helps reduce flight time skews between clock and strobe signals thus providing additional margin to the memory system.

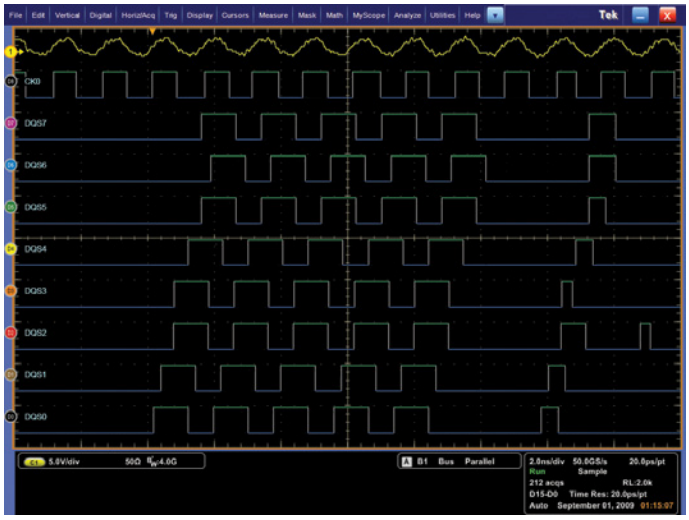


Figure 22. DQS0 – DQS7 skew relative clock during write leveling operation.

DQ/DQS Margining

As mentioned earlier JEDEC outlines many measurements required for standards conformance. Silicon and component designers are looking beyond evaluation of basic parametric testing to understand and characterize the design over a range of process, voltage and temperature. A common example is to vary the Vref or Vdd lines and monitor data (DQ) and strobe (DQS) for noise immunity and sensitivity. This provides a higher confidence of the device working over a wider range of operating conditions.

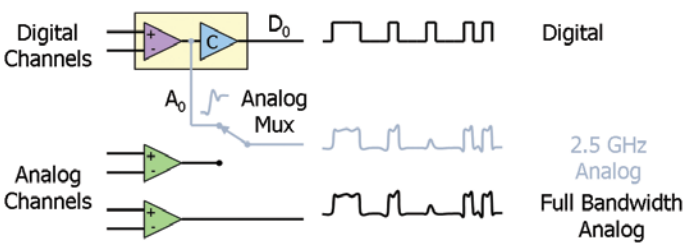


Figure 23. iCapture architecture.

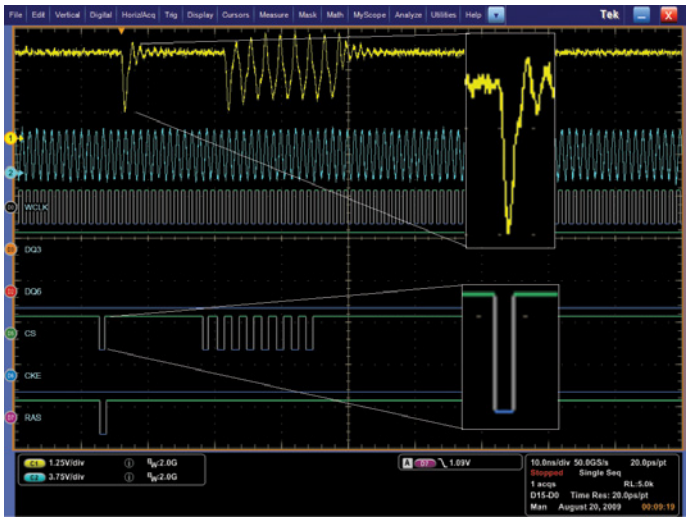


Figure 24. iCapture showing Chip Select line with analog and digital views.

Combining Digital and Analog Views

As discussed previously there are many options for accessing DDR signals, from interposers to solder-in probe tips. It's not uncommon to need to monitor many digital lines and then after uncovering a signal integrity issue add another probe to view the signal in its analog form. This is known as "double probing". It's an arrangement that can compromise the impedance environment of your signals. Using two probes at once will load down the signal, degrading the device's rise and fall times, amplitude, and noise performance.

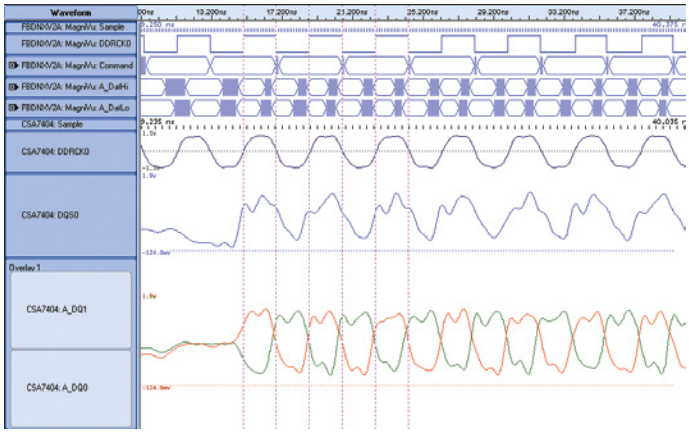


Figure 25. Using iCapture with a TLA7000 Series for System State views of a DDR2 design.

With the iCapture feature the MSO70000 allows you to see time-correlated digital and analog behavior, without extra loading capacitance and setup time required for double-probing. Any of the sixteen digital channels can be "muxed" through the oscilloscope's analog signal path thereby providing a side by side digital and analog representation of the signal of interest. Figure 24 shows a simple illustration of verifying the Chip Select line on a GDDR5 design. This can be helpful in ensuring correct logic thresholds are used in sampling the digital data or verifying signal integrity with greater precision. If system state monitoring requires greater than 20 measurement channels, the iCapture capability can extended to include a Tektronix TLA7000 Series logic analyzer capable of 100+ channels of acquired digital behavior. As illustrated in Figure 25; the logic analyzer displays captured digital signals alongside 4 analog channels from the Tektronix oscilloscope through iCapture capability.

Summary

In this application note we've explored many of the challenges associated with DDR testing and have introduced tools needed for validation and debug of memory designs. Tektronix offers a comprehensive tool set including performance mixed signal oscilloscopes, true differential TDRs, and logic analyzers with Nexus Technology memory supports to enable embedded and computer designers to perform quick and accurate electrical testing and operational validation of DDR-basedmemory designs. For more details about DDR testing visit the JEDEC page at http://www.jedec.org/ or http://www.memforum.org/index.asp. Here you will find detailed DDR specifications, white papers, and other support materials. Additional information about DDR testing can be found at www.tektronix.com/memory. This site includes extensive materials like application notes, webinars and recommended test equipment.

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For Further Information
Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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