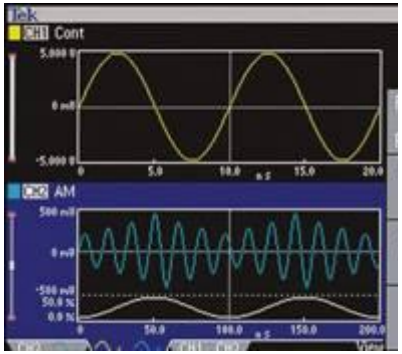
USB 3.0 Physical Layer Testing



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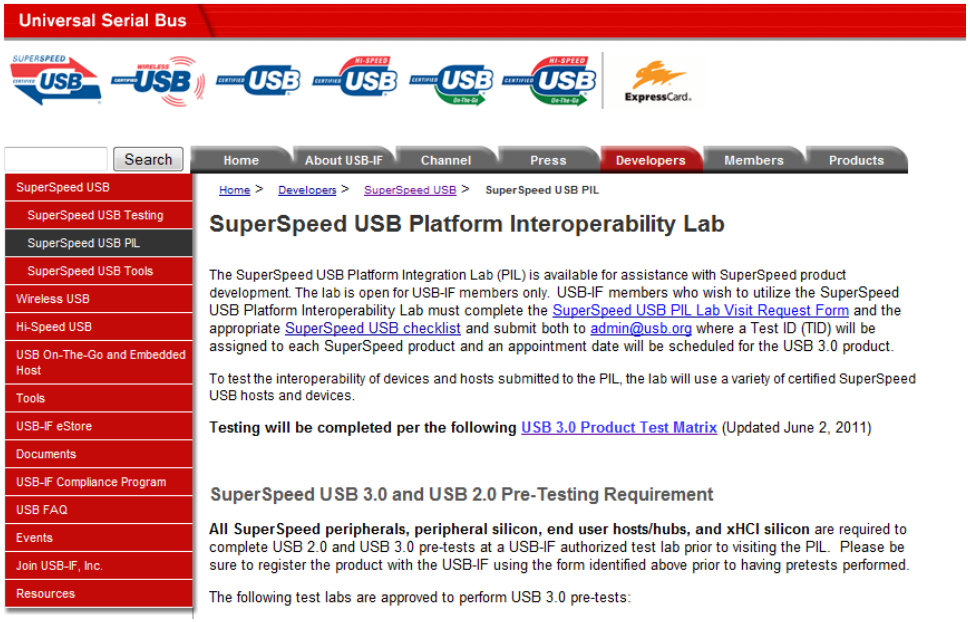
USB CTS Updates

- Draft 0.9 is available on the USB-IF site
- Updates not in 0.9 Specification
  - Tethered Devices (i.e Flash Drive) are tested with 11” Host Channel Only
    - Short cable is used for RX testing
    - Host channel is embedded for TX testing
  - Receiver Calibration Eye Height Limits: 145mV for Device and 180mV for Hosts
  - Receiver Jitter Tolerance Frequencies: 10 MHz, 20 MHz, and 33 MHz have been added
  - Updated Calibration Procedure

SuperSpeed Compliance

- PIL Lab
- USB Workshops
- Test Labs can provide pre-testing support and are currently being certified for USB testing
- Tektronix solutions are available in all locations!



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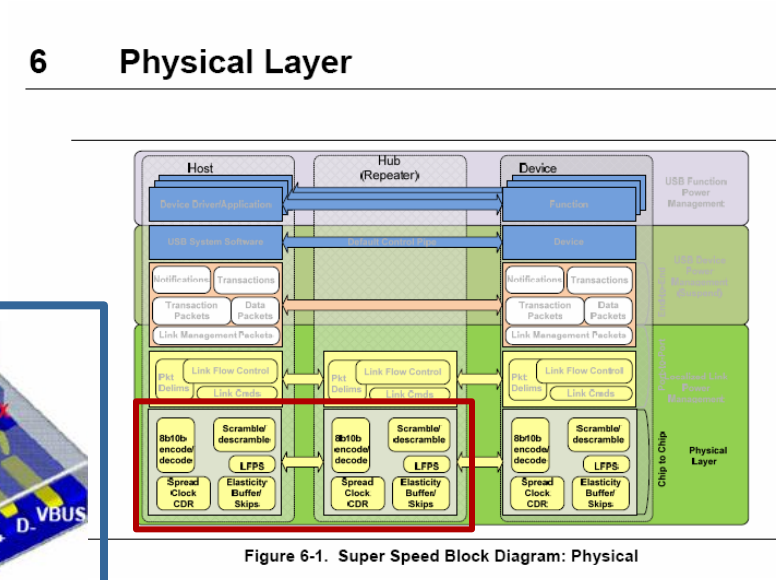
USB 3.0 Key Considerations

- Receiver Testing Now Required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel Considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Test Strategy
  - Cost-effective tools
  - Flexible solutions

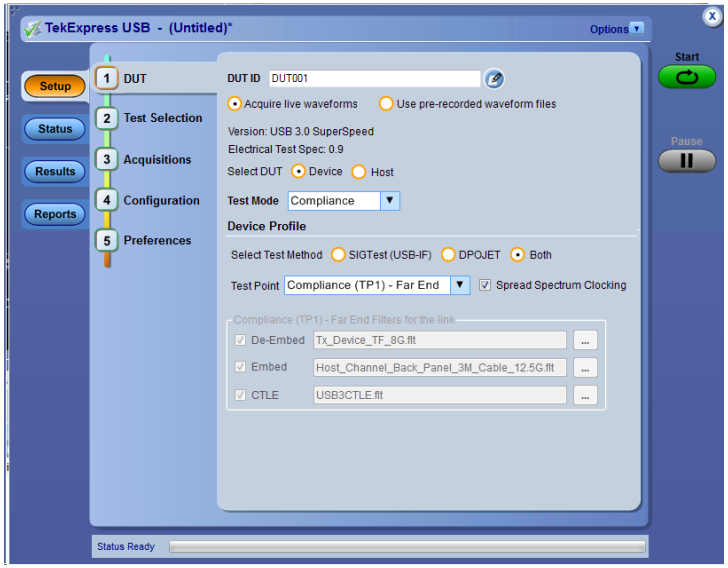


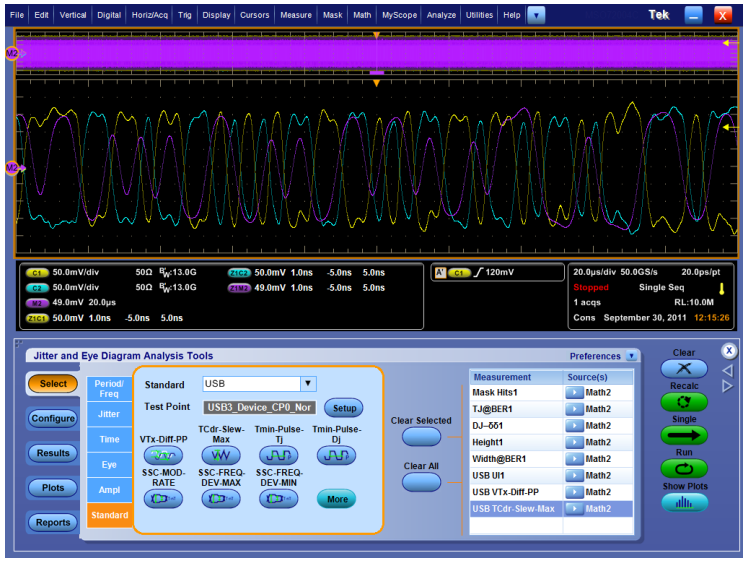
Source: USB 3.0 Rev 1.0 Specification

Tektronix

Transmitter Solutions

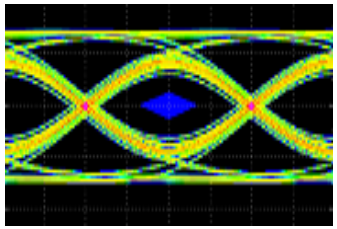
- Comprehensive Solution Goes Beyond Compliance
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results
- Complete Toolset for Characterizing USB 3.0 Designs
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG





USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
  - Reference channel is embedded and CTLE is applied
- USB 3.0 Reference Channels
  - Host Reference Channel
    - 11” back panel is applied for device testing
  - Device Reference Channel
    - 5” device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels
- USB 3.0 Reference Equalizer
  - Attenuates the low frequency content of the signal to open the eye



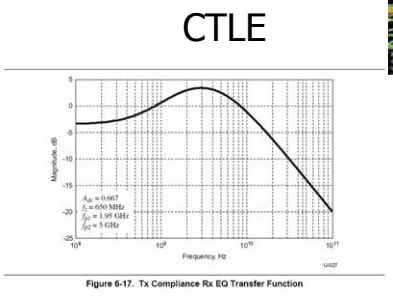


Figure 6-17. Tx Compliance Rx EQ Transfer Function

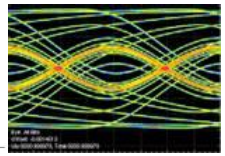
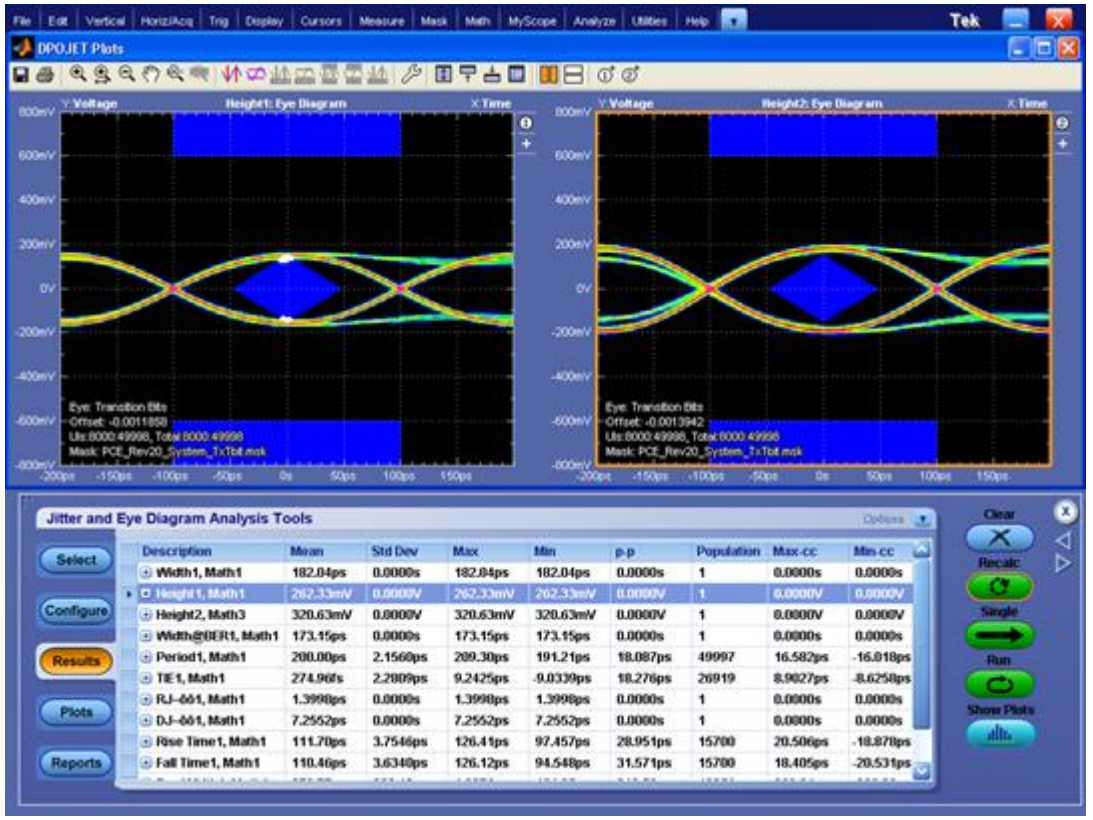


Figure 6-14. Tx Normative Setup with Reference Channel

Fixture and Channel De-Embedding

- Why de-embed – Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins
- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software

Before → **After**



Channel Embedding

- Compliance Testing is done by embedding the compliance channel, but many designers want to validate other channel models
  - Understand transmitter margin given worst case channels
  - Model channel and cable combinations beyond compliance requirements
  - Create interconnect models with SDLA software to analyze channel effects

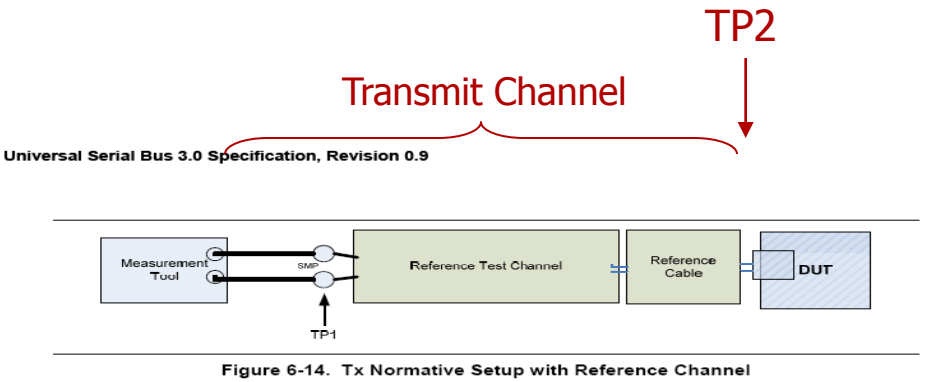
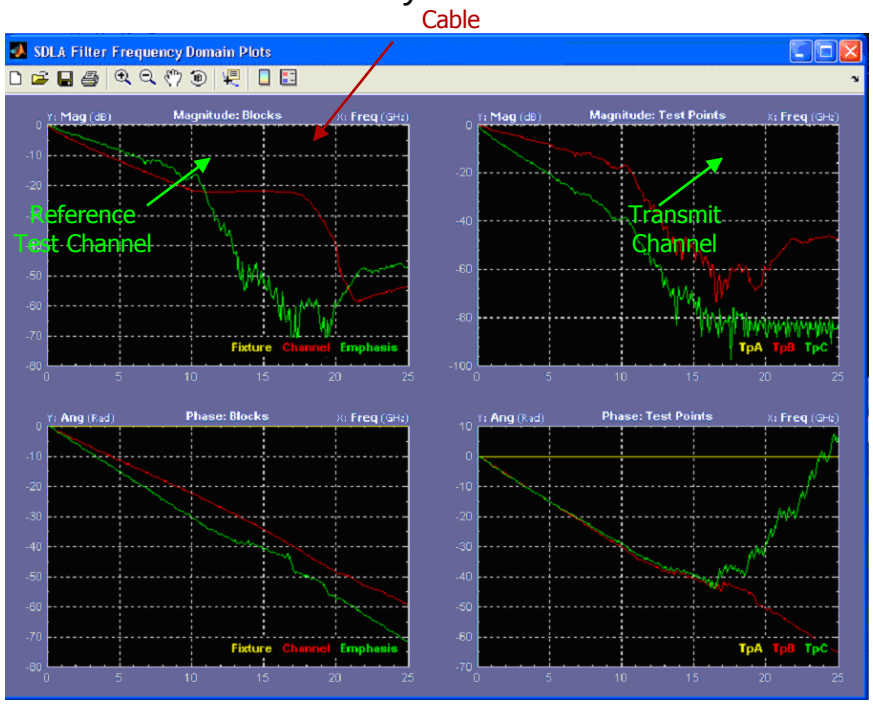
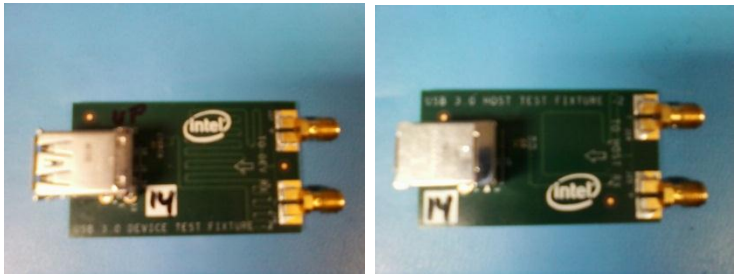


Figure 6-14. Tx Normative Setup with Reference Channel

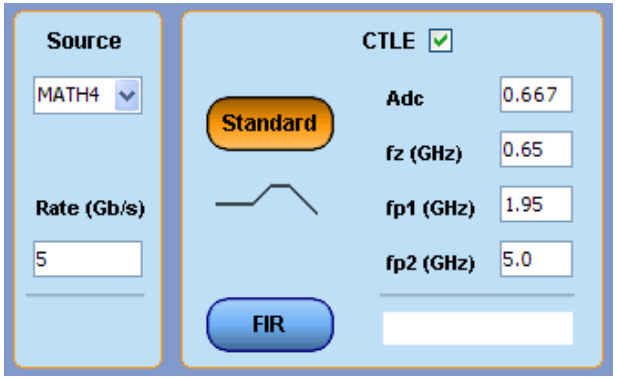


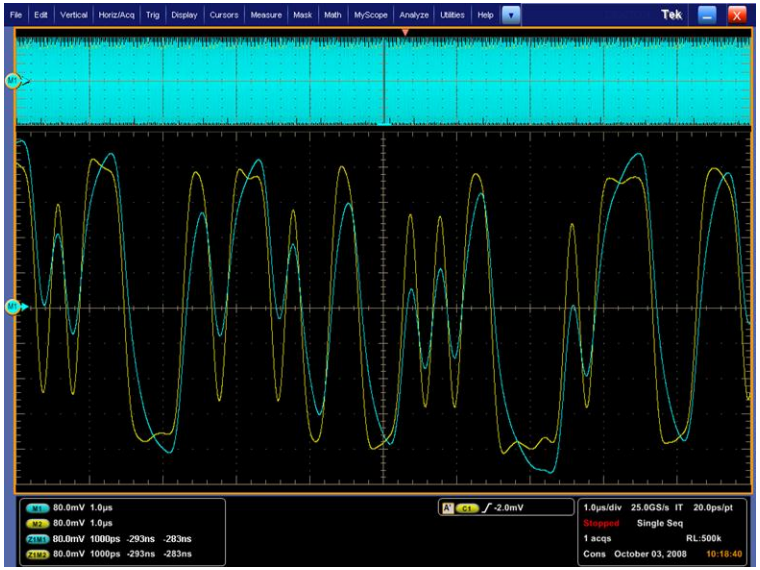


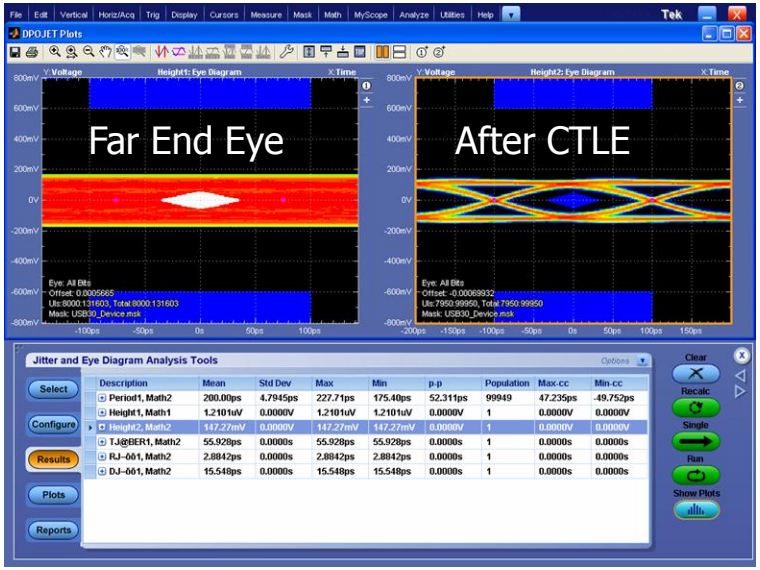
USB-IF Host & Device HW Channels

Receiver Equalization

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix' USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)

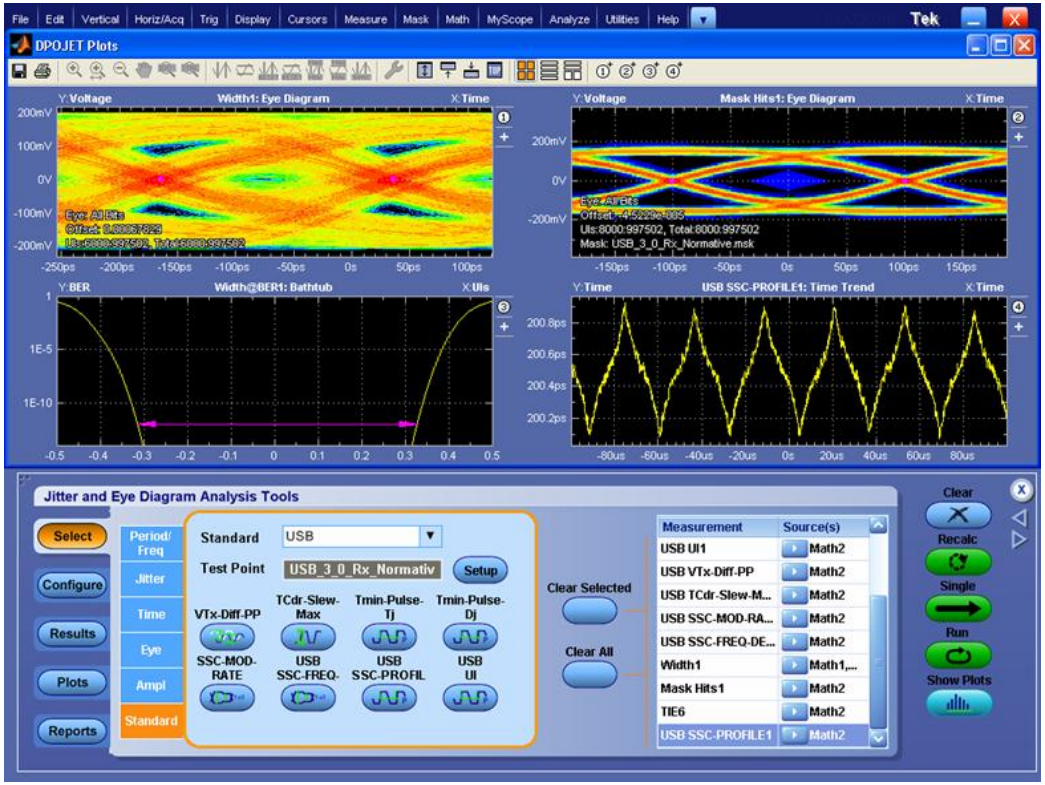






USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation



SuperSpeed Transmitter Compliance Testing

1. Connect DUT to scope via test fixture.
2. Transmit CP1 (toggle pattern) & measure 10^6 consecutive UI
   - This step used to measure RJ
3. Repeat with CP0 (scrambled D0.0)
   - Will combine RJ (step 2) with DJ to extrapolate TJ (step5)
4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   - Channels are S-Parameter-based and are embedded into captured waveform
5. Extrapolate jitter to 10^{-12} BER

Spec	Min	Max	Units
Eye Height	100	1200	mV
Rj @ 10^{-12} BER		0.23	UI
Tj @ 10^{-12} BER		0.66	UI

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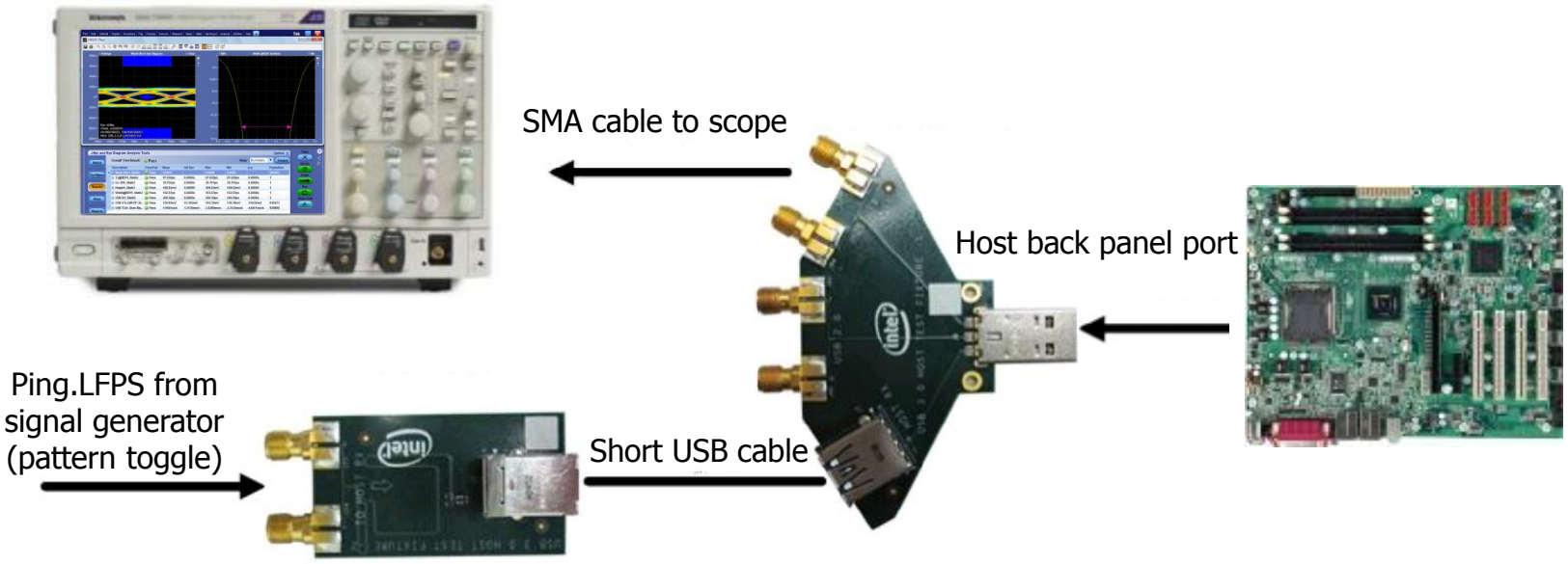
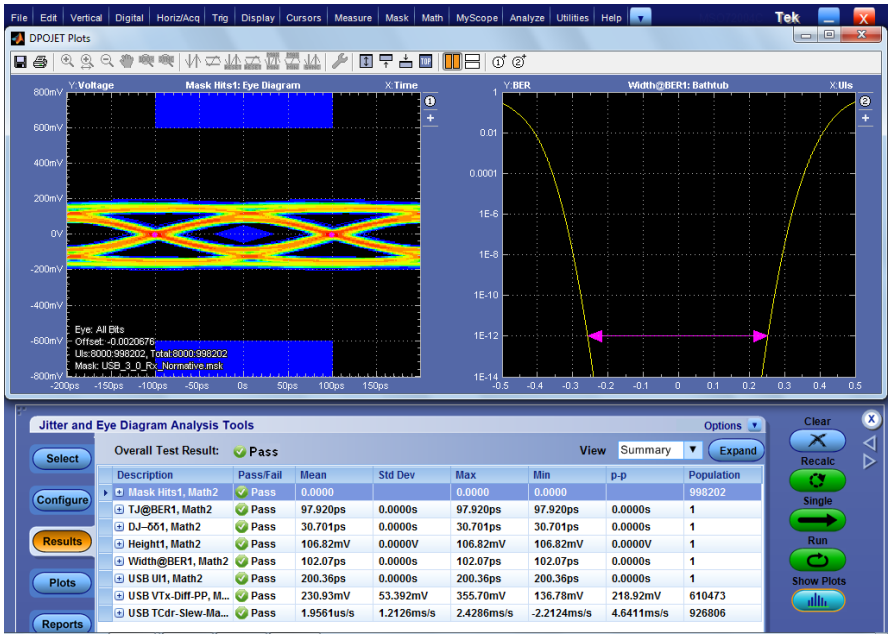
Example Host Test Setup



Voltage and Timing

- Tj – Dual Dirac at 10–12 BER
- Tx Deterministic Jitter – Dual Dirac
- Tx Random Jitter – Dual Dirac
- Differential p-p Tx Voltage Swing
- Transmitter Eye – Dual Dirac@BER
- Eye Width@BER
- Eye Mask Hits



LFPS TX Measurements

- LFPS signaling is critical for establishing link communication
- LFPS TX test verify common mode, voltage, tPeriod, tBurst, tRepeat
- Channel is not embedded for LFPS tests

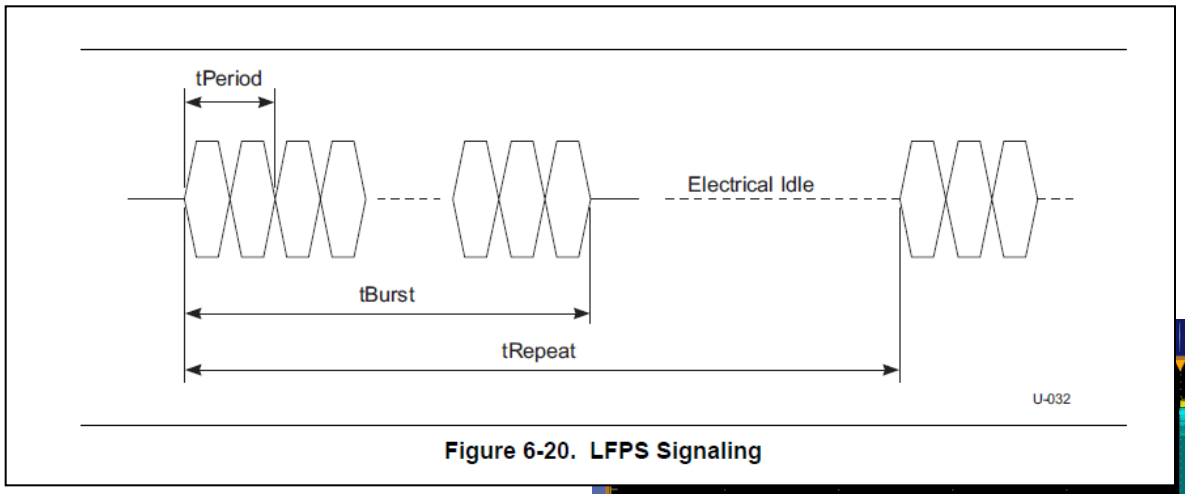
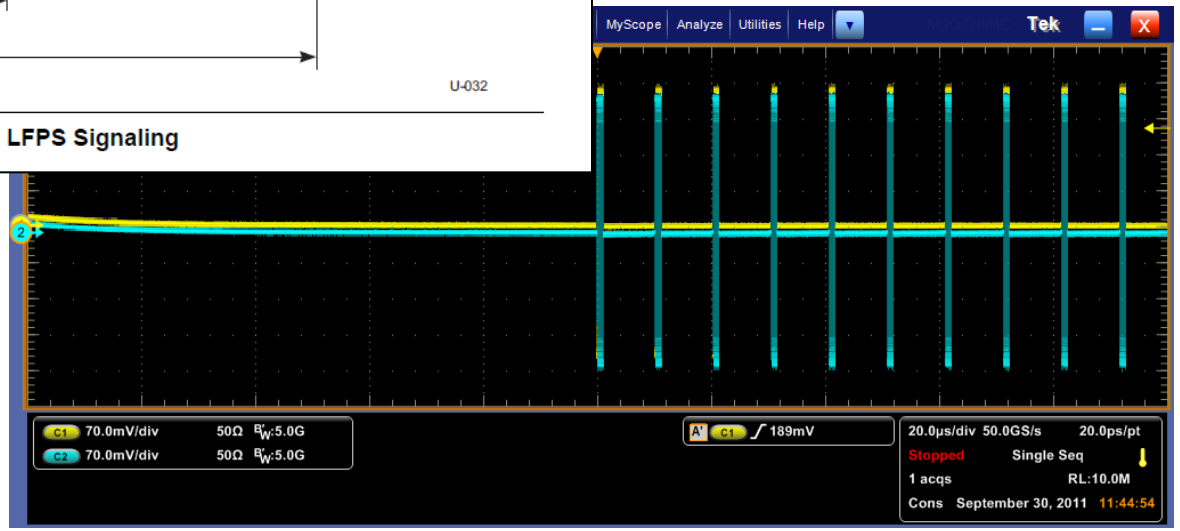
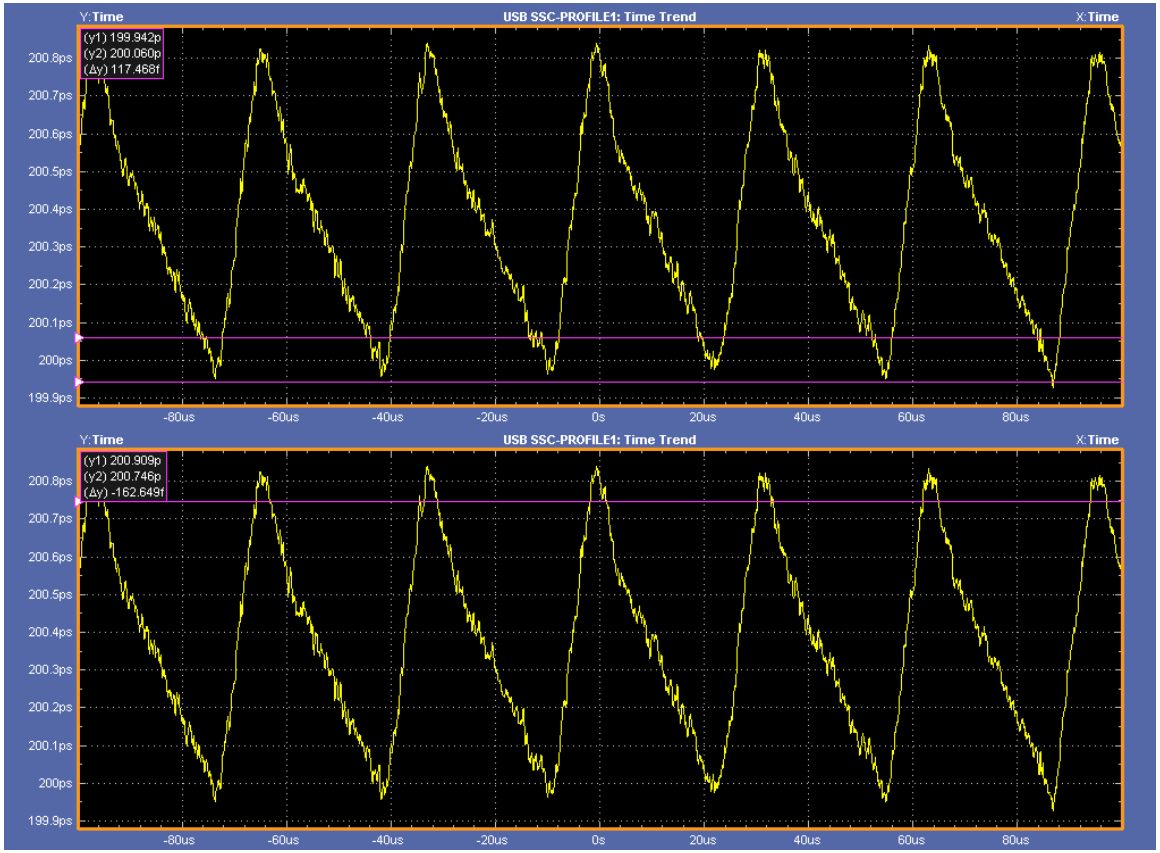


Figure 6-20. LFPS Signaling



SSC Measurements

- Both Maximum and Minimum Frequency Deviation must be considered
  - Assume nominal UI of 200ps
  - Limits are +0/-4000ppm and +0/-5000ppm, plus +/- 300ppm for ref clock accuracy
- Compliance Channel is not embedded for SSC measurements



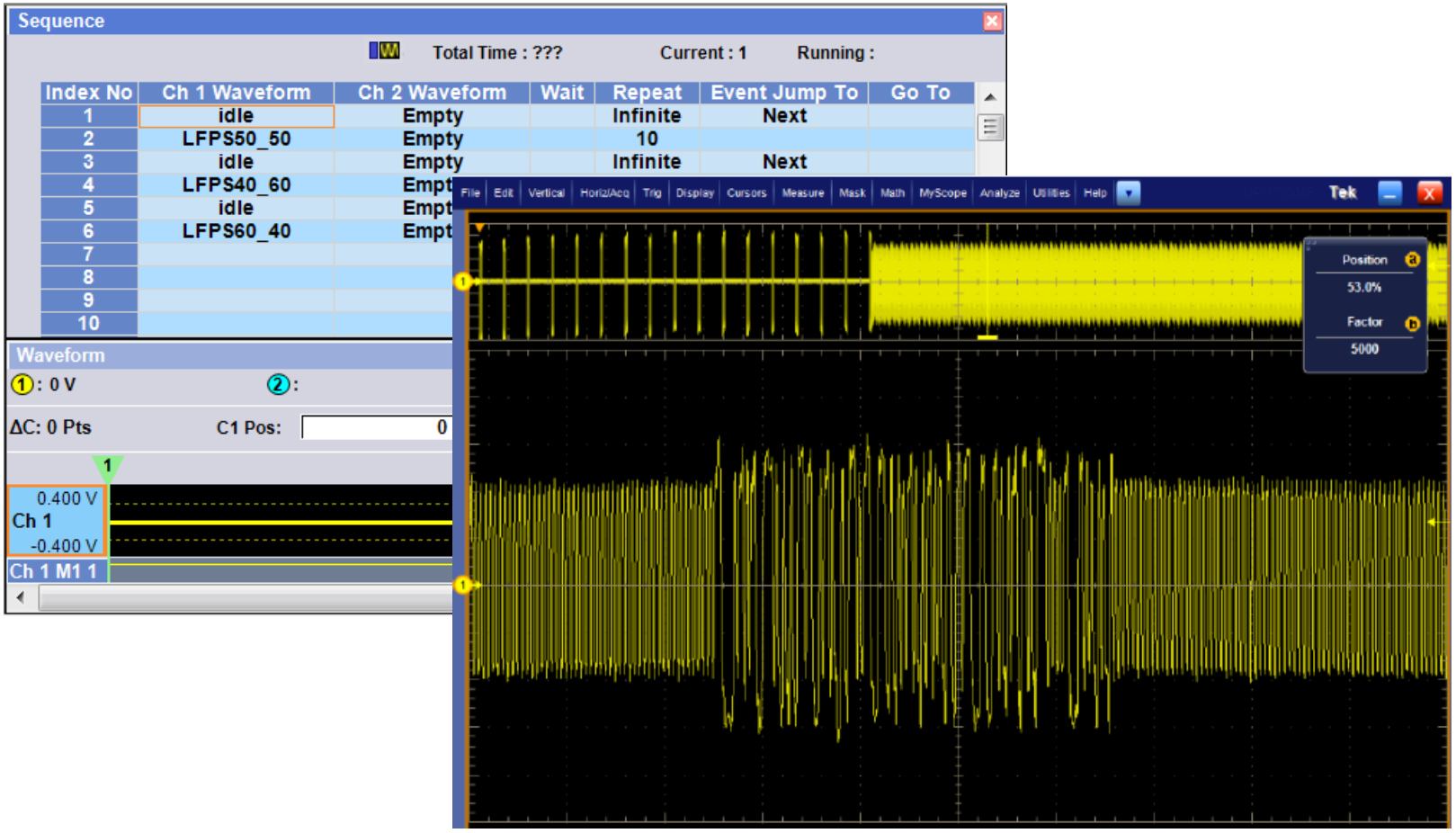
LFPS RX Test

- Required Compliance Test to verify that the DUT RX will respond to LFPS signaling
- Test is ran across four different settings

tPeriod	VTX-DIFF-PP-LFPS	Duty Cycle
50ns	800mV	50%
50ns	1000mV	40%
50ns	1000mV	60%
50ns	1200mV	50%

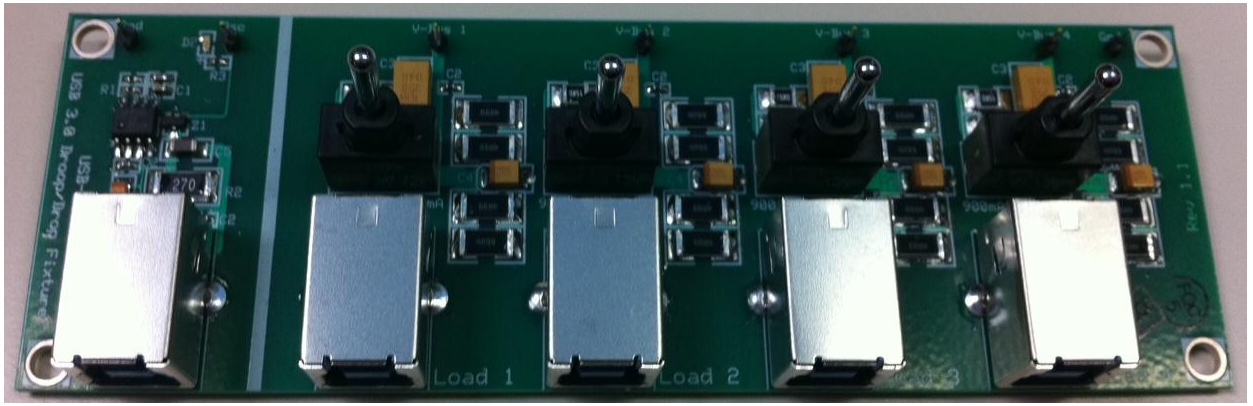
LFPS RX Test

- AWG generates spec compliant LFPS signaling
- Validate LFPS response with RT Scope



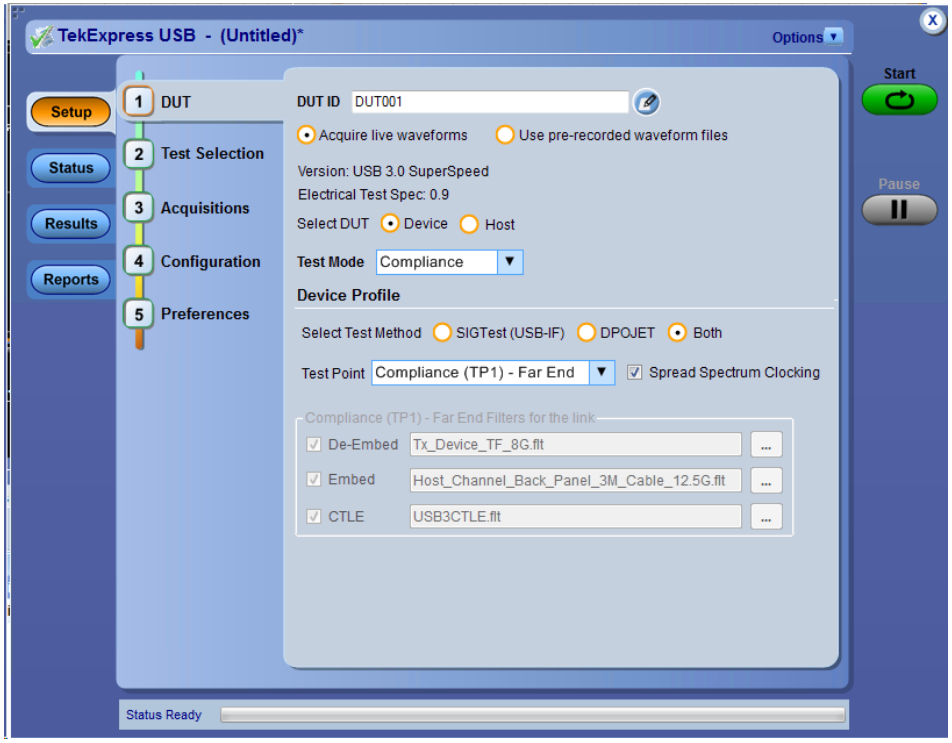
USB 3.0 Droop / Drop Test

- New Test Fixture Available from USB-IF
  - Provides 150mA / 900mA load
  - Previous fixture provides 100mA / 500mA load
- Amount of power drawn is changed from 500mA to 900mA for high power devices
- Fixture is orderable at: http://www.usb.org/developers/estoreinfo/USB_product_order_form.pdf



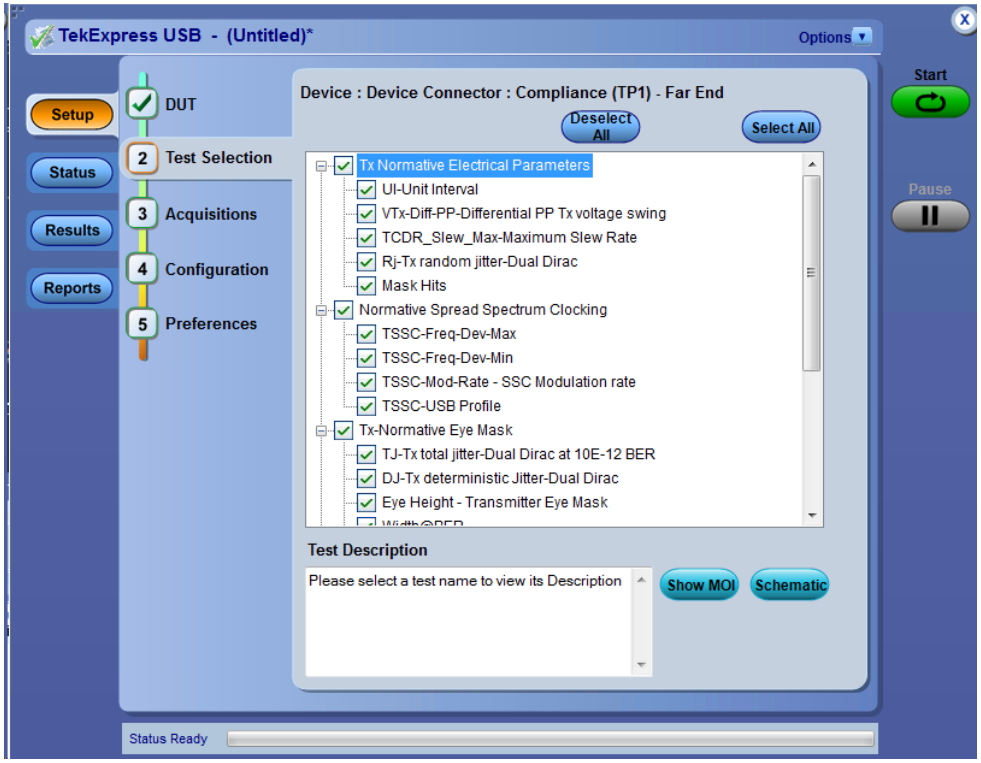
USB 3.0 Compliance and Automation

- Complete Automation of USB 3.0 Measurements with TekExpress
- No need to learn technology specific software applications- TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
- TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug



TekExpress USB 3.0 Automated Solution

- Supports testing for USB 3.0 Hosts and Devices
- Automatically selects the correct channel emulation filter when software is selected
- Easily select measurements of interest for test execution
- Supports all compliance and LFPS TX measurements
- User choice of algorithm execution- SigTest or DPOJET
- Automates DUT toggling to acquire CP0, CP1, and LFPS Patterns

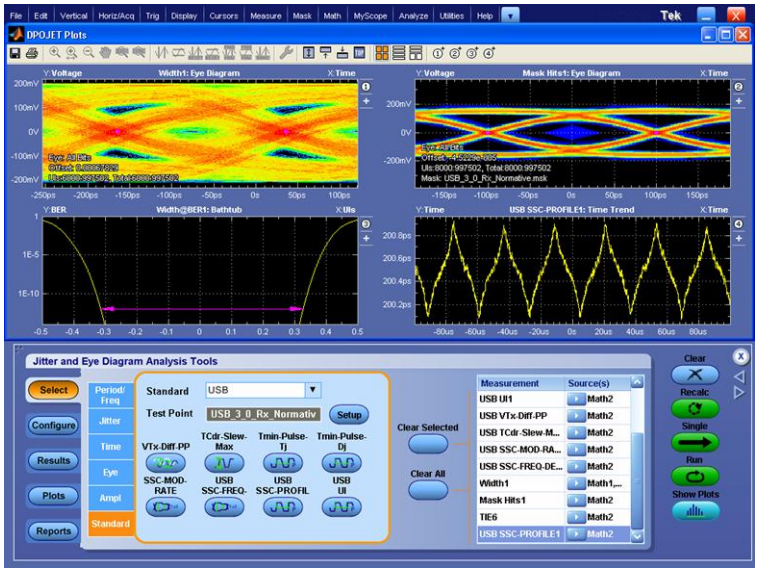


Complete USB 3.0 Transmitter Solution

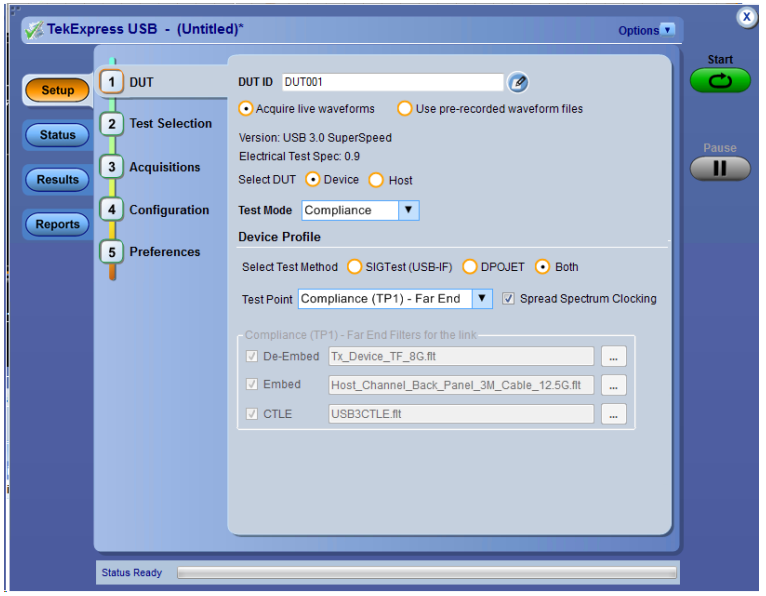
DPO/DSA70000 Series Oscilloscopes

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures
- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)
- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50 GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

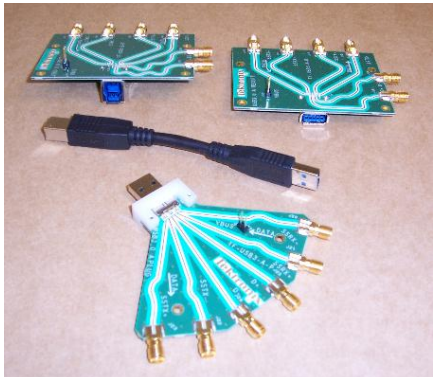
Opt. USB3



Opt. USB-TX



TF-USB3-AB-KIT



NEW Debug and Analysis Tools

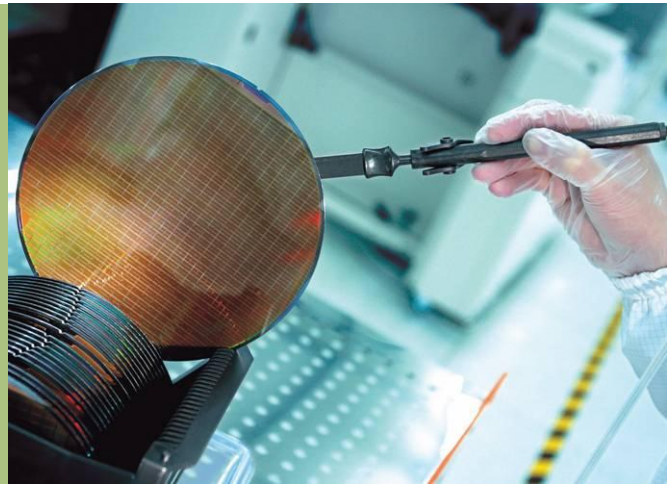
- USB3 Decode with Hierarchal Bus display
- Includes Digital, 8b10b, PHY, LINK, and Transaction layers
- Enables decode, search and trigger, available with option SR-USB

Decode and Trigger Examples

USB3 Link Training

USB3 Trigger Setup

USB 3.0 Receiver Testing



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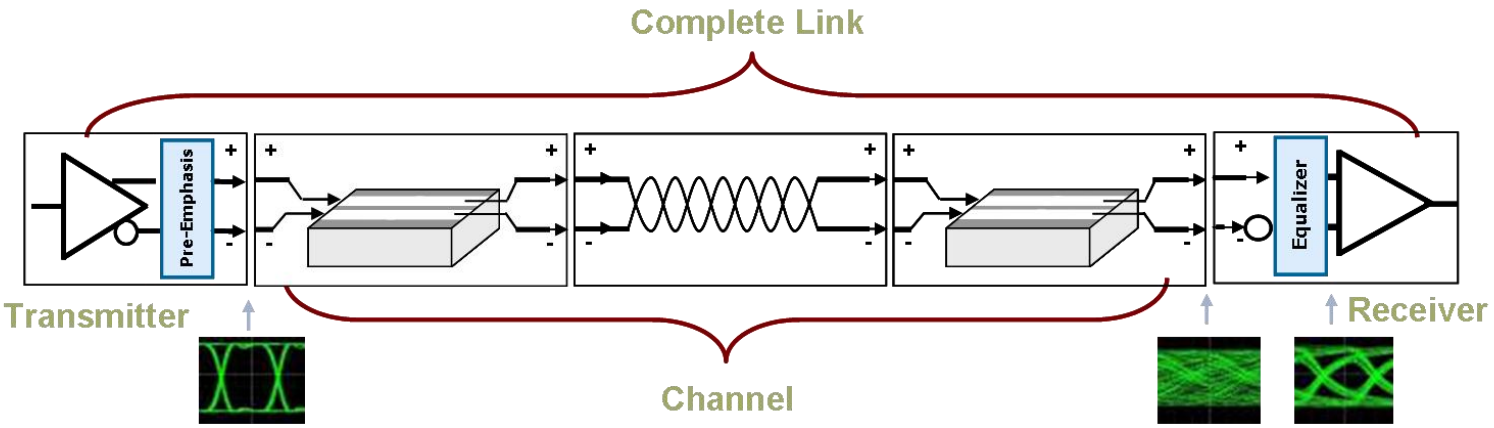
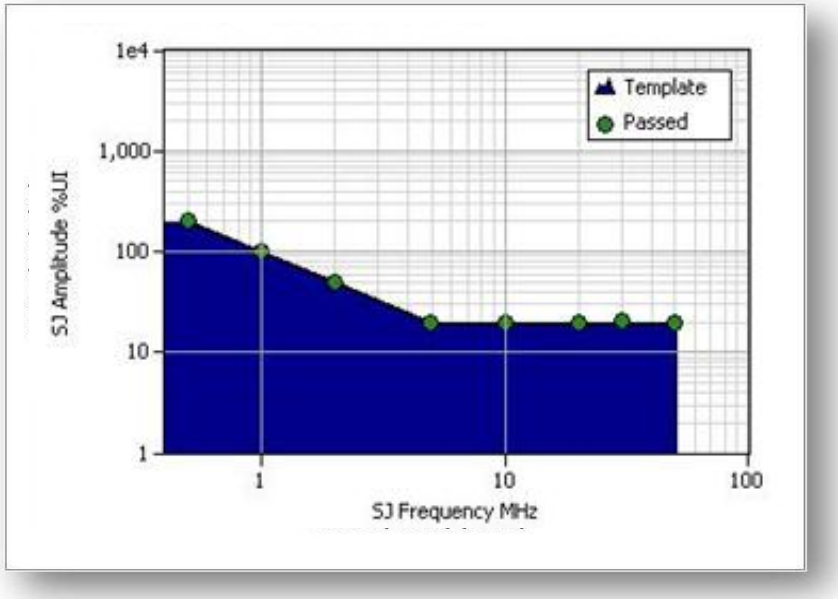
USB 3.0 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions



USB 3.0 Compliance Receiver Tolerance Test Overview

- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- De-Emphasis Level is set to -3dB
- Amplitude at the end of the compliance channel: 180mV Hosts and 145mV Devices
- Each SJ term in the table below is tested one at a time after the device is in loopback mode



Frequency	SJ	RJ
500kHz	400ps	2.42ps RMS
1MHz	200ps	2.42ps RMS
2MHz	100ps	2.42ps RMS
4.9MHz	40ps	2.42ps RMS
10MHz	40ps	2.42ps RMS
20MHz	40ps	2.42ps RMS
33MHz	40ps	2.42ps RMS
50MHz	40ps	2.42ps RMS

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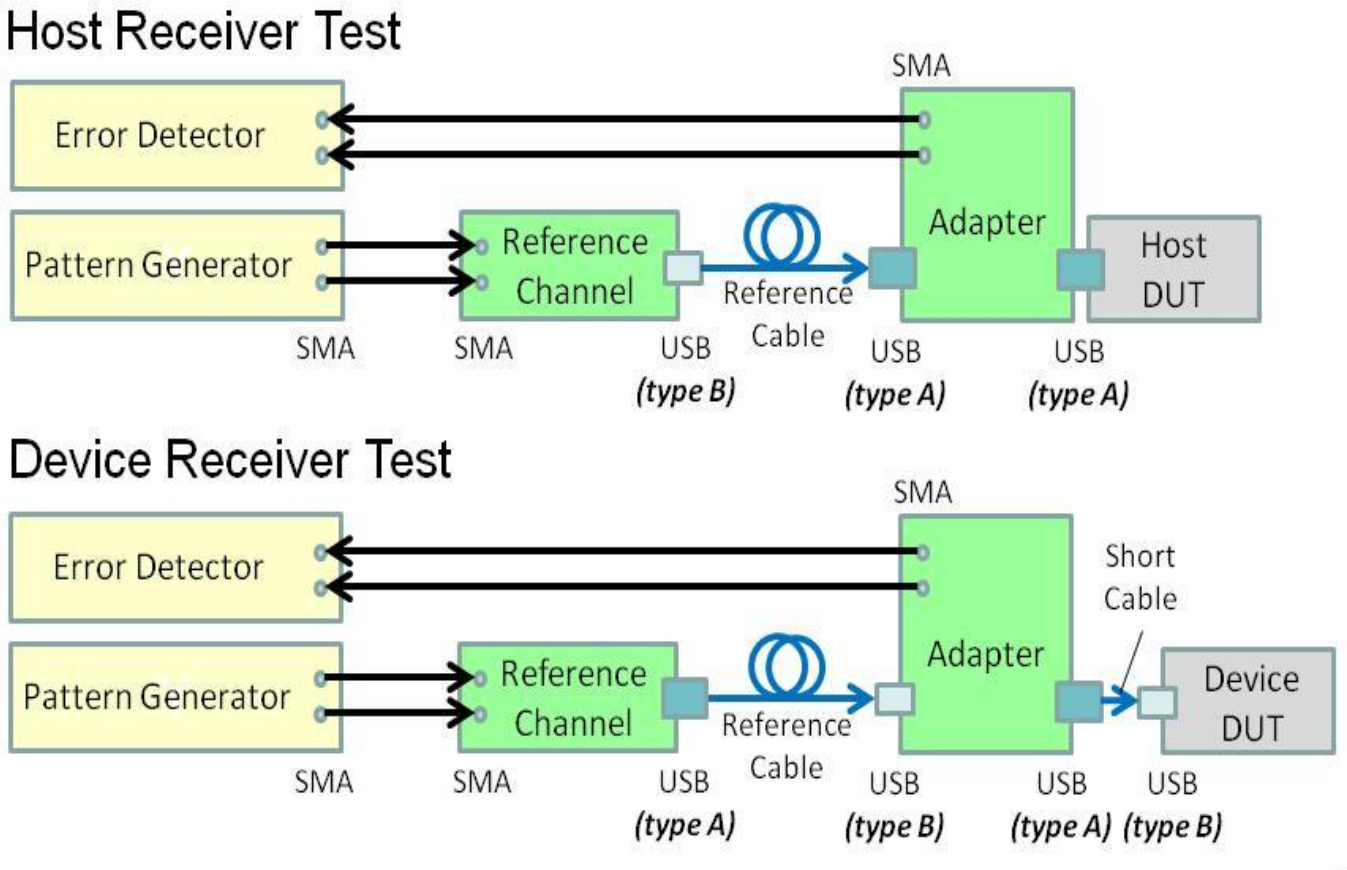
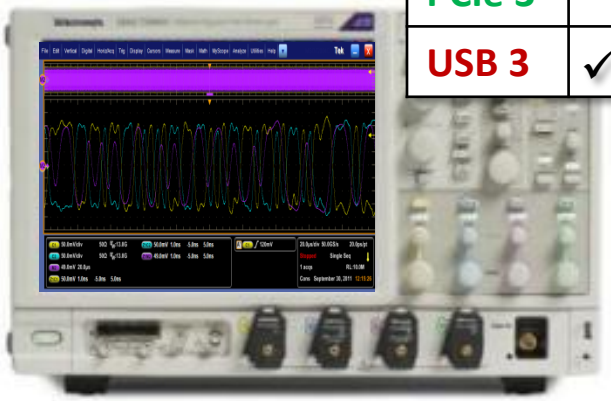
Generic USB 3.0 RX Test Configuration



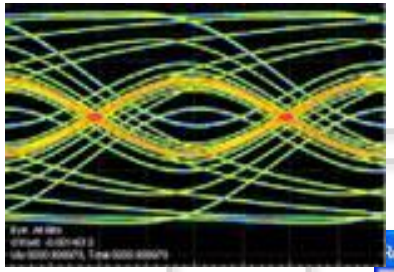
USB 3.0 Stress Recipe - Calibration

PCIe 3	
USB 3	✓

Long waveform **capture by Real Time Scope**



Tx Eq



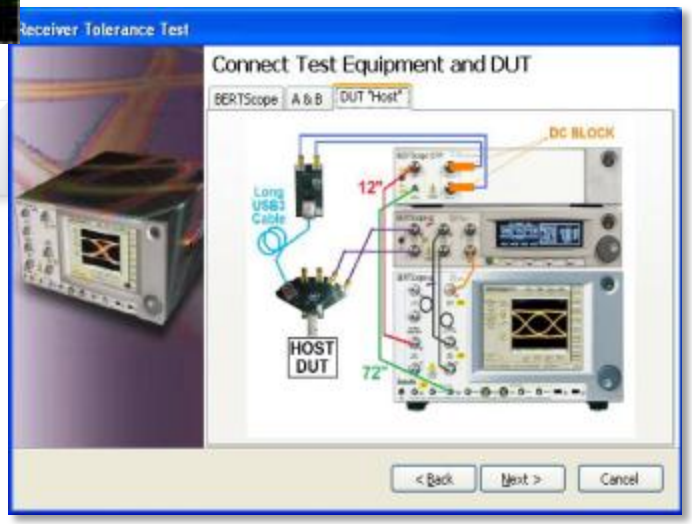
Channel

Test Equipment

SigTest Post-processing

RJ Source

SJ Source



Mature standard with **fully automated** solutions for stress calibration and **good correlation**

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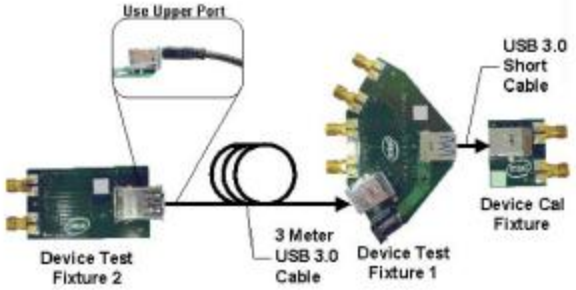
USB 3.0 Calibration

- **Host Calibration Setup**

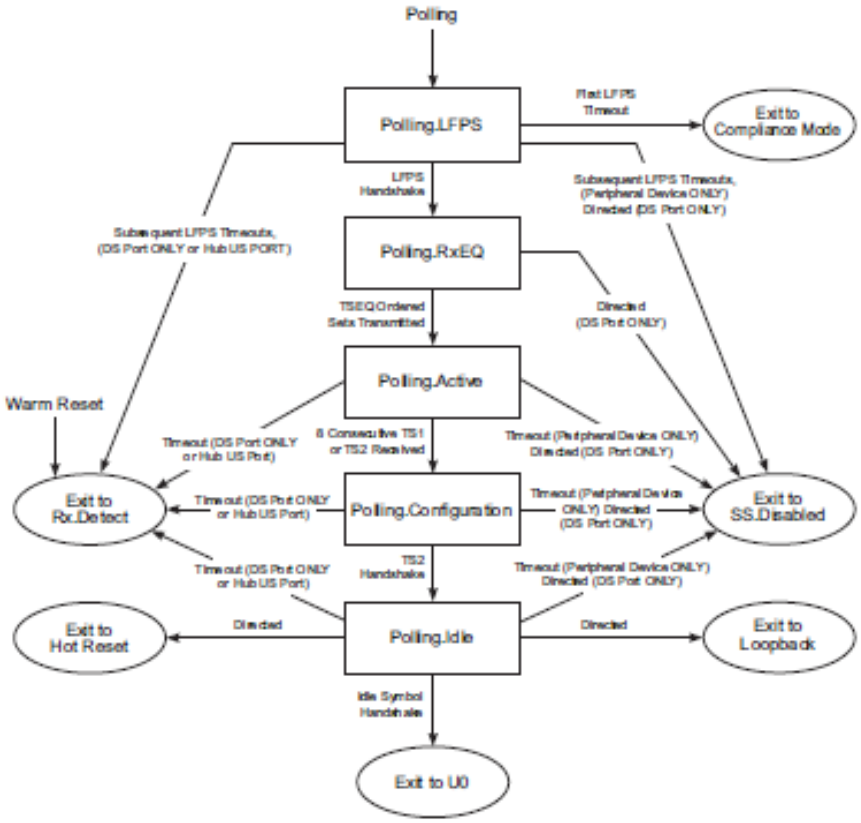
- **Device Calibration Setup**



- **Calibration Procedure**
  - ✓ Connect signal source directly to scope
  - ✓ Calibrate de-emphasis to 3.0 dB + 5/-0% dB using CP0 with SSC off and CTLE off
  - ✓ Connect signal source through the compliance channel
  - ✓ Measured peak to peak TJ
  - ✓ Calibrate RJ(2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10-10) with CP1 at the end of the channel applying CTLE and JTF
  - ✓ Calibrate SJ using CP0 until measured peak to peak TJ increases by that amount. Apply CTLE and set JTF at 50Khz.
  - ✓ Expected Tj with jitter off should be less than 100 ps. If this threshold is exceeded, replace the channel fixture(s) and/or cable(s).

USB 3 Loopback Negotiation

- **RX Detect**
  - SuperSpeed Link Partner is Availability is determined
- **Polling.LFPS**
  - DUT and Generator Send LFPS and establishes LFPS Handshake
- **Polling.RxEQ**
  - DUT and Generator send TSEQ in order to establish DUT RX Equalization Settings
- **Polling.Active**
  - DUT and Generator send 8 TS1
- **Polling.Configuration**
  - Generator instructs DUT to loopback by setting the loopback bit in the TS2 training sequence
- **Polling.Idle**
  - DUT directed to Loopback



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Two Solutions for USB 3.0 Receiver Testing

BERTScope BSA85C and AWG7122C

- **Tektronix has the right solution to meet your needs**
  - Both provide fully automated Receiver Compliance and Jitter Tolerance Testing
  - Both offer advanced impairments to debug problems caused by SSC or other anomalies
  - Both support a wide range of HSS Standards
  - Both support asynchronous clocking (SKP order set rejection)
- **BERTScope**
  - Performance that you need up to 26Gb/s for next generations standards including DisplayPort 1.2, SATA/SAS, 10G KR, PCI Express 3.0
  - Impairments can be changed on the fly to see the effect of increasing or reducing jitter
  - Debug and analysis tools enable quick identification of RX errors
  - True BER measurements
- **Arbitrary Waveform Generator**
  - Common platform for MIPI, HDMI, USB 3.0, and SATA
  - Only solution available that provides a common setup between transmitter and receiver testing without the need of RF switches and additional setup complexity
  - Easily apply sparameter models to verify designs under different channel conditions without the need of physical ISI channels
  - Generate SJ > 1Ghz to debug elusive problems caused by other system clocks

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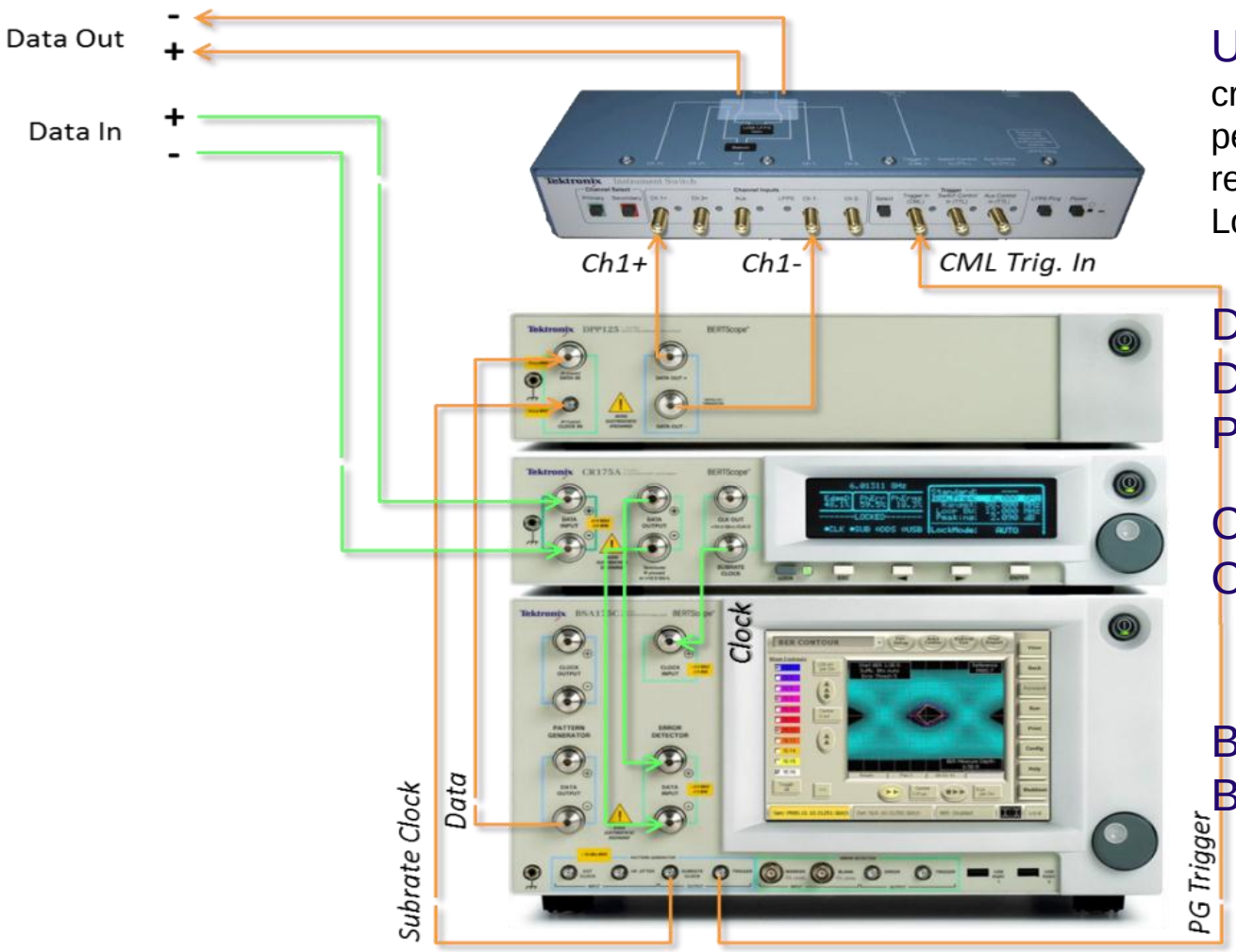
BERTScope USB 3.0 RX Test Configuration



USB Switch
creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

DPP125B
De-emphasis Processor

CR125A
Clock Recovery

BSA85C
BERTScope

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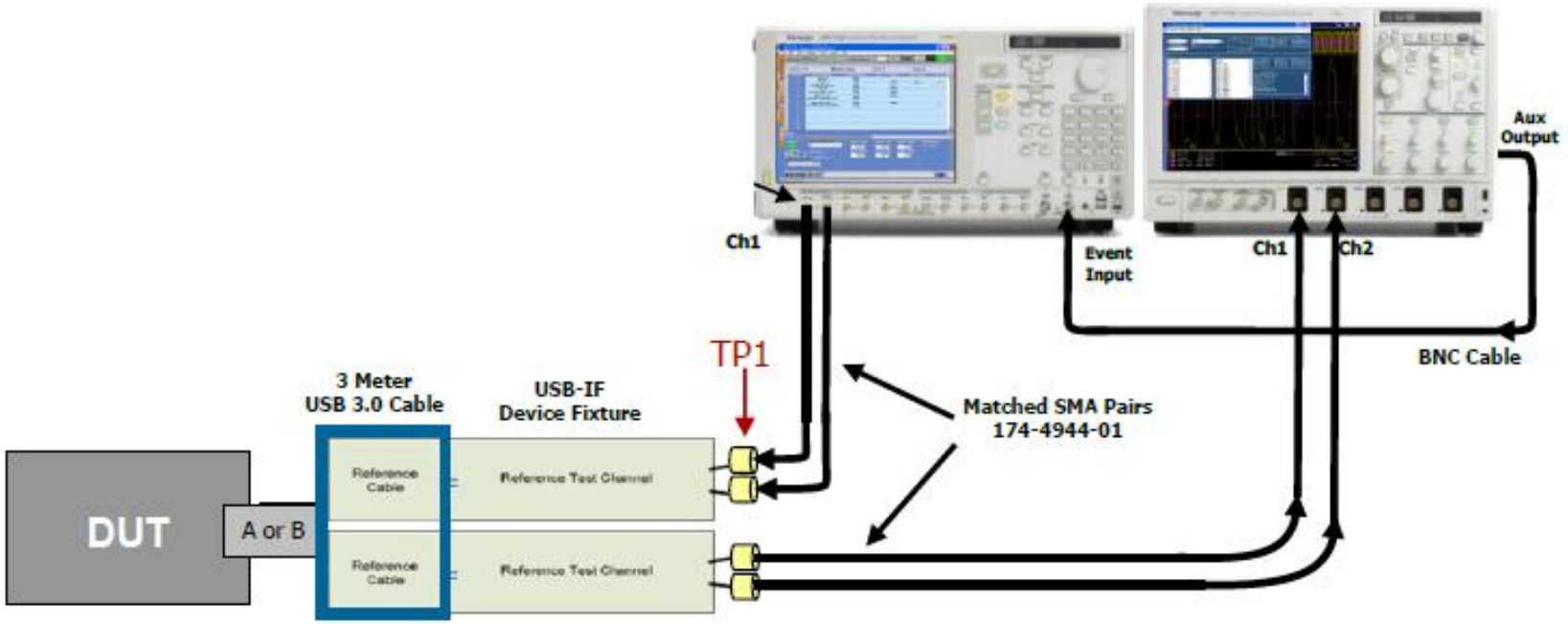
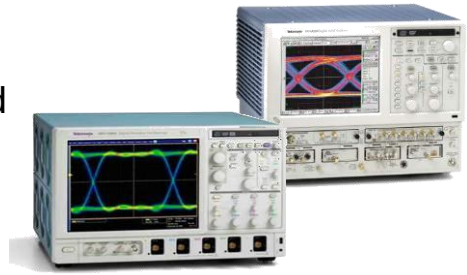
AWG USB 3.0 RX/TX Test Configuration

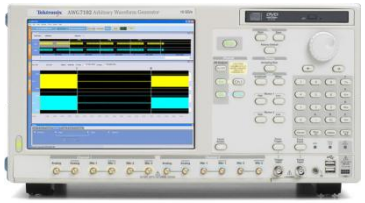
- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)



Tektronix USB 3.0 Summary

- **Complete**
  - Solutions available today for USB3.0 Transmitter, Cable, Channel, and Receiver Testing
- **More than a Compliance Solution**
  - Solutions to meet debugging, characterization, and compliance needs
  - Receiver stresses that go beyond compliance
- **Increased Productivity**
  - Fully automated transmitter and receiver test solutions
  - Analysis tools integrated on the BERTScope enable the isolation and root cause determination of receiver errors
- **Performance**
  - 26Gb/s BERTScope provides coverage for next generation testing needs Low noise floor enables measurements of small data eyes for compliance testing and receiver calibration
  - Only 6.25Gb/s hardware serial trigger to capture protocol events that are causing failures or interoperability problems
- **Expertise**
  - Actively engaged in the USB Working Groups
  - Regional support by Tektronix Application Engineering Experts





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Resources

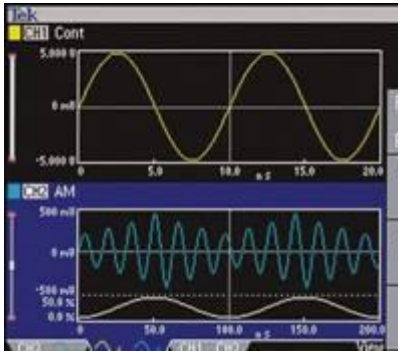
Extensive application information at:

www.tek.com
USB: **USB-IF,** www.usb.org

Resources

- Access to Specifications
  - Rev 1.0, http://www.usb.org/developers/docs/
- Tektronix USB Electrical PHY Tools and MOI's
  - www.tektronix.com/usb
  - www.tektronix.com/software

Introduction to USB 3.0 SuperSpeedPlus



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Disclaimer

Presentation Disclaimer: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of USB-IF or other member companies.

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Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging
- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture
- **USB 3.0, 10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation

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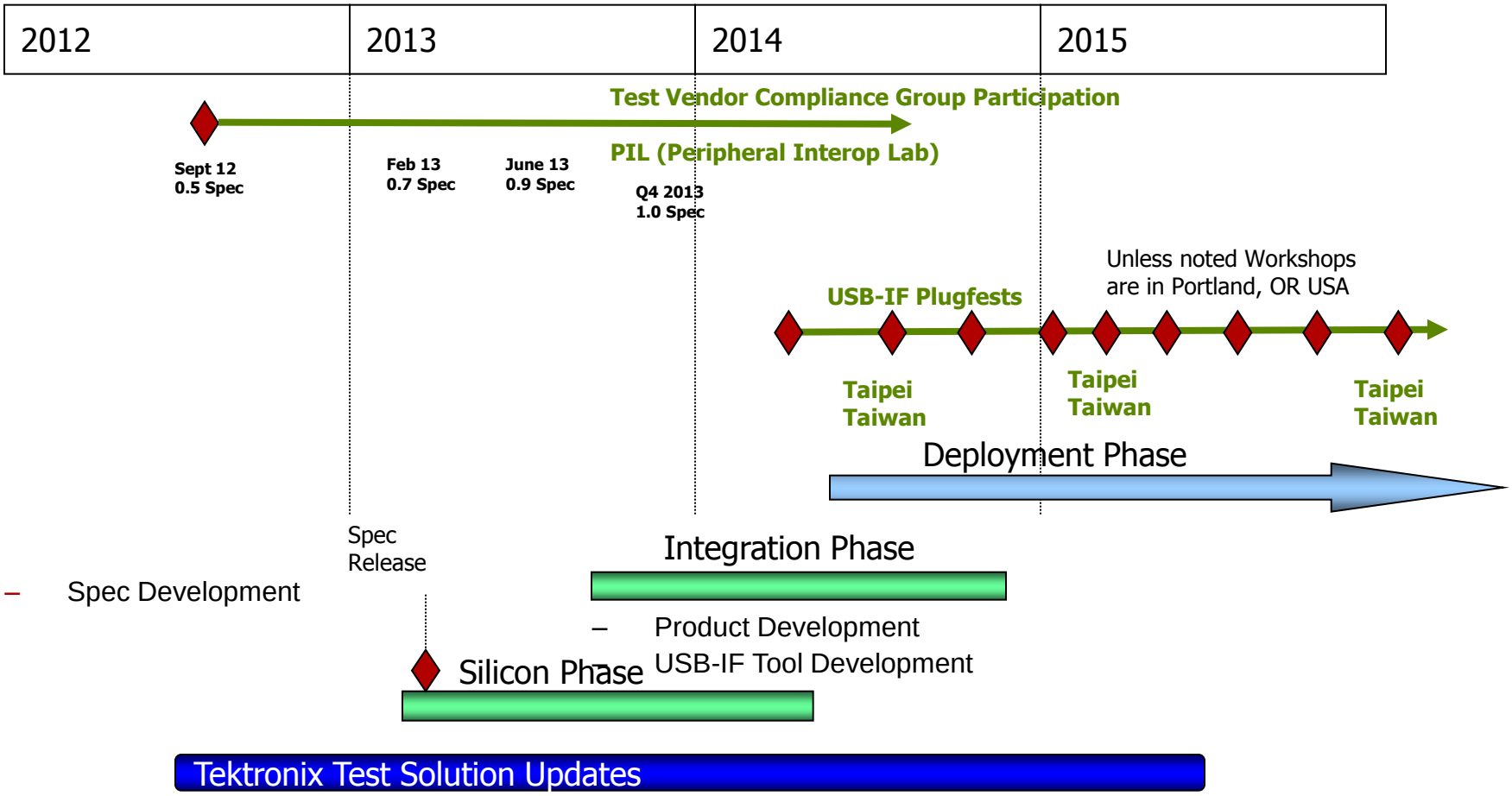
USB 3.0 SuperSpeedPlus Technology Timeline



Transmitter, Receiver, Channel

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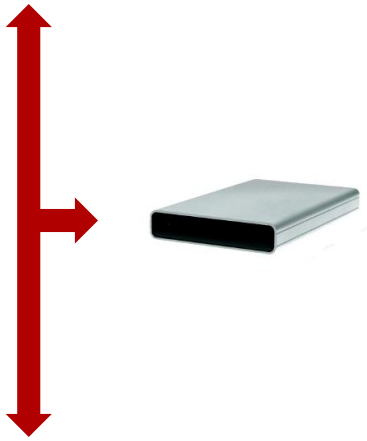
Why 10 Gb/s?

Video

- HD video adapters with multi display outputs
- Dual HDMI/DVI with simultaneous 1080p displays

Storage

- 5 Gb/s with 8b/10b -> 400 MB/s
- High performance SSD saturation-> ~600 MB/s



Hub/Dock

- Multi-function, ‘All in One’ docking
- Faster backups, multiple monitors, etc.

Naming convention

- SuperSpeed (SS) = 5 Gb/s
- SuperSpeedPlus (SSP) = 10 Gb/s

- Similar to other standards
  - Gen1 = 5G
  - Gen2 = 10G
  - GenX = 5G or 10G

- SS and SSP are qualifiers not names
  - E.g. SuperSpeedPlus device, host or hub

- Enhanced SuperSpeed = ≥ Gen1 speed
  - Reference for possible future higher data rate

5 Gb/s Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

6 Physical Layer

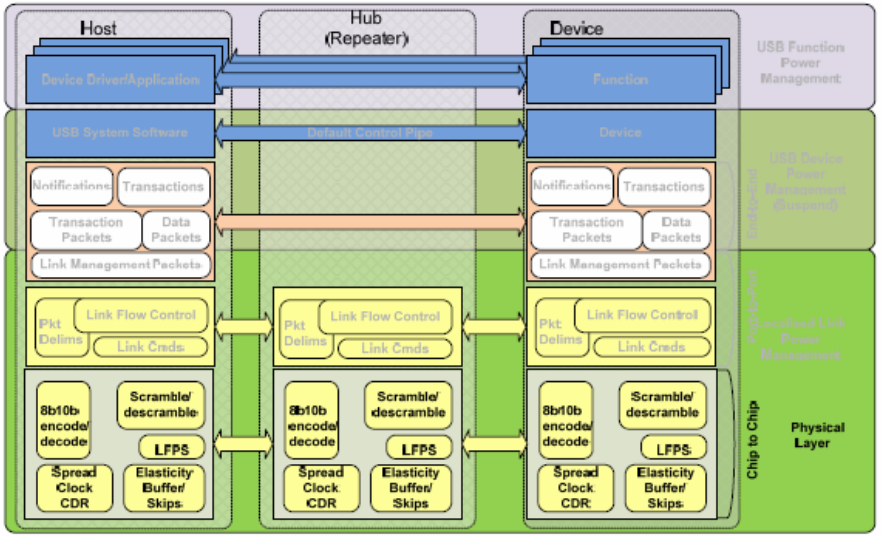


Figure 6-1. Super Speed Block Diagram: Physical

Source: USB 3.0 Rev 1.0 Specification

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USB 3.0 Comparison

	SuperSpeed	SuperSpeedPlus
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-20dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

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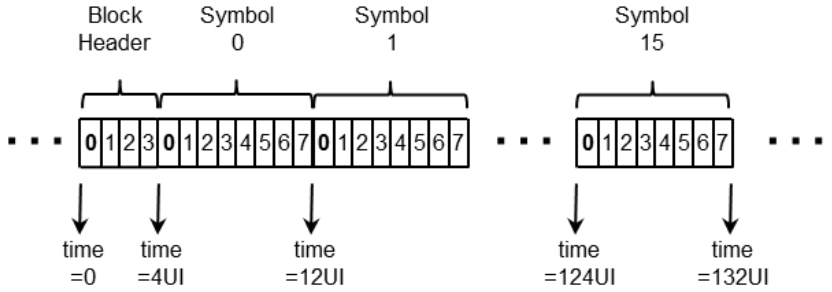
128b/132b Encoding and Compliance Patterns

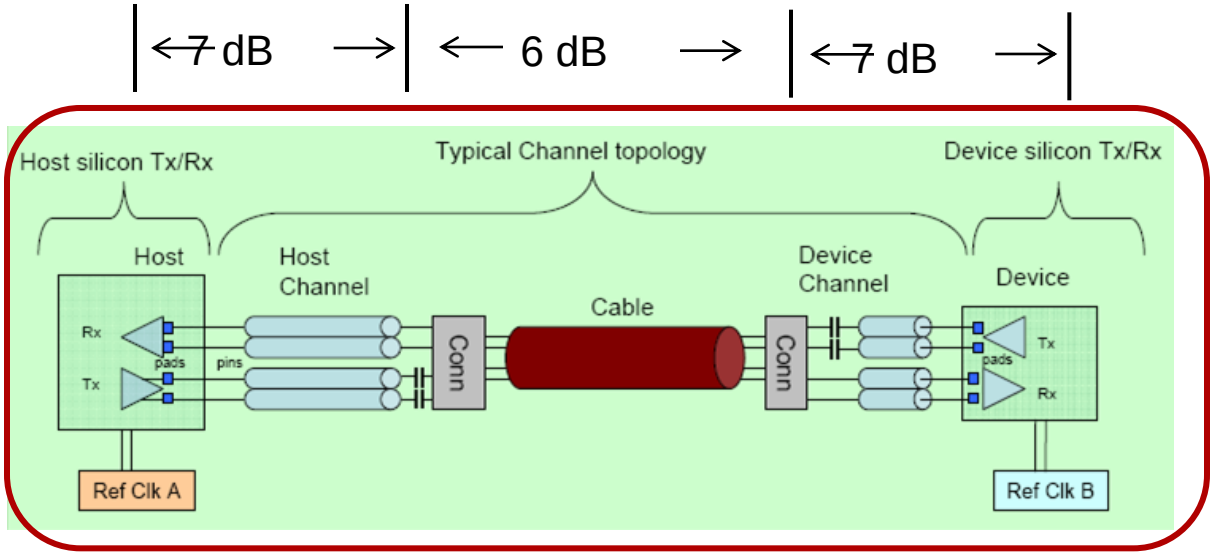
- 4-bit block header (0011 -> control, 1100 -> data)
- 128-bit (16 bytes) non-encoded payload
- Similar to PCI Express but with 4-bit header
  - 1 bit error (self correcting)
  - 2 bit error (detection)



- Higher order scrambler (X^{23} vs. X^{16})
  - Improves EQ training with long, rich pattern
- Compliance with scrambled data (00h) and Nyquist (Ah)
- Pattern toggle between Gen1 and Gen2
  - Order TBD

Channel Budget

- Target 20 dB (5 GHz) end-to-end loss budget
- Transmitter Equalization
  - < 3.5 dB (short channel), minimal loss profile
  - ≥ 3.5 dB (long channel), need Tx optimization
- Repeater may be required if host/device loss > 7 dB
- Tx/Rx compliance at TP1 (far end)

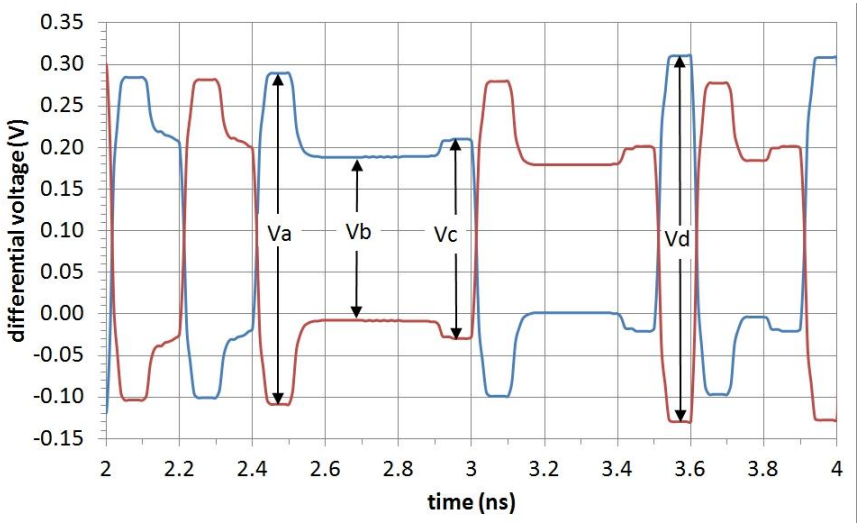


Source: USB 3.0 Rev 1.0 Specification

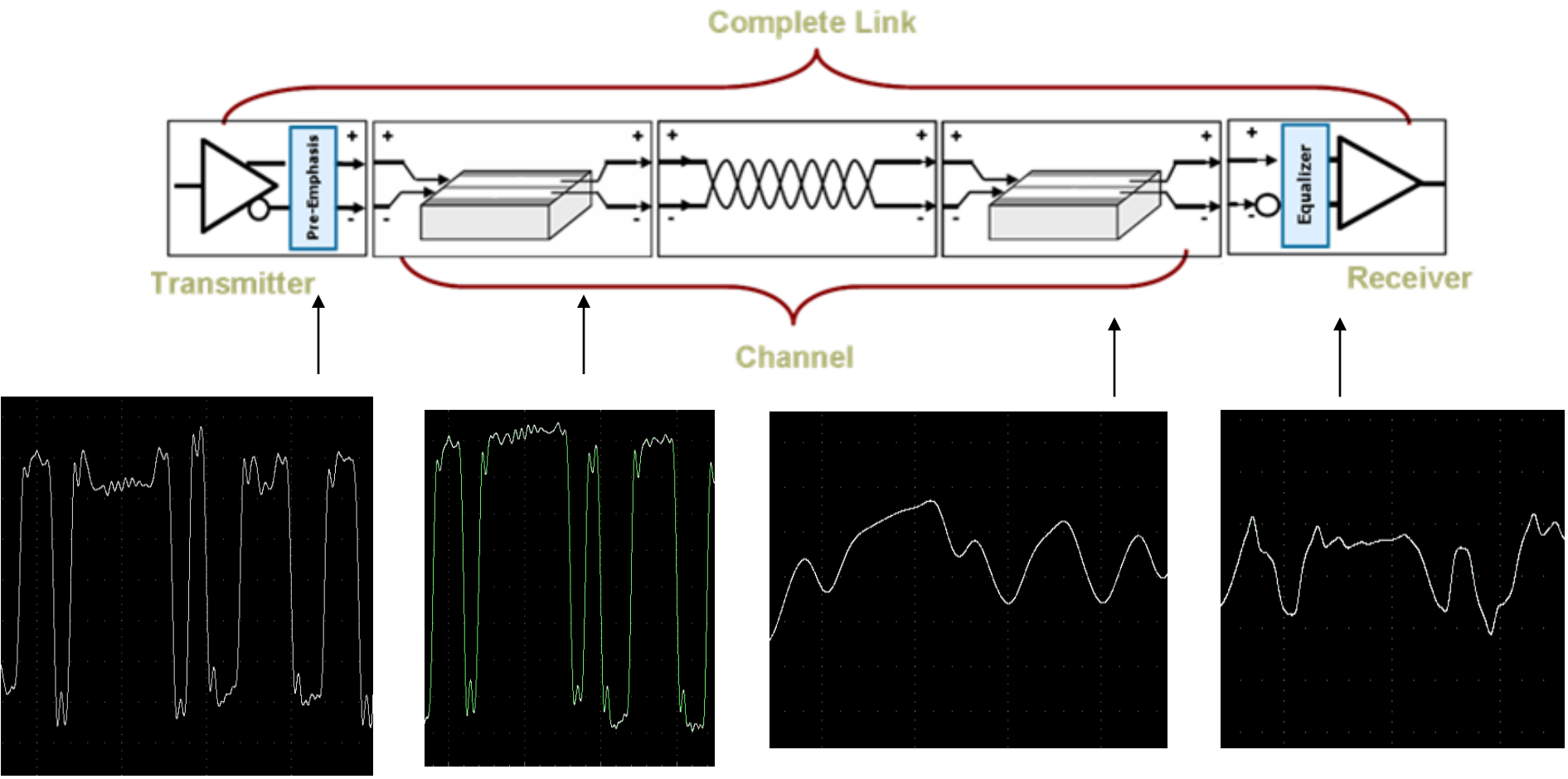
Reference Transmitter Equalization

- USB channel profiles are dynamic (consumer)
- Need flexible solution space for link optimization
- Below are recommended Tx settings for good margin with target reference channels

Host/Device Loss	<3.5dB	≥3.5dB
C_{-1}	0.000	-0.125
C_1	-0.100	-0.125
Va/Vd	1.00	0.80
Vb/Vd	0.75	0.55
Vd/Vd	0.75	0.75



End-to-end PHY Validation

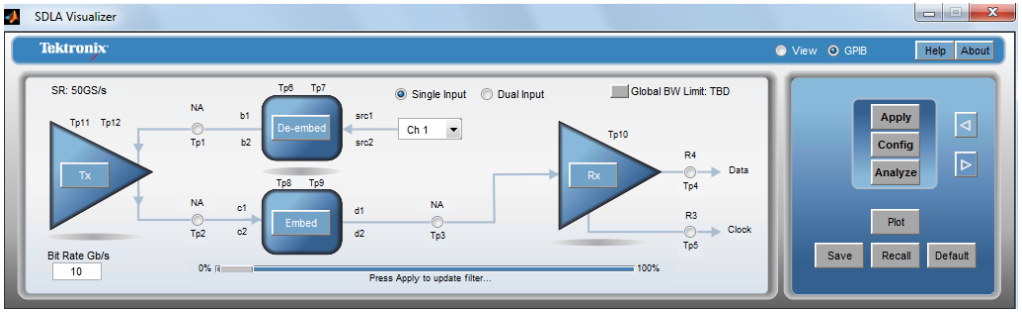


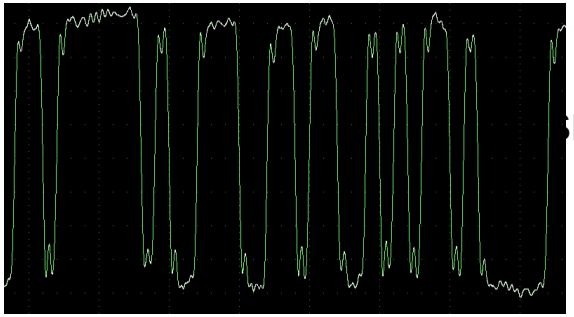
PHY Test Tools

- Similar process for USB 3.0 Gen1 Tx/Rx compliance testing
- Individual subsections (Tx, Rx, etc.) evaluated within system budget
  - ‘Far End’ Tx measurement including reference channels
- Next few slides outline current approach for electrical validation
- Let’s start with an example for Tx

Transmitter Validation Example - SDLA

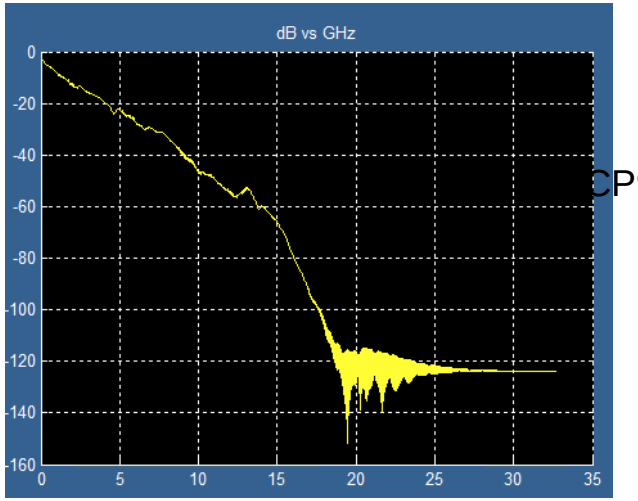
- Capture CP9 (Scr0) and CP10 (Ah)
- Input reference channel models

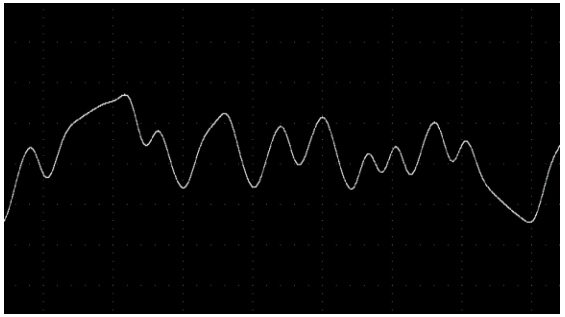




crambled Pattern (TP0)

B3 Reference Channel

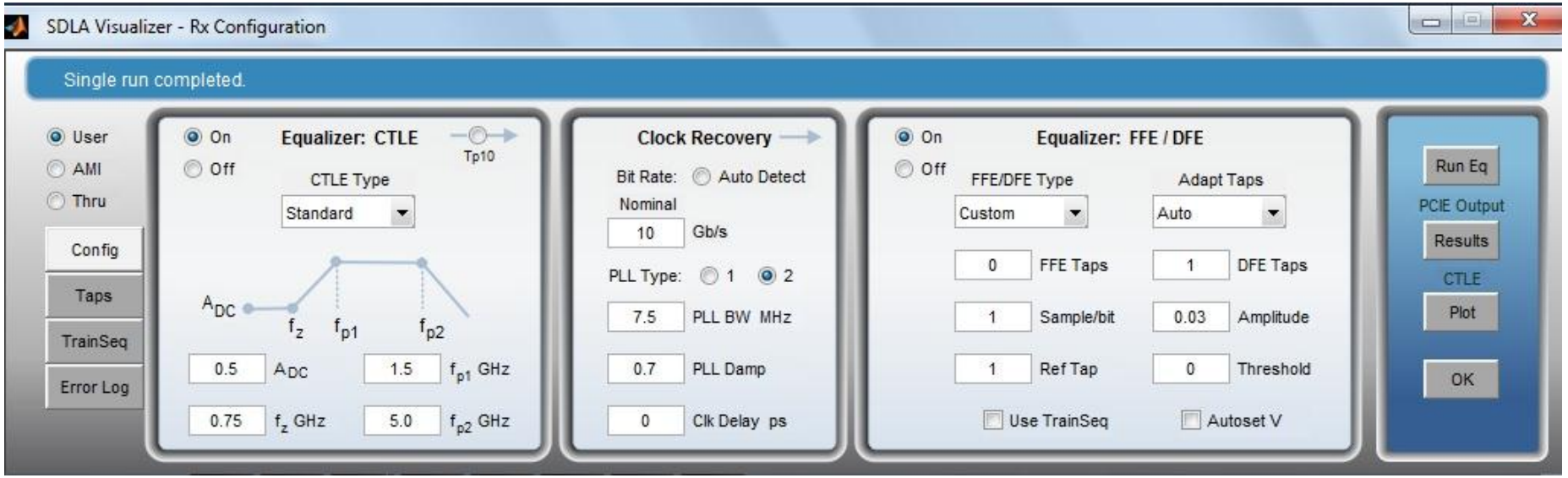


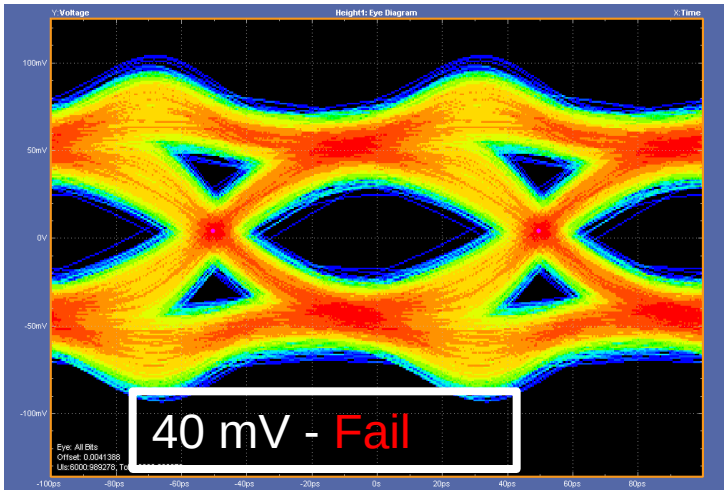


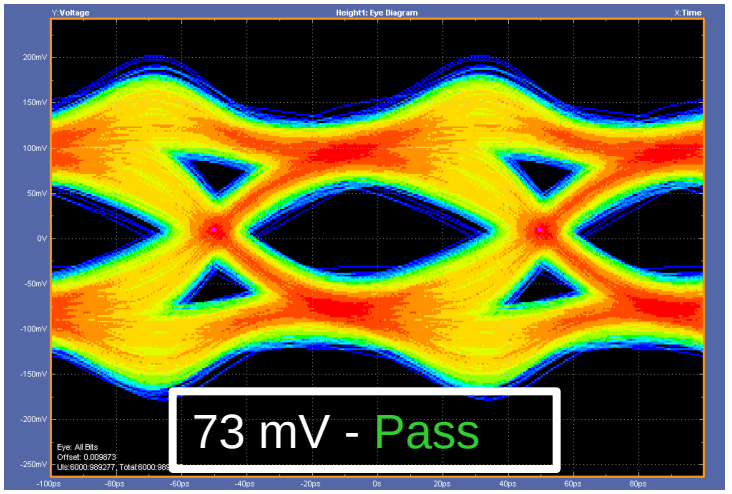
CP9 Scrambled Pattern (TP1)

Transmitter Validation Example - SDLA

- Find optimum Eye height vs. Rx EQ

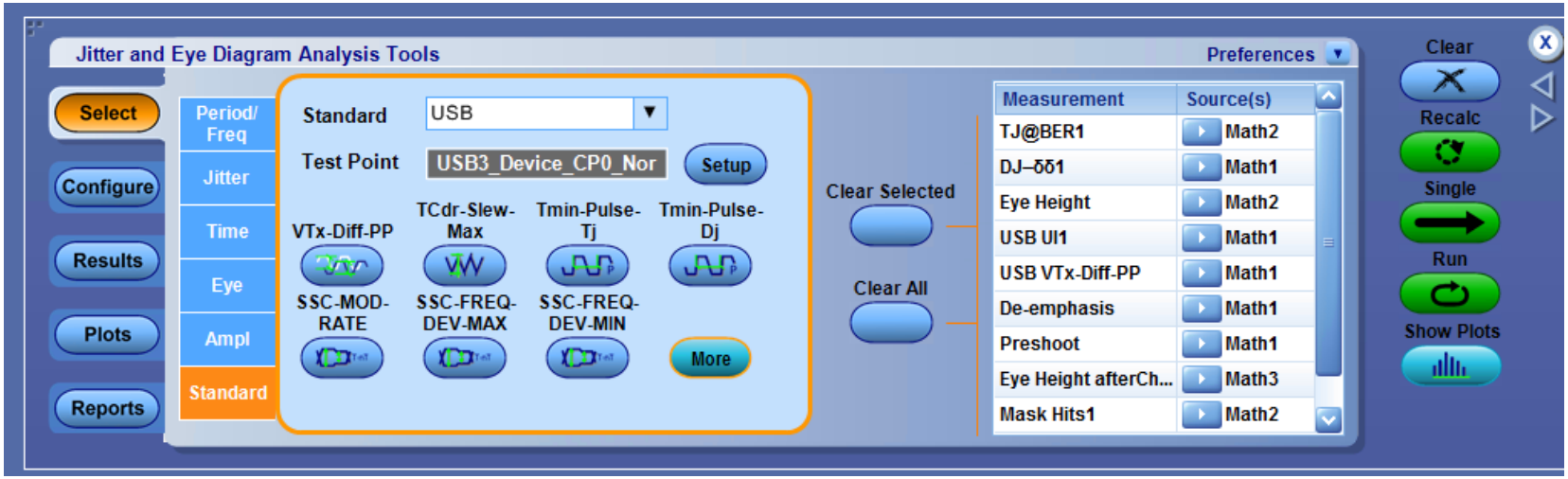




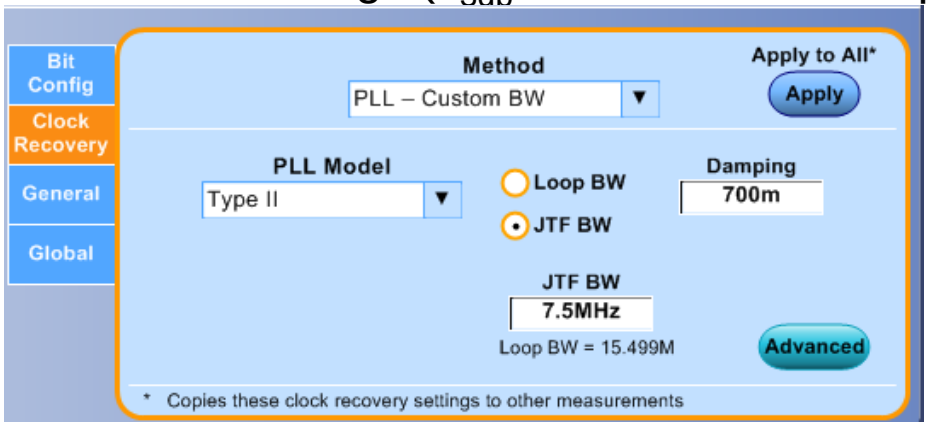


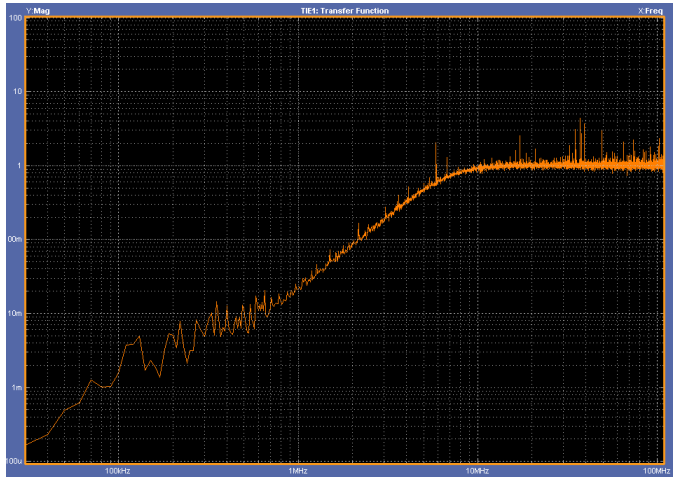
Transmitter Validation Example - DPOJET

- Recall DPOJET SSP setups



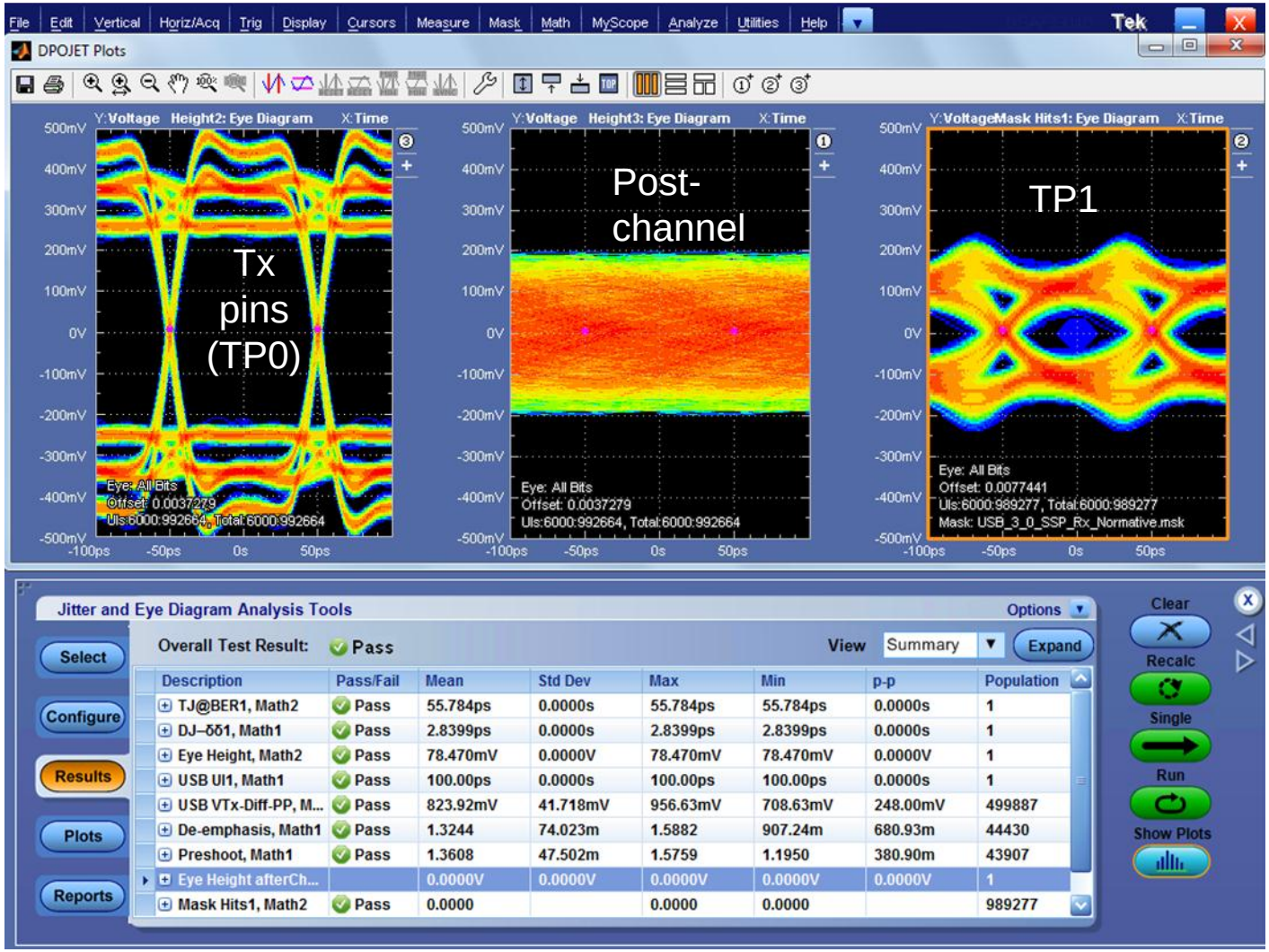
- Check JTF settings (f_{-3db} 7.5 MHz, 40dB slope)





Transmitter Validation Example - DPOJET

- Measure Eye height and jitter at TP1



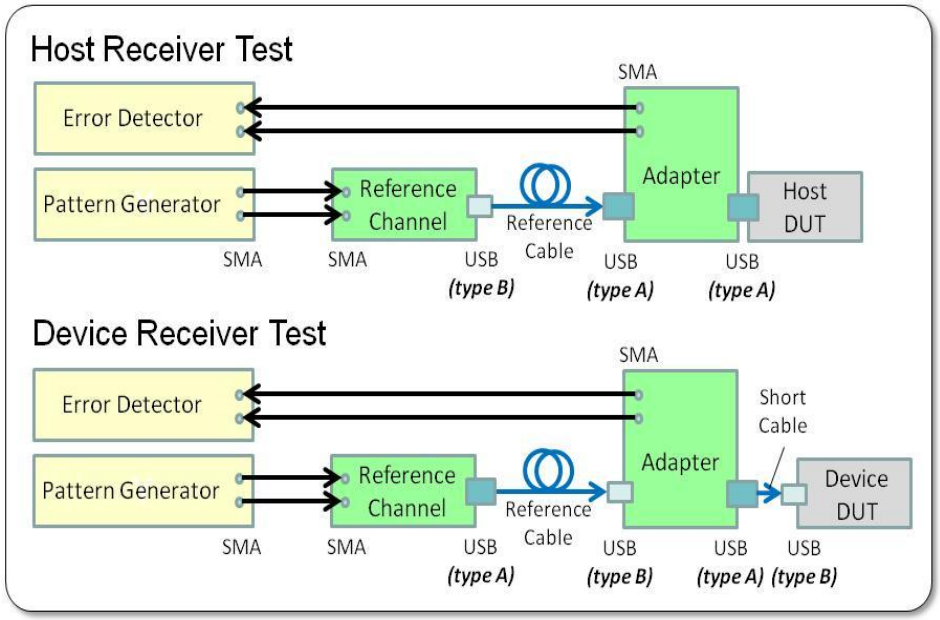
Recommended Transmitter Solution

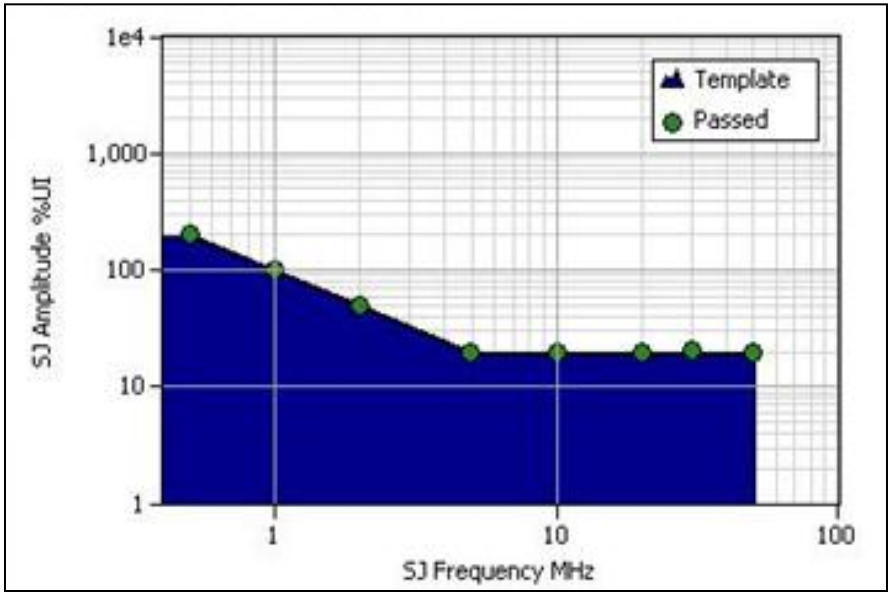
- ≥20 GHz BW, 100 GS/sec preferred
  - DSA72004C or higher recommended
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation. Increase memory depth if interpolation will be enabled, or if >1MUI captures are desired.
- Option DJA Advanced DPOJET required, signal analysis
- Option SLA Advanced SDLA required, cycle through 7 CTLE/1 DFE settings
- Option USB3 recommended, provides USB3 TX specific measurements

For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.

Receiver Testing

- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions





JTOL Template Comparison

Symbol	Parameter	Gen 1	Gen 2	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	.184	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	2.56	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	1.28	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.64	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.32	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	TBD	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.7 Post= -3.3	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-1

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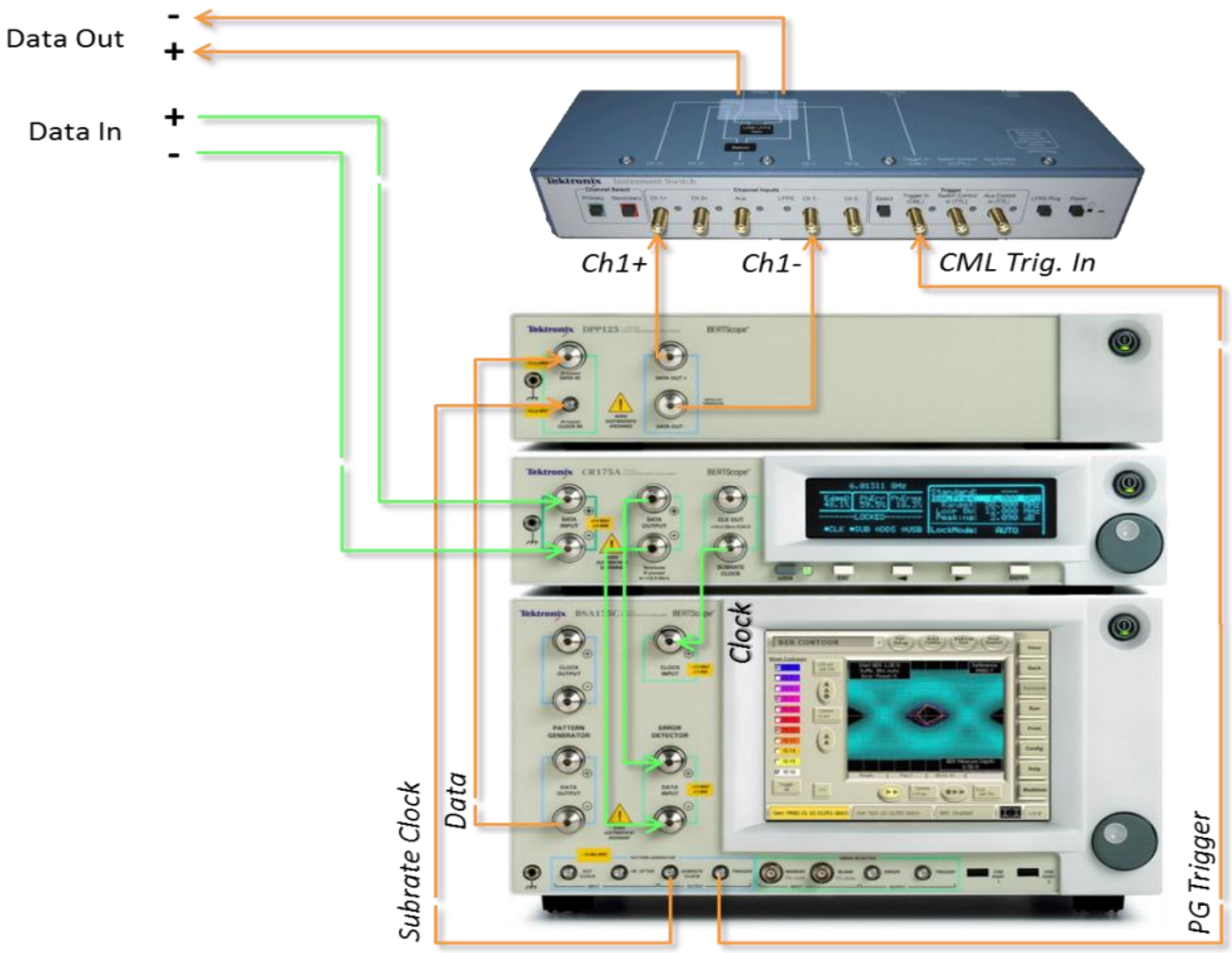
BERTScope USB 3.0 RX Test Configuration



USB Switch
creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

DPP125C
De-emphasis Processor

CR125A
Clock Recovery

BSA125C
BERTScope

Summary

- New opportunity for growth with USB 10 Gb/s
- Adds additional challenges beyond legacy requirements (backwards compatibility)
- Higher performance, more complex design but feasible within current infrastructure
- Extensive PHY validation tools for early designs
  - New USB SSP DPOJET setups for Tx validation
  - BERTScope USB library with JTOL templates
  - DSA8300 Sampling oscilloscope for channel characterization
  - Test procedures documented in Methods of Implementation (MOI)

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