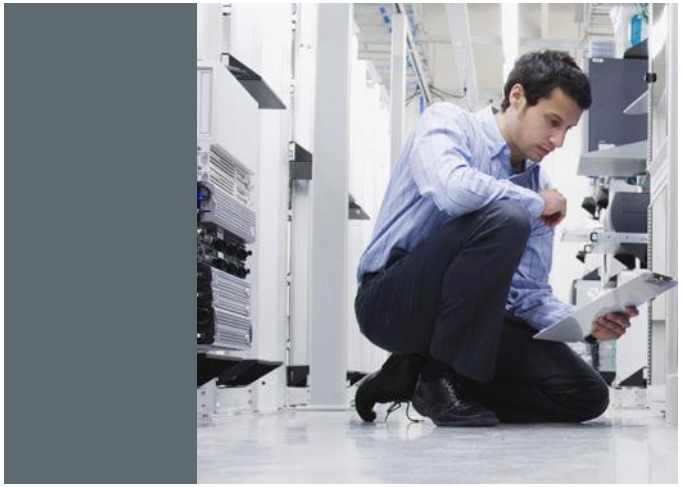
DisplayPort Solutions-Customer Presentation



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DisplayPort 1.2 Spec Update Agenda

- DisplayPort 1.2 Overview
- DisplayPort Transmitter Testing
  - What's New: T2, TP3, TP3EQ
  - Physical Layer Test Overview for DP1.2
    - Manual measurements / DPOJET / SDLA
    - CTLE required in Rx
  - DP-AUX: Control DUT parameters
    - Controls ALL TX. RX devices without vendor-specific control SW
- Test Automation:
  - Full Main Link testing with DP12 Automated tool set
  - DP 1.2 Tx:
    - Including Single-Ended and Diff Measurements (Intra-Pair Skew, AC Common Mode)
    - Using RF Switch Integration
    - Improved Debug Tools
- DisplayPort Sink/Receiver Testing
  - BSA125C configurations towards Rx testing
    - Jitter Impairment profile and observation times
- eDP testing for eDP 1.4 specification

Reference: VESA® DisplayPort® PHY Compliance Test Specification Version 1.2

DisplayPort – Technology Overview

DisplayPort is expanding its foot print

- Standard DisplayPort
  - Specification Version 1.2
  - CTS Version 1.2b
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Box to Box (1, 2, 4 lanes)
- eDP
  - Specification Version 1.4
  - CTG in progress
  - Data Rates 1.62Gbps to 5.4Gbps
  - Embedded(single box – Laptops) (1,2,4 lanes)
- MyDP
  - Specification Version 1.0
  - CTS Version 1.0 (in approval)
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Mobiles (1 lane)
- iDP
  - Specification Version 1.1
  - CTG
  - Data Rates 3.24 , 3.78
  - LVDS replacement

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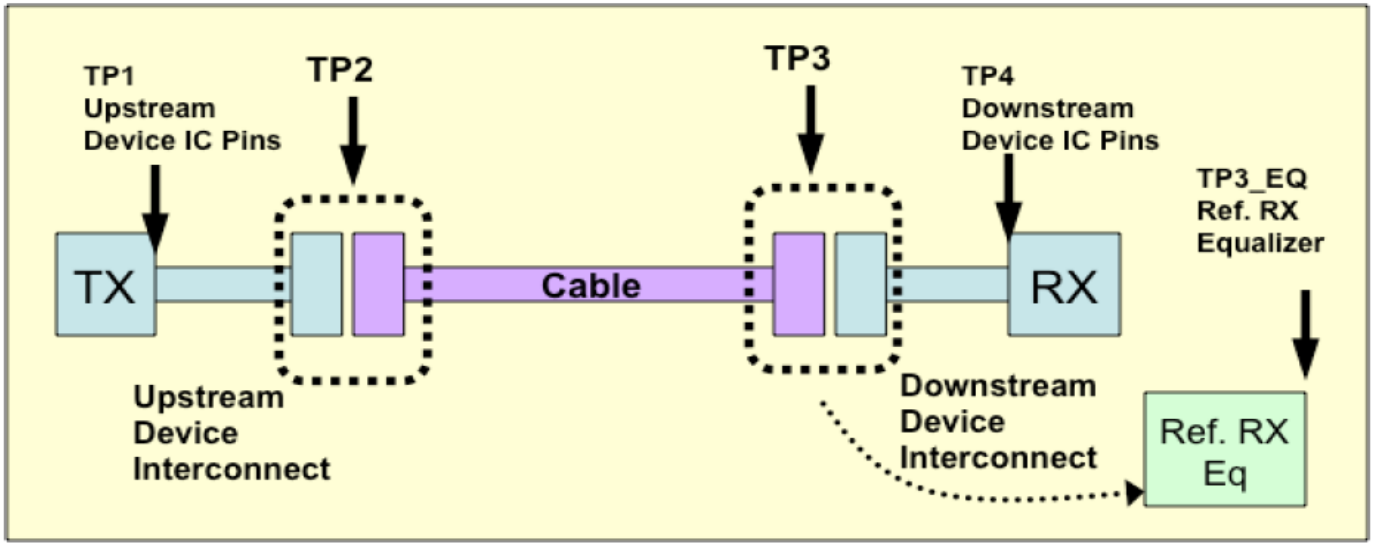
DisplayPort 1.2 Overview

The DisplayPort PHY Compliance Test Specification establishes a test regimen to determine compliance of DisplayPort devices - segmented into:

- Source
- Receiver
- Copper Cable
- Hybrid devices
- Tethered devices

- Test Point Definitions
  - TP1: at the pins of the transmitter device.
  - TP2: at the test interface on a test access fixture
  - TP3: at the test interface on a test access
  - TP3_EQ: TP3 with equalizer applied.
  - TP4: at the pins of a receiving device



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DisplayPort CTS1.2b

Source Test Suite

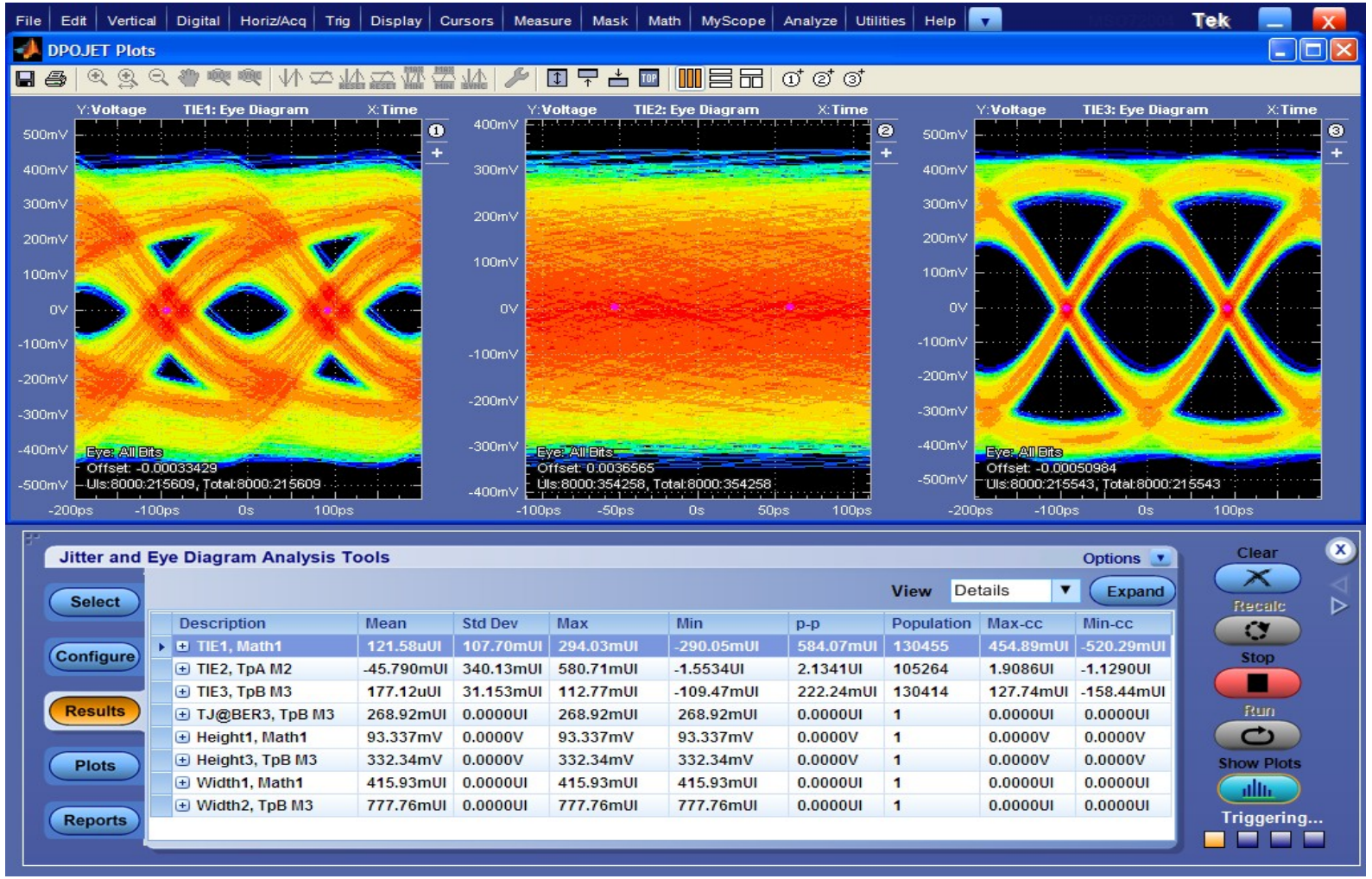
1.EYE Diagram
2.Non Pre-Emphasis Level Verification
3.Pre-Emphasis Level Verification and Maximum Differential Pk-Pk Output Voltage
4.Inter-pair Skew
5.Intra-Pair Skew
6.Differential Transition Time
7.Single Ended Rise and Fall Time Mismatch
8.Overshoot and Undershoot Test
9.Frequency Accuracy
10.AC Common Mode Noise
11.Non ISI Jitter Measurement
12.Total Jitter and Random Jitter Measurement
13.Unit Interval
14.Main Link Frequency Compliance Stability
15.1Spread Spectrum Modulation Frequency
16.Spread Spectrum Deviation
17.dF/dt Spread Spectrum Deviation HF Variation
18.Dual-mode TMDS Clock (NOW supported)
19.Dual-mode EYE Diagram Testing (NOW supported)
20.AUX lane Eye Diagram(NOW supported)
21.Aux lane Rx sensitivity(NOW supported)

DUT Configuration

- 1. Bit Rates: RBR, HBR or **HBR2**
- 2. Patterns: D10.2,PRBS7, COMP,
- PLTPAT,PCTPAT
- 3. FFE (Pre-Emphasis): 0dB, 3.5dB,
- 6dB, 9.5dB
- 4. Output Levels: 400mV, 600mV,
- 800mV, 1200mV
- 5. SSC (Spread Spectrum): On/Off
- 6. Post-Curser2: Level 0,1,2,3
- 7. Lane Width, 1,2,4

Eye Diagram Test using Eye Compliance Pattern

An Eye diagram test for 800mV , 0dB pre-emphasis at TP2,TP3, TP3-EQ.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
TIE1, Math1	121.58uUI	107.70mUI	294.03mUI	-290.05mUI	584.07mUI	130455	454.89mUI	-520.29mUI
TIE2, TpA M2	-45.790mUI	340.13mUI	580.71mUI	-1.5534UI	2.1341UI	105264	1.9086UI	-1.1290UI
TIE3, TpB M3	177.12uUI	31.153mUI	112.77mUI	-109.47mUI	222.24mUI	130414	127.74mUI	-158.44mUI
TJ@BER3, TpB M3	268.92mUI	0.0000UI	268.92mUI	268.92mUI	0.0000UI	1	0.0000UI	0.0000UI
Height1, Math1	93.337mV	0.0000V	93.337mV	93.337mV	0.0000V	1	0.0000V	0.0000V
Height3, TpB M3	332.34mV	0.0000V	332.34mV	332.34mV	0.0000V	1	0.0000V	0.0000V
Width1, Math1	415.93mUI	0.0000UI	415.93mUI	415.93mUI	0.0000UI	1	0.0000UI	0.0000UI
Width2, TpB M3	777.76mUI	0.0000UI	777.76mUI	777.76mUI	0.0000UI	1	0.0000UI	0.0000UI

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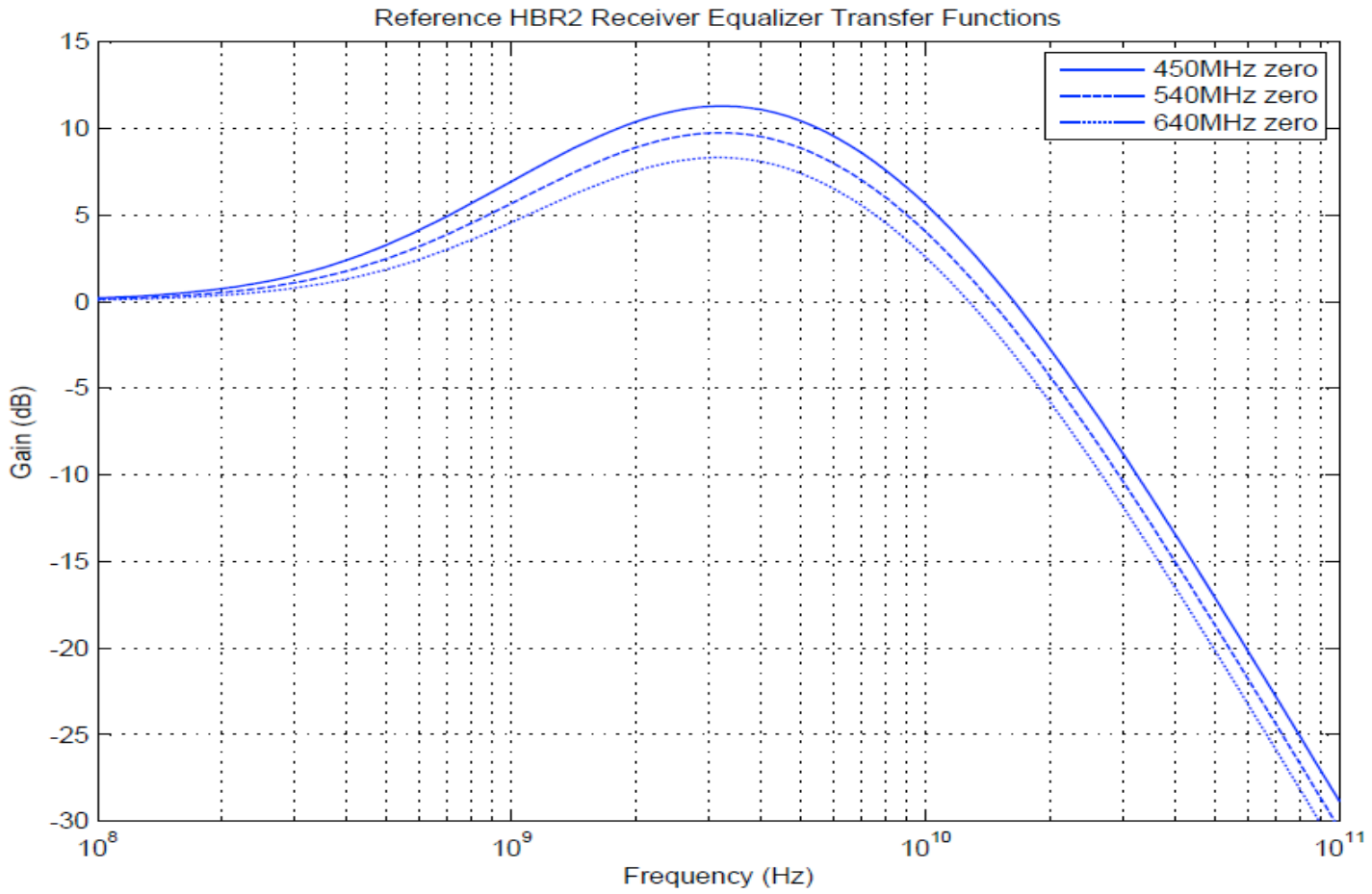
DisplayPort 1.2
CTLE Properties

1.2 CTS requires adaptive application of one of three reference equalizers to the far end signal, to find a passing condition.



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Key Elements of DisplayPort 1.2 Transition: Eye Diagram/Mask

- 1.2 CTS Requires Adaptive Eye Diagram
  - Find the highest vertical eye point between .375 -- .625 UI at 10E-9BER
  - Analytical tools which examine the vertical noise components project the Rn components to 10E9 BER. These tools have been proven in the field in SATA where they have been deployed for over two years.

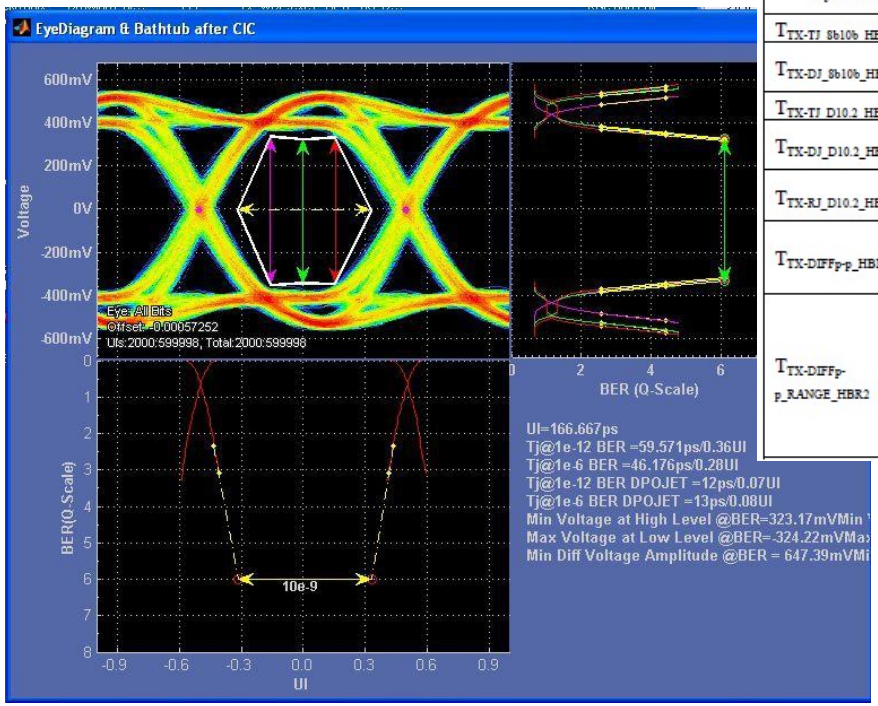

Table 3-19: DisplayPort Main Link Transmitter (Main TX) TP3 EQ Parameters

TX TP3_EQ (Compliance Cable Model with HBR2 Reference Receiver Equalization – Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Units**	**Comments**
$T_{TX\text{-}TJ\_8b10b\_HBR2}$	Maximum TX Total Jitter			0.62	UI	For HBR2. Measured at 1E-9 BER using the HBR2 Compliance EYE pattern.
$T_{TX\text{-}DJ\_8b10b\_HBR2}$	Maximum TX Deterministic Jitter			0.49	UI	
$T_{TX\text{-}TJ\_D10.2\_HBR2}$	Maximum TX Total Jitter			0.40	UI	For HBR2. Measured at 1E-9 BER using the D10.2 compliance pattern.
$T_{TX\text{-}DJ\_D10.2\_HBR2}$	Maximum TX Deterministic Jitter			0.25	UI	
$T_{TX\text{-}RJ\_D10.2\_HBR2}$	Maximum TX Random Jitter			0.23	UI	
$T_{TX\text{-}DIFFp\text{-}p\_HBR2}$	TX Differential Peak-to-Peak EYE Voltage	110			mV	For HBR2. Measured at 1E-9 BER using the HBR2 Compliance EYE pattern.
$T_{TX\text{-}DIFFp\text{-}p\_RANGE\_HBR2}$	TX Differential Peak-to-Peak EYE Voltage Measurement Range	0.375		0.625	UI	For HBR2. Uses 0.5 CDF of the jitter distribution as the 0UI reference point. TX Differential Peak-to-Peak EYE Voltage requirement can be met anywhere within this UI range.

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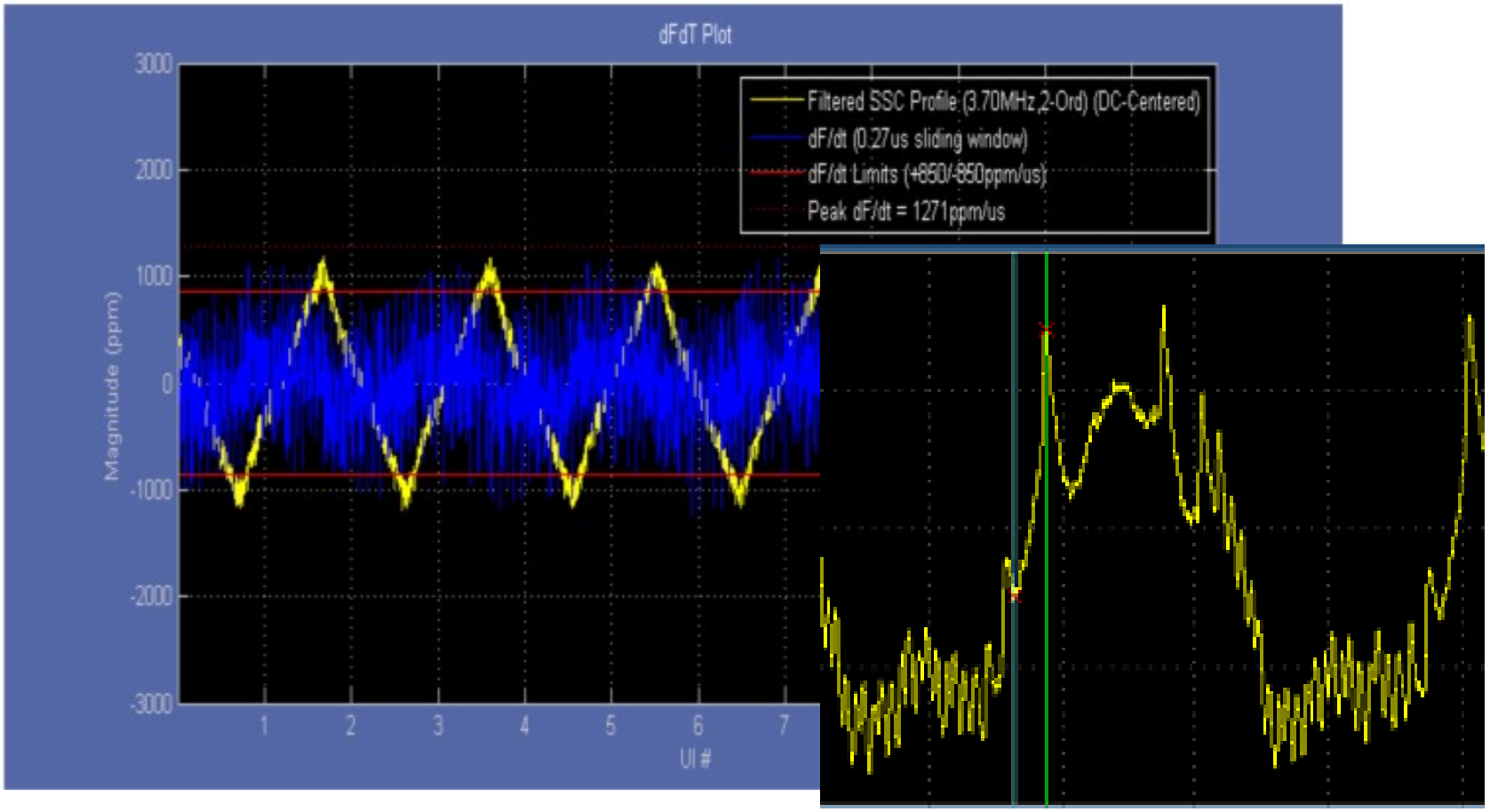
Key Elements of DisplayPort 1.2 Transition: dFdT

While dFdT measurements have a unique origin emerging from the SATA and SAS specifications where the history of examining SATA dFdT has led this to become a highly recommend analysis. The dFdT contributing components will rarely appear in the normal Jitter budget due to their low frequency nature.



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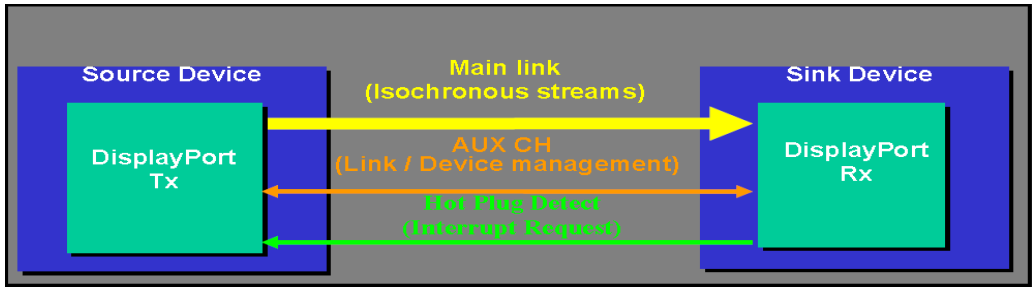
DisplayPort Auxiliary Channel Controller (DP-AUX)

Why use Aux channel controller in physical layer testing?



- Speeds Up Test Time - No User Interaction is Required to Change Source Output Signal or Validate Sink Silicon State or Error Count
- No Need to Learn Vendor-specific Software - A Single GUI Supports All Vendors
- View & Log Decoded AUX Traffic and Hot Plug Detect (HPD) Events from the Device under Test to the DP-AUX DisplayPort AUX Controller
- Ability to Read and Write DPCD Registers Supports Debug Activities
- Tektronix DP-AUX can serves as a DP1.2 Sink - Enables source to transmit the required patterns for testing.

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Automation: DisplayPort testing is a large task!

Combination Parameters For DP1.2 Testing

- Data Rate - 3
- Lanes - 4
- Pre-Emphasis - 4 Levels
- Voltage Swing - 4 Levels
- Post Cursor2 - 4 Levels
- SSC - 2 Levels(SSC On and Off)
- Patterns - 5 Supported Patterns

Combination of Tests

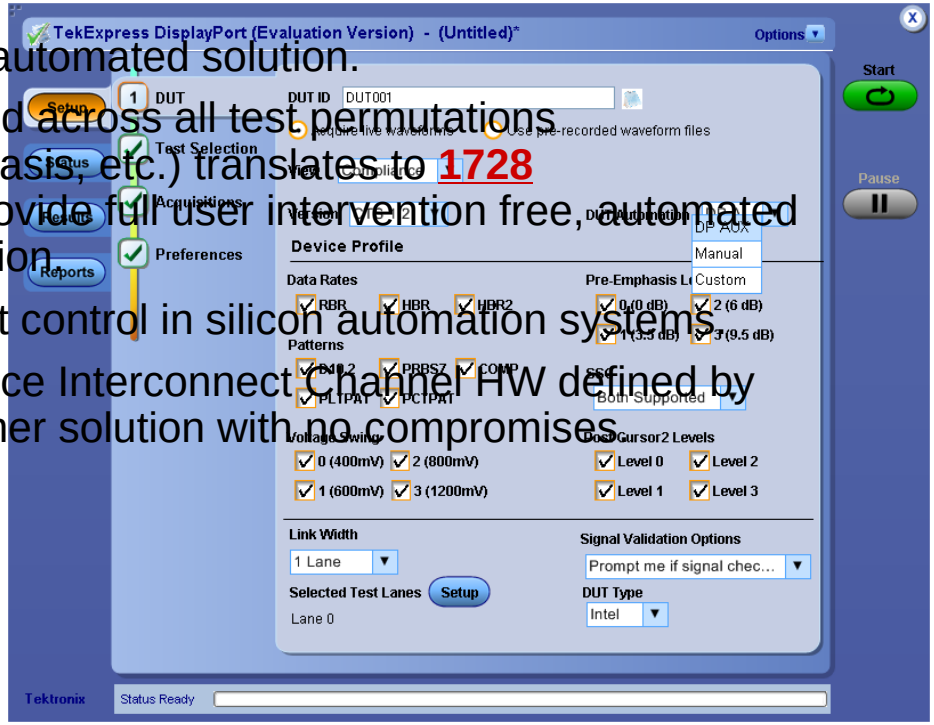
1. Differential Tests
2. Single Ended Tests

Test	Waveforms (SSC, 4 Lanes Possible Combinations)
Eye Diagram Test	80
Pre-Emphasis Test	240
Non-Pre-Emphasis	32
Total Jitter	80

~432 Acquired signals for DP1.2 Normative Measurements per lane.
X4 lanes results in 1728 Automated Acquisitions per DUT.

TekExpress DisplayPort 1.2 Automation

- Comprehensive Display Port Version 1.2 Physical Layer Conformance and Compliance Verification Tool
  - All Core DP1.2 measurements
  - Keithley RF Switch and DP-AUX fully automated solution.
  - Selected measurements can be applied across all test permutations (SSC,CTLE's, swing, rates, pre- emphasis, etc.) translates to **1728 measurements**. DP12 will provide full user intervention free, automated testing. This is the killer value proposition.
  - Factory Automation API for full product control in silicon automation systems.
  - Complimentary Fixtures and Compliance Interconnect Channel HW defined by VESA make this package a full customer solution with no compromises.



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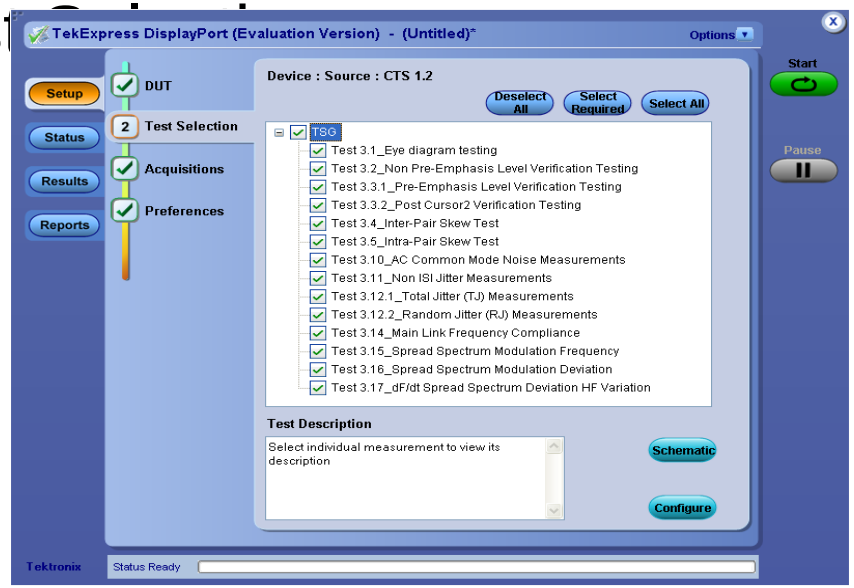
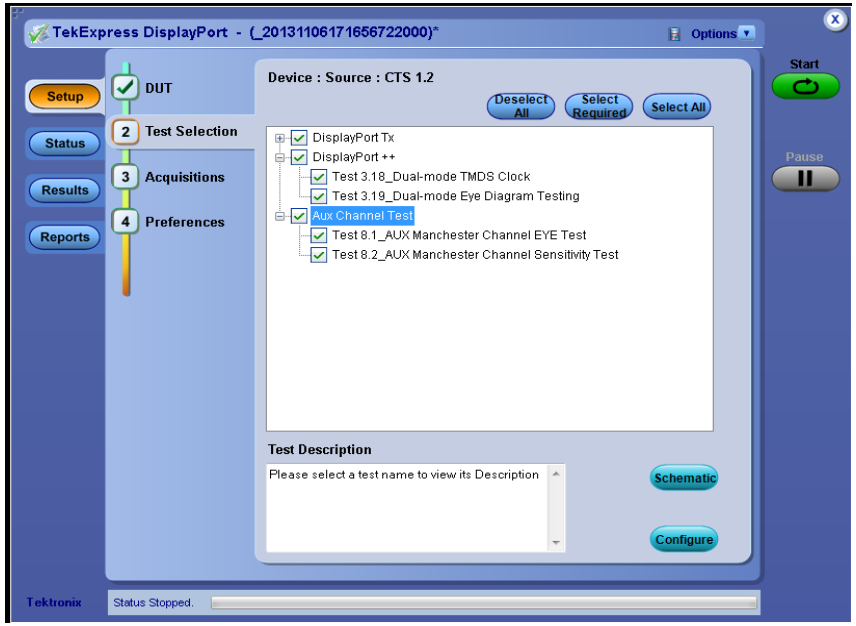
DisplayPort 1.2 Test

- DP1.2
  - Measurement selection is now provided as a function of the user specified test target capabilities.
  - If Post Curser 2 capabilities are not present in the DUT, the measurement list will not show them.
  - Configuration schematics and online help available for all measurements





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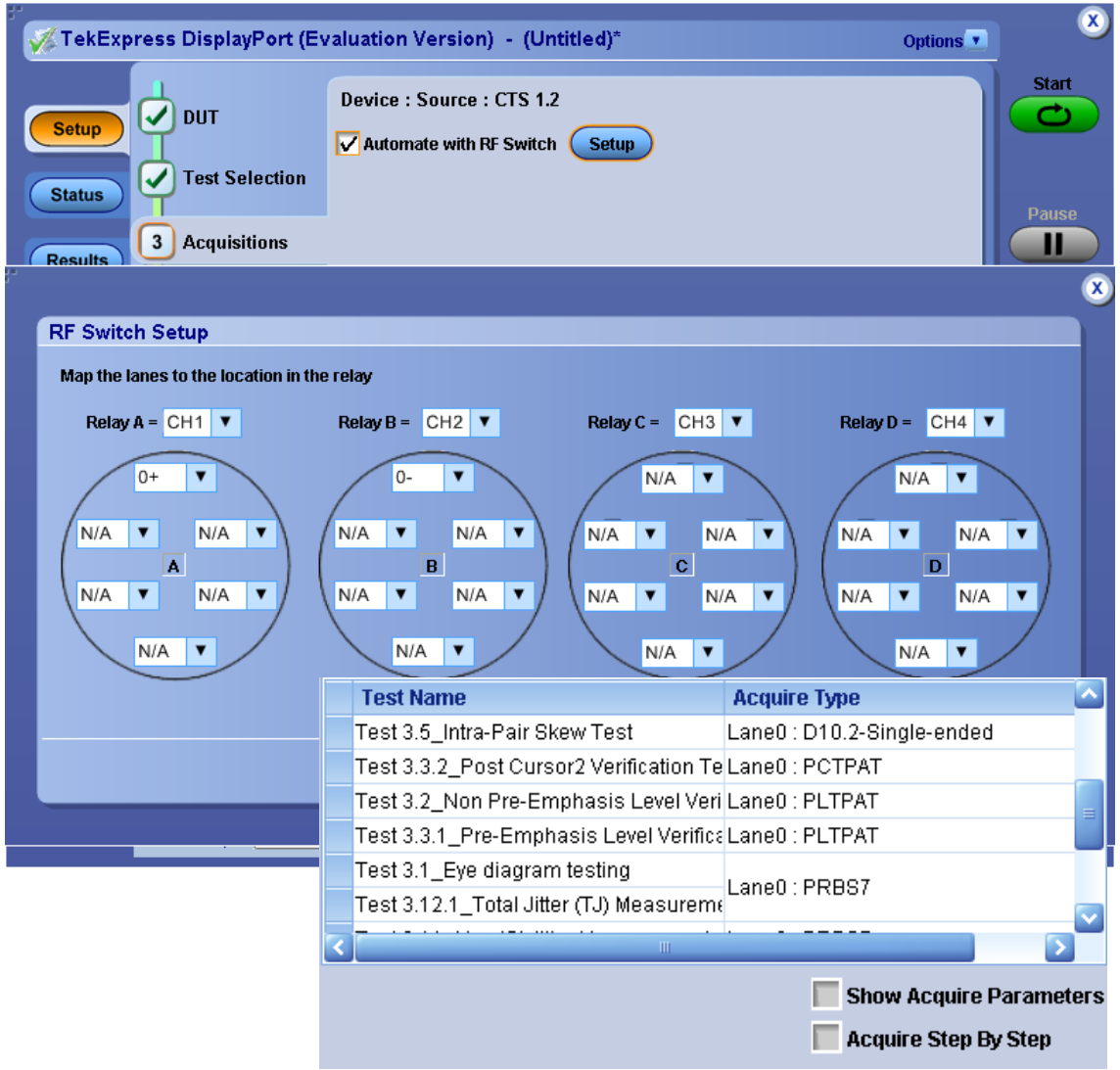
DisplayPort 1.2 Acquisitions

- DP1.2
  - Various signal interconnect methods are supported.
  - Direct TCA (SMA input) on user selected channels.
  - Differential Probe (P7313SMA) inputs for true 4 channel concurrent interconnect. (No single ended measurements)
  - 24:4 Keithley RF Switch allows fully automated control of all 8 single ended inputs for hands free comprehensive testing.
- Test Patterns
  - Automatic verification of test patterns (which can be disabled) ensures the correct patterns are used for the correct test under manual operation.



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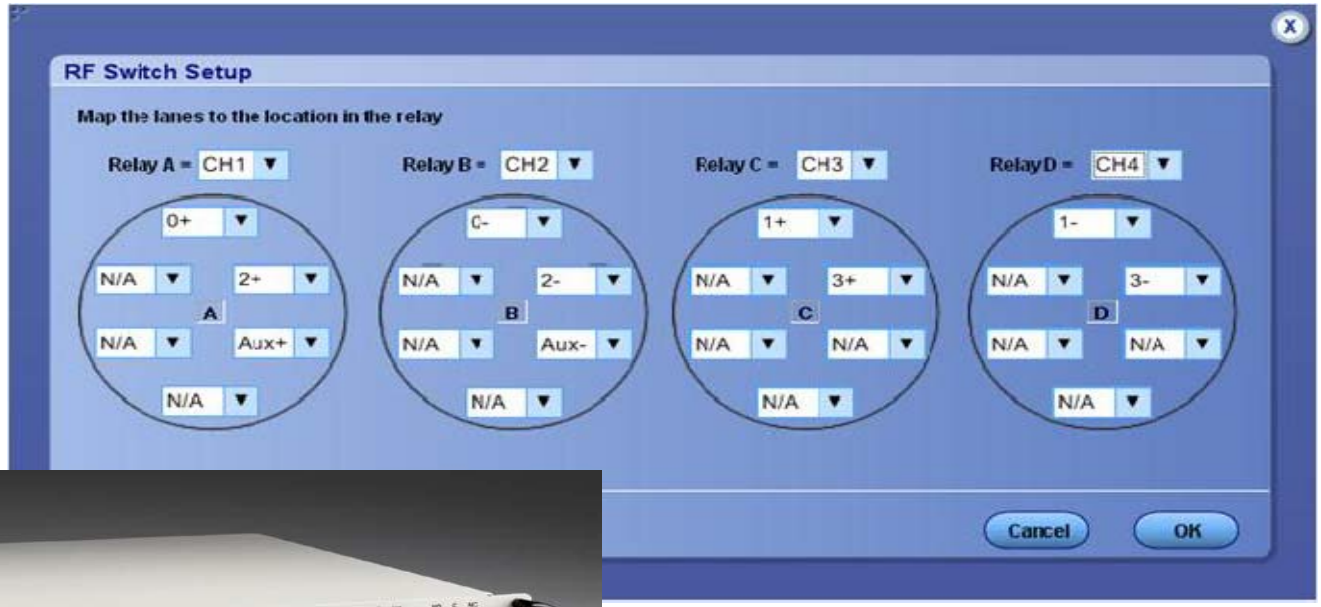
Keithley RF Switch Integration and Automation

DisplayPort transmitter has both Differential tests and Single ended tests and with the integration of RF switch we have complete automated solution without any user intervention for switching between lanes with both single ended and differential tests in sequential automated passes.



Keithley is now part of Tektronix.

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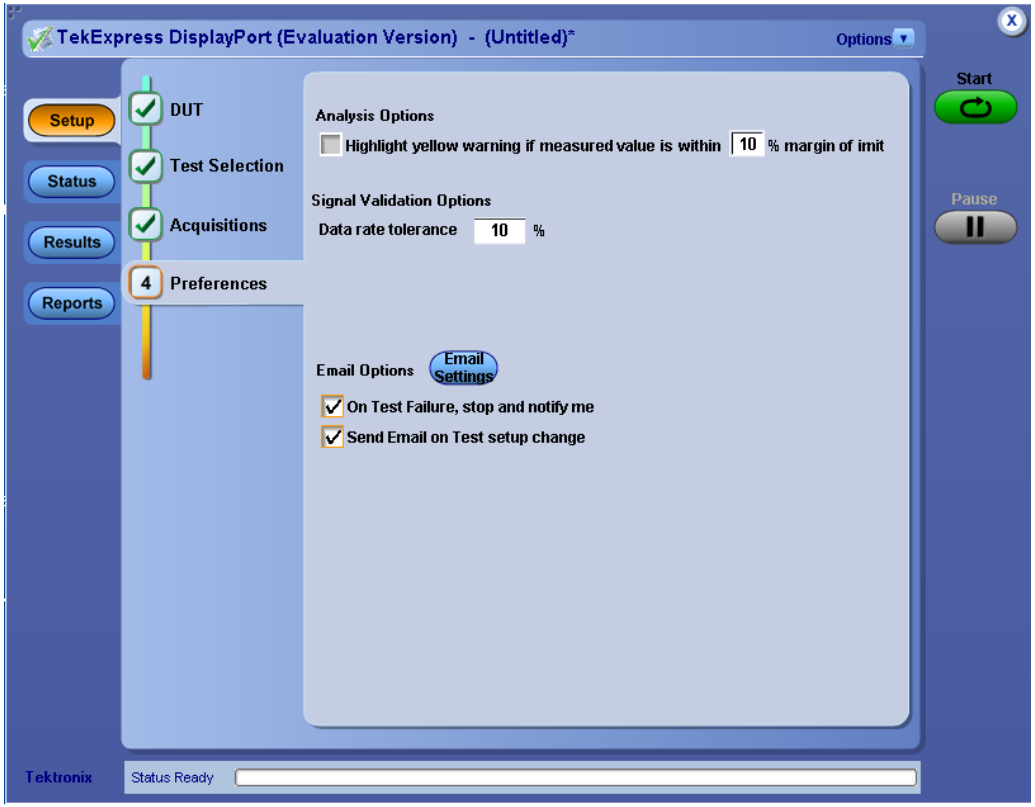
DisplayPort 1.2
User Preferences

- DP1.2
  - User defined test margin controls and auto highlighting of measurements within a user specified tolerance of either the standard spec limits or user defined custom limits.
  - Email controls allow notification of test conditions directly to users.



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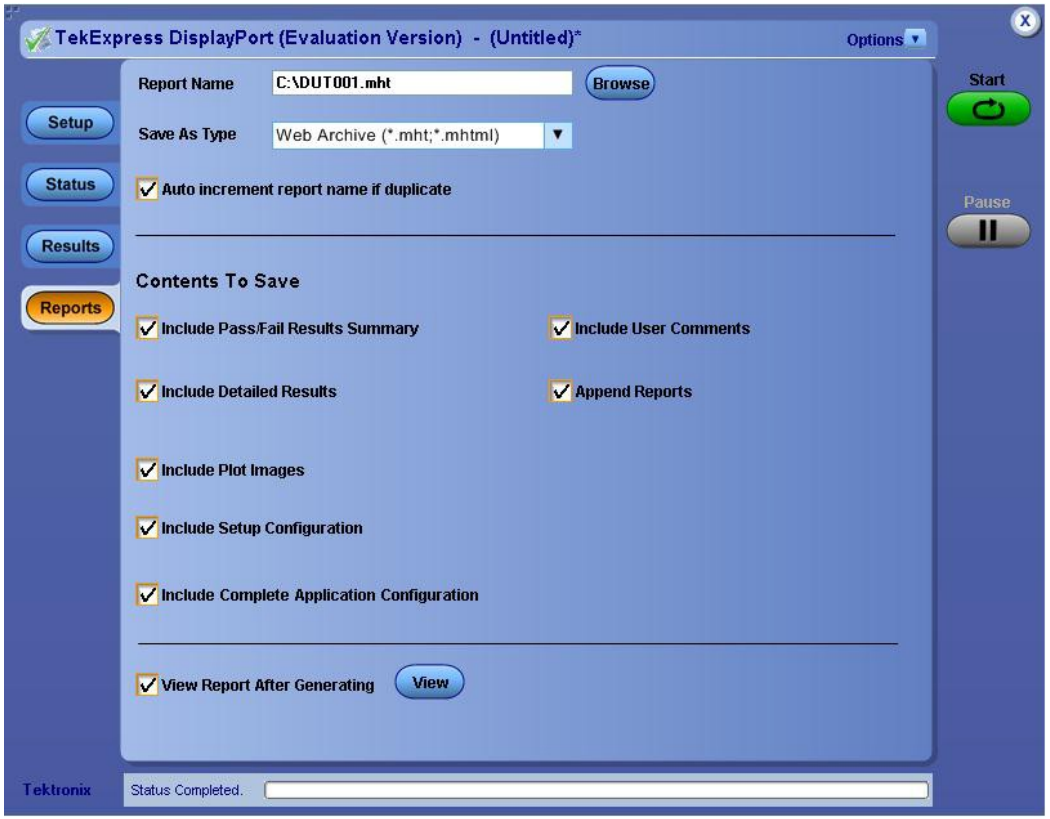
DisplayPort 1.2 Reporting

- DP1.2
  - Custom html reports which include user specified degrees of detail.
  - Reports and Session raw data are stored together allowing recalling a previous run and re-running the test (with different measurement configurations or limits) and re-generating a new report, **without the actual DUT present**.



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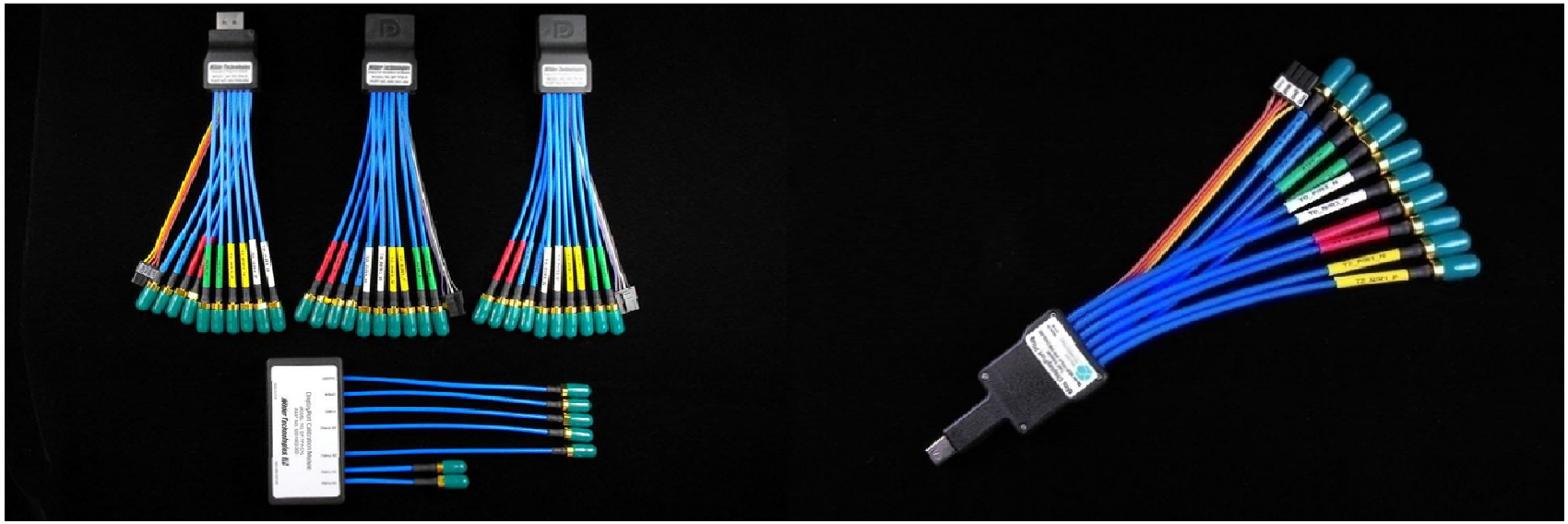
Conventional Display Port Fixtures + CIC

- Partnership with Wilder Technologies to design and channel high performance DP fixtures



- Wilder TF-DP-TPA-PRC fixtures and BSA12500ISI available directly from Tektronix

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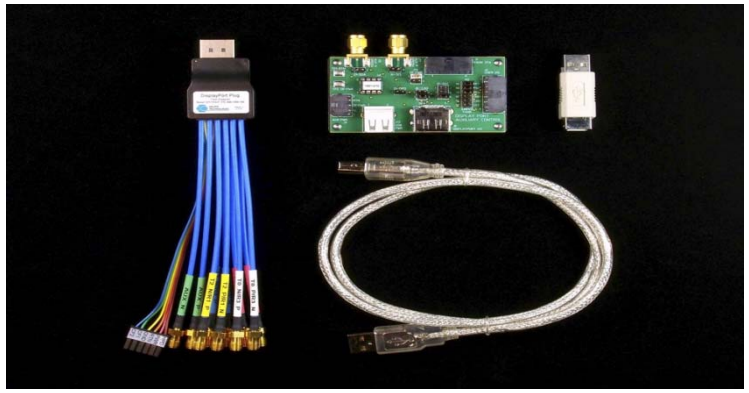
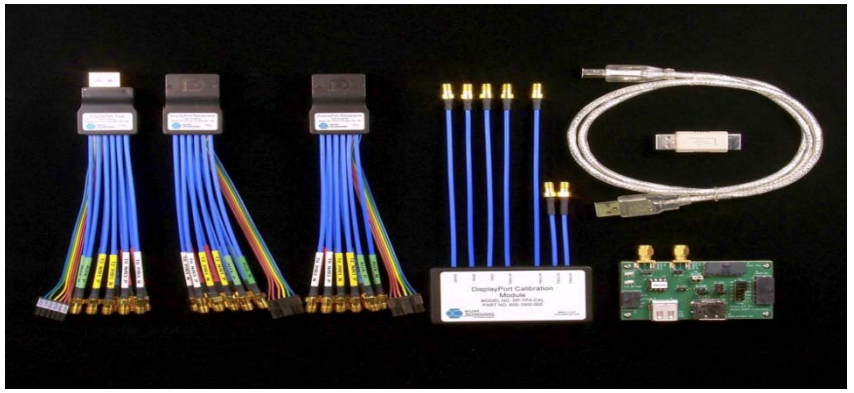
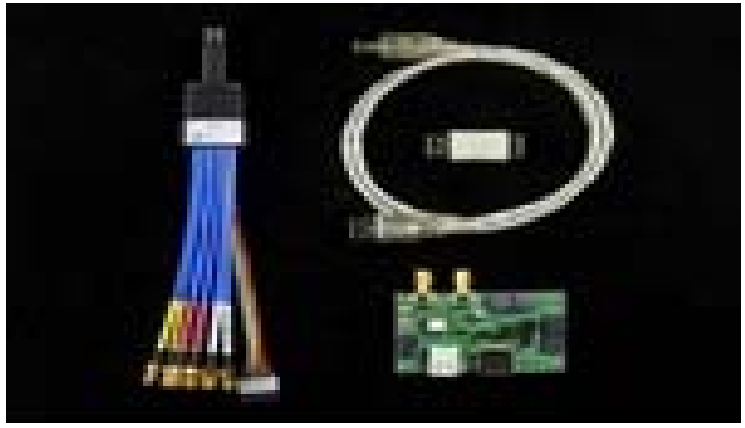
DP++ fixtures



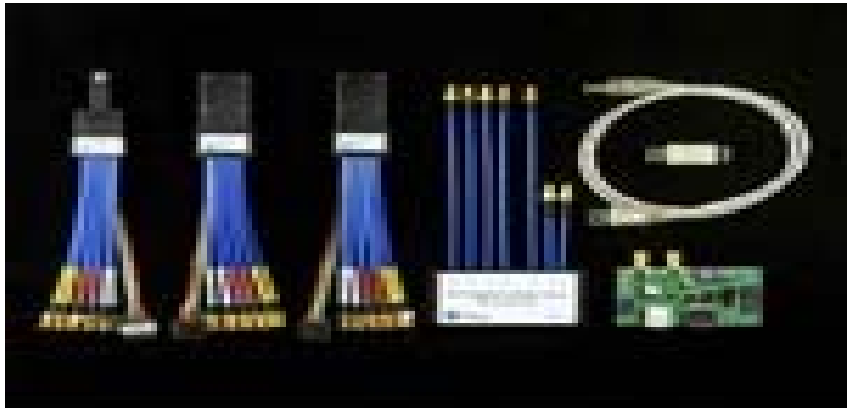
TF-DPI-TPA-PA



TF-DPI-TPA-PRRCA



TF-MDPI-TPA-PA



TF-MDPI-TPA-PRRCA

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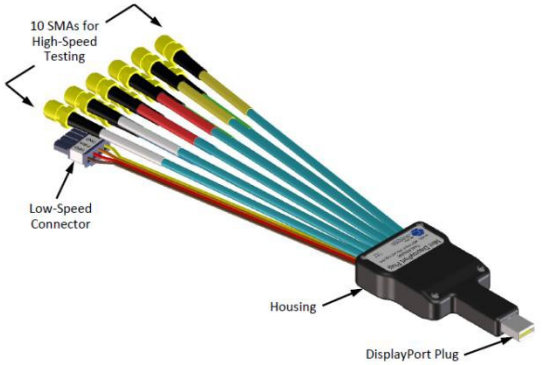
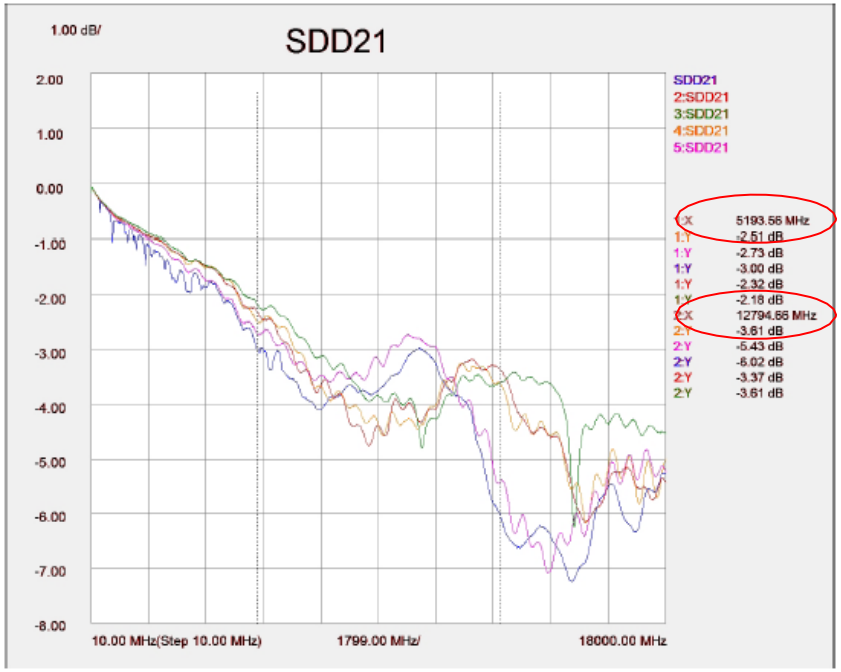
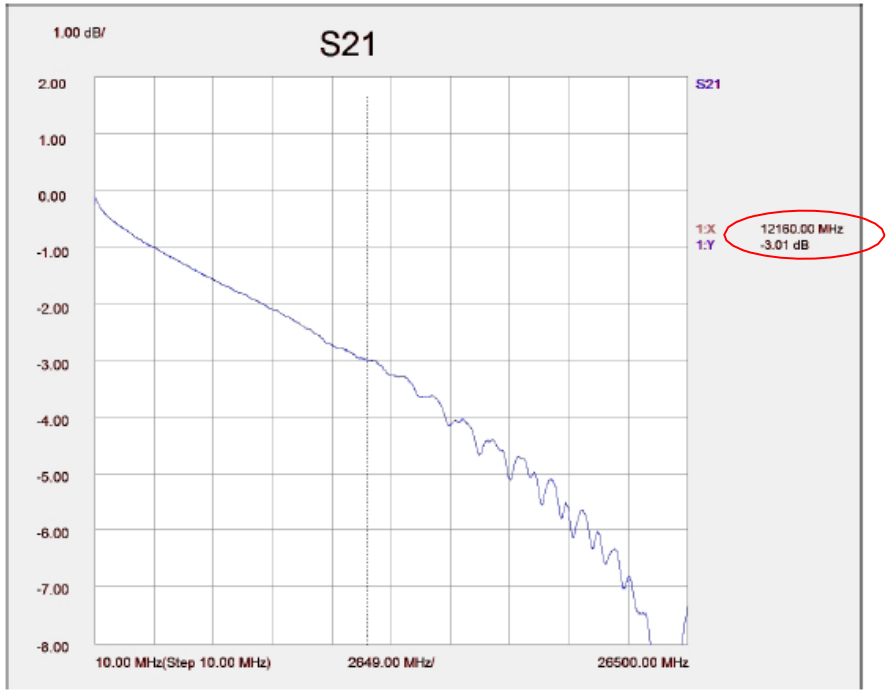
Channel Bandwidth: 16 GHz Recommended

- **Mated miniDPconnector analysis**
  - The mated channel performance is 3dB down at 5 GHz and 6dB down at 12.7 GHz.
  - Nominal back end instrument performance in the ~16GHz region is recommended and will capture all relevant signal harmonics for accurate characterization.
  - The DP1.2 CTS calls out a 12.5GHz minimum.







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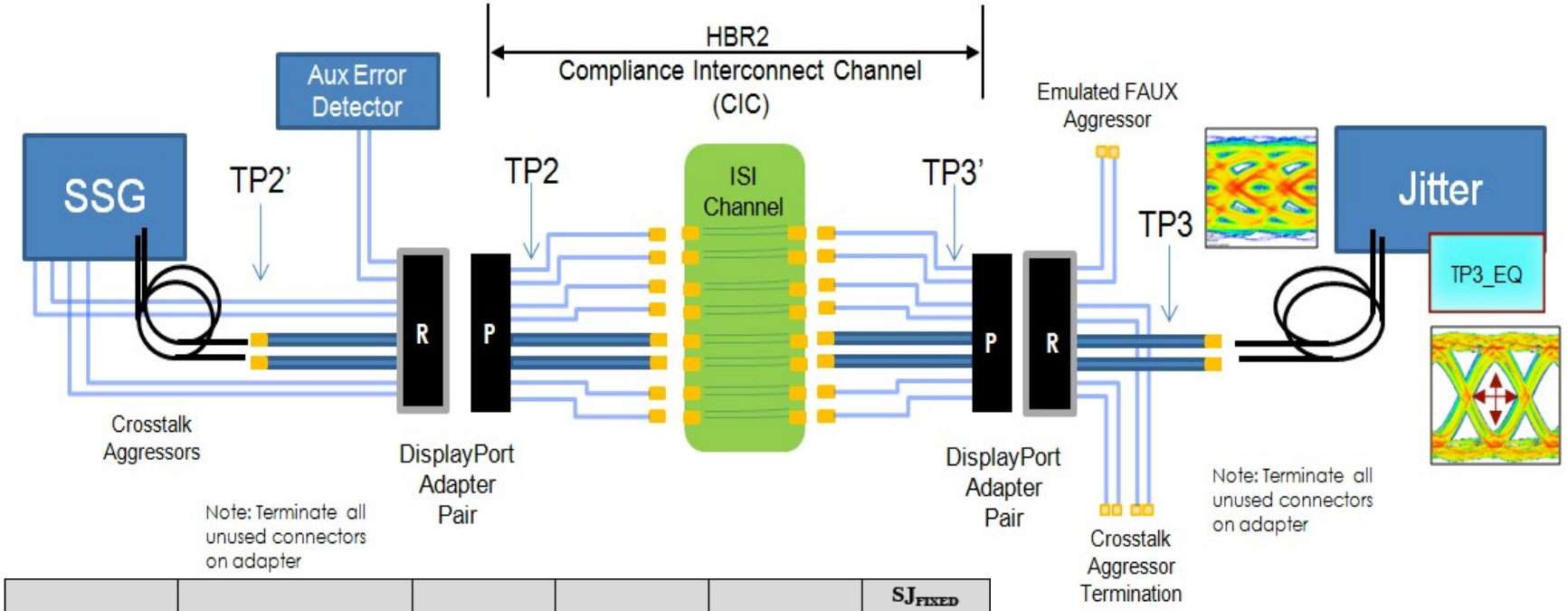
DisplayPort 1.2
Sink (Rx) Test Overview

Receiver testing is performed with a Tektronix BSA125C BertScope and Wilder HBR2 ISI Channel. BER observation times range from 37 seconds 10.5 minutes depending on the data rate and jitter frequency being tested. e version 1.2 CTS outlines 17 Tx validation tests which are typically evaluated with a 12.5GHz or higher bandwidth oscilloscope.



f(SJ)	TJ(JTHBR2rx)	ISI	RJ(RMS)	Approximate SJ_{SWEEP}	SJ_{FIXED} @ 200MHz
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]	[mUI]
2	1026	220	16.7	505	100
10	636	220	16.7	116	100
20	624	220	16.7	104	100
100	620	220	16.7	100	100

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DisplayPort 1.2
Sink (Rx) Test Observation Time

Four Principal Test Frequencies at 2, 10, 20 and 100 MHz SJ

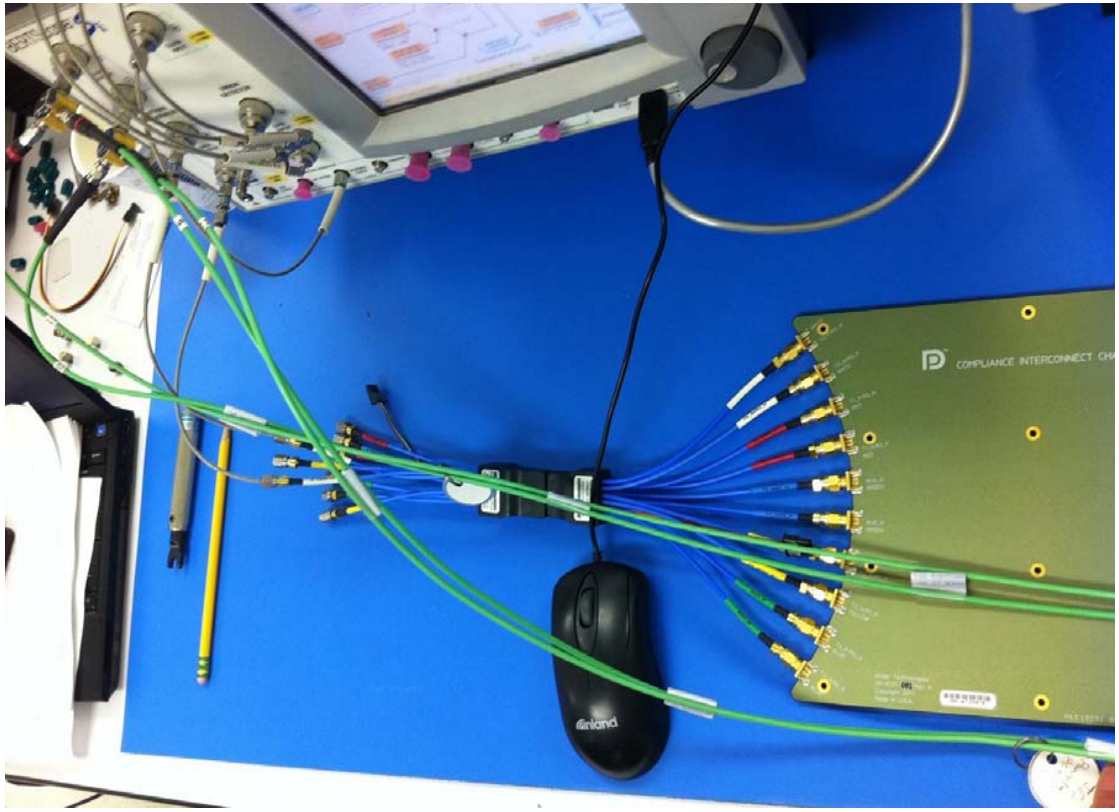
Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR2 *HBR* *RBR*	*2 MHz*	*10^{12}*	*1000*	*HBR2 =185s* *HBR=370s* *RBR=620s*	*0*
HBR2 *HBR* *RBR*	*10 MHz*	*10^{11}*	*100*	*HBR2=19s* *HBR=37s* *RBR=62s*	*+350ppm* *+350ppm* *+350ppm*
HBR2 *HBR* *RBR*	*20 MHz*	*10^{11}*	*100*	*HBR2=19s* *HBR=37s* *RBR=62s*	*0*
HBR2 *HBR*	*100 MHz*	*10^{11}*	*100*	*HBR2=19s* *HBR=37s*	*0*
*To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds*					

BertScope Receiver Test Solution

Typical Configuration

- BertScope BSA85C
  - Option STR
- DPP125A (no 4T needed)
- BSA12500ISI
- DP-AUX
- TF-DP-CIC-C1
  - Wilder DP 1.2 ISI Board



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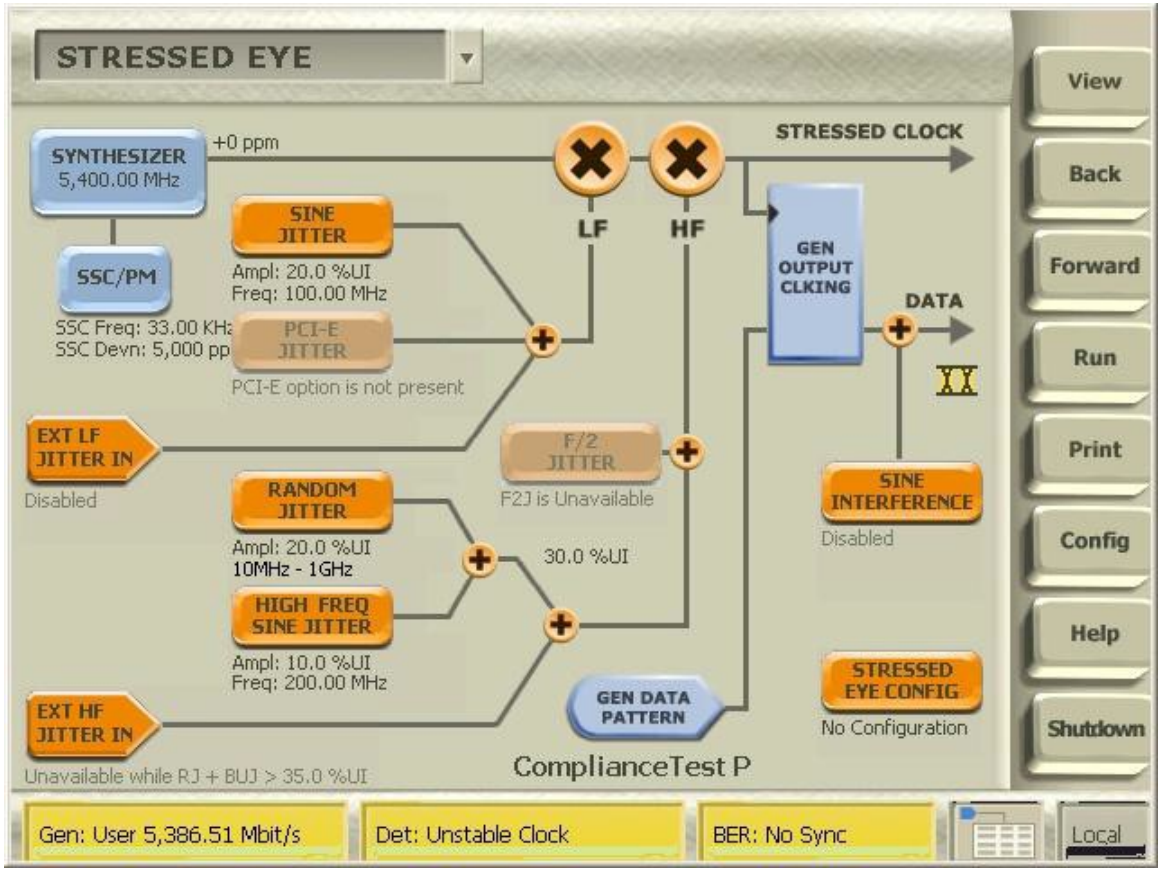
Two Tone SJ, with Stationary HFSJ Parked at 200 MHz.

New HFSJ source for fixed 200 MHz SJ as required by DP1.2.



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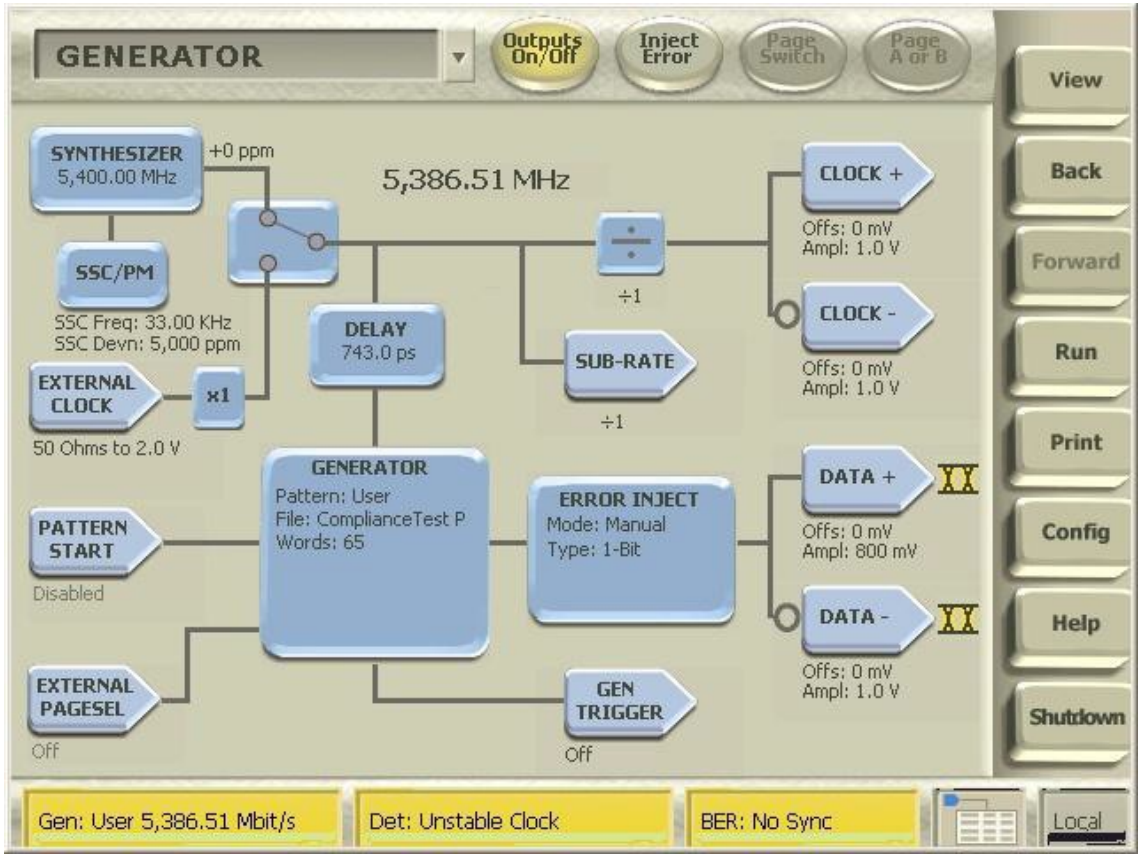
DisplayPort 1.2
Crosstalk (BUJ) Configuration

Generator page showing Patterns and capability of generation large amount Crosstalk with differential sub-rate Clock Outputs.



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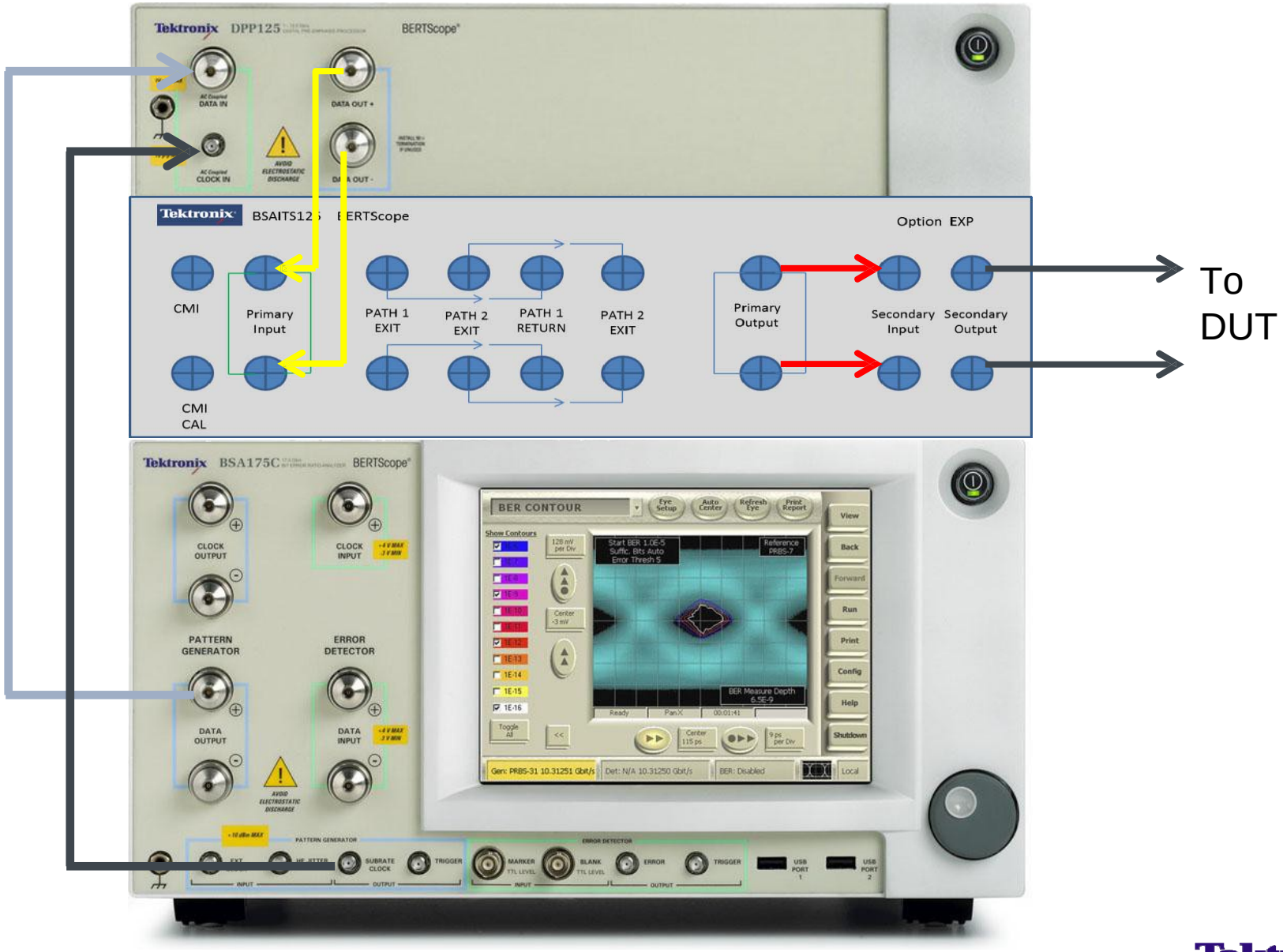
DisplayPort 1.2 -High end BeRTScope configuration



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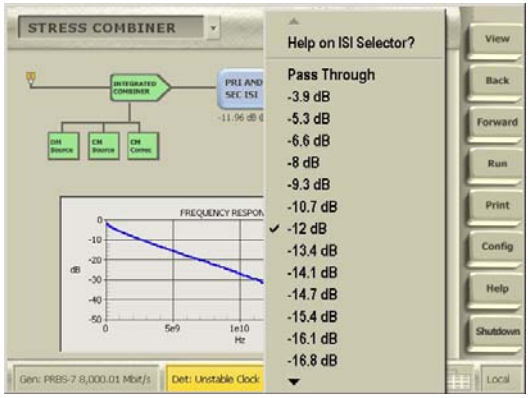
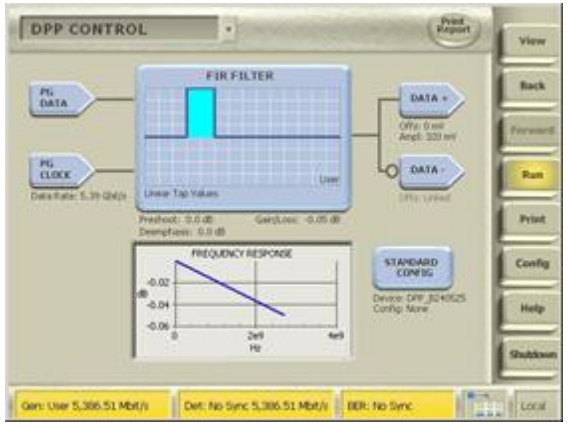
DisplayPort 1.2 -High end BeRTScope configuration

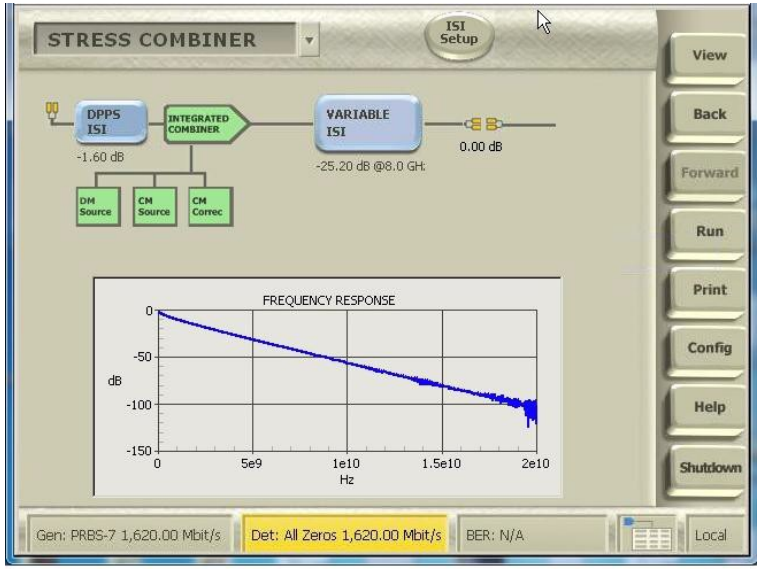
BSAITS125 generates multiple, fixed selections for ISI…



Use BERTScope DPPB or DPPC to generate low pass filter to fine tune ISI



On BSAITS GUI, you can simply dial in the amount of ISI needed…and DPP and BSAITS will adjust to generate requested ISI…



- Can automate calibration when using BSAITS with DPP
- Can precisely tune ISI at all data rates
- Can generate additional ISI to test margin of DUT

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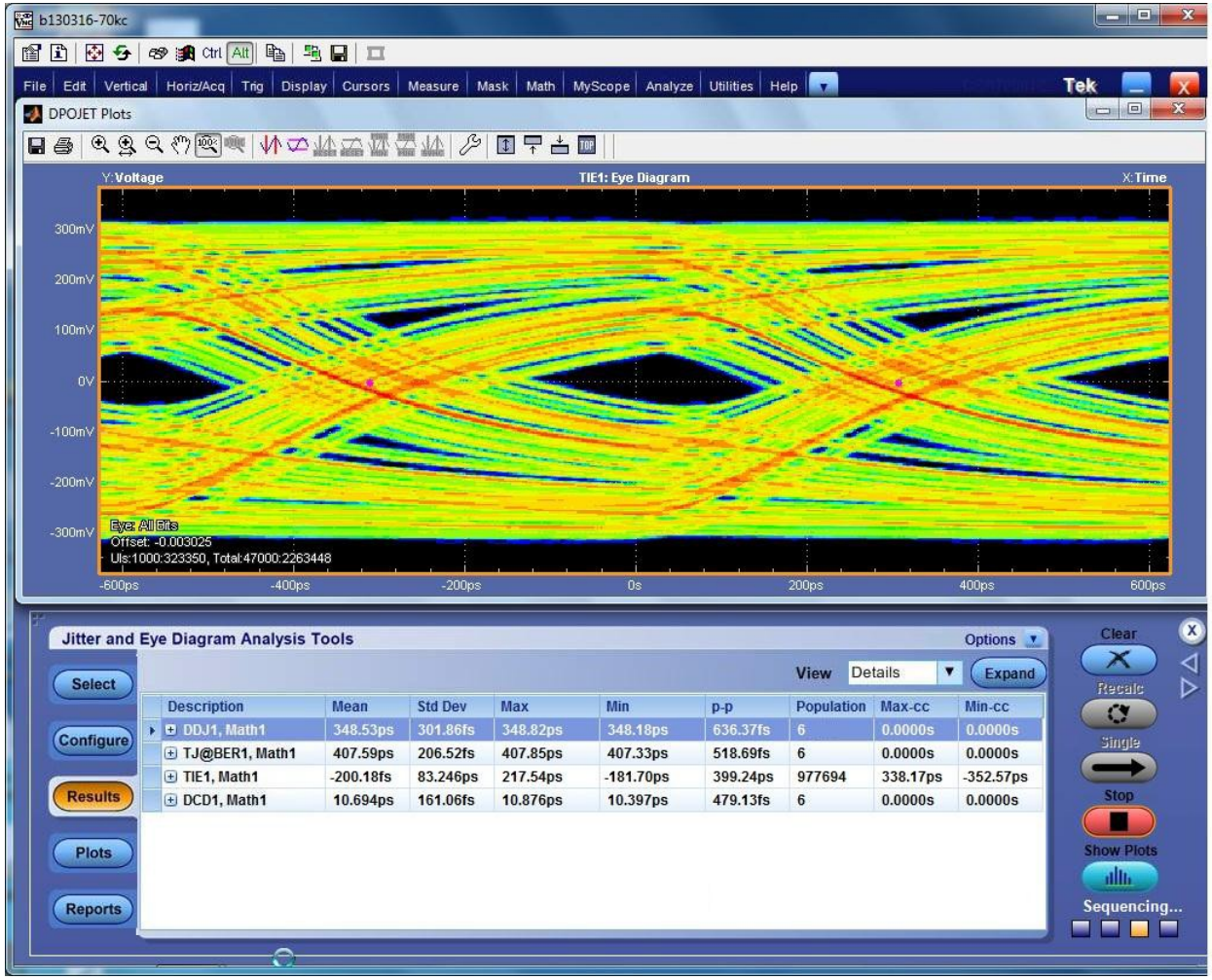
DisplayPort 1.2 -High end BeRTScope configuration

RBR ISI created using BSAITS
and DPP125B



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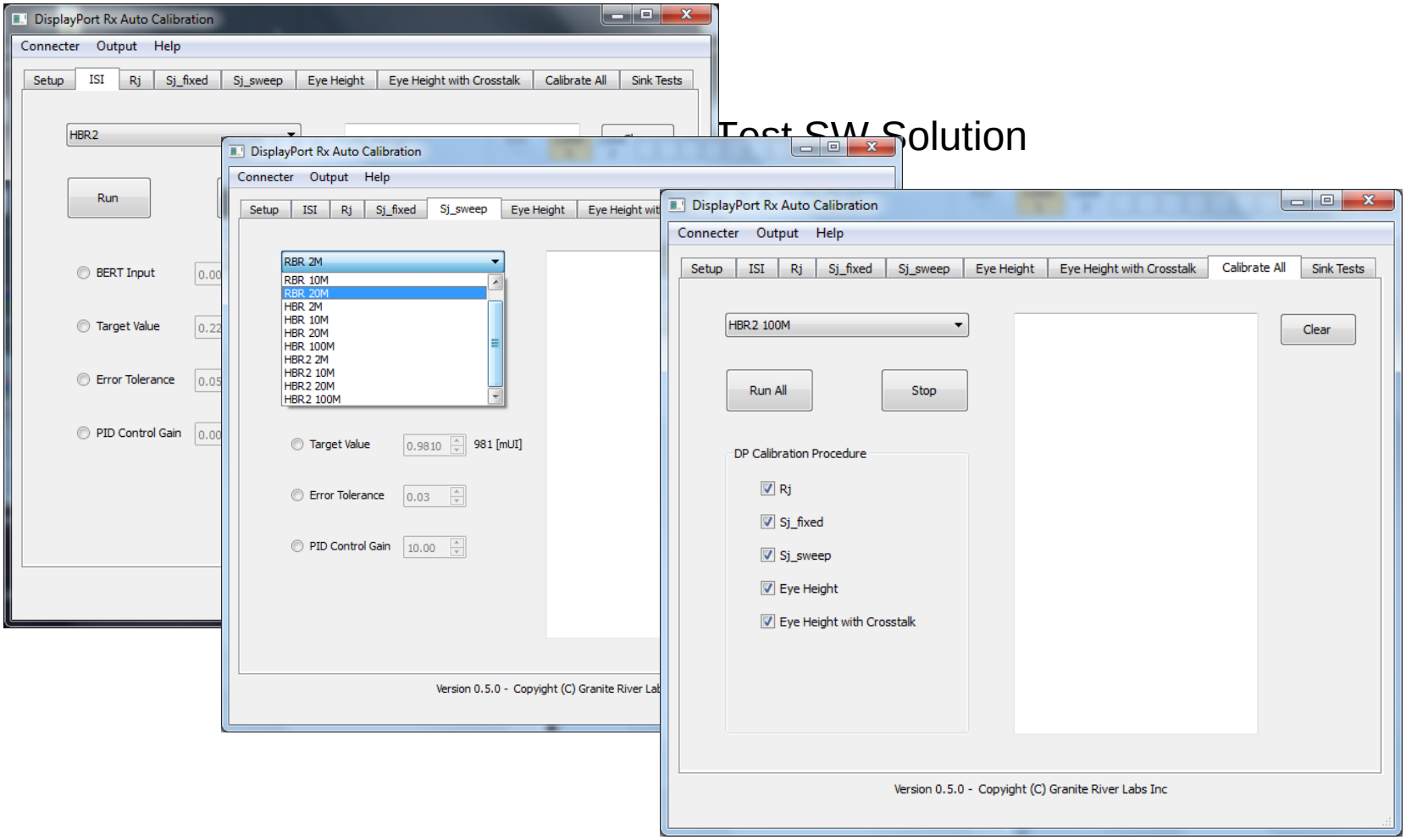
DisplayPort 1.2b Sink automation SW

- DP 1.2b PHY CTS
- Vendor Methods of Implementation MOIs
- Tek_DP_PHY12bCTS_Source_MOI_D2 01-14-2013
- Tek_DP_PHY12bCTS_BERTScope_SINK_MOI_D2_01-14-13

Automation Needed!!

DPCD Automation Support



Test SW Solution

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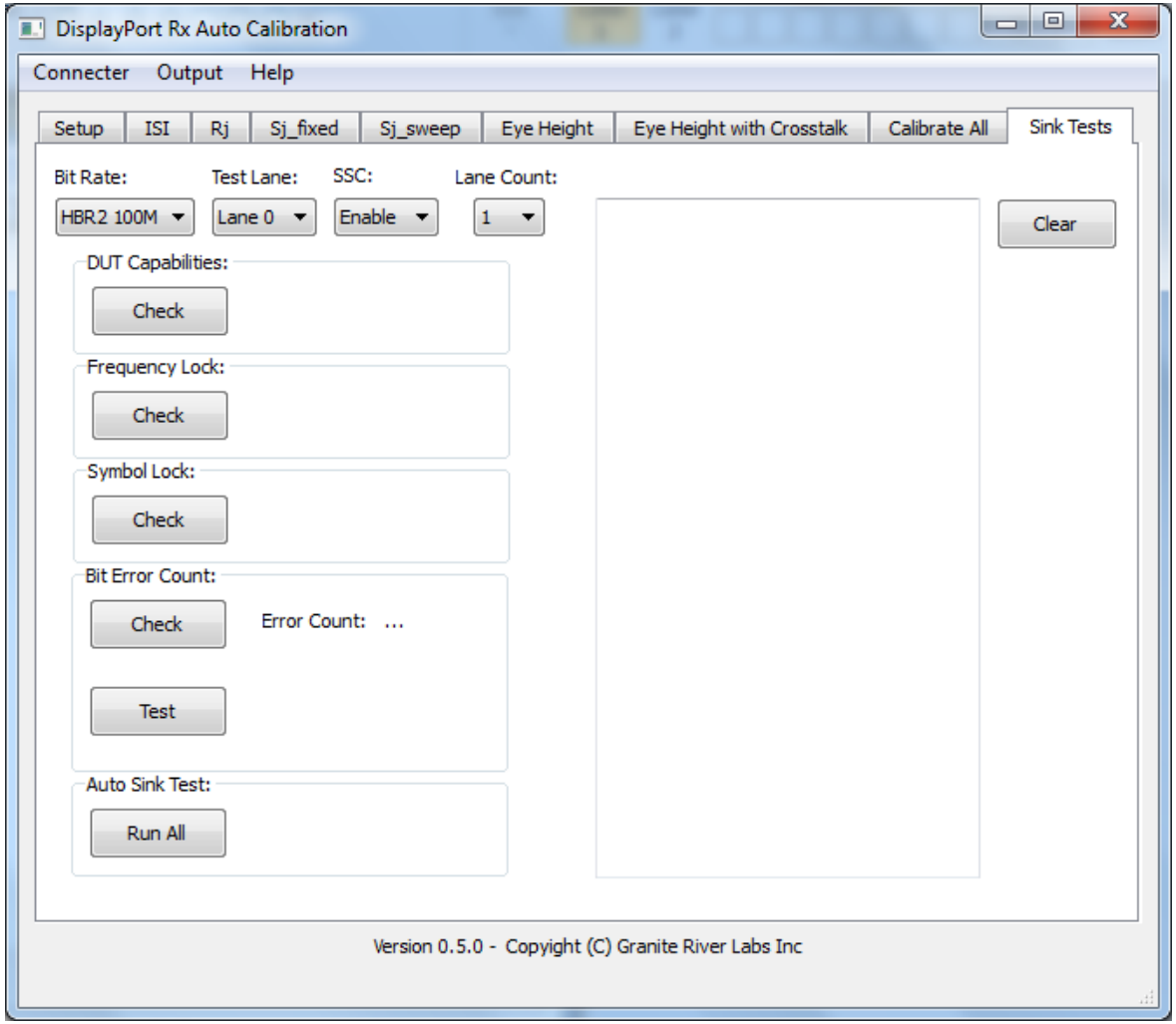
DPCD Automation Support



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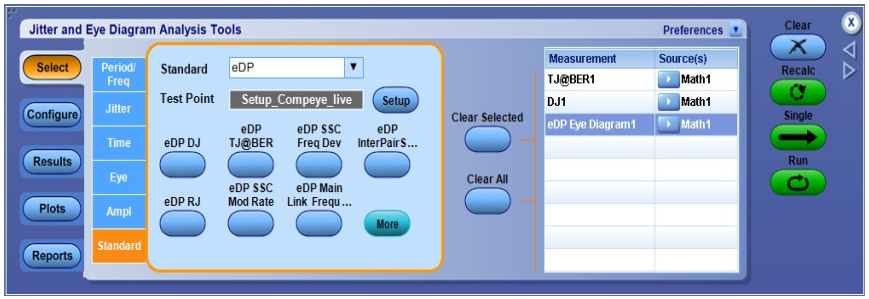
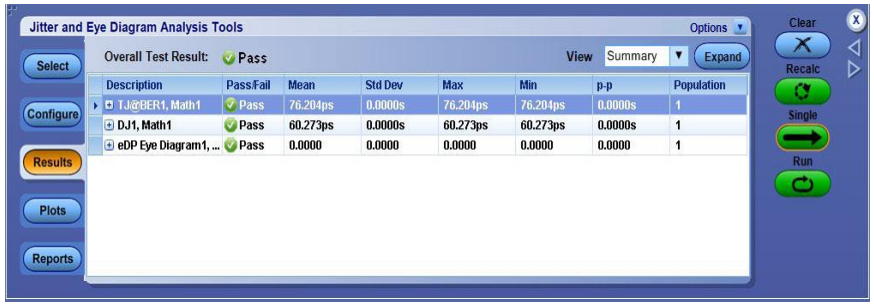
Embedded Display Port-eDP

Option EDP is designed to provide component and system designers with a comprehensive verification and debug solution the latest Embedded DisplayPort Specification 1.4.

Using the familiar DPOJET look and feel the user can select the setup based on their specific measurements requirements. In addition, as the 1.4 specification allows the data rate to be anywhere within a range of speeds from RBR to HBR2 rates opt EDP will provide the dynamic mask generation required to ensure proper testing





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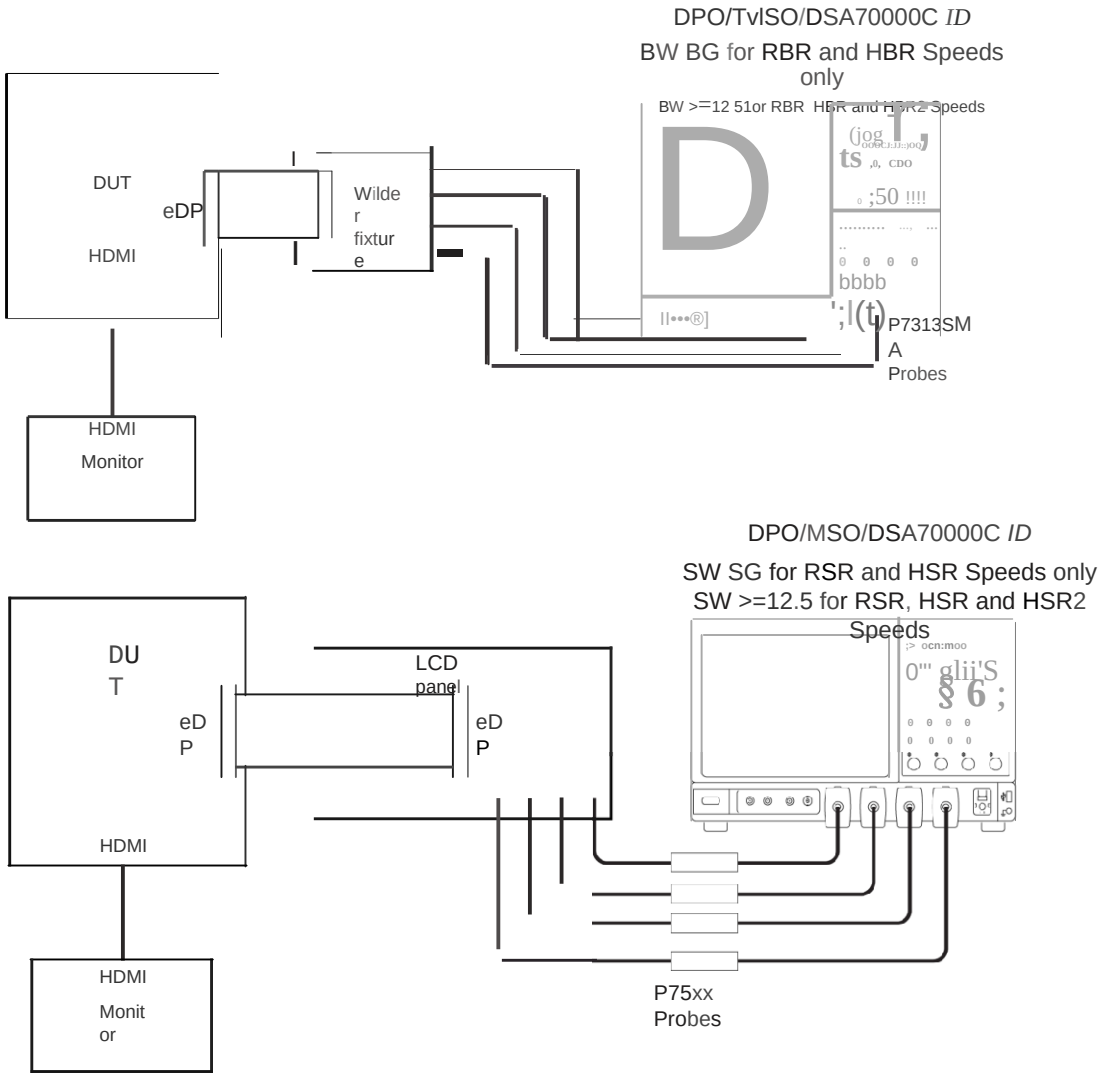
Embedded Display Port-eDP Typical connection



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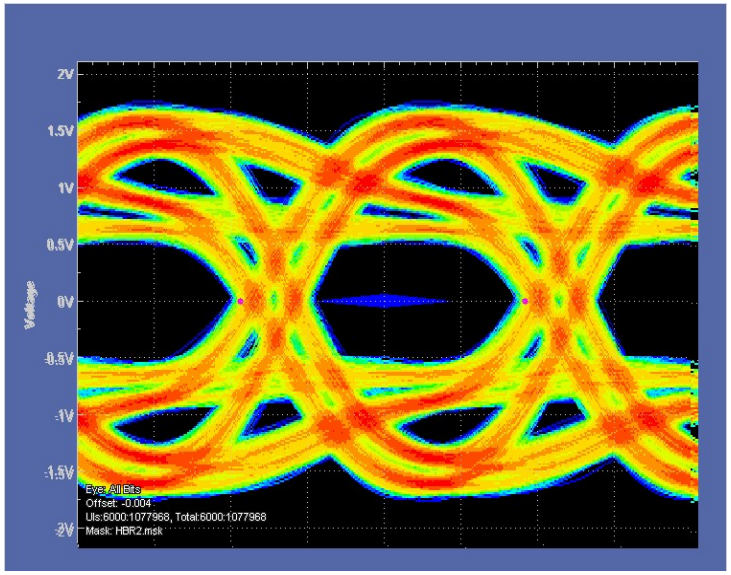
Embedded Display Port-eDP

eDP source measurements: Test 3.1 - Eye Diagram Test Test 3.2 - Inter Pair Skew test
Test 3.3 - Non-ISI Jitter Measurements Test 3.4 - Total Jitter
Test 3.5 - Deterministic jitter Test 3.6 - Random Jitter
Test 3.7 - Main Link Frequency Stability
Test 3.8 - Spread Spectrum Modulation Frequency Test 3.9 - Spread Spectrum Modulation Deviation



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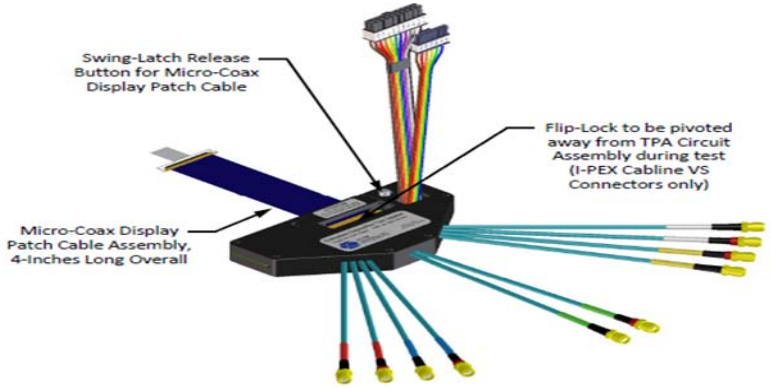
Embedded Display Port-eDP

Oscilloscope Requirements

- Option EDP requires a DPO/DSA/MSO 70K scope running firmware version
- 6.4.0 or higher and DPOJet version 6.0 or higher.
- For customers testing RBR (1.62 Gb/sec) and HBR (2.7 Gb/sec) a minimum bandwidth of 8Ghz is required.
- For customers testing HBR2 (5.4 Gb/sec) a minimum 12.5GHz BW is required.

Probing

- For customers testing RBR (1.62 Gb/sec) or HBR (2.7 Gb/sec) Qty 4 P7380 or P7380SMA are required if testing more then two lanes at one time.
- For customers testing HBR2 (5.4 Gb/sec) and HBR (2.7 Gb/sec) and RBR
- (1.62 Gb/sec) Qty 4 P7313 or P7313MA are required if testing more then two lanes at one time.
- An optional eDP fixture is available on the Tektronix PAL:TF-EDP-TPA-PRC



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Complete Tektronix DisplayPort Instrument Portfolio

Receiver/Sink Tests (Characterization) Receiver Silicon characterization and compliance testing capability to 26Gbps	**BSA125C** with JMAP and SSC and HW Options DPP 125A and CR125A provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features.	
DP Channel Tests Source and Sink electrical channel performance, Crosstalk, Impedance and return loss. High Dynamic Range instrument	**DSA8300** 80E10 TDR Sampling Module for DSA8200 Sampling Scope S-Parameter Analysis Software 80SICON Software	 
Cable Tests Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8300** 4X 80E08 TDR Sampling Module for DSA8300 Sampling Scope	
Transmitter/Source Tests Signal timing stability and SSC analysis, Transmitter AC parametric, Jitter, Amplitude.	**DSA71254C** DPOJET Jitter Analysis software SMA Adapters TCA-SMA 2 per scope Differential SMA Probe P7313SMA (optional) + DP-AUX controller + DP12 (Sw Option)+Option eDP	

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Tektronix Displayport Solution Equipment Configuration

- 1# DPO/DSA/MSO70000 C/D/DX series Real time Oscilloscope with BW >/= 12.5GHz
- Option DPTX12 SW or Opt eDP essesntials or TEK-GRL-DP-SINKSW
- 4# P7313SMA probes OR Direct SMA or Using RF Switch
- Display port Fixtures – Based on specific customer needs for normal/mini/DP++/eDP
- BertScope BSA85C with Opt STR
- DPP125A (no 4T needed)
- BSA12500ISI
- DP-AUX