PCI Express 3.0 Base Stressed Eye Calibration and Receiver Testing

Methods of Implementation using Tektronix BERTScope BSA85C Analyzer, CR125A Clock Recovery, BERTScope ISI Board, Tektronix AFG3000 Function Generator, DPP12B De-emphasis Processor, and Series 70000 Real-Time Oscilloscope

Draft Version October 1, 2012

Copyright © Tektronix. All rights reserved. Licensed software products are owned by Tektronix and are protected by United States copyright laws and international treaty provisions.

Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specifications and price change privileges reserved.

TEKTRONIX, TEK, BERTScope, and RT-Eye are registered trademarks of Tektronix, Inc.

Contacting Tektronix

Tektronix, Inc.
14200 SW Karl Braun Drive or P.O. Box 500
Beaverton, OR 97077 USA

Table of Contents

List of Figures

Revision History

Version	Date	Summary of Changes
1.0	October 1, 2012	Initial Release

1 Overview

This document provides procedures for PCI Express Generation 3.0 Base Receiver testing using Tektronix instruments. This procedure will focus mainly testing and calibration of 'Long Channel' Stressed Voltage in accordance with the PCI Express Generation 3.0 Base specification requirements. This document is based on the PCI Express Base Specification, Rev 3.0(November 10, 2010).

For Base Calibration, there are two calibration approaches that may be used---simulation or measurement. This MOI describes the *measurement* calibration method.

Although, this BASE calibration and testing can be stepped through manually, it is **HIGHLY RECOMMENDED** that the BERTScope PCIE Automation Software is used to aid calibration.

2 Equipment and Software Requirements

Base Testing defines a **Stressed Voltage Test** (shown below):

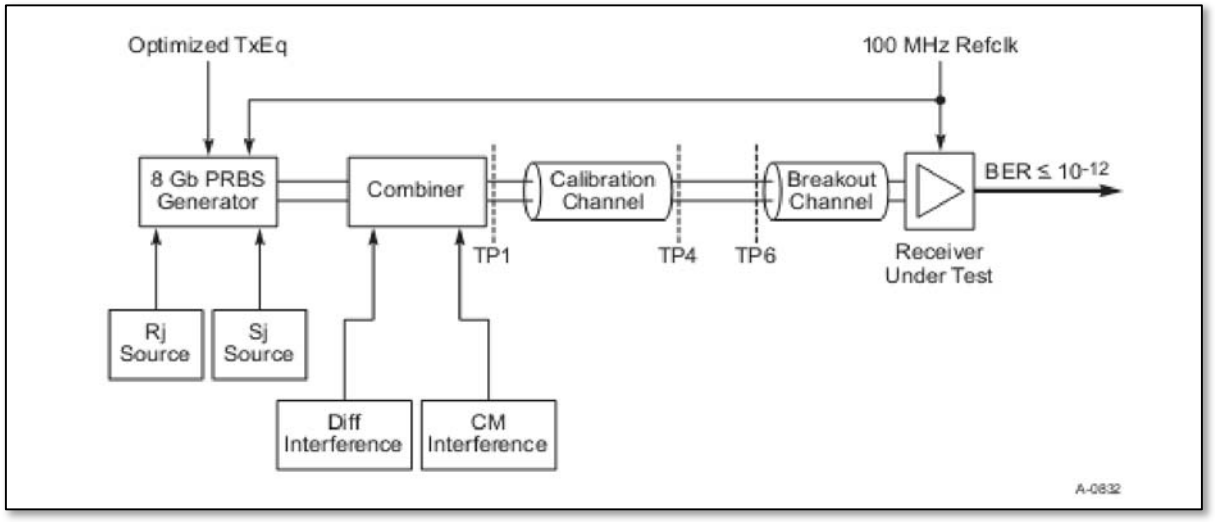


Figure 1: Stressed Voltage Calibration test configuration

The **BERTScope BSA85C** will generate required patterns, *RJ Source*, *SJ Source*, and *Diff Interference* (in conjunction with combiner). Optimized TxEQ will be generated with **BERTScope Digital Pre-emphasis Processor (DPP).** The **BERTScope ISI Board** will generate *Calibration Channel* and *Breakout Channel*. In conjunction with Combiner, the **Tektronix Arbitrary Waveform Generator** will be used to generate *CM Interference*.

Further description of equipment follows:

2.1 *BSA85C Bit Error Ratio Analyzer*

The BERTScope BSA85C Bit Error Ratio Analyzer provides test and calibration data patterns, and several jitter sources required for Base testing. Option STR (Stressed Eye) is required for receiver testing.

Figure 2: BERTScope BSA85C Bit Error Ratio Analyzer

2.2 *CR125A Clock Recovery Instrument*

The BERTScope CR125A Clock Recovery instrument is used to recover a synchronous clock from the TX data retransmitted from the DUT. (The recovered clock may also be used as a synchronous full rate clock input to the pattern generator in cases where a full rate synchronous clock is not available from the DUT). The instrument allows full control of parameters including loop bandwidth, peaking/damping, and roll-off.

Figure 3: BERTScope CR125A Clock Recovery Instrument

2.3 *DPP125B Digital Pre-Emphasis Processor*

The BERTScope Digital Pre-emphasis Processor DPP125B takes in single-ended data and clock inputs and conditions the signal by adding controllable amounts of pre-emphasis.

Figure 4: BERTScope DPP125B Digital Pre-Emphasis Processor

2.4 *BERTScope ISI Board*

The BERTScope ISI Board, which has multiple trace lengths, generates calibrated amounts of Intersymbol Interference.

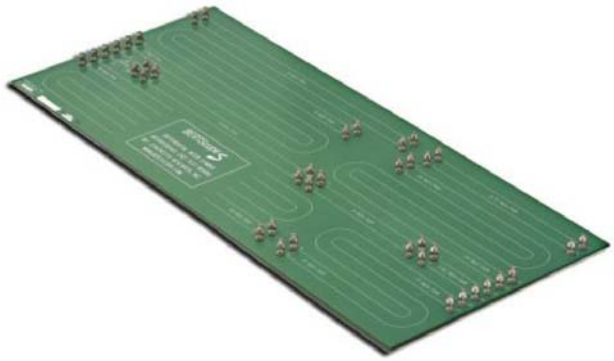


Figure 5: BERTScope ISI Board

2.5 *Real-Time Oscilloscope*

A Real-Time Oscilloscope is used for calibration of the PCIe Gen 3 stress levels. The procedures detailed in this MOI are based on the use of a Tektronix DPO/DSA70000, MSO70000 Series real-time oscilloscope. The Oscilloscope captures critical signal information with a four-channel system bandwidth of 20 GHz, combined with high waveform capture capability. Note that jitter analysis requires that SIGTEST software be installed on the oscilloscope, as described in Section 2.7.

Figure 6: DPO/DSA70000, MSO70000 Real-Time Oscilloscope

2.6 *BERTScope Calibration Software*

It is highly recommended that the BERTScope software package is used to aid with calibration. The following applications will be needed:

- PCIe Gen3 Automation Software
- Visa Socket Gateway
- SigTest Server

Please refer to your Tektronix Representative for information regarding the above software.

2.7 *PCISIG SIGTEST Analysis Software*

SIGTEST software is required for BASE stress calibration. It is recommended that SigTest be installed on the Real-Time Oscilloscope that is used for calibration.

SIGTEST software is available directly from the PCISIG, and may be downloaded at: http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library.

2.8 *Combiner*

Differential-Mode Interference (DMI) and AC Common Mode are added to the stressed Rx test pattern as required by the Base test specification. When using the single-ended Sinusoidal Interference (SI) output of the BERTScope Analyzer, the Combiner can be used to meet requirement for DMI. The Tektronix Arbitrary Function Generator (AFG), described below, will be used to generate AC Common Mode. The following components can be configured to provide the required DMI and AC Common Mode:

- A balun (e.g. MiniCircuits NCS1-292+/WTB-419+) to convert the single-ended SI output to a differential signal
- Two pickoff tees (e.g. Picosecond 5371-112)
- Two Directional Couplers
- Power Divider

2.9 *Arbitrary Function Generator (AFG)*

The AFG is used to provide AC Common Mode stress required by the Base test specification. The AFG will be used to generate a 120MHz sinusoid which will be applied data.

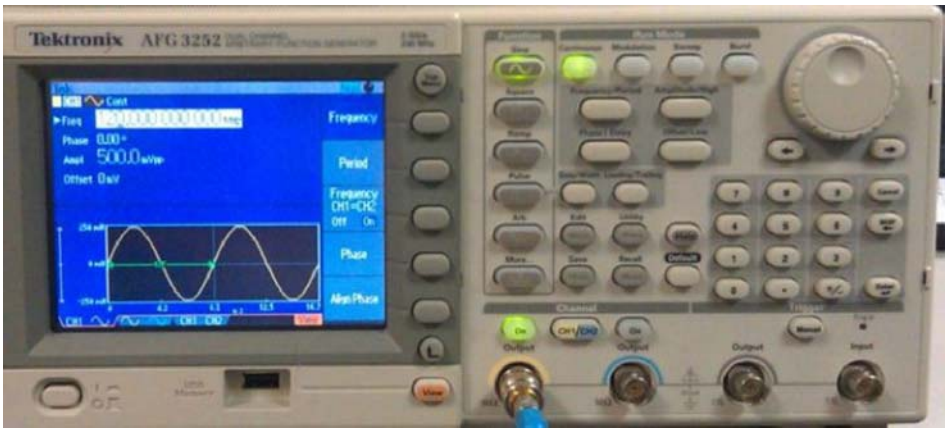


Figure 7: Arbitrary Function Generator (AFG)

3 Receiver Jitter Tolerance Test: Stressed Voltage

IMPORTANT: The section details the procedure for *testing* the BASE specification. It is assumed that calibration has been completed and the stressed calibration configuration has been saved. A detailed procedure for calibration can be found in Section 4: Appendix A of this document.

For Stressed Voltage, a BER of 1E-12(with 95% confidence) or better is required at a fixed SJ frequency of 100MHz.

3.1 Stressed Voltage Receiver Testing

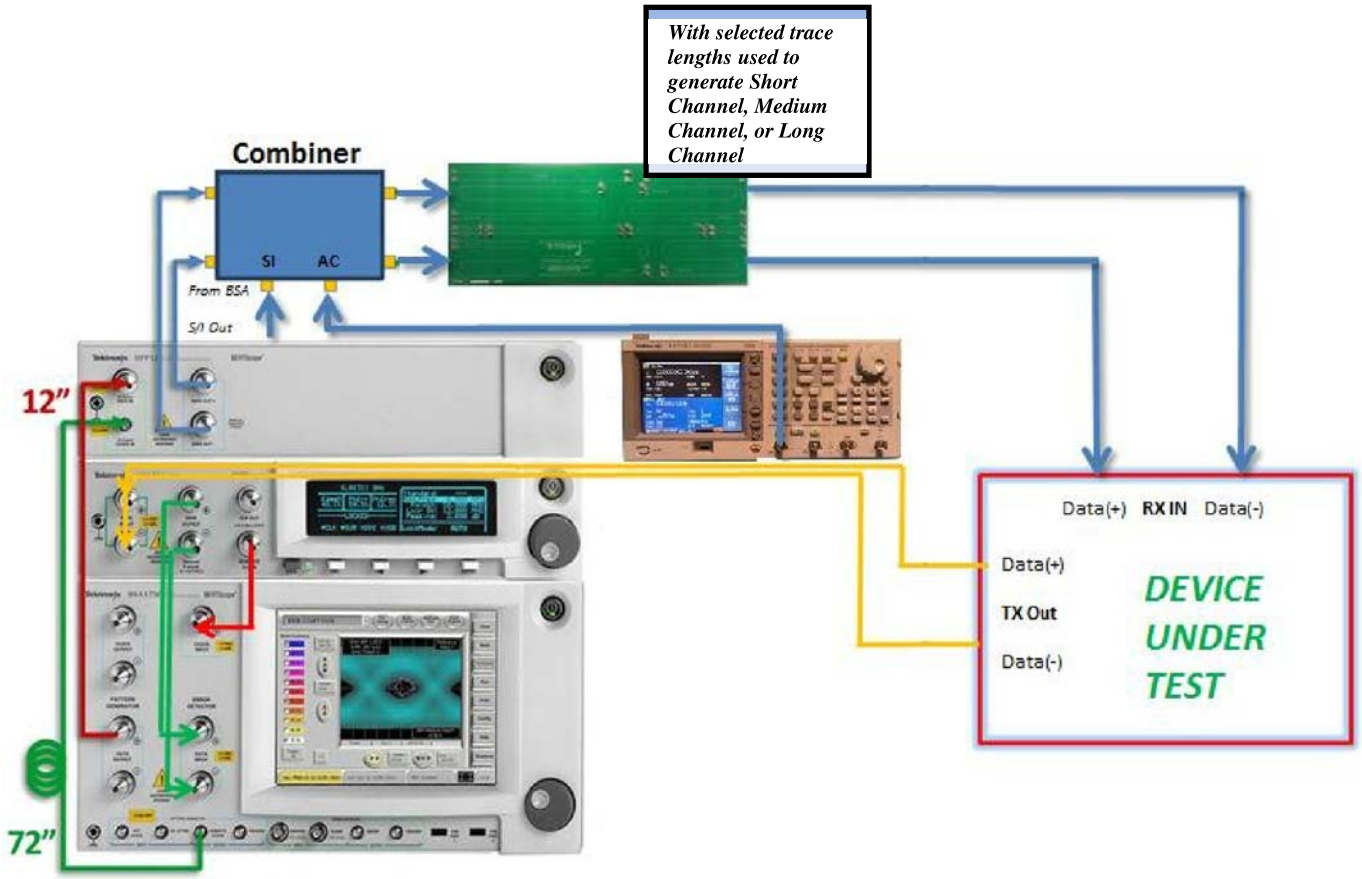


Figure 8: Basic Stressed Voltage test configuration. ***Note****: The ISI Board will have the appropriate trace lengths selected depending on whether testing long channel, short channel, or medium channel*

3.1.1 Stressed Voltage Equipment Connections (detailed cable connections):

a. **Connect** BSA Data Out+ to DPP Data In. The cable length should be approximately 12″.

b. **Connect** BSA Sub-rate Clock Out to DPP Clock In. The cable length should be approximately 72″.

c. **Connect** the DUT TX output to CR Data Inputs using a phase-matched SMA cable set.

d. **Connect** CR Data Out (+/–) to BSA Detector Data In (+/–) using a phase-matched SMA to SMA cable set.

e. **Connect** CR Sub-rate Clock Out to BSA Detector Clock In.

f. **Connect** the DPP Data Out (+/–) to the input of the Combiner (+/–) using a phase-matched SMA to SMA cable set.

g. **Connect** the Combiner Out (+/–) to input of the BERTScope ISI Board

h. **Connect** the output of the ISI Board to DUT RX input channel

i. **Connect** the 'SI Output' on the rear connector panel of the BSA to the SI Input of the Combiner.

j. **Connect** CH1 of Arbitrary Waveform Generator to Combiner AC Common Mode Input. Enable CH1 to appropriate frequency and amplitude that were developed during calibration.

NOTE:

- *The outputs of the DPP unit are AC-coupled, and therefore do not require DC blocks.*

3.2 Select Test Configuration

Load the BERTScope configuration file that was saved at the end of the calibration procedure detailed in Section 5: Appendix A. (The configuration will load the appropriate patterns on the Pattern Generator and Error Detector. In addition, all calibrated stress values and equipment settings will be recalled.)

a. From the BERTScope Analyzer local control interface, **select** ***Config → Restore Configuration*****:**

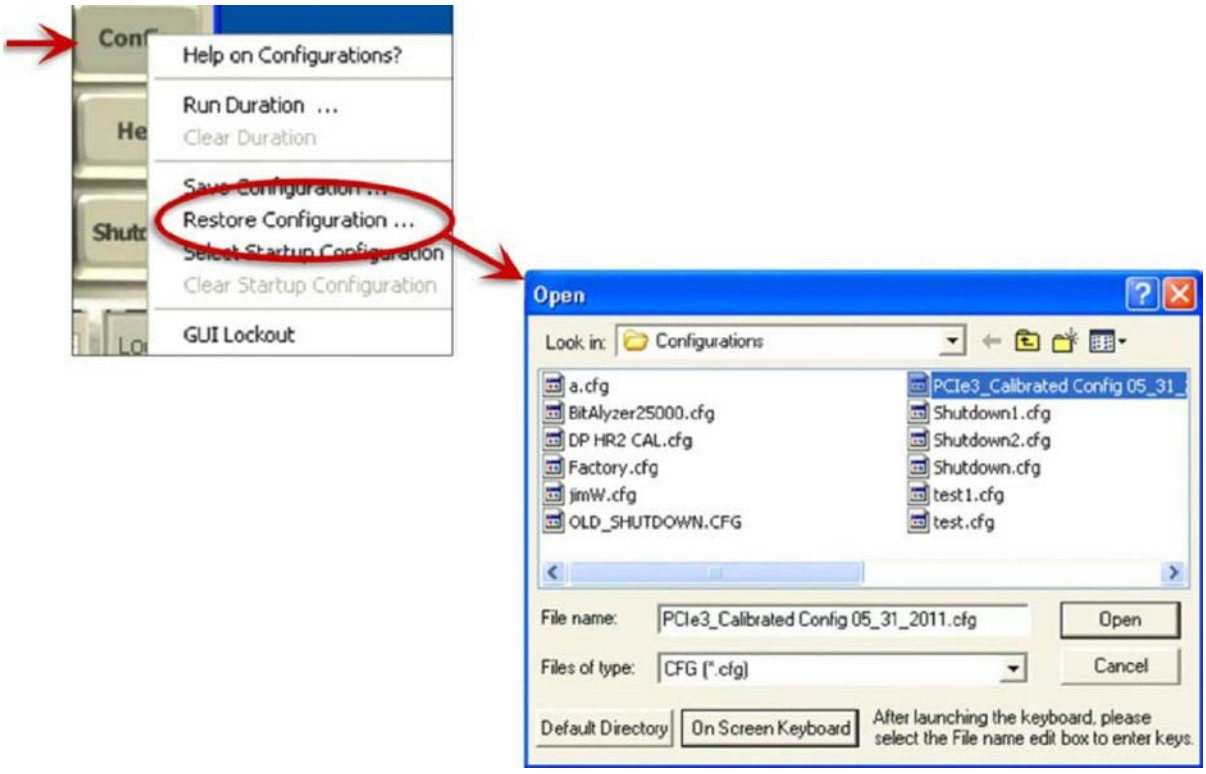


Figure 9: Select saved Base Calibration configuration. Restoring configuration will load appropriately calibrated stresses and patterns. (See Appendix A for complete procedure for Base calibration.)

3.2.1 Check Detector Synchronization

a. **On the BERTScope Detector** page, **click** *Auto Align* to optimize the detector sample point: ***View → Detector → Auto Align***

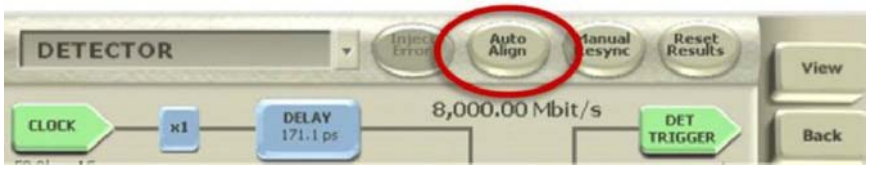


Figure 10: Auto Align to Optimize Detector Sample Point

If the setup has achieved the appropriate loopback mode, then Detector should be synchronized to the *Modified Compliance Pattern* that restoring configuration loaded into the Pattern Generator.

b. **Confirm** Detector synchronization by switching to the Detector Page, and confirming that the ERROR DETECTOR box indicates that it is synchronized to the "User" pattern. The Error Detector should indicate '**Detected**: **User**' (this indicates the user pattern has been synchronized.)

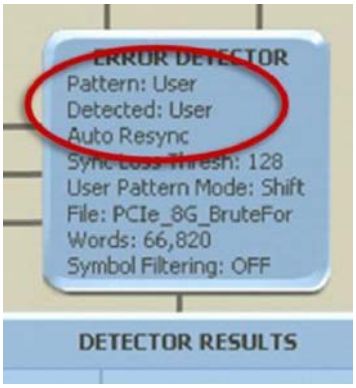


Figure 11: Check that Detector is in Sync

3.3 Loopback Tips

- If the BER from the DUT is too high, it will appear as if the DUT were not in loopback. (If BER greater than 1E-3 or so, then the BERTScope will tend to indicate that it is not synchronized.) Some tips to try:
  - Try adjusting Rx EQ settings on DUT receiver
  - Try adjusting DPP pre-shoot/de-emphasis settings. For Base Testing, Preset 7 is allowed for Long Channel and Presets 4 is allowed for Medium and Short Channel
  - Try an alternate, shorter pattern like PRBS-7 to determine if DUT is in loopback, but simply generating significant errors.

- Try decreasing impairments. This can be done on the *Stressed Eye* Page. It is suggested that Stresses be turned to 0% UI, but not disabled

3.4 BER Testing

With the DUT in loopback and the BERTScope Analyzer synchronized to the *Modified Compliance Pattern,* the compliance test may now be performed:

3.4.1 Perform Compliance Test

a. **Select** the *Detector Page* on BERTScope ***View → Detector***

b. **Reset** the '*Detector Results'* panel by clicking on the 'Reset Results' button.

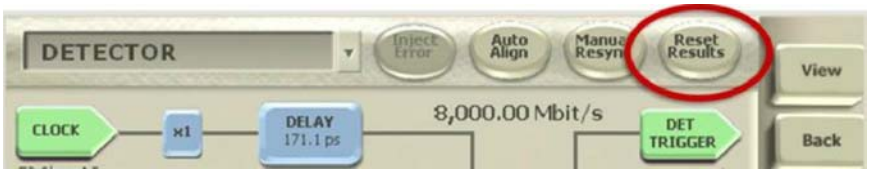


Figure 12: Reset Detector Results

c. **Start** the test by clicking on the Run button.

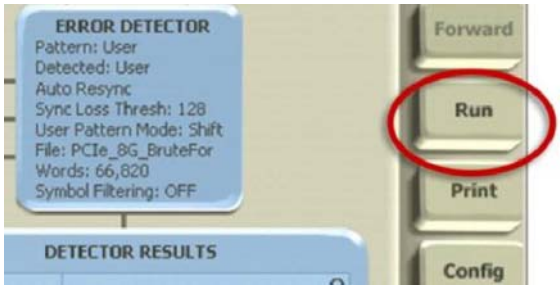


Figure 13: Click the Run Button to Start Test

d. **Stop** the test when the Bit count reaches 1 x 10^{12} bits by clicking on the Run button a second time.

e. **Verify** that the Detector counted no more than one (1) error.

NOTE:

- *The user may wish to set the "Run Duration" to 2 minutes, 5 seconds, to have the BERTScope automatically stop the test when the correct number of bits has been evaluated.*

4 Appendix A: Stressed Voltage Eye Calibration

Base Testing specifies Stressed Voltage Calibration (shown below) and Swept Jitter Calibration. The calibration will focus mainly on Stressed Voltage Calibration with Long Channel (-20dB).

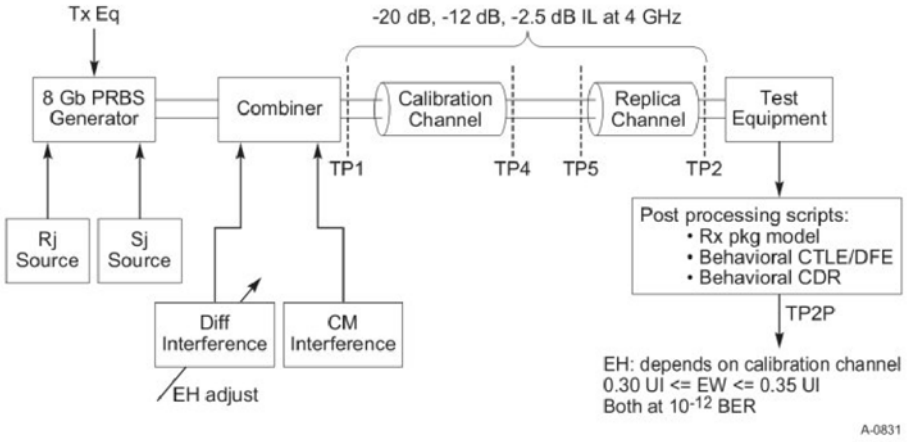


Figure 14: Block Diagram Stressed Voltage Calibration Setup

Table 4-22: Stressed Voltage Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800	mVPP	Measured at TP1 Figure 4-65. $V_{RX-LAUNCH-8G}$ may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mVPP.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mVPP	Eye height @ BER=10^{-12}. Notes 1,2.
$T_{RX-SV-8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER=10^{-12}. Note 2
$V_{RX-SV-DIFF-8G}$	Differential mode interference	14 or greater	mVPP	Adjusted to set EH. Frequency = 2.10 GHz. Note 3.
$V_{RX-SV-CM-8G}$	Rx AC Common mode voltage at TP2P	150 (EH < 100 mVPP) 250 (EH ≥ 100 mVPP)	mVPP	Defined for a single tone at 120 MHz. Note 3.
$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.
$T_{RX-SV--RJ-8G}$	Random Jitter	2.0	ps RMS	Rj spectrally flat before filtering. Notes 4,5.
$V_{RX-MAX-SE-SW}$	Max single-ended swing	±300	mVP	Note 6.

Notes:

1. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the Rx DUT is capable of equalizing over a range of channel loss profiles. The test also guarantees the Rx is capable of operating over a sufficient dynamic range of eye heights. The "SV" in the parameter names refers to stressed voltage.
2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ are referenced to TP2P and are obtained after post processing data captured at TP2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.
3. $V_{RX-SV-DIFF-8G}$ measurement is made at TP2 without post processing. $V_{RX-SV-CM-8G}$ may be made at either TP1 or TP2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
4. $T_{RX-SV-SJ-8G}$ and $T_{RX-SV-RJ-8G}$ measurements are made at TP1 without post processing.

Figure 15: Stressed Voltage Eye target parameters

Listed below are steps to be followed for the Stressed Voltage Calibration:

Step	Calibration	Test Point
1	**Clock/Data Skew Calibration**	N/A
2	**DPP Amplitude Equalization**	TP1
3	**Launch Amplitude Calibration**	TP1
4	**TXEQ Calibration**	TP1
5	**Random Jitter Calibration**	TP1
6	**Sinusoidal Jitter Calibration**	TP1
7	**Channel Calibration**	TP3 –TP4
8	**Differential Mode Inter. Calibration**	TP2
9	**AC Common Calibration**	NA
10	**SigTest Template**	N/A
10	**Eye Width**	TP2P
11	**Eye Height**	TP2P

4.1 *Stressed Eye Calibration Software*

The calibration may be aided by using *Tektronix PCIe 3.0 Receiver Testing Software*. ***It is strongly recommended that the automation software be utilized as it contains the latest procedures from both Tektronix and the PCI SIG***. The MOI will illustrate general techniques for manual calibration, but may not be updated in a timely manner.

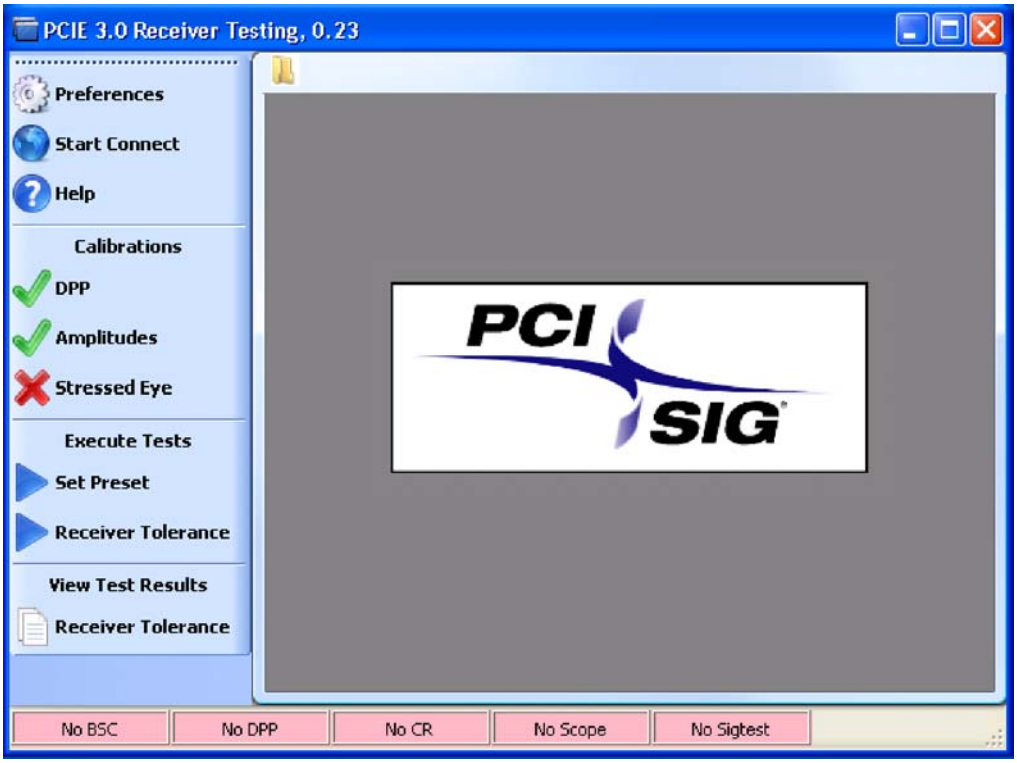


Figure 16 Tektronix PCIe 3.0 Receiver Testing Software Home Screen

4.2 *Set DPP Clock to Data Skew*

To correctly compensate for the delay in the Data Out vs. the Sub-rate Clock output from the BERTScope, the cable interconnecting the Sub-rate Out to the DPP125B should be approximately 1.6 meters (60 inches) longer than the cable connecting the BERTScope Data Out to the DPP125B Data In. With the additional cable length providing the rough delay match, use the calibration method described below to fine tune the delay match to ensure optimum DPP timing.

4.2.1 Connection and configuration for clock-to-data skew optimization

4.2.1.1 Connect the DPP125B to the BERTScope Analyzer.

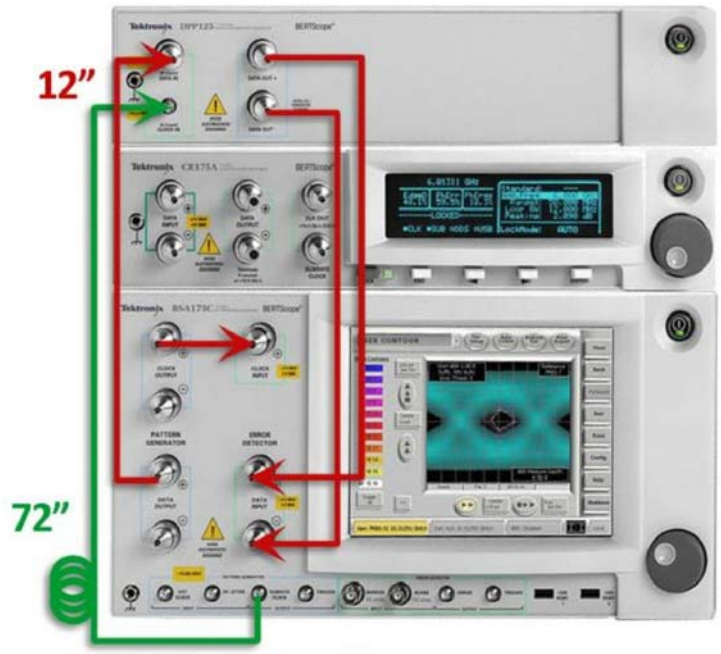


Figure 17: DPP Timing Calibration Connections

a. **Connect** the BERTScope Generator Data(+) Output to the DPP125B Data Input using a cable approximately 0.3 m (12″) long.
b. **Connect** the BERTScope Generator’s Sub-rate Clock Out to the DPP125B Clock In, using a cable approximately 1.8 m (72″) (This should be 60” longer or 72”) longer than the data cable.
c. **Loop back** the DPP125B Outputs to the Analyzer Error Detector Inputs.
d. **Connect** BSA Clock Out to Error Detector Clock In.
a. **Enable** SJ. ***(View → Stressed Eye → Sine Jitter → Enable)***
b. **Set** SJ amplitude to 30 %UI.
c. **Set** SJ frequency to 100 MHz
e. **Enable** RJ. ***(View → Stressed Eye → Random Jitter → Enable)***
f. **Set** RJ amplitude to zero. “*Intrinsic Limit”* will be indicated.

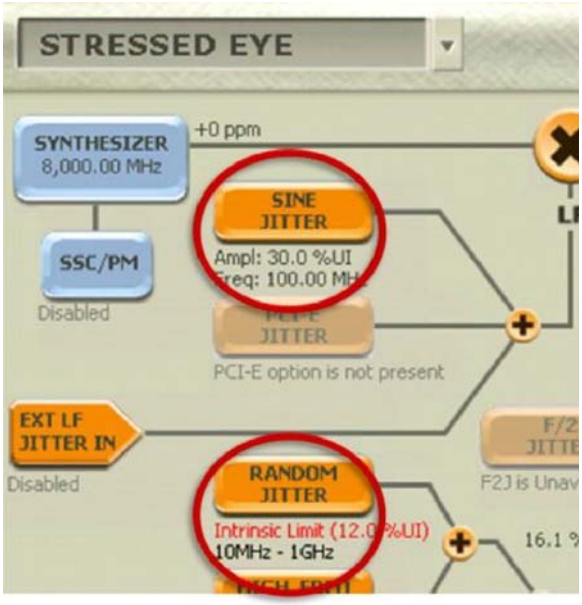


Figure 18: Set Stress Levels

4.2.1.2 Calibrate to remove the Clock to Data delay

a. **Set** the *Generator Delay* to 125ps: ***View → Generator → Delay***

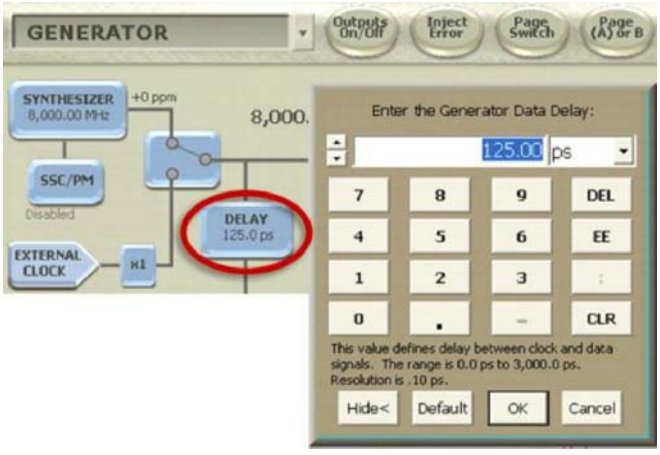


Figure 19: Set Generator Delay

b. In the BERTScope Detector view, **check** for error free operation (click Run to begin error counting). If not operating error free, advance the Generator delay to 183 ps. Verify that the Detector is operating error free at this point. Record the Generator Delay.

c. Once error free operation is obtained, **find** the boundary between error free and errored operation by ***decreasing*** the Generator Delay and using a binary search method as shown in Figure 21 below. Record the Generator Delay.

d. **Return** the Generator Delay to the error free point found in Step 2.

e. **Find** the boundary between error free and errored operation by ***increasing*** the Generator Delay and using a binary search as shown in the figure below. Record the Generator Delay.

f. **Set** the Generator Delay to the average of the Delay values found in Steps [c] and [e]. Record this Generator Delay value for later use in creating a Calibration Configuration file.

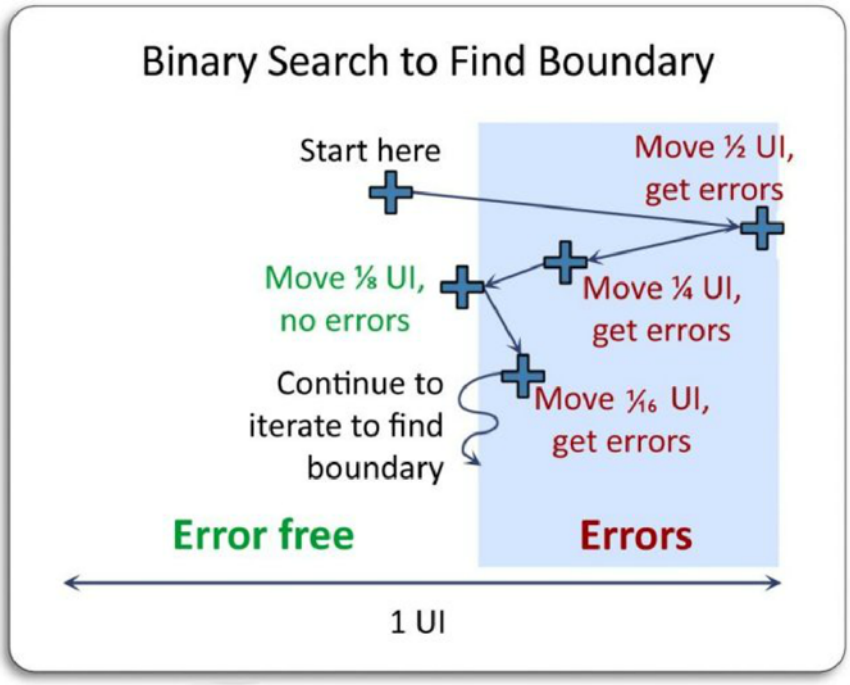


Figure 20: Find Optimum Delay

4.2.1.3 Record Generator Delay value

a. Following completion of the Clock to Data skew calibration, **record** the BERTScope Generator Delay setting for use in the Calibrated BERTScope Configuration file.

4.3 Amplitude, Jitter, and TxEQ calibrations @ TP1

The following calibrations will be done at **TP1**:

- **Amplitude Equalization:** Equalize the low frequency and high frequency signal amplitudes at the end of the SMA cables that connect to the BERTScope ISI Board
- **Launch Amplitude**: Generator launch amplitude *after* combiner should be 800mV
- **TxEQ:** calibration of pre-shoot and de-emphasis for optimized Preset 7 and Preset 4
- **SJ:** calibration of Sinusoidal Jitter (target 0.1UI @ 100MHz)
- **RJ:** calibration of Random Jitter (target 2.0ps RMS)

4.3.1 Required Equipment

Stress and DPP amplitude calibrations require the following equipment:

- BERTScope BSA85C
- BERTScope DPP125B
- DPO/DSA70000, MSO70000 Real-Time Oscilloscope with SIGTEST installed
- Cables, as indicated in diagrams

4.3.2 Test Equipment Connections

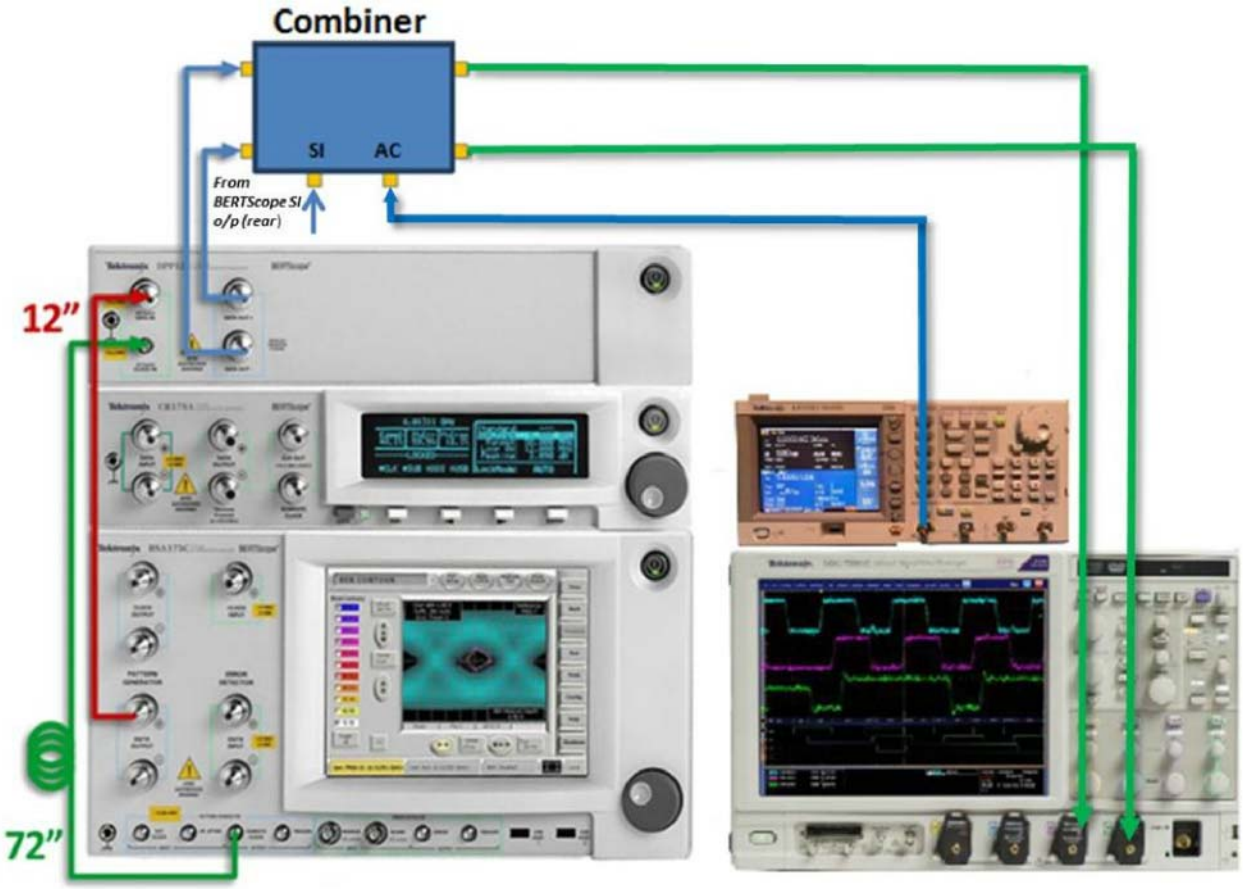


Figure 21: Stress Configuration setup for Stressed Voltage

4.3.2.1 Connect BERTScope to DPP

a. **Connect** BSA Generator Data Out+ to DPP Data In using the short (12″) cable.

b. **Connect** BSA Generator Sub-rate Clock Out to DPP Clock In using 72" cable

4.3.2.2 Connect DPP to Combiner

a. **Connect** DPP Data (+) to Combiner Data In (+).

b. **Connect** DPP Data (-) to Combiner Data In (-).

4.3.2.3 Connect AFG/BERTScope to Combiner

a. **Connect** AFG CH1 Output to Combiner AC Common Mode Input. Do not Enable CH1 at this point.

b. **Connect** the BERTScope 'SI-Out' (in rear of BERTScope) to the Combiner SI Input.

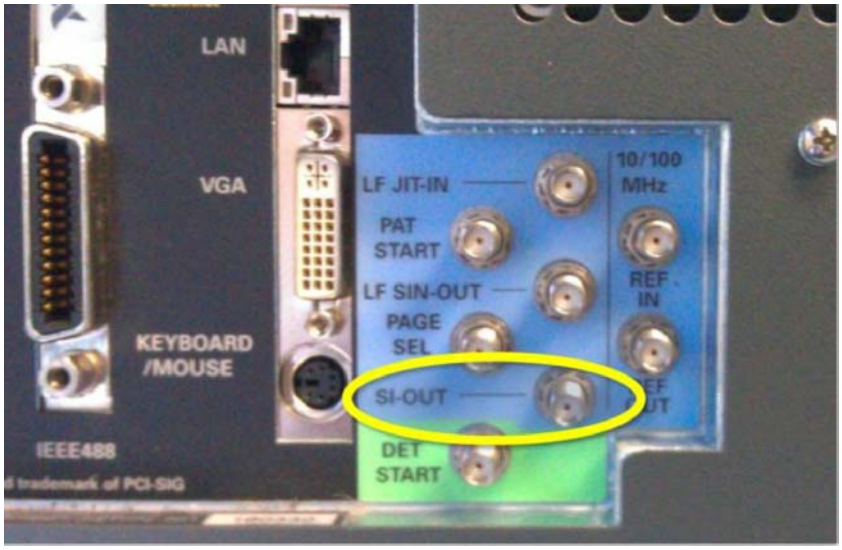


Figure 22: BERTScope Rear Panel with SI-Out highlighted. SI-Out should be connected to SI Input on Combiner. The BERTScope SI-Out will generate a 2.1GHz sine wave needed for Differential Mode Interference.

4.3.2.4 Connect Combiner to RT Scope

a. **Connect** Data(+) Out from Combiner to CH3 on RT Scope
b. **Connect** Data(-) Out from Combiner to CH4 on RT Scope

4.3.3 Calibrate DPP Output Amplitude@ TP1

Calibration of DPP Output will involve two steps:

- **Equalize** low frequency and high frequency signal amplitudes at **TP1.** A small of amount of de-emphasis is added at this step to ensure that high frequency components and low frequency components have the same amplitude at the output of the Combiner.

- **Set** 800mV Launch Amplitude required at **TP1**.

4.3.4 BERTScope Setup

a. **Load** the BERTScope Pattern Generator with the user pattern "256 bit pattern (64 one's, 64 zero's and a 128 bit clock pattern" ***(View → Generator → Load User File)***
b. **Configure** the BERTScope for Internal Synthesizer for 8 GHz

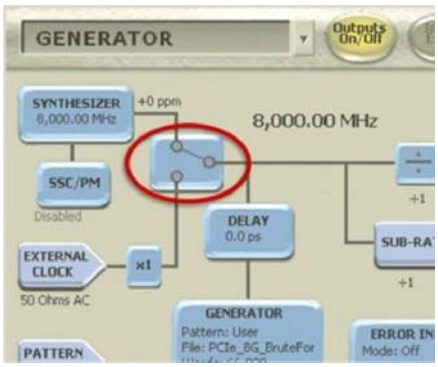


Figure 23: Set Internal Synthesizer

4.3.5 DPP Setup

a. **Load** DPP Configuration "Preset 4" (no pre-shoot, no de-emphasis; PCIe_P4_0dB.dpp) via the DPP control view on the BERTScope ***(View → DPP Control → Standard Config → Restore Config)***

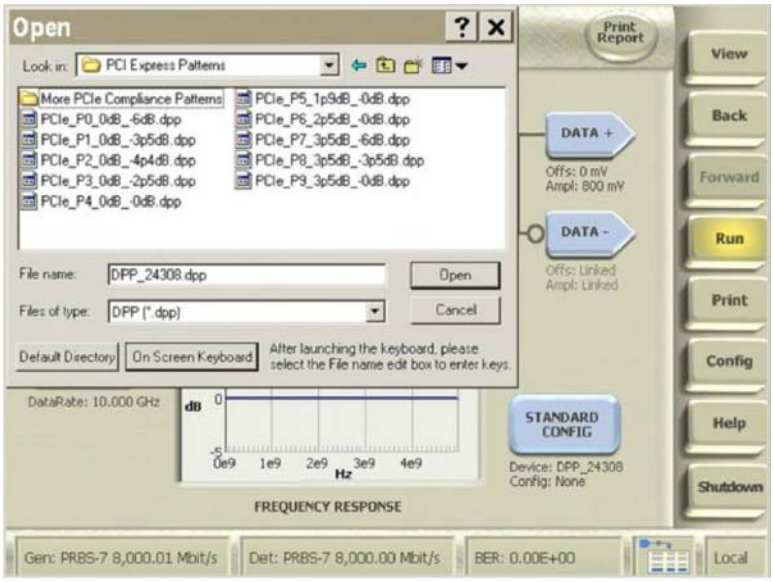


Figure 24: Load DPP Pattern Preset 4

4.3.6 RT Scope Setup

4.3.6.1 Press the "Default Setup" button on the oscilloscope front panel. Ensure these connections are in place:

a. Cable from Combiner Data Output (+) to the oscilloscope Channel 3.
b. Cable from Combiner Data Output (-) to the oscilloscope Channel 4.

4.3.6.2 Configure oscilloscope Acquisition Mode to "Averaging". See Figure 26 for details:

a. Click *Horiz/Acq* menu at top of screen.
b. Click *Horizontal/Acquisition Setup*.
c. Click *Acquisition* tab.
d. Set the Acquisition Mode by clicking “Average”. Set #of Wfms=16.

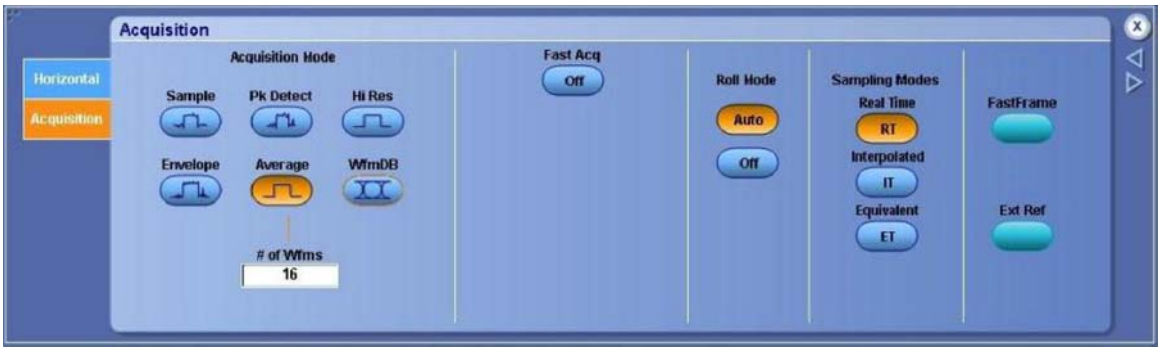


Figure 25: Oscilloscope Acquisition Mode Configuration

4.3.6.3 Configure oscilloscope Sample Mode to "Real Time Only".

a. Click *Horiz/Acq* menu at top of screen.
b. Scroll down and click *Sampling Modes*.
c. Click "Real Time Only"

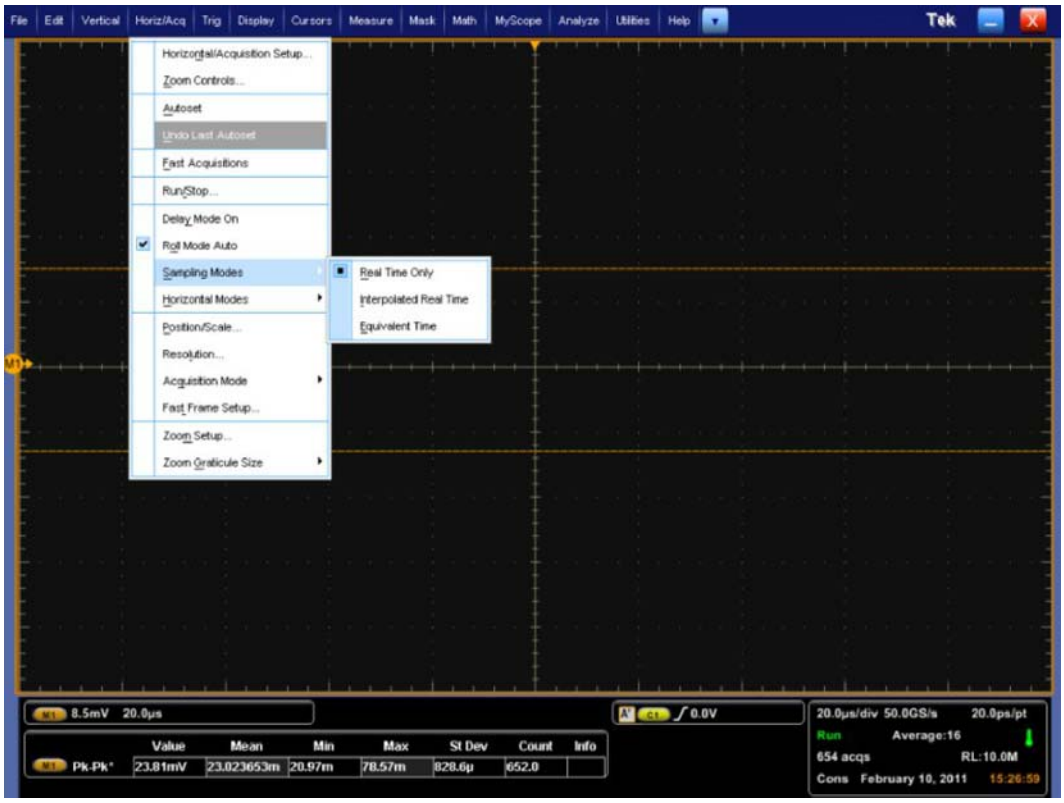


Figure 26: Configuring Oscilloscope Sample Mode

4.3.6.4 Set the Trigger type

a. Click *Trig* menu at top of screen
b. Scroll down and click *A_Event (Main) Trigger Setup…*
c. Set Trigger Type to "Timeout"
d. Set Source to the applicable channel.
e. Leave other settings (e.g. Level, Timer, Trigger When…) as default values

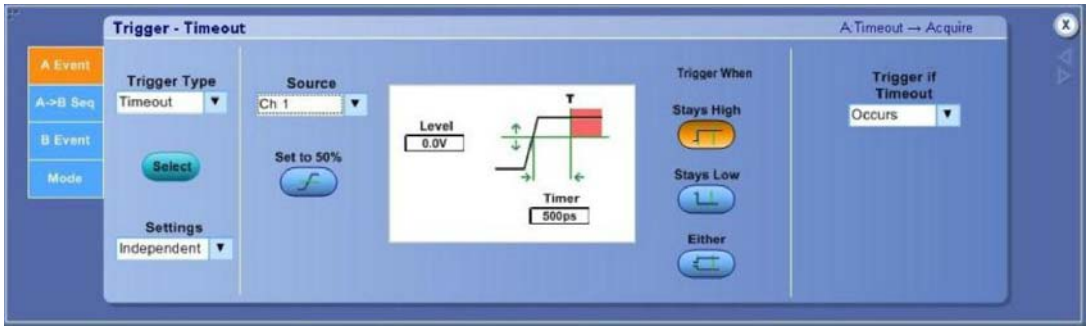


Figure 27: Set Trigger type as 'Timeout'.

4.3.6.5 Configure the oscilloscope so both Channel 3 and 4 are displayed and fill the screen vertically.

a. Display Channel 3 and Channel 4 by turning both on via oscilloscope front panel.
b. Begin by adjusting the vertical scale (via the "Scale" buttons on the front panel) of both channels so the signals fill the screen, but no clipping results. Ensure the same scale setting is used for both channels.
c. Next, refine the vertical scaling to fill the screen by clicking the *Vertical* menu at the top of the screen followed by the *Vertical Setup* menu. Again, ensure the same scale setting is used for both channels.

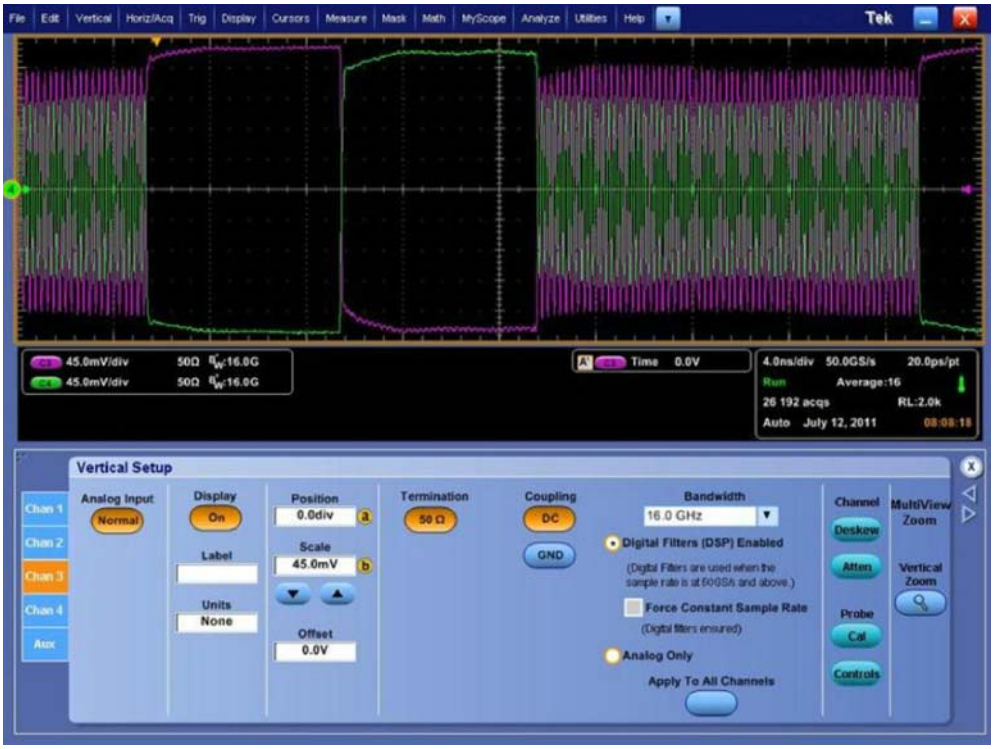


Figure 28: Vertical Setup Menu Displaying Example Configuration

d. Continuing with the Vertical Setup by ensuring Position and Offset values are zero for both channels.
e. Set the Bandwidth by clicking “Digital Filters (DSP) Enabled” and “16 GHz” followed by the “Apply to All Channels” button. Again, ensure there is no clipping.
f. Figure 30 provides an example of properly displayed Channel 3 and Channel 4 signals.

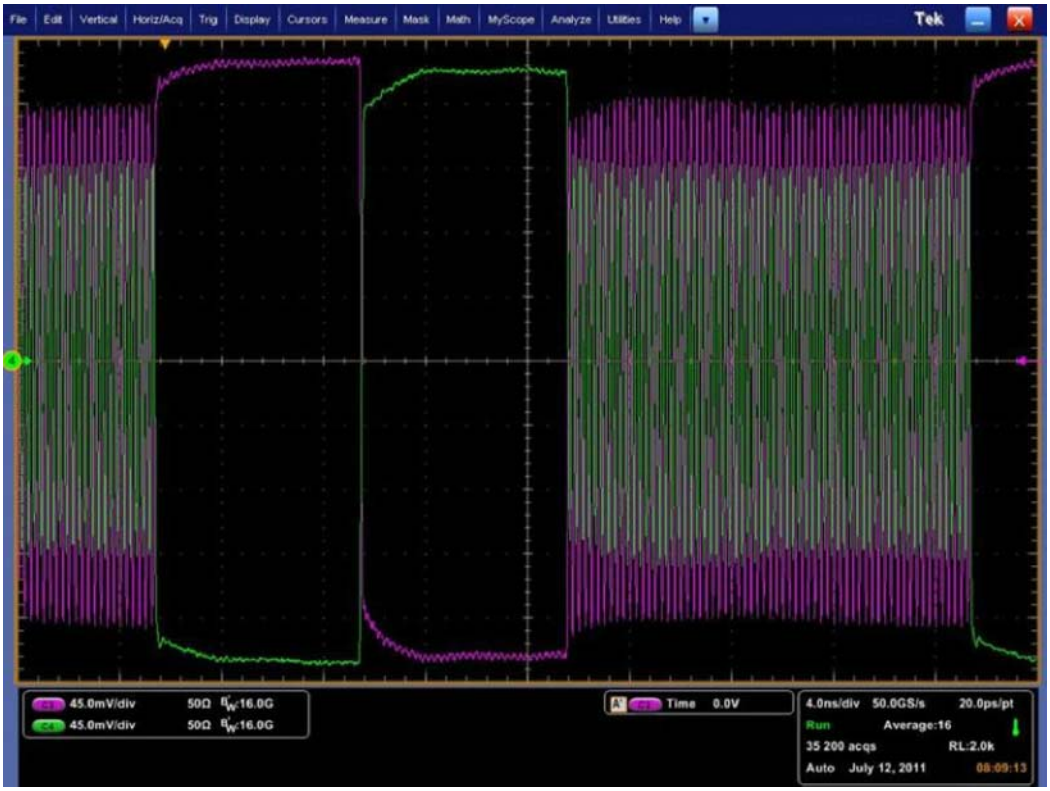


Figure 29: Example of Properly Displayed Oscilloscope Channels

4.3.6.6 Configure and display the oscilloscope’s Math waveform.

a. Click *Math* menu at top of the screen.
b. Click *Math Setup* menu.
c. Set Math1 function to “Ch3-Ch4”. Click Display ON to display math waveform.
d. Ensure Math1 Position=0.
e. Turn Channel 3 and Channel 4 display off via the oscilloscope front panel. Math1 will now be displayed.

4.3.6.7 Configure the DPP

a. Set DPP Precursors and Post-cursors such that de-emphasis is set 0 dB. (Set tap settings on DPP to 1 0 0 0.)
b. Adjust the Post-Cursor value until the amplitude of the low frequency and high frequency portions of the pattern are equal in amplitude. Position the oscilloscope's horizontal cursors along the mean portion of the high frequency signal, and adjust Post-Cursor until the low frequency signal is equivalent in amplitude. **Note:** This is only performed at the upper portion of the signal.
c. Record the resulting Post Cursor value.

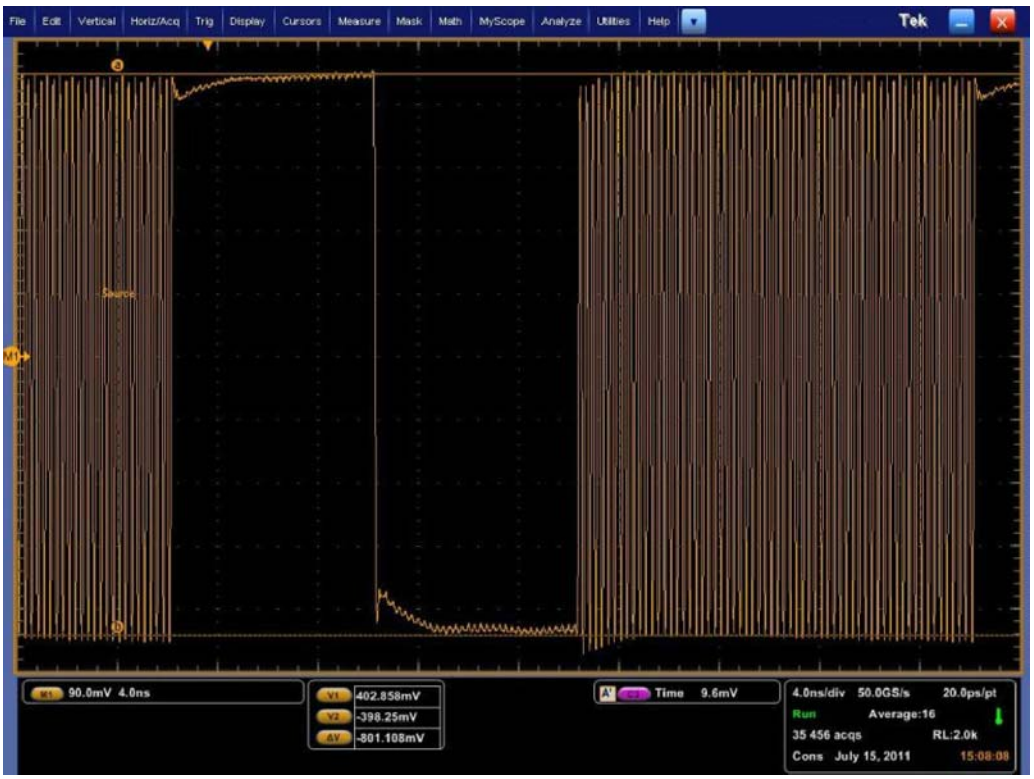


Figure 30: Properly Equalized Low and High Frequency Amplitudes

4.3.6.8 Measure the peak-to-peak amplitude of the math function being displayed.

a. Manually position the oscilloscope's horizontal cursors along the upper and lower portions of the signal.
b. View the resulting V_{ampt} (ΔV as measured by the horizontal cursors) value.
c. **Adjust** the DPP amplitude until the RT Scope measures 800 mV. (The DPP should be set to approx. 400mV single-ended on the DPP.)

NOTE: Upon changing the DPP Amplitude value, it may be necessary to wait a period of time for the oscilloscope mean value to settle.

4.3.6.9 Record the resulting DPP Amplitude value.

4.3.7 TX Equalization(TX_EQ) Calibration @ TP1

This procedure calibrates the following:

1) Preset 7: -3.5dB pre-shoot and -6dB de-emphasis
2) Preset 4: 0dB pre-shoot and 0dB de-emphasis

Base calibration uses Preset 7 and Preset 4. This procedure will focus on Preset 7 which requires de-emphasis and pre-shoot. A Preset 7 configuration will be loaded onto the DPP and the pre-shoot and de-emphasis will be fine-tuned as needed.

Detailed Method

4.3.7.1 BSA Setup

a. Pattern Generator by ***VIEW > Generator > Load User File***

4.3.7.2 DPP Setup

a. **Load** pre-stored Preset 7 (3.5dB pre-shoot, -6dB de-emphasis) from ***VIEW > DPP Control > Standard Config > Restore Config***

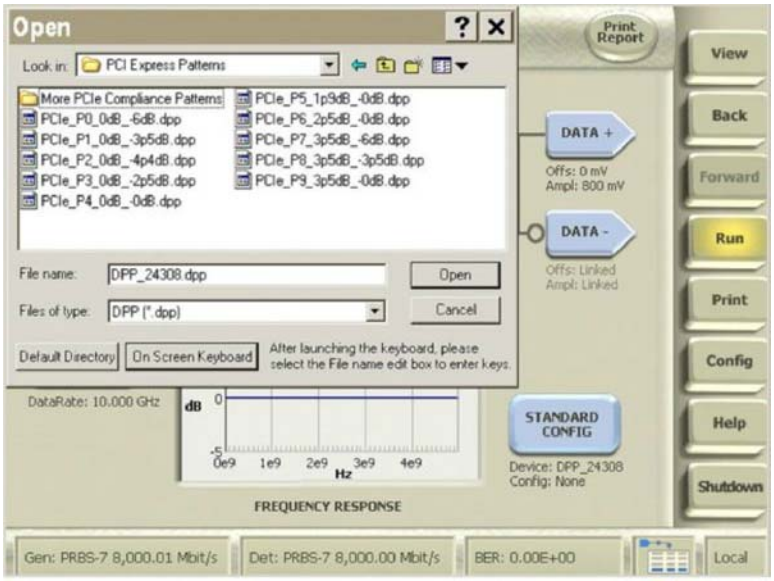


Figure 31: DPP Preset Selection

Note: After enabling Preset**,** use the oscilloscope horizontal cursors to verify ΔV is still 800 mV. Adjust DPP Amplitude slightly if required.

4.3.7.2.1 Configure oscilloscope Acquisition Mode to "Averaging". See Figure 25 for details.

a. Click *Horiz/Acq* menu at top of screen.
b. Click *Horizontal/Acquisition Setup*.
c. Click *Acquisition* tab.
d. Set the Acquisition Mode by clicking "Average". Set #of Wfms=16.

4.3.7.2.2 Refer to Figure 25 34 to understand voltages to be measured via the oscilloscope. Calculate De-emphasis and Preshoot Ratio's.

a. De-emphasis = 20 log [V_b/V_a]
b. Pre-shoot = 20 log [V_b/V_c]

4.3.7.2.3 Adjust the DPP Pre-Cursor and Post-Cursor values until the De-emphasis and Pre-shoot Ratio's above result in Pre-shoot of 3.5 dB ± 0.1 dB and de-emphasis of -6 dB ± 0.1 dB

4.3.7.2.4 Record tap values Pre-Cursor and Post-Cursors. Also, record the DPP Amplitude values for use in Eye Height and Width Calibration.

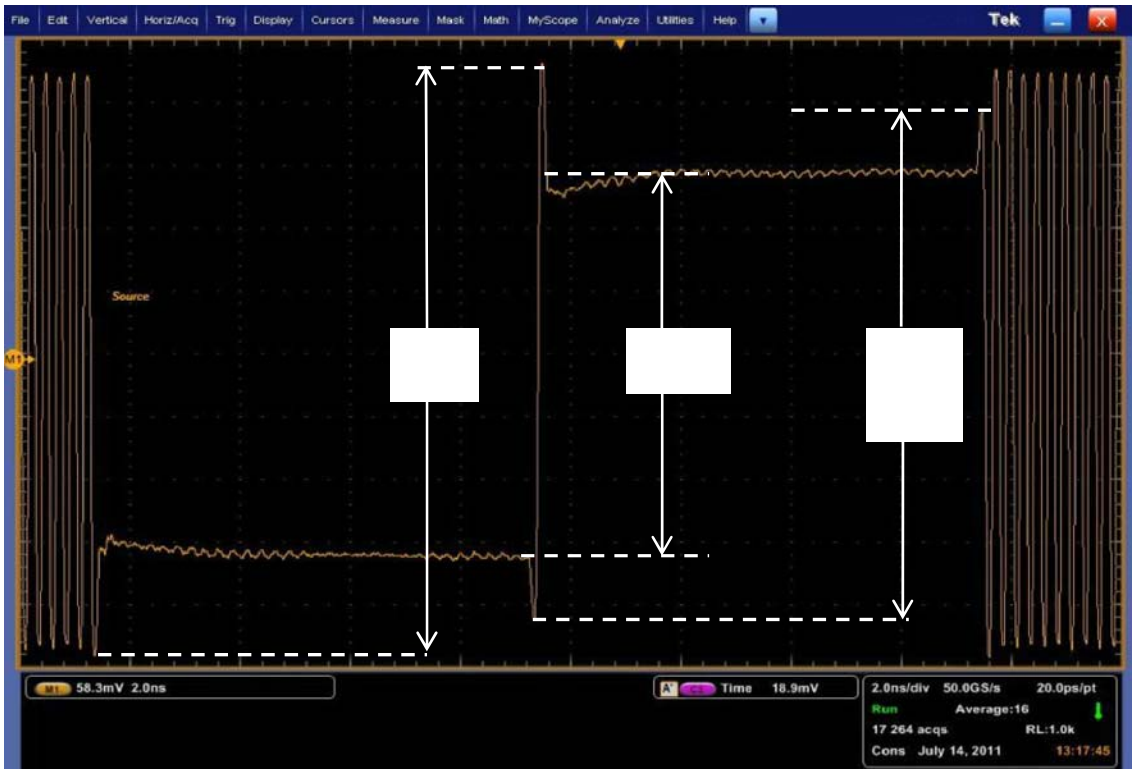


Figure 33: De-emphasis and Pre-shoot measurements

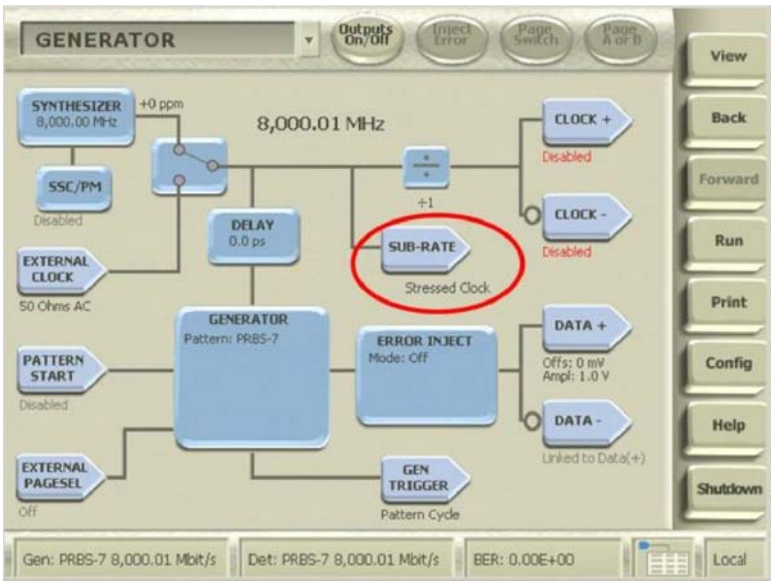
4.3.8 Calibrate Sinusoidal Jitter (SJ) @ TP1

This procedure will calibrate the target SJ at TP1. This procedure will use the delta-TJ method for SJ calibration. A reference TJ will be measured with SJ set to 0% UI on the BERTScope. SJ amplitude on the BERTScope will be increased. A new TJ will be measured. The delta in TJ will be considered the amount of SJ added. The target SJ is 0.10UI. SigTest will be used as the calibration tool.

4.3.9 BERTScope Setup

NOTE:

- *To ensure stress is applied, set the BERTScope Analyzer Sub-rate Clock Mode to Stressed Clock from VIEW > Generator > Sub-rate Mode > Stressed.*



a. **Turn off** all jitter sources. (***View → Stressed Eye → Sine Jitter → Uncheck 'Enable').*** Repeat for all enabled sources.

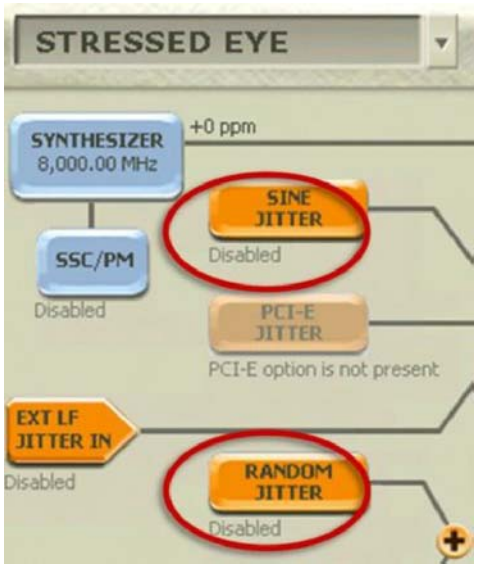


Figure 34: Turn Off Jitter Sources

b. **Enable** SJ ***(View → Stressed Eye → Sine Jitter → Enable)***
c. **Set** the SJ amplitude to zero (0% UI).
d. **Set** the SJ frequency to 100 MHz
e. **Load** the Gen3 compliance pattern **(View → Generator → Generator icon → User Pattern → Load User File → PCI Express → PCIe_modified_compliance_lane0.ram)**

4.3.10 DPP Setup

a. **Load** DPP Configuration "Preset 4" (no pre-shoot, no de-emphasis) via the DPP control view on the BERTScope ***(View → DPP Control → Standard Config → Restore Config)***

b. Set the Pre-Cursor and Post-Cursor equalization to the Calibrated Preset 4 settings from the **Amplitude equalization** process. Or Recall the saved Calibrated P4 settings.

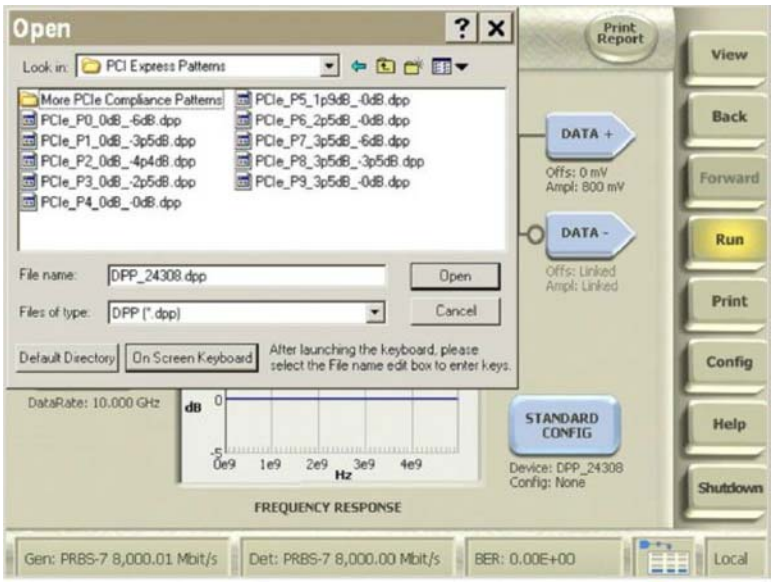


Figure 35: Load DPP Pattern Preset 4

NOTE:	• *The BERTScope ISI Board is not used for this calibration.*

4.3.11 RT Scope Setup

a. **Set** the maximum sample rate of 50 GS/s and the record length of 10 M points. (Select Horiz/Acq → Horizontal/Acquisition Setup → Horizontal → Average).

Figure 36: Set Record Length and Sample Rate

b. **Set** individual channels to use the most dynamic range of the scope's A/D without clipping by adjusting the Scale knob until the displayed waveform fills at least 75% of the vertical display area

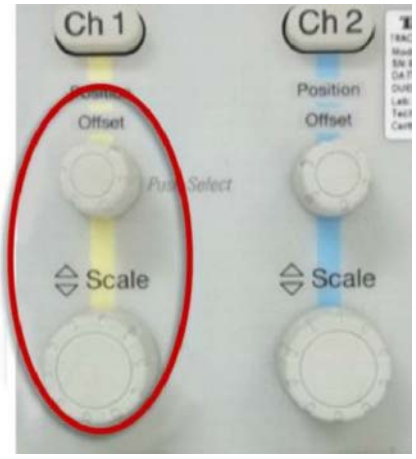


Figure 37: Adjust Oscilloscope Vertical Scale

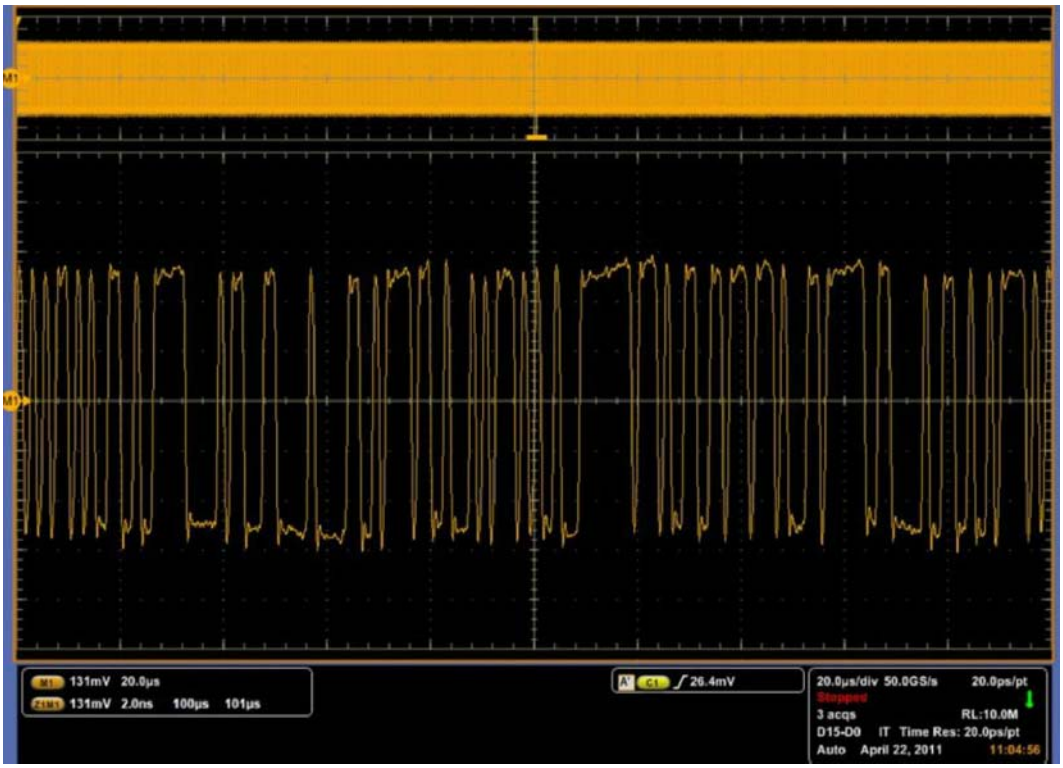


Figure 38: View of Waveform for Analysis

4.3.12 **Capture and Save the Baseline Waveform**

a. **Capture** the waveform by pressing the Run/Stop button on the Oscilloscope.

b. Upon completion of the capture, **save** the waveform on the oscilloscope for later use as a baseline for use in the SIGTEST jitter calibration. (File → Save As → Waveform).

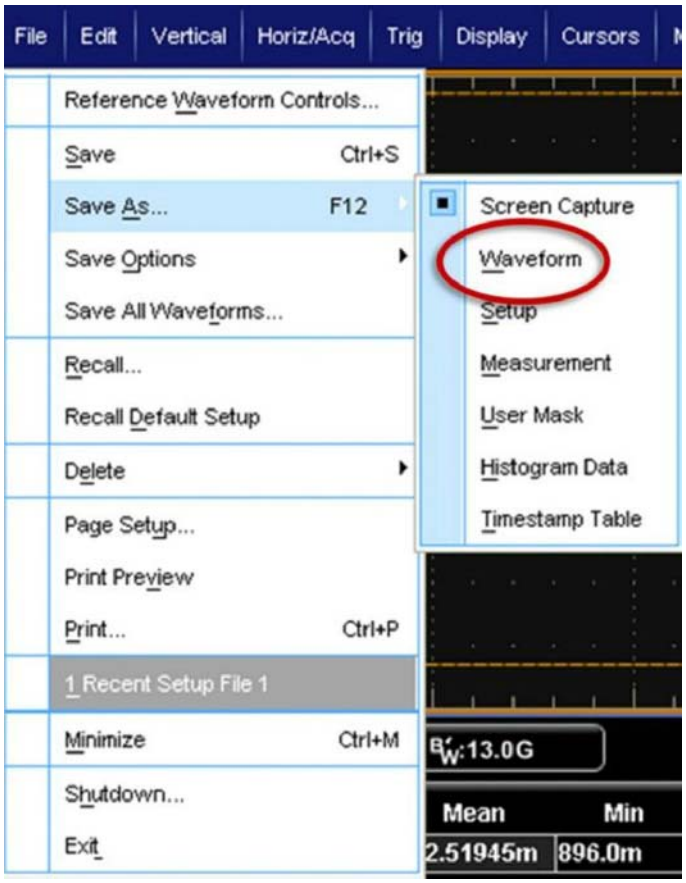


Figure 39: Save the Baseline Waveform

4.3.13 **Analyze Baseline Waveform with SIGTEST**

a. **Open** the SIGTEST program on the Oscilloscope (Start → Programs → SIGTEST)

b. **Browse** to open the saved baseline (.WFM) waveform file.

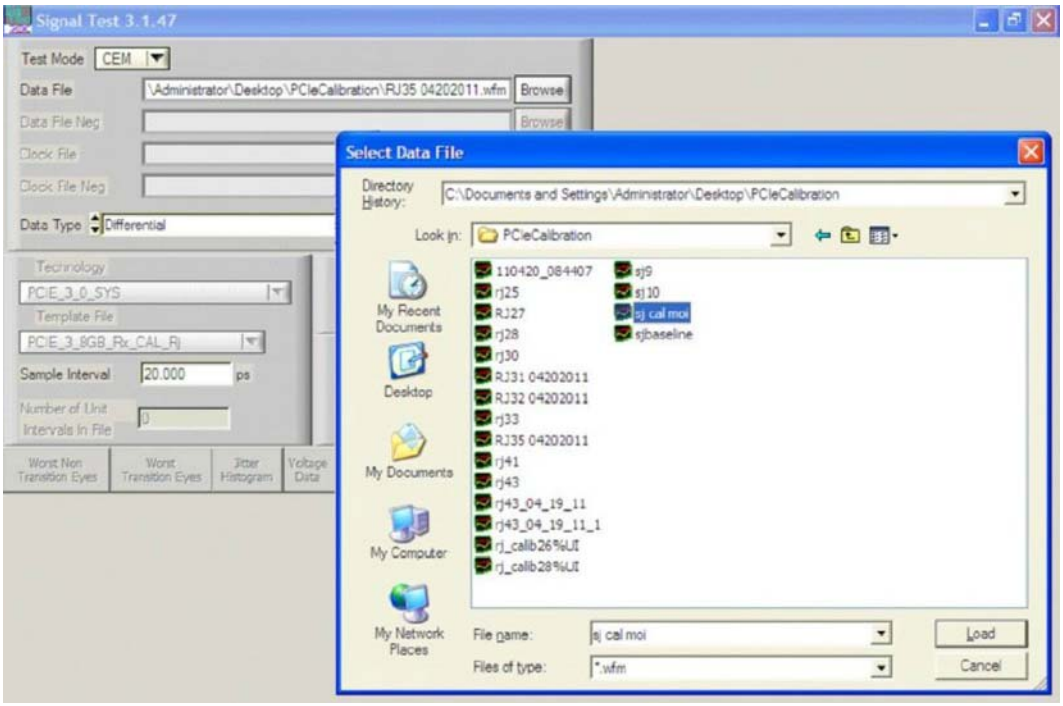


Figure 40: Locate and Load the Saved Waveform File

c. **Select** (in the Signal Test dialog):

- Load and Verify Data File

The Technology is PCIE_3_0_RX_CAL.

The template file for SJ cal is PCIE_3_8Gb_Rx_SJ_CAL

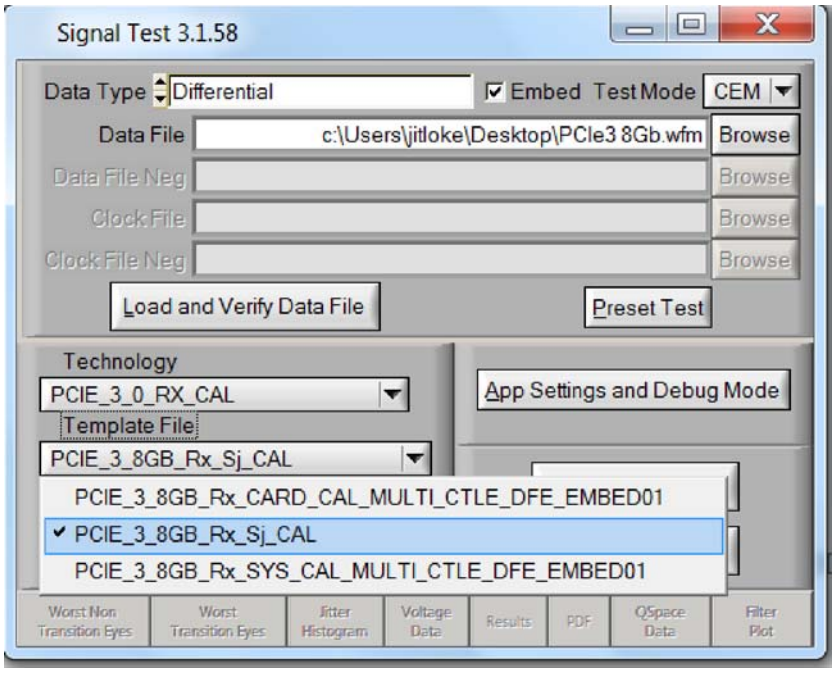


Figure 41: Select Pattern File and Initiate Test

d. **Measure** and note the baseline Total Jitter (TJ)

In this example, TJ is 18.2 ps.

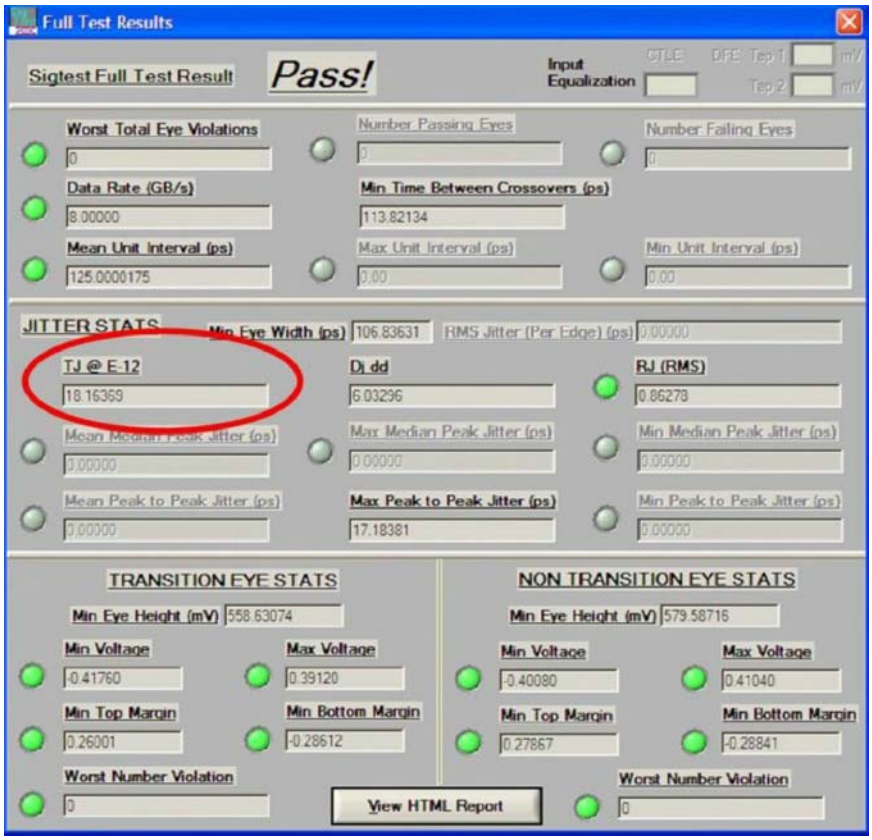


Figure 42: Baseline TJ Measured at 18.2 ps

4.3.14 **Adjust SJ**

a. **Set** the SJ frequency to 100 MHz ***(View → Stressed Eye → Sine Jitter → Frequency)***

b. Adjust the SJ amplitude on the BERTScope at ***View → Stressed Eye → Sine Jitter → Amplitude***

c. **Recapture** waveform for SigTest processing.

d. **Reselect** TEST in the SIGTEST home screen until TJ equals baseline TJ + Specified SJ (12.5ps for BASE Calibration).

In this case, the Calibrated TJ is 30.4 ps.

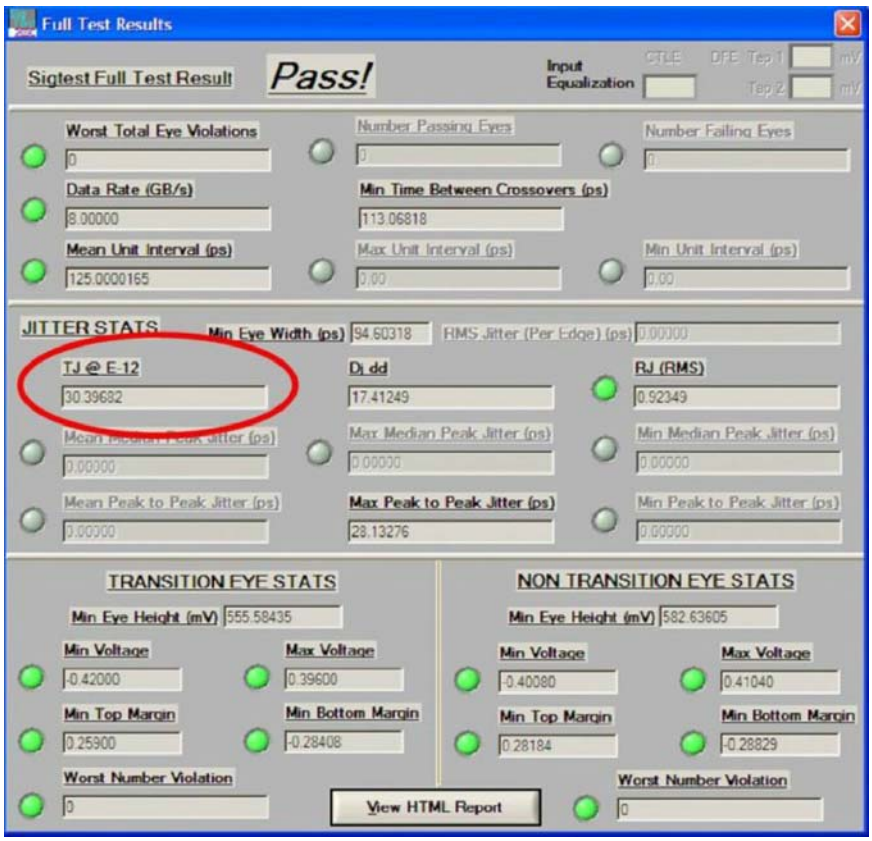


Figure 43: TJ at 30.4 ps

NOTE:

- *If calibrating for the 0.1 UI BASE specifications, it should be ≈10 %UI on the BERTScope Analyzer SJ setting.*

4.3.15 **Record SJ Amplitude value**

a. Following completion of the SJ calibration, **record** the BERTScope SJ Amplitude setting for use in creating the Calibrated BERTScope Configuration file.

4.3.16 Calibrate Random Jitter (RJ) @ TP1

This procedure will calibrate RJ using test pattern 1010. The target RJ is 2.0ps RMS. SigTest will be the calibration tool.

4.3.17 BERTScope setup

a. **Load** a clock pattern (1010.ram) into the BERTScope Pattern Generator. ***(View → Generator → Generator → User Pattern → Load User File)***

b. **Enable** SJ on the BERTScope Analyzer ***(View → Stressed Eye → Sine Jitter → Enable) and set the Amplitude to 0% UI) for baseline jitter (View → Stressed Eye → Sine Jitter → Amplitude*).**

c. **Check** to ensure that the Sub-rate Clock Mode is set to "Stressed Clock." ***(View → Generator → Subrate → Mode → Stressed)***

4.3.18 DPP setup

a. Set the Pre-Cursor and Post-Cursor equalization to the Calibrated Preset 4 settings from the **amplitude equalization** process, or recall the saved Calibrated P4 settings.

4.3.19 RT Scope Setup

a. **Set** the maximum sample rate of 50 GS/s and the record length of 10 M points (see Figure 45). Select Horiz/Acq → Horizontal/Acquisition Setup → Horizontal → Average

Figure 44: Set Record Length and Sample Rate

4.3.20 Adjust RJ

a. **Analyze** the waveform just captured using SIGTEST, configured as follows:

The Technology is PCIE_3_0_RX_CAL.

The template file for RJ cal is PCIE_3_8Gb_Rx_SJ_CAL

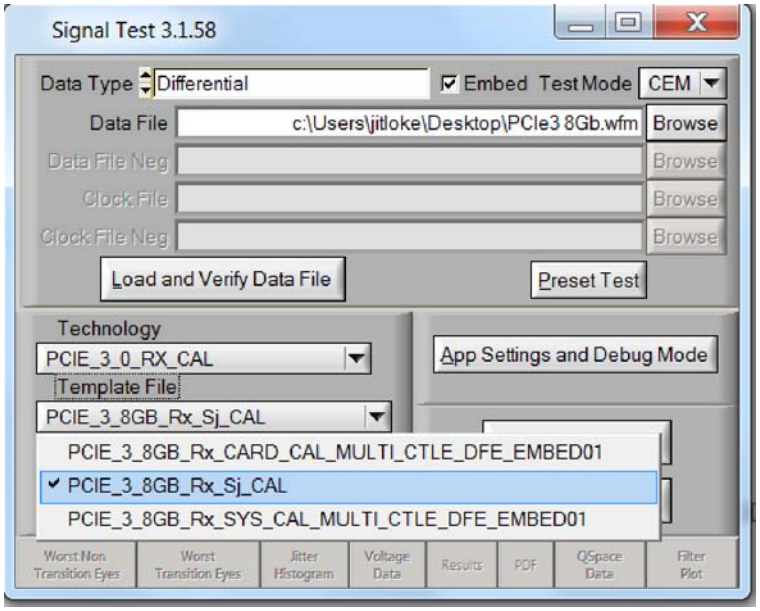


Figure 45: SIG Test Screen

b. View the R_J (RMS) value reported by SIGTEST. See Figure 47.
c. If the reported R_J (RMS) value is 1.80 – 2.2ps RMS, R_J calibration is complete.

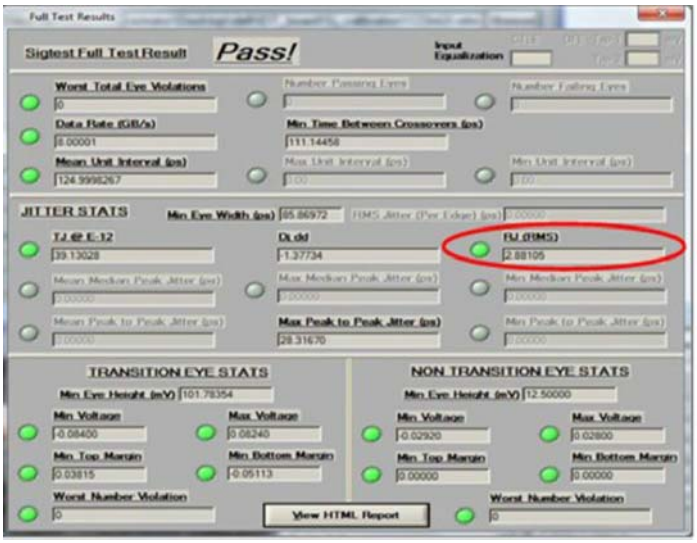


Figure 46: RJ measured on SigTest

d. If not, adjust the BSA RJ amplitude until SIGTEST displays a targets value of RJ in ps.

4.3.21 Record RJ Amplitude value

a. **Record** the BSA SJ Amplitude setting after completing RJ calibration, for use in setting the Calibrated BERTScope Configuration file.

This completes the calibration at TP1.

4.4 Breakout Channel, Medium Channel, and Long Channel.

The Base Spec uses differing insertion losses (Short Channel, Medium Channel, and Long Channel) as a means of requiring the RX DUT to adjust its equalizer over a representative range of minimum to maximum length channels encountered in real platforms. The BERTScope ISI Board will be used to generate Breakout Channel, Medium Channel, Long Channel and combinations of these channels as required for Stressed Voltage Calibration

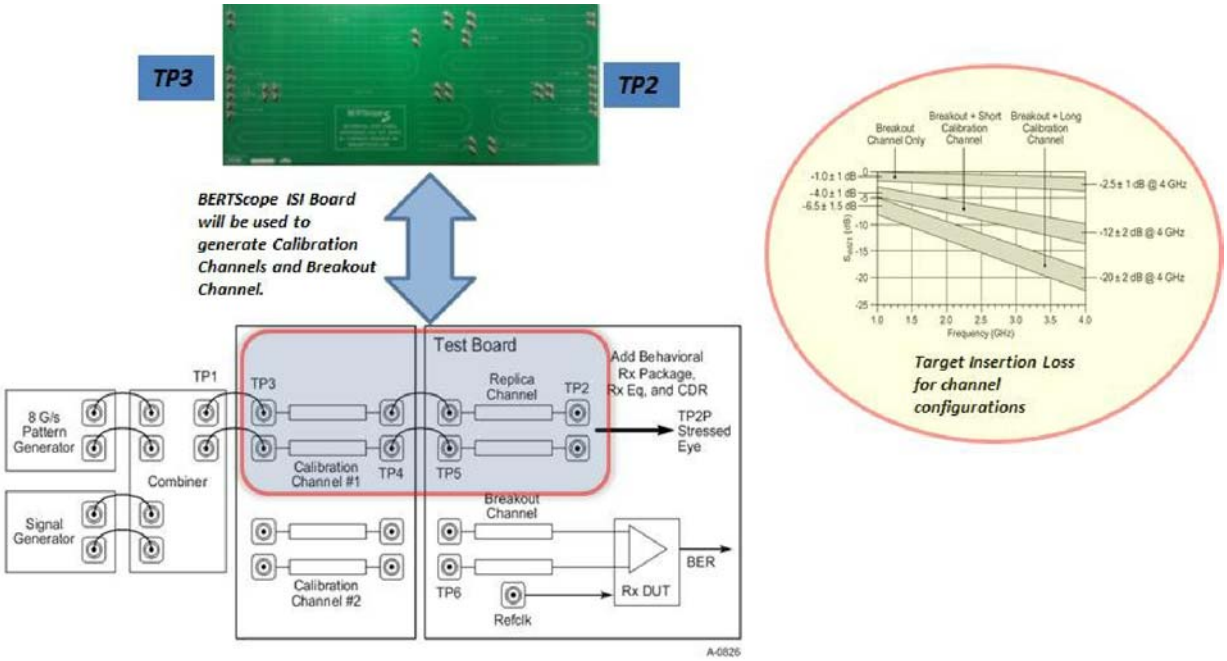


Figure 47: Calibration Channels.

Select the appropriate *BERTScope ISI Board* trace lengths combinations to generate required Insertion Loss:

	2.42 inch	5 inch	6.75 inch	9 inch	12 inch	17 inch	24 inch	31 inch	40 inch
FREQ MHz	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB
4000	-0.89	-1.73	-2.34	-2.99	-3.9	-5.49	-7.63	-9.7	-12.54

Figure 48: Insertion Loss @ 4GHz for various trace lengths on the BERTScope ISI Board

Initial Channel Calibration trace lengths for variation configurations:

	Target Insertion Loss(I.L.)	**Trace Length(Insertion Loss)**
Replica Channel	-2.5 +/- 1dB	6.75 inch (-2.34dB) Total I.L. = -2.34dB
Replica Channel + Short Channel	-12.0 +/- 2dB	6.75 inch (-2.34dB) 31 inch (-9.7 dB) Total I.L. = -12.04 dB
Replica Channel + Long Channel	-20 +/- 2dB	6.75 inch (-2.34dB) 17inch (-5.49 dB) 40 inch (-12.54 dB) Total I.L. = -20.46 dB

Note: Actual total insertion loss may vary with insertion of cables between trace lengths. In addition, it may be better to set IL to the upper limit. For 20dB+/-2dB, it is suggested that the IL be closer to 22dB to minimize the amount of DMI needed to achieve final Eye Height.

Note: The Breakout Channel is used only to 'replicate' the expected insertion loss of the DUT breakout channel. The Replica channel will be removed for actual testing.

Quick Method to verify Channel lengths (if needed):

1. Set BERTScope *Pattern Generator* to 10.ram.
2. Set Synthesizer on BERTScope to 8Gb/s. (With the 10.ram pattern, this generates a 4GHz clock on the DATA path.)
3. Disable all stresses on BSA.
4. On RT Scope, measure Vpp amplitude ***before*** ISI Board at TP1(after cables from Combiner). Note measurement as V_1.
5. Measure Vpp after selected trace lengths on BERTScope ISI Board at TP2. Note as V_2.
6. Insertion Loss(IL) = 20 log (V_1/V_2)
7. The IL should meet required loss for Channel and can now be inserted in calibration path.

4.5 Differential Interference and AC Common Mode@ TP2

The following parameters will be measured at TP2:

- **Differential Interference**
- **AC Common Mode**

4.5.1 Calibrate Differential Mode Interference @ TP2

4.5.2 Configuration for Differential Mode Interference

Note: The appropriate length of BERTScope ISI Board traces should be used. With Long Channel, the 40inch + 17inch+ 6.75inch traces should be used.

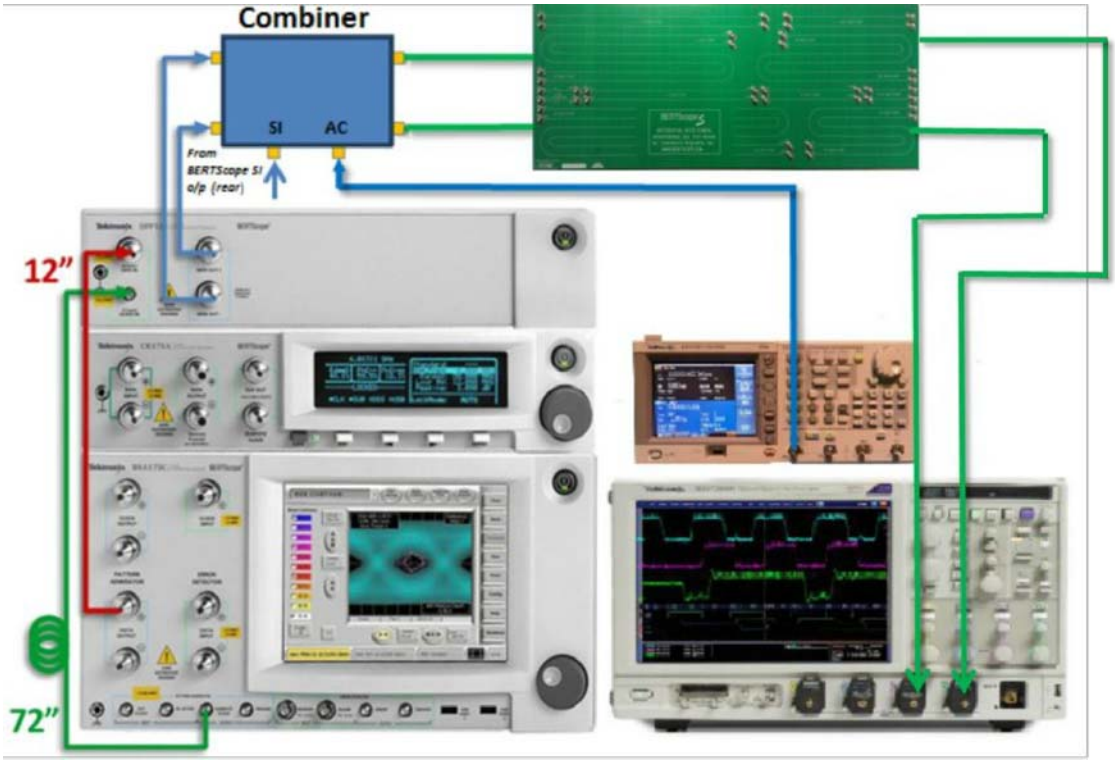


Figure 49: Setup for Differential and AC Common Mode Calibration.

4.5.2.1 BERTScope Setup

a. **Turn off** (disable) all jitter sources (***View → Stressed Eye).***

b. **Set** the Pattern Generator to "All Zeros." ***(View → Generator → Generator → Pattern → All Zeros)***

c. **Set** Sine Interference frequency to 2100 MHz ***(View → Stressed Eye → Sine Interference → Frequency)*** and the amplitude to approximately 100 mV ***(View → Stressed Eye → Sine Interference → Amplitude).***

d. **Sinusoidal Interference** should be set on External Mode. ***View →Stressed Eye → Sine Interference → Mode → External***

e. Disable output on the Arbitrary Waveform Generator

4.5.2.2 RT Scope Setup

a. **Set** Average acquisition. (Select Horiz/Acq → Horizontal/Acquisition Setup → Horizontal → Average)

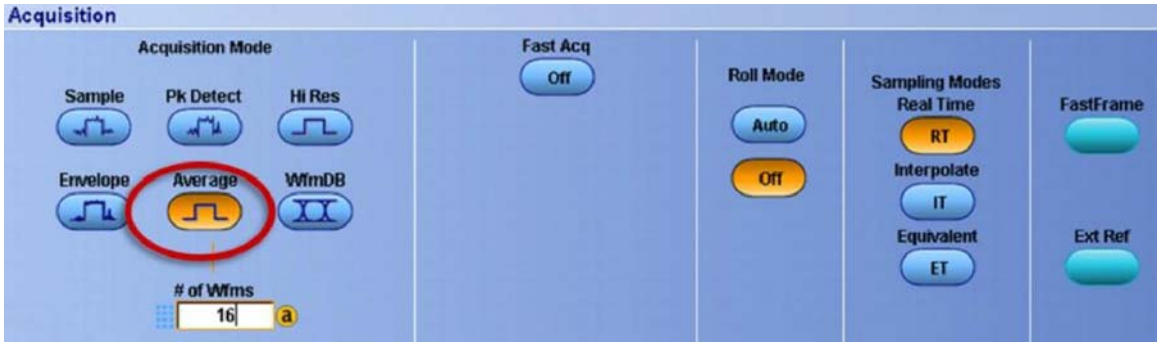


Figure 50: Set Average Acquisition

a. **Select** the peak-to-peak voltage measurement (Measure → Measurement Setup).

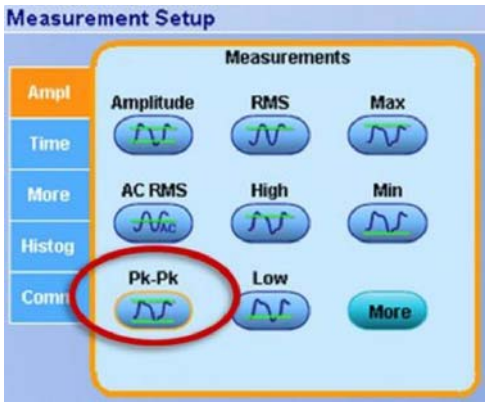


Figure 51: Set for Peak-to-Peak Voltage Measurement

4.5.3 Adjust the Sine Interference Amplitude

a. A**djust** the Sine Interference amplitude on the BERTScope Analyzer to get a calibration value greater than or equal to the specification (≥14 mV for BASE).

In Figure 53, the RT Scope measurement is 16 mV.

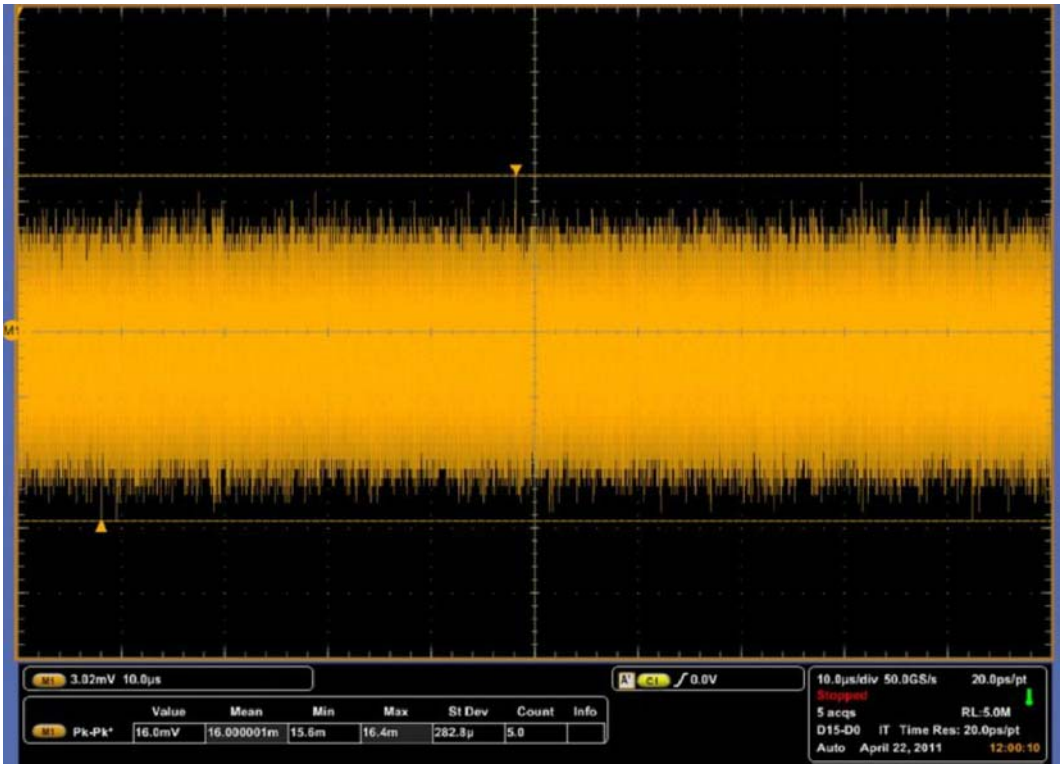


Figure 52: Measure Average Peak-to-Peak Voltage

4.5.4 Record SI Amplitude

a. Following completion of the Interference calibration, **record** the BERTScope SI Amplitude setting for use in setting the Calibrated BERTScope Configuration file.

4.5.5 AC Common Mode Calibration

This procedure will add AC Common Mode at TP2. (The Base specification allows AC Common Mode to be measured at TP1 or TP2.) AC Common is defined as: Max Peak-to-Peak amplitude of (CH3+CH4)/2. We will use the mean peak-to-peak amplitude for (CH3+CH4)/2

Note: To some extent, AC Common Mode may affect Differential Mode amplitude. For example if cables used are not phase-matched or if scope is not de-skewed, then AC Common mode may increase DMI.

a. **Disable** all other stresses on BERTScope. Go to ***VIEW →STRESSED EYE*** and verify all other stresses are turned off.

b. **Set** the Pattern Generator to "All Zeros" pattern. Go to ***View →Generator →Generator Icon → Pattern →All Zeros***

c. **Set** MATH1 function on Scope to (CH3+CH4)/2

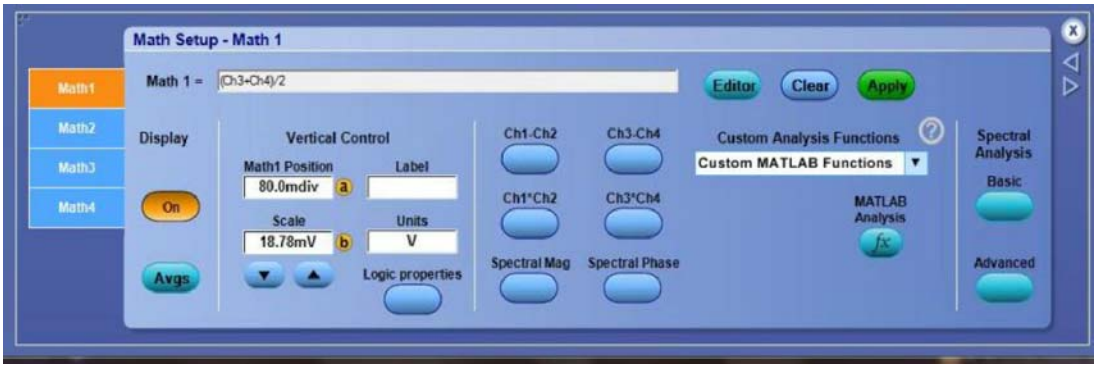


Figure 53: MATH1 function should be set to (CH3+CH4)/2

d. **Set** AFG Frequency on CH1 to 120MHz.

e. **Set** Amplitude initially to 300mV - 500mVpp, depending on Combiner used.

f. **Enable** Output on CH1

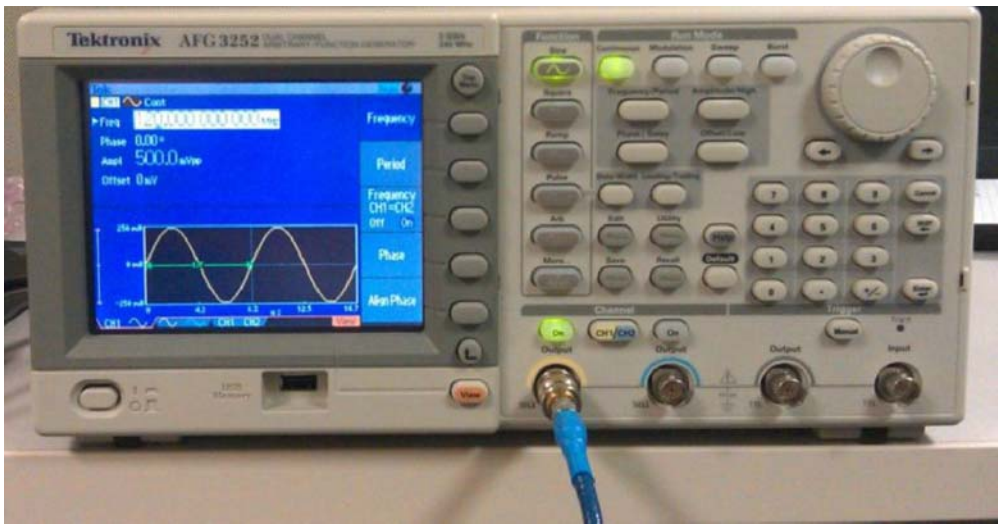


Figure 54: Front panel of AFG

g. **Adjust** peak-to-peak amplitude generated by the AFG until measured peak-to-peak amplitude is reached. In this example for long channel, the Pk-Pk amplitude is 150.2mV @ TP2.

Note: **AC Common Mode calibration may add addition DMI. It may be helpful to re-verify and adjust DMI amplitude, if needed, with calibrated AC Common Mode enabled.**

This completes calibration at TP2.

4.6 SigTest Templates for Eye Width and Eye Height Calibration:TP2P

The current templates for SigTest(Ver. 3.1.70) reflect calibration for CEM testing. The SigTest templates may be modified for BASE calibration.

Current Template for AIC: **PCIE_3_8GB_Rx_CARD_CAL_MULTI_CTLE_DFE_EMBED01**

This template has DFE, CTLE, and Embedding functions enabled. Base testing, however:
Taken from PCI Express Base Specification, Rev.3.0(Pg. 372):

> *"Eye width and eye height are defined after applying post-processing and are defined at TP2P. TP1 represents the output of the combiner or generator (if the combiner is internal to the generator). TP2 represents the signal at the far end of the breakout channel at Rx DUT's pin, as if the DUT 15 were an ideal termination. The long calibration channel utilizes both CTLE and DFE, while the medium and short channels calibration channels use CTLE only. EH is set by adjusting the amount of differential noise until the value defined by VRX-SV-8G is obtained. If it is not possible to maintain a sufficient eye width by adjusting only the differential noise, it is acceptable to inject less differential noise and adjust the generator launch voltage."*

To reflect the differing requirements of CTLE and DFE highlighted above, the SigTest templates will need to be modified for specific BASE Calibration:

- **DFE**
  - **Enabled:** For Long Channel(-20dB), DFE is *enabled*
  - **Disabled:** For Short(2.5dB) and Medium Channel(-12.5dB), DFE is *disabled*
- **CTLE** remains *enabled* in all cases. (There are 7 potential CTLE profiles that may be used in SigTest for Base calibration)
- **Embedding** should be *disabled* in all cases

The SigTest templates will need to be modified to reflect BASE testing.

Disabling Embedding for Long Channel

1. On instrument with SigTest installed, navigate to SigTest's Windows Program folder, typically found here: **C:\Program Files (x86)\SigTest 3.1.70\Templates\PCIE_3_0**
2. Locate template file : **PCIE_3_8GB_Rx_CARD_CAL_MULTI_CTLE_DFE_EMBED01**
3. Right-click on file and open with *Notepad* or any other user-selected option
   a. Step 1: Scroll down to "Apply S-parameter …"
   b. Step 2: Change *DoSParmEmbed* to 0 to disable embedding

c. Step 3: Verify

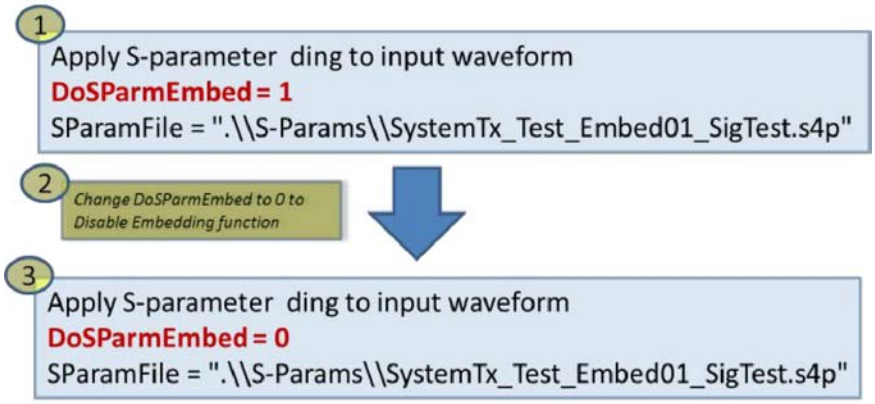


Figure 55: Disabling Embedding in SigTest Template

4. Save template file as: **PCIE_3_8GB_Rx_CARD_CAL_MULTI_CTLE_DFE.** *This template should only be used for LONG CHANNEL calibration*

Note: For Short and Medium Channel, DFE will need to be disabled.

4.7 *Eye Height and Eye Width Calibration*

A final calibration of the eye opening is performed by enabling all calibrated stresses and ISI and evaluating the resulting eye opening using the RT Scope and SIGTEST software. For this step, the SIGTEST analysis includes the appropriate CTLE and DFE for Breakout Channel, Medium Channel, and Long Channel.

4.7.1 Configuration for BASE Eye Height/Width Calibration

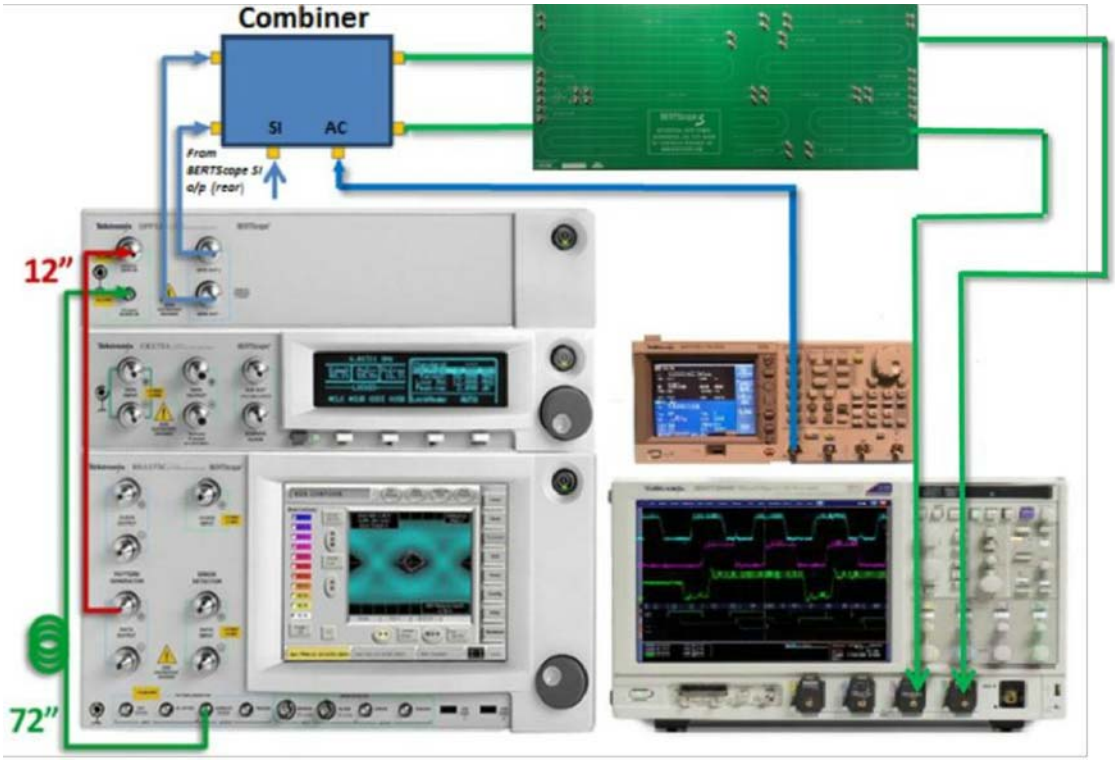


Figure 56: Equipment Setup for BASE Eye Height/Width Calibration

4.7.2 Eye Height/Width Calibration Procedure

a. **Set** all required Stresses on BERTScope to calibrated values. This can be done by recalling saved configuration or restoring calibration values obtained in earlier part of calibration process.
b. **Set** DPP Amplitude to calibrated Pre-Cursor, Post-Cursor, and amplitude values for P7 for Long Channel
c. **Enable** AFG to calibrated frequency and amplitude.
d. **Set** the Scope per the settings previously used in Section
e. **Capture** and save the waveform per instructions previously used.
f. **Open** SigTest and perform post-processing on the captured waveform using the appropriate template files.

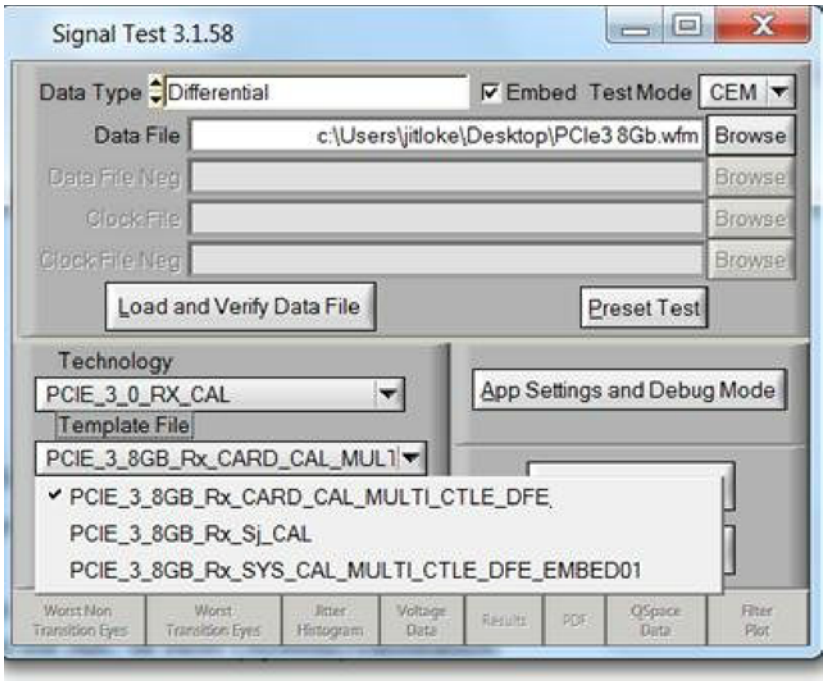


Figure 57: SigTest showing template for LONG CHANNEL calibration. Embed removed.

4.7.2.1 Eye Height and Eye Width numbers that SIGTEST reports

NOTE:

- *For Eye Height measurement, use the lesser of transition eye height and non-transition eye height.*

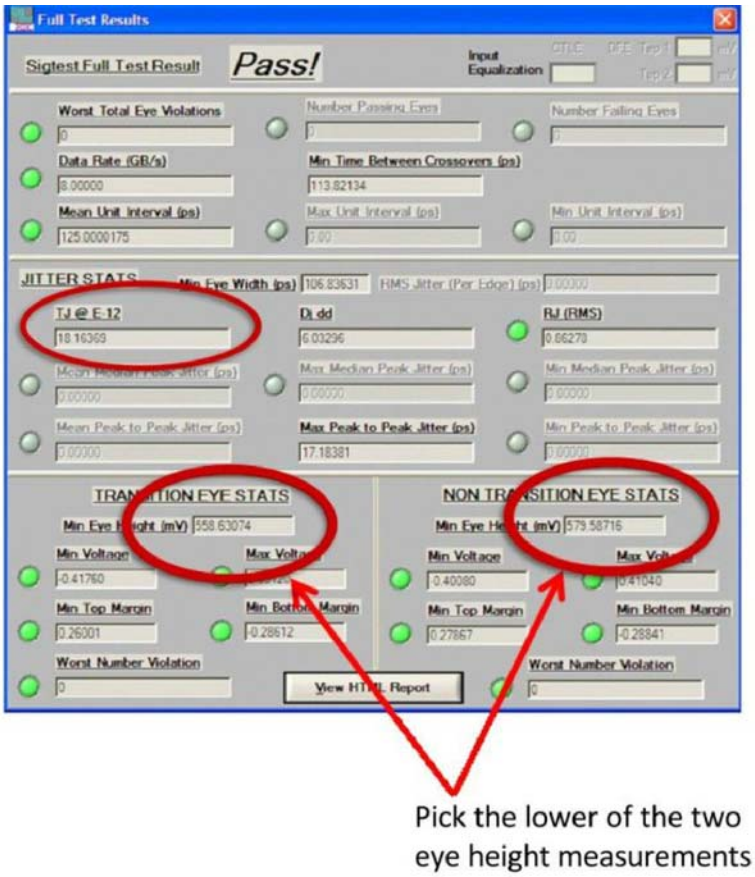


Figure 58: Transition Eye Height and Non-Transition Eye Height

1. **Eye Width:** 0.30 to 0.35 UI @ 1e-12
   - If needed, **adjust** the ISI trace lengths and re-run SIGTEST until the desired value for Eye Width is reached.

2. **Eye Height:** Long Channel: 25mV$_{pp}$ @ 1E-12

   SigTest, the calibration tool used, does not estimate Eye Height at 1E-12, but measures only at waveform capture size. SigTest, in the above configuration, will report EH @ 1E-06.

   This methodology will use Sigtest to measure 50mV EH @ 1E-06.

   - While adjusting *Sinusoidal Interference* or *Launch Amplitude*, measure the target EH of 50mV. If the results fall outside the required range, the *Sinusoidal Interference* or *Launch Amplitude* can be adjusted to attain the required amplitude.

Note the any modified values for *Launch Amplitude* and SI, for use in creating the Calibrated Configuration file.

3. **Create Calibrated Configuration File**

   - **Load PCIe Baseline Configuration File**

a. From the BERTScope local control interface, **select** ***CONFIG →Restore Configuration. Select the file PCIe3_Uncalibrated_Baseline.cfg***

   - **Modify Settings**

From the settings recorded during the calibration process, modify the BERTScope configuration as follows:

a. **Set the Generator Delay** (View → Generator →Delay) to the value noted at the end of the DPP Clock to Data Skew calibration

b. **Set the DPP Amplitude** (View → DPP → Data → Amplitude) to the value noted at the end of the DPP Amplitude calibration

c. **Set the Sinusoidal Jitter Amplitude** (View → Stressed Eye →Sine Jitter → Amplitude) to the value noted at the end of the Sine Jitter calibration

d. **Set the Random Jitter Amplitude** (View → Stressed Eye →Random → Amplitude) to the value noted at the end of the Random Jitter calibration

e. **Set the Sinusoidal Interference** (View → Stressed Eye →Sine Interference → Amplitude) to the value noted at the end of the Sinusoidal Interference calibration

   - **Save Calibrated Configuration File**

a. **Save** a new Configuration file for later use in setting up the equipment for Compliance testing. Go to Config → Save Configuration, and assign an appropriate file name, such as PCIe3_Calibrated_Config_mm_dd_yy.cfg. Separate calibration files will be required for AIC and Host.

The calibration process is now complete.

5 Appendix B: Sdd21 for trace lengths on BERTScope ISI Board

	2.42 inch	5 inch	6.75 inch	9 inch	12 inch	17 inch	24 inch	31 inch	40 inch
FREQ MHz	S21 dB	S21 dB	S21 dB	S21 dB	S21 dB	S21 dB	S21 dB	S21 dB	S21 dB
3800	-0.89	-1.62	-2.29	-2.88	-3.74	-5.26	-7.33	-9.31	-12.02
3825	-0.87	-1.62	-2.27	-2.88	-3.76	-5.26	-7.35	-9.34	-12.06
3850	-0.87	-1.64	-2.31	-2.92	-3.8	-5.3	-7.4	-9.41	-12.14
3875	-0.87	-1.68	-2.3	-2.93	-3.82	-5.31	-7.43	-9.45	-12.21
3900	-0.87	-1.66	-2.3	-2.92	-3.82	-5.33	-7.45	-9.49	-12.25
3925	-0.88	-1.67	-2.32	-2.94	-3.85	-5.36	-7.49	-9.54	-12.32
3950	-0.88	-1.68	-2.33	-2.96	-3.87	-5.41	-7.54	-9.59	-12.39
3975	-0.89	-1.7	-2.34	-2.98	-3.9	-5.46	-7.59	-9.65	-12.46
4000	-0.89	-1.73	-2.34	-2.99	-3.9	-5.49	-7.63	-9.7	-12.54
4025	-0.91	-1.73	-2.32	-2.99	-3.91	-5.5	-7.68	-9.76	-12.62
4050	-0.89	-1.67	-2.31	-2.97	-3.9	-5.49	-7.68	-9.77	-12.63
4075	-0.9	-1.73	-2.33	-3	-3.94	-5.53	-7.76	-9.84	-12.73
4100	-0.92	-1.69	-2.34	-3.03	-3.98	-5.55	-7.78	-9.88	-12.78
4125	-0.9	-1.7	-2.35	-3.02	-3.98	-5.57	-7.81	-9.92	-12.83
4150	-0.91	-1.73	-2.36	-3.06	-4.05	-5.62	-7.87	-9.99	-12.92
4175	-0.92	-1.74	-2.39	-3.09	-4.08	-5.66	-7.92	-10.05	-13
4200	-0.93	-1.74	-2.41	-3.13	-4.1	-5.69	-7.97	-10.1	-13.07
4225	-0.96	-1.75	-2.44	-3.18	-4.11	-5.72	-8.02	-10.17	-13.15
4250	-0.95	-1.73	-2.41	-3.14	-4.09	-5.72	-8.03	-10.18	-13.19
4275	-0.92	-1.74	-2.38	-3.13	-4.09	-5.73	-8.04	-10.21	-13.23
4300	-0.98	-1.76	-2.44	-3.18	-4.12	-5.79	-8.11	-10.28	-13.32
4325	-0.95	-1.76	-2.43	-3.18	-4.14	-5.8	-8.13	-10.32	-13.37
4350	-0.97	-1.77	-2.48	-3.21	-4.18	-5.86	-8.19	-10.38	-13.47
4375	-1	-1.79	-2.49	-3.23	-4.22	-5.89	-8.23	-10.44	-13.55
4400	-1.02	-1.81	-2.51	-3.25	-4.26	-5.92	-8.28	-10.51	-13.64
4425	-1.04	-1.84	-2.5	-3.26	-4.29	-5.94	-8.33	-10.56	-13.71
4450	-1.06	-1.86	-2.49	-3.29	-4.3	-5.97	-8.38	-10.61	-13.79
4475	-1.03	-1.87	-2.48	-3.28	-4.29	-5.99	-8.4	-10.64	-13.83
4500	-1.05	-1.88	-2.5	-3.3	-4.3	-6.03	-8.45	-10.7	-13.89
4525	-1.06	-1.9	-2.51	-3.34	-4.32	-6.07	-8.51	-10.75	-13.95
4550	-1.06	-1.9	-2.52	-3.34	-4.35	-6.09	-8.53	-10.78	-14.01
4575	-1.09	-1.94	-2.54	-3.4	-4.38	-6.13	-8.6	-10.85	-14.1
4600	-1.09	-1.95	-2.55	-3.42	-4.4	-6.14	-8.64	-10.9	-14.17

4625	-1.09	-1.97	-2.58	-3.43	-4.45	-6.17	-8.68	-10.95	-14.24
4650	-1.1	-1.97	-2.6	-3.43	-4.47	-6.22	-8.73	-10.99	-14.29
4675	-1.09	-1.97	-2.61	-3.43	-4.48	-6.25	-8.77	-11.04	-14.34
4700	-1.1	-1.97	-2.62	-3.44	-4.48	-6.28	-8.82	-11.08	-14.38
4725	-1.13	-2	-2.67	-3.45	-4.51	-6.33	-8.87	-11.14	-14.45
4750	-1.12	-1.99	-2.66	-3.45	-4.51	-6.34	-8.9	-11.18	-14.5
4775	-1.13	-2	-2.7	-3.48	-4.53	-6.36	-8.95	-11.24	-14.58
4800	-1.13	-2	-2.72	-3.51	-4.54	-6.39	-9.01	-11.31	-14.65
4825	-1.11	-1.98	-2.69	-3.53	-4.55	-6.42	-9.05	-11.34	-14.7
4850	-1.1	-1.97	-2.68	-3.55	-4.59	-6.45	-9.09	-11.39	-14.76
4875	-1.1	-1.98	-2.68	-3.57	-4.61	-6.48	-9.11	-11.44	-14.81
4900	-1.11	-1.99	-2.69	-3.59	-4.64	-6.51	-9.16	-11.48	-14.87
4925	-1.12	-2	-2.71	-3.61	-4.66	-6.54	-9.21	-11.53	-14.93
4950	-1.12	-2.01	-2.73	-3.65	-4.71	-6.58	-9.27	-11.59	-15.02
4975	-1.12	-2.01	-2.72	-3.65	-4.71	-6.59	-9.29	-11.63	-15.07
5000	-1.12	-2.04	-2.75	-3.68	-4.74	-6.66	-9.35	-11.71	-15.17
5025	-1.09	-2.05	-2.75	-3.64	-4.71	-6.66	-9.36	-11.72	-15.2
5050	-1.1	-2.05	-2.76	-3.65	-4.72	-6.69	-9.39	-11.76	-15.26
5075	-1.09	-2.09	-2.78	-3.66	-4.75	-6.72	-9.44	-11.82	-15.32
5100	-1.09	-2.08	-2.78	-3.66	-4.76	-6.73	-9.44	-11.85	-15.37
5125	-1.1	-2.13	-2.83	-3.7	-4.82	-6.78	-9.49	-11.93	-15.46
5150	-1.11	-2.16	-2.88	-3.75	-4.87	-6.82	-9.55	-12	-15.54
5175	-1.11	-2.17	-2.89	-3.77	-4.89	-6.85	-9.59	-12.06	-15.59
5200	-1.11	-2.18	-2.92	-3.8	-4.92	-6.9	-9.66	-12.12	-15.66
5225	-1.12	-2.22	-2.94	-3.85	-4.93	-6.96	-9.72	-12.16	-15.74
5250	-1.1	-2.08	-2.81	-3.75	-4.84	-6.88	-9.66	-12.11	-15.72
5275	-1.09	-2.11	-2.85	-3.77	-4.87	-6.92	-9.7	-12.16	-15.79
5300	-1.12	-2.17	-2.89	-3.83	-4.91	-6.97	-9.76	-12.24	-15.89
5325	-1.12	-2.19	-2.91	-3.85	-4.94	-7	-9.81	-12.31	-15.96
5350	-1.14	-2.22	-2.94	-3.88	-4.98	-7.05	-9.85	-12.37	-16.04
5375	-1.16	-2.22	-2.95	-3.88	-5.03	-7.11	-9.88	-12.44	-16.11
5400	-1.15	-2.2	-2.94	-3.88	-5.04	-7.11	-9.9	-12.48	-16.16
5425	-1.13	-2.21	-2.94	-3.88	-5.07	-7.14	-9.95	-12.53	-16.23
5450	-1.17	-2.2	-2.96	-3.91	-5.08	-7.15	-10.01	-12.59	-16.3
5475	-1.09	-2.16	-2.9	-3.84	-4.99	-7.09	-9.95	-12.53	-16.27
5500	-1.09	-2.2	-2.92	-3.86	-5.06	-7.15	-10.03	-12.62	-16.37
5525	-1.13	-2.2	-2.95	-3.89	-5.07	-7.18	-10.06	-12.66	-16.45
5550	-1.18	-2.22	-3.01	-3.97	-5.11	-7.26	-10.15	-12.74	-16.55
5575	-1.23	-2.24	-3.06	-4.02	-5.14	-7.32	-10.21	-12.81	-16.63
5600	-1.26	-2.26	-3.11	-4.07	-5.19	-7.37	-10.26	-12.88	-16.72
5625	-1.25	-2.27	-3.12	-4.06	-5.22	-7.38	-10.29	-12.9	-16.77
5650	-1.25	-2.27	-3.14	-4.07	-5.25	-7.41	-10.33	-12.97	-16.83

6 Appendix C: Abbreviations and Acronyms

AIC	Add-In Card
ATX	Advanced Technology eXtended motherboard form factor specification
BSA	BERTScope Analyzer, BSA85C
CBB	Compliance Base Board
CEM	Card Electro-Mechanical specification (for PCI Express Add-In Cards)
CLB	Compliance Load Board
CR	BERTScope Clock Recovery, CR125A
DMI	Differential Mode Interference
DJ	Deterministic Jitter
DPP	BERTScope Digital Pre-Emphasis Processor, DPP125B
Gen3	PCI Express Generation 3.0
ISI	Inter-symbol interference
PCIe	Peripheral Component Interconnect Express
RJ	Random Jitter
SI	Sinusoidal Interference
SJ	Sinusoidal Jitter
SMA	Sub-Miniature Type A connector
STR	BERTScope Analyzer Option STR, Stressed Eye
TJ	Total Jitter
UI	Unit Interval