PCI Express Method of Implementation for PLL Loop Bandwidth Response in Add-in Cards

Version 1.0

September 17, 2013

Contents

Revision History

Version	Date	Summary of Change(s)	Contributors
1.0	9/17/2013	Release Version	Herb Tretzen, Tim Bieber, David Hite

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1. Overview

This document provides information for using the Tektronix BERTScope Clock Recovery instruments to test PCI Express PLL Loop Bandwidth Response in Add-in PCIe cards.

Note: *This document shows text and illustrations using the CBB3. Rev 3.0 of the PCI Express Compliance Base Board for testing PCI Express Add-in Cards. You can use a CBB2 Rev2.0 test board. Additional notes for using the CBB2 test board are provided in this document.*

The PLL Loop Response test measures the bandwidth and peaking of the PLL used in Add-in cards for generating the Tx clock from the distributed 100 MHz REF_CLK signal. The loop response is determined by substituting a test clock for the locally generated REF_CLK which contains a calibrated level of sinusoidal jitter. The Tektronix clock recovery instrument measures the transferred jitter by applying the transmitted compliance pattern output from the Add-in card under test (DUT) into a reference PLL. The phase deviation is digitized and analyzed within the instrument to determine its spectral components. The frequency of the modulating sinusoidal jitter is incrementally swept, with measurement data taken at each frequency step. The instrument automatically computes the PLL magnitude and phase, along with jitter transfer function.

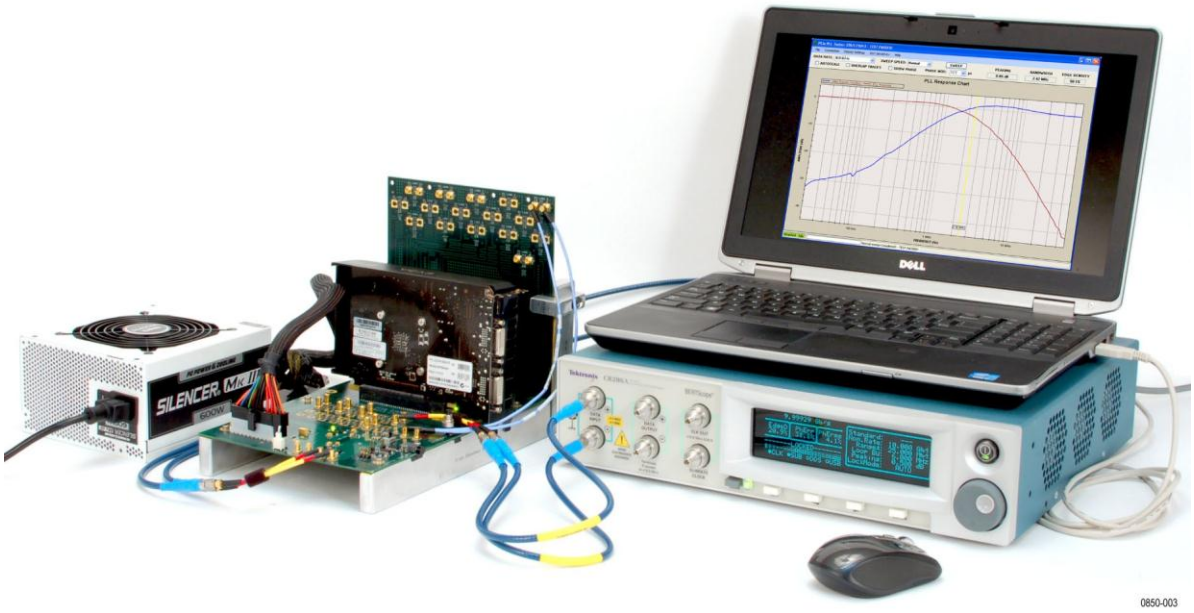


Figure 1. . Typical test setup with a Tektronix BERTScope clock recovery instrument

In addition to measuring the loop response, the clock recovery instrument contains the synthesizer used to generate the jitter modulated REF_CLK. The jitter appears as true phase modulation in the REF_CLK output, maintaining a 50% duty factor at all times. This allows the clock recovery instrument to be used with all types of clock generation PLLs, including those which incorporate dual edge phase detectors.

Incorporating the synthesizer within the instrument facilitates internal self calibration, eliminating the need to manually normalize the test setup calibration. Once the cabling to the CBB3 fixture is connected, you can begin testing immediately.

An external PC provides host system control and report generation software. This program plots the PLL Loop Response, compares the measured bandwidth and peaking against the specification limits, and can generate a test report in hard copy or HTML file format.

1.1 Required equipment

The following equipment is required for PLL Loop Response testing to revision 1.1 requirements:

- Tektronix BERTScope CR125A, CR175A, or CR286A Clock Recovery instrument with Option PCIE (for Gen 1 or Gen 2 applications) or PCIE8G (for Gen 1, Gen 2, or Gen 3 applications).
- The clock recovery instrument comes with the following items:
    - BERTScopePC Standalone Software CD-ROM (installs the clock recovery control interface on a user supplied PC), Tektronix part number, 063-4308-xx.

      NOTE. The BERTScopePC software can also be downloaded from the Tektronix Web site at www.tektronix.com; search for "BERTScopePC".
    - USB cable, type A to Type B. Tektronix part number: 174-5912-xx
- CBB3. Rev 3.0 of the PCI Express Compliance Base Board for testing PCI Express Add-in Cards

  For more information on the test board go to the following Web site: http://www.pcisig.com/specifications/order_form.
- Precision torque wrench for installing/removing cables. (Tektronix recommends using the H+S 74–Z-0–021/Ncm 100 torque wrench available from Huber Suhner.)
- SMP-F 50 Ω terminators for unused lanes. See the note below. Tektronix recommends using eight (8) ST2645 SMP-Female terminators available from Fairview Microwave Inc. http://www.fairviewmicrowave.com.

- Two (2) 1.0 m Huber+Suhner (H+S) SMA-to-SMA interconnect cables to connect the clock recovery instrument rear panel outputs to the CBB3 fixture inputs:
    - H+S Description SF104PE/11PC35/11PC35/1000mm
    - H+S Part number 84210103
    - Cable length 1.0 m
- Two (2) 0.5 m Huber+Suhner (H+S) SMA-to-SMA interconnect cables to connect the CBB3 fixture Lane 0 outputs to the clock recovery front panel inputs:
    - H+S Description SF104PE/11PC35/11PC35/500mm
    - H+S Part number 84210099
    - Cable length 0.5 m
- Four (4) 102 mm Huber+Suhner (H+S) SMA-to-SMP interconnect cables to connect the SMA interconnect cables to the SMP connectors on the CBB3 fixture:
    - H+S Description SM86FEP/16SMP/21SMA/102mm
    - H+S Part number 84210148
    - Cable length 102 mm
- Two (2) Rosenberger SMP right-angle to SMP right-angle cables to connect the CBB3 fixture CMTS outputs to the Riser board Rx Lane 0 inputs.

  Note: These cables are not needed if you have a CBB2 fixture.
    - Rosenberger Description SMP right-angle to SMP right-angle cable
    - Rosenberger Part number 71L-19K2-19K2-00305C
    - Cable length 12 in
- Host PC to operate application software:
    - With Microsoft Windows 2000, XP, or Windows 7 (set for XP) 32-bit operating system (can also be run in a 32-bit virtual machine on a 64-bit computer)
    - One free USB port
    - Optional printer or network port to create output of test reports
- ATX type PC Power supply, with outputs as required to power Add-in card to be tested through the CBB3 fixture. A higher quality, low noise supply may be required for some Add-in cards.

- ESD dissipating mats for the work surface and wrist straps. (*Preventing electrostatic discharge (ESD)*.)

Note: As allowed in the PCI Express standard, some Add-In cards require termination of unused lanes in order to initiate generation of the compliance test pattern. The CBB3 fixture can be configured with various combinations of connectors installed to access the Tx lanes. Lanes without access connectors will be properly terminated. PLL Loop response testing is performed by measuring the Tx output on lane 0 only. If the Add-in card under test requires termination of unused Tx lanes to initiate compliance pattern generation, terminate the required lanes that have access connectors on the CBB3 fixture.

1.2 Preventing electrostatic discharge (ESD)

CAUTION. *To prevent damaging internal circuit boards and their components due to electrostatic discharge (ESD), please read the following guidelines.*

Electrostatic discharge (ESD) is a concern when handling any electronic equipment. The instrument is designed with robust ESD protection; however it is still possible that large discharges of static electricity directly into the signal input may damage the instrument.

To avoid damage to the instrument, use the following guidelines to prevent electrostatic discharge to the instrument:

- Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while connecting and disconnecting cables and adapters. The instrument provides a front panel connection for this purpose

- Discharge any static voltage from all cables before connecting them to the instrument or device under test by momentarily grounding the center conductor of the cable, or by connecting a 50 Ω termination to one end, prior to attaching the cable to the instrument.

- A cable that is left unconnected on a bench can develop a large static charge. Nothing capable of generating or holding a static charge should be allowed on the work surface.

2. Test preparation

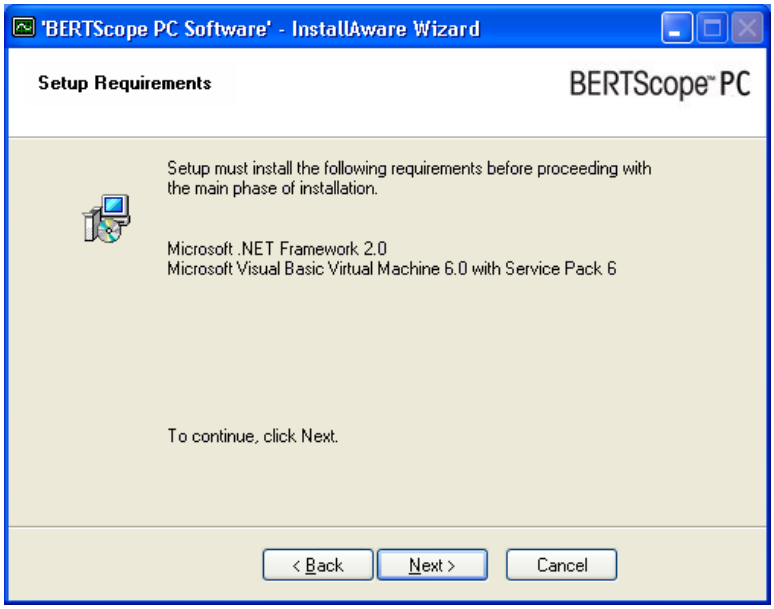
2.1 Install the control software:

Install the control software on the host PC before connecting the clock recovery instrument. The software only needs to be installed once on the host PC. It is installed from the CD-ROM supplied with the Tektronix Clock Recovery instrument or can be downloaded from the Tektronix Web site (at www.tektronix.com; search for *"BERTScopePC"*).

1. Turn on the host PC and wait for the operating system to fully boot. Install the CD-ROM into the drive or double-click the BERTScopePC Installer executable file downloaded from the Tektronix Web site.

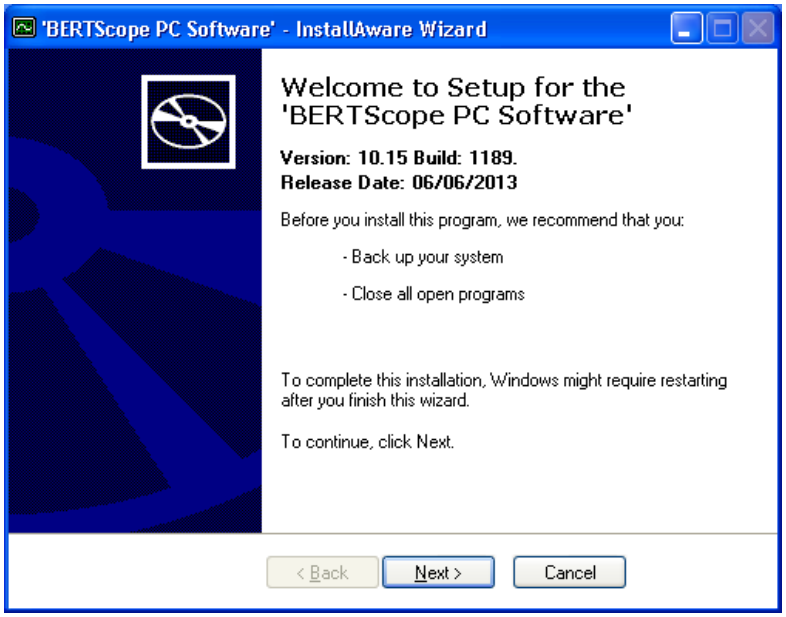
The InstallAware Wizard with a progress indicator appears.

The Setup Requirements screen appears:



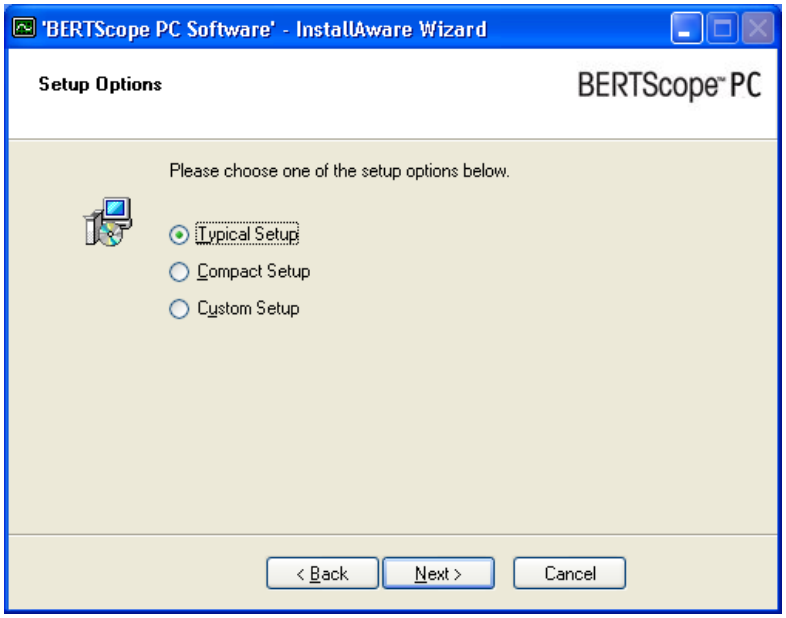
2. If the required add-ins are not installed, they can be downloaded for no charge from the Microsoft web site: www.microsoft.com.

The Welcome screen appears (the version number might be different depending on the software available with your instrument):

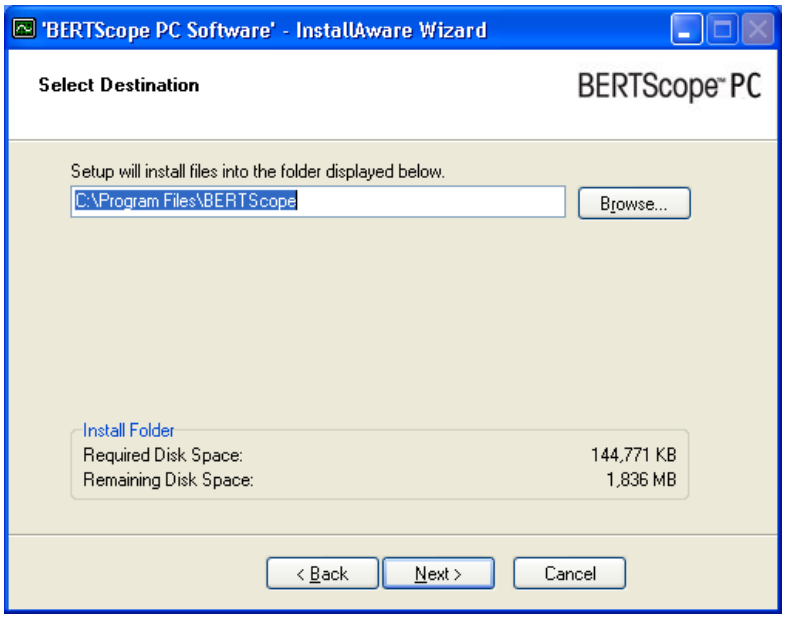


3. Click Next to continue.

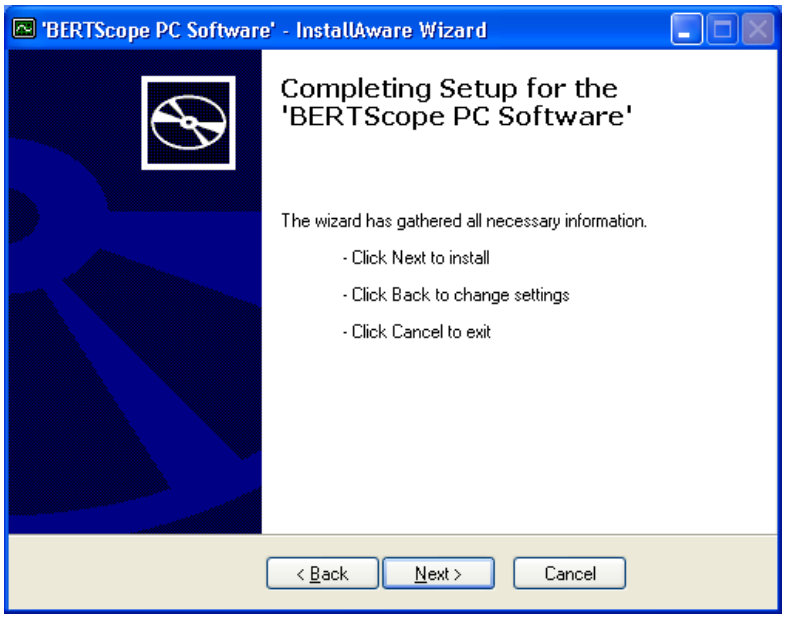
4. Select Typical Setup and then click Next.



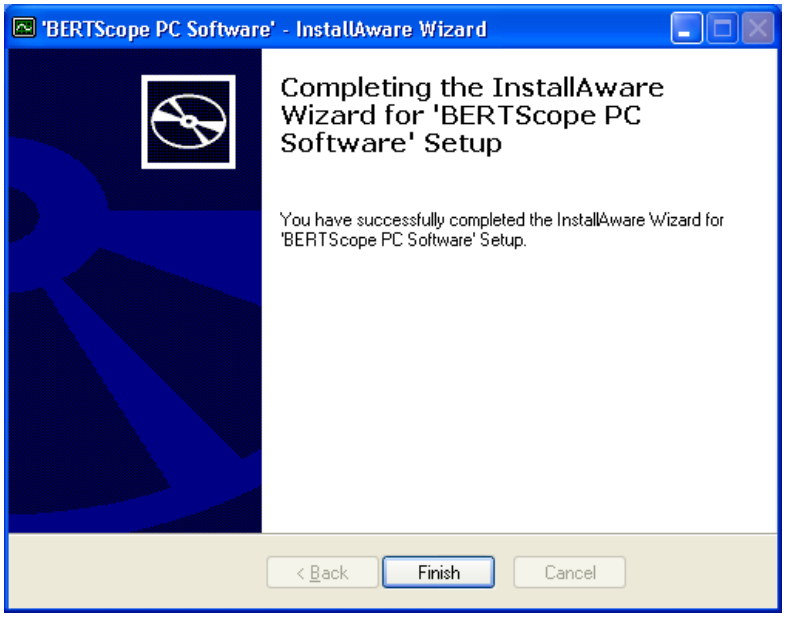
5. Select the default path as shown and click Next.



6. Click Next to install the setup.



A window with a progress bar appears, showing the installation status. At the completion, the following window will appear:



7. Click Finish.

2.2 Install the USB driver

The software installer installed and loaded the control software, but did not install the USB driver for the clock recovery instrument. You will be prompted to install the driver the first time the clock recovery instrument is connected to the host computer. The driver only needs to be installed once.

1. Be sure the control software has been loaded as described above. (See *Install the control software*.)
2. Turn on the host PC and wait for the operating system to fully boot, if not already done.
3. Connect clock recovery instrument to a power source and then push the front panel power button.
4. If you have not already done so, connect the USB cable from the USB IN connector on the rear panel of the instrument to an open USB port on the host PC.
5. The "Found New Hardware" wizard notice will appear in the lower right side of the Windows Desktop screen. After the operating system detects the type of device, the installation wizard will start.
6. The opening window will appear:

7. Select **No, not this time** and then click **Next**.

   The Wizard identifies the device as a **"Tektronix BERTScope CR"**.

8. Use the default **Install the software automatically (Recommended)** option, then click **Next**.

9. If the Hardware Installation dialog box stating that the driver has not been tested for "Windows XP compatibility" message appears, click **Continue Anyway**.

10. After the Completion dialog windows appears, click **Finish** to complete installation.

The instrument is now ready to operate.

3. Completing the instrument test setup

3.1 Configure the CBB3 fixture

The CBB3 fixture has a switch (SW4) that selects either a clock signal applied to the REF CLK INJ SMP connectors (J25 and J26, labeled P and N respectively) or to an internal reference clock. Ensure that SW4 is in the EXT REF CLK position.

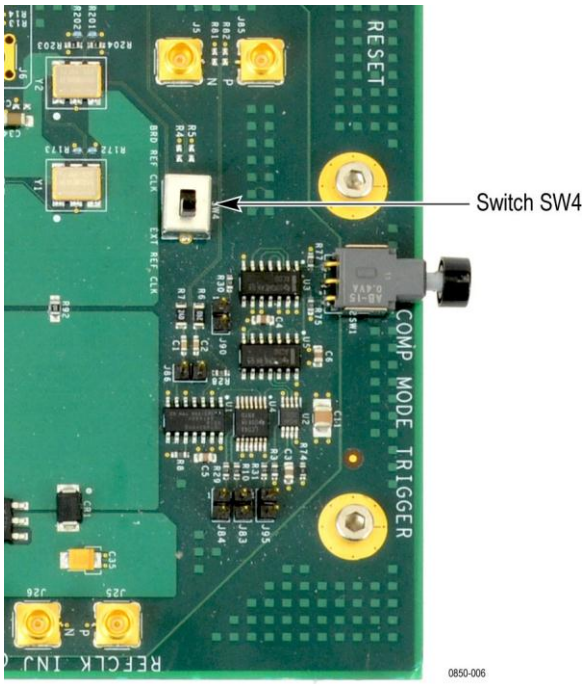


Figure 2. Location of SW4 on the CBB3 fixture

3.2 Connect the test hardware

Before configuring the test setup, prepare the area for testing. Tektronix recommends using an ESD dissipating mat with the work surface with antistatic wrist straps. A grounding connection is located on the front of the clock recovery instrument.

NOTE: **The following steps assume that you are using the CBB3 fixture as part of the test hardware.**

A CBB2 fixture can be used instead of the CBB3 fixture. The CBB2 PCIe 2.0 compliance toggle circuit creates a 1 ms duration pulse of a 100 MHz REFCLK that inputs directly into the RX0 lane of the DUT to generate the stimulus to switch signal speed and or de-emphasis levels.

NOTE: **These setup instructions assume that the Riser board and DUT are already connected to the CBB3 fixture.**

Refer to the following steps to connect the cables between the CBB3 fixture and Riser board:

NOTE: The following steps are not needed if you have a CBB2 fixture; the CBB2 fixture has the required circuitry to directly connect to the RX Lane 0 input.

1. Connect one of the SMP right-angle to SMP right-angle cables from the CMTS J3 (N) output connector on the CBB3 board to the Rx LANE 0 J18 (N) input connector on the Riser board.

2. Connect the other SMP cable from the CMTS J83 (P) output connector on the CBB3 board to the Rx LANE 0 J2 (P) input connector on the Riser board.

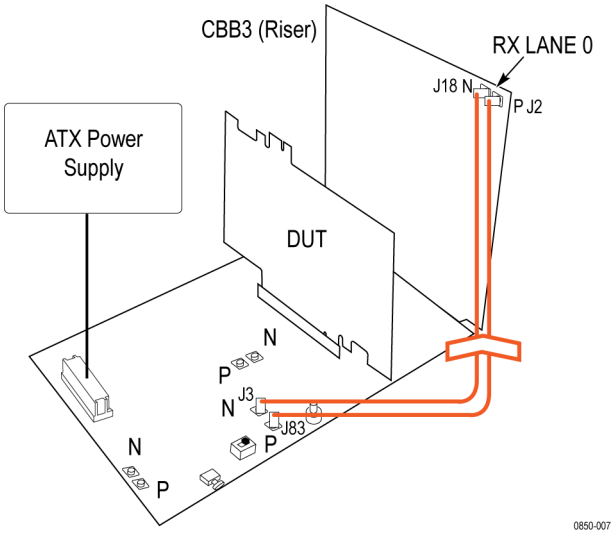


Figure 3. Preliminary connections

The following figure shows the connections between a CR286A instrument (front and rear) and the CBB3 fixture. Refer to this illustration for a quick overview of the hardware test setups. If your setup has a different clock recovery instrument, the connections are similar.

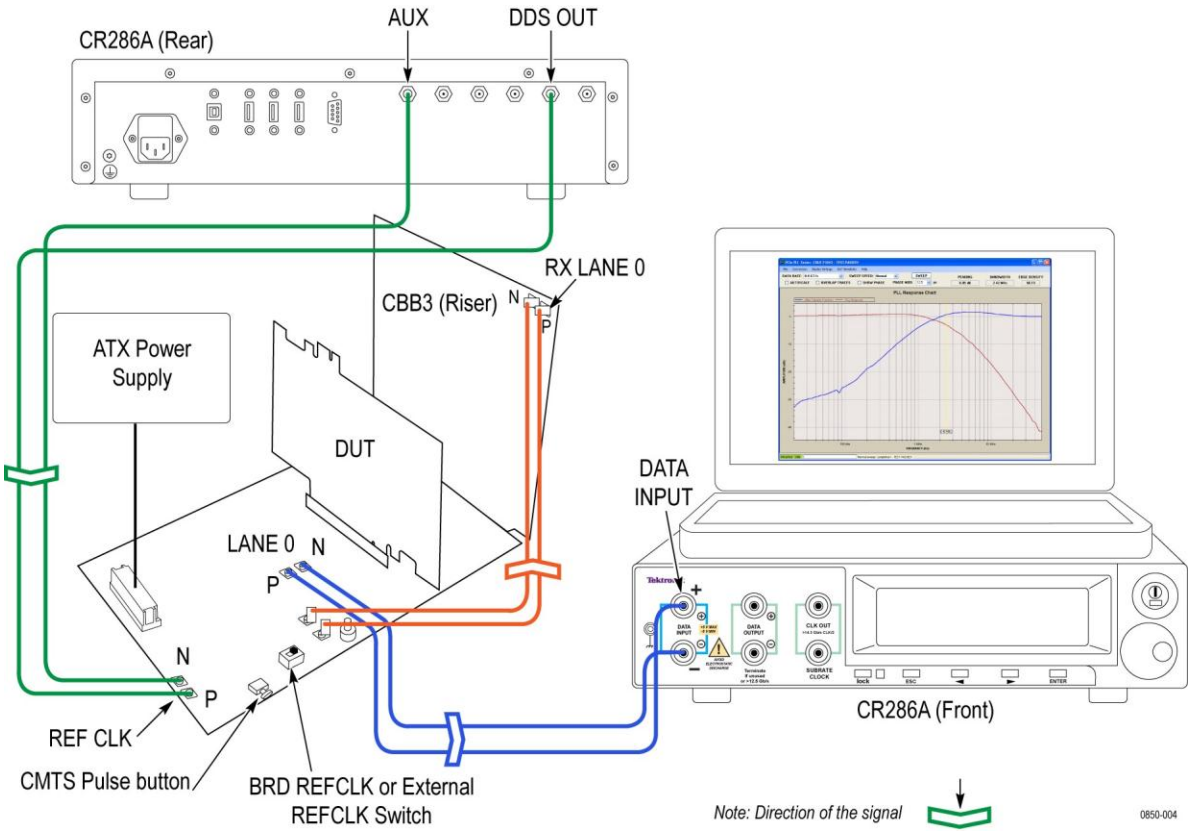


Figure 4. Hardware connections from the clock recovery instrument to the CBB3.0 main board

Configure the instrument and cabling as described:

1. Connect the ATX PC Power Supply to the power connector on the CBB3 fixture.
2. Connect one of the 102 mm SMP-to-SMA cables one end of each SMA interconnect cables.
3. Connect one of the 1.0 interconnect cables from the AUX output on the rear of the clock recovery instrument to the REF CLK P SMP input connector on the CBB3 fixture.
4. Connect the second 1.0 m interconnect cable from the DDS OUT output on the rear of the clock recovery instrument to the REF CLK- SMP input on the CBB3 fixture.

Figure 5. Clock recovery instrument rear panel connections

The REF_CLK connector locations and LANE 0 connector locations on the CBB3 fixture are shown below.

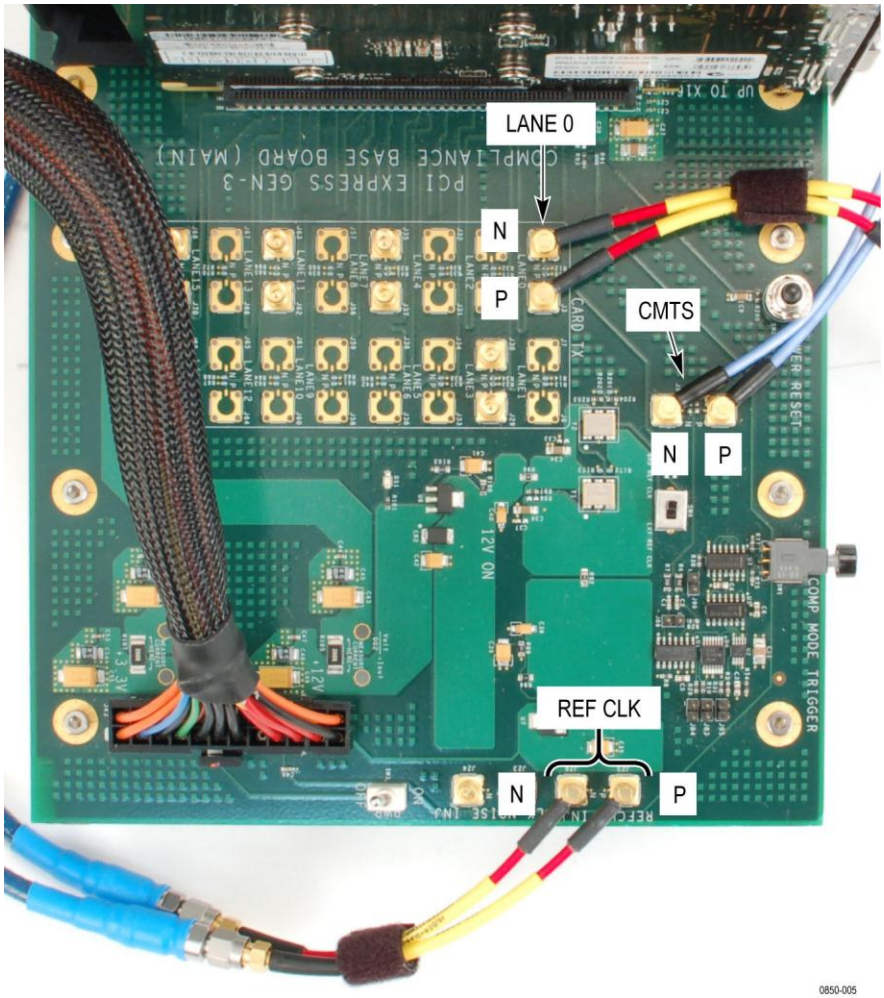


Figure 6. CBB3 fixture connector locations

5. Connect one of the 0.5 m interconnect cables from DATA INPUT + on the front of the clock recovery instrument to the Tx LANE 0 P SMP connector on the CBB3 fixture.

6. Connect the other 0.5 m interconnect cables from the DATA INPUT - on the clock recovery instrument to the Tx LANE 0 N SMP connector on the CBB3 fixture.

Figure 7. CR286A front panel connections

7. If required by the Add-in card to initiate compliance output pattern, terminate unused Tx lanes with SMP connectors with 50 Ω terminators.

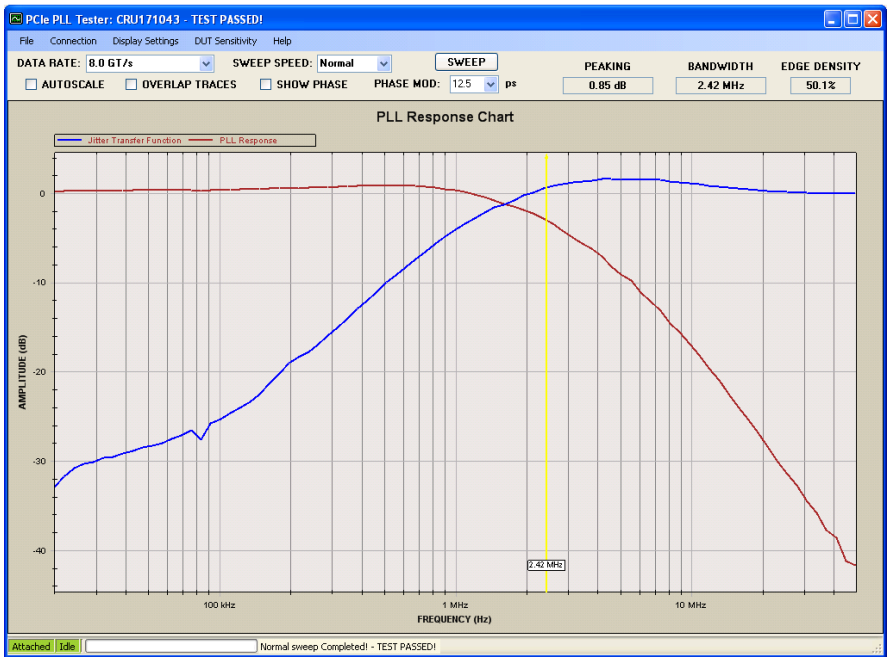
4. Test the PLL Loop Response

With the cable configuration completed, the system is ready to perform PLL Loop Response measurements. No user calibration or normalization steps are required.

Initiate the testing by powering up the host PC and the clock recovery instrument. Start the Control software application by clicking

START > PROGRAMS > BERTScope > BERTScope PCIe PLL Tester

The application opens with the single window used for control and display:



In the DATA RATE pull down menu, select **8 GT/s.**

The phase modulation defaults to 12.5 ps, the maximum allowed by the compliance spec. This setting should be used for a normal compliance test. Other modulation levels can be entered to characterize sensitivity to modulation level, and observe test margin to this parameter.

Perform the test using the following procedure:

1. If required by the Add-in card to initiate compliance output pattern, terminate unused Tx lanes with SMP connectors with 50 Ω terminators.

2. Turn on the power supply.

3. Turn on the device power using the PWR switch on the CBB3 fixture. Note The response characteristics in the Tx clock generation PLL in some devices have been known to drift during warm up. When this occurs, the drift appears to have a relatively fast time

constant. It the card being tested demonstrates this effect, wait approximately 10 seconds before initiating the test.

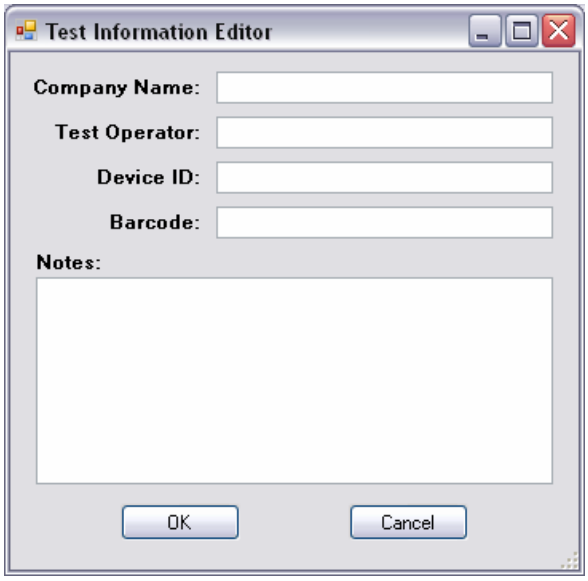
4. Push the CMTS (Compliance Mode Toggle Signal) button (SW1) on the side of the CBB3 board at least four (4) times to place the Add-In card into the PCIe3 (8 GT/s) mode.

   You can verify this by checking the CR display to ensure that the PLL is locked at 8 GT/s.

5. Click **SWEEP** to begin the test. The test will take approximately 15 seconds to complete. Prior to stepping the Sj modulation, the clock recovery instrument initiates the test by generating a clean REF_CLK signal, and measures the edge density of the Tx output. The measured edge density is displayed continuously in real time in the upper right corner of the application software window. If the device is generating a normal compliance pattern without gaps, the transition density measurement should read approximately 48.6%.

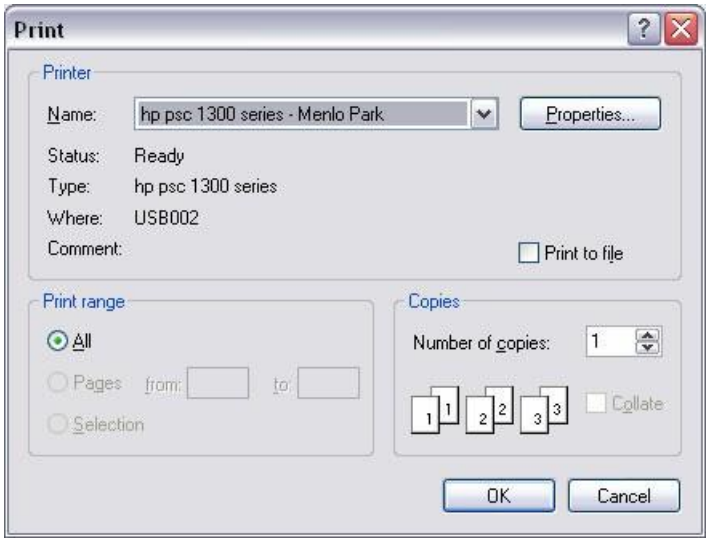
6. At the completion of the test sweep, the measured loop bandwidth and peaking will be displayed. The software also compares these results against the compliance limits for a generation 3.0 device, and displays TEST PASSED or TEST FAILED at the top banner of the window.

7. To generate a test report hard copy, click FILE-PRINT from the top menu area. A Test Information dialog box will first appear to record information which will appear on the test report.



8. Enter the appropriate information and click **OK**

   The standard Windows Print Dialog box appears.



9. Select the printer of choice and click **OK** to generate a test report. To generate the test report and save as an HTML file for later printing, select **FILE-PRINT TO FILE** from the top menu in the application

This completes the PLL Loop Response test.

Appendix A: Abbreviations

PCIE	Peripheral Component Interconnect Express
Gen-2	Generation-2 PCI Express
CLB	Compliance Load Board
SMP	Sub-miniature Type P connector
SMA	Sub-miniature Type A connector
UI	Unit Interval