Tektronix®

Characterizing and Troubleshooting Jitter with Your Oscilloscope

APPLICATION NOTE

Introduction

Clocks are the heartbeats of embedded systems, providing timing references and synchronization between components, subsystems, and entire systems. Disruptions and distortions of clock signals can cause degraded or intermittent system operation, so thorough characterization of clock signals is a critical step in reliable embedded system design.

Jitter is a common way to express the performance of a clock circuit. Put simply, jitter is the deviation of the timing of a signal edge from where it should be. There are a variety of measurements to characterize jitter.

This application note provides several examples of jitter measurements using the standard and optional measurement capabilities available in the 5 and 6 Series MSOs.

This application note

- Gives a brief orientation of simple timing analysis measurements on clock signals
- Explains how to interpret timing and jitter measurements
- Gives examples of measurements on non-modulated clocks, spread-spectrum clocks, serial data with embedded clock, and clocked data
- Explains how advanced jitter measurements can improve timing characterization and troubleshooting

This application note uses the 5 Series MSO mixed signal oscilloscope to illustrate jitter measurements. The 6 Series MSO and 7 Series DPO operate identically, but are available with higher bandwidth and offer lower input noise. Many of the measurements shown can be performed with other modern Tektronix oscilloscopes, although specific setups will vary. Some of the measurements in this application note take advantage of the optional Advanced Jitter Analysis software for the 5, 6 and 7 Series Oscilloscopes.

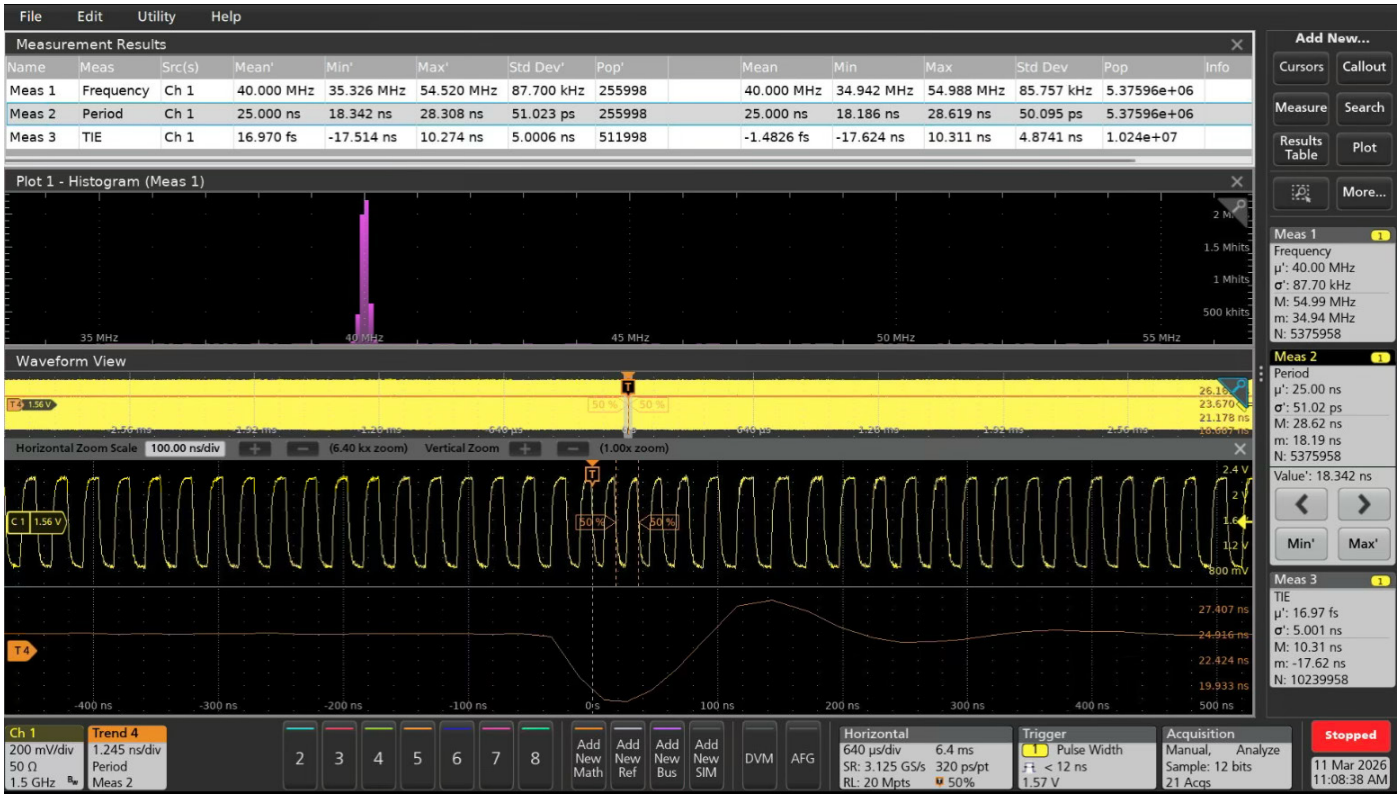

Figure 1. Frequency, Period and TIE results of a 40 MHz clock. Note the few cycles where the periods get shorter than expected on T4 trace.

Clock Jitter Characterization

Using Standard Automated Measurements

Standard measurements included on a modern Tektronix oscilloscope, shown in **Figure 1**, provide a good starting point for jitter analysis. With the standard measurements you can verify whether the clock frequency meets your requirements; add measurement statistics, such as minimum and maximum, providing confidence that the clock pulses are continuous; and see the standard deviation (σ) as a quantitative measure of the frequency stability. These statistics give some needed insight into the manner of frequency variation.

Standard graphical tools such as measurement histograms provide additional information about the characteristics of measurement variations. The measurement system can also quickly find outliers, helping you uncover problems and get to debugging. Frequency, Period, and Time Interval Error (TIE) measurements on a 40MHz clock are shown in **Figure 1**.

A mean value alone can suggest a clock is performing as designed, and in this case it does. Experienced engineers know that the mean only tells part of the story. That's why Tektronix oscilloscopes, unlike others on the market, are uniquely equipped with the measurements and analysis to tell the whole story. Enabling statistics in the measurement badges at the right side of the display tells the whole story. The min and max values let you know there are outliers. Notice Plot 1 - Histogram of Frequency results has most of the hits right at 40 MHz, but the scale of the plot tells you that other values outside that range exist but not very often. When you look at the shape of the T4 Trend in orange you can see that 99.999% of the time everything is stable except for a few cycles where the clock changes then restabilizes. The zoom window helps you see clock dispersions, found quickly using the toolset of statistics, plots, and Min/Max results finder in the oscilloscope measurement system.

Also worth noting is how the Results Table placed at the top of the screenshot collects this data. The statistics on the left side represent the current acquisition, while the statistics on the right side represent the accumulation of all acquisitions made over time.

All measurements shown in **Figure 1** are in the standard measurement set on a modern Tektronix oscilloscope. For more advanced jitter analysis, including separation of random and deterministic components, the optional Advanced Jitter and Timing Measurements can be used.

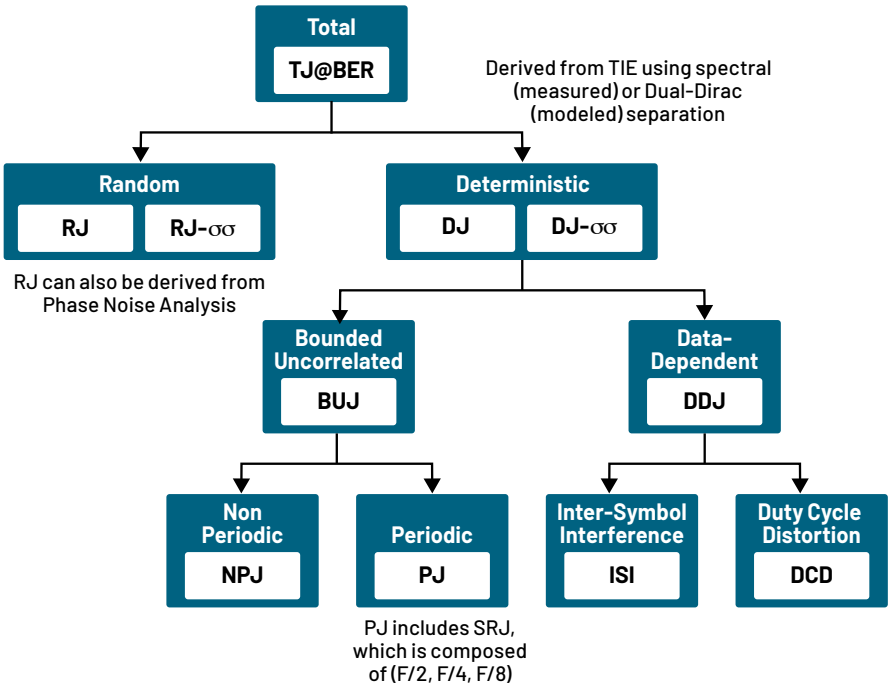

Figure 2. Diagram of jitter decomposition available on modern Tektronix oscilloscopes providing insight into the root cause of timing variations. Using Tektronix's patented spectral analysis method, Tektronix oscilloscopes are the only oscilloscopes on the market that actually measure jitter components directly from the signal — giving engineers a fast, accurate path to root cause without relying solely on statistical approximations.

Using Advanced Jitter Analysis

As shown in **Figure 2**, timing jitter can be decomposed into components, providing insight into the root cause of the timing variations. Tektronix's patented spectral analysis method measures jitter components directly from the signal — giving engineers a fast, accurate path to root cause without relying solely on statistical approximations. Where needed, industry-standard statistical modeling techniques such as dual Dirac are also supported, enabling compliance-driven evaluation alongside hands-on debug. Let's dive into some practical examples using the Advanced Jitter Analysis software (option DJA) to demonstrate jitter decomposition and interpretation of the results.

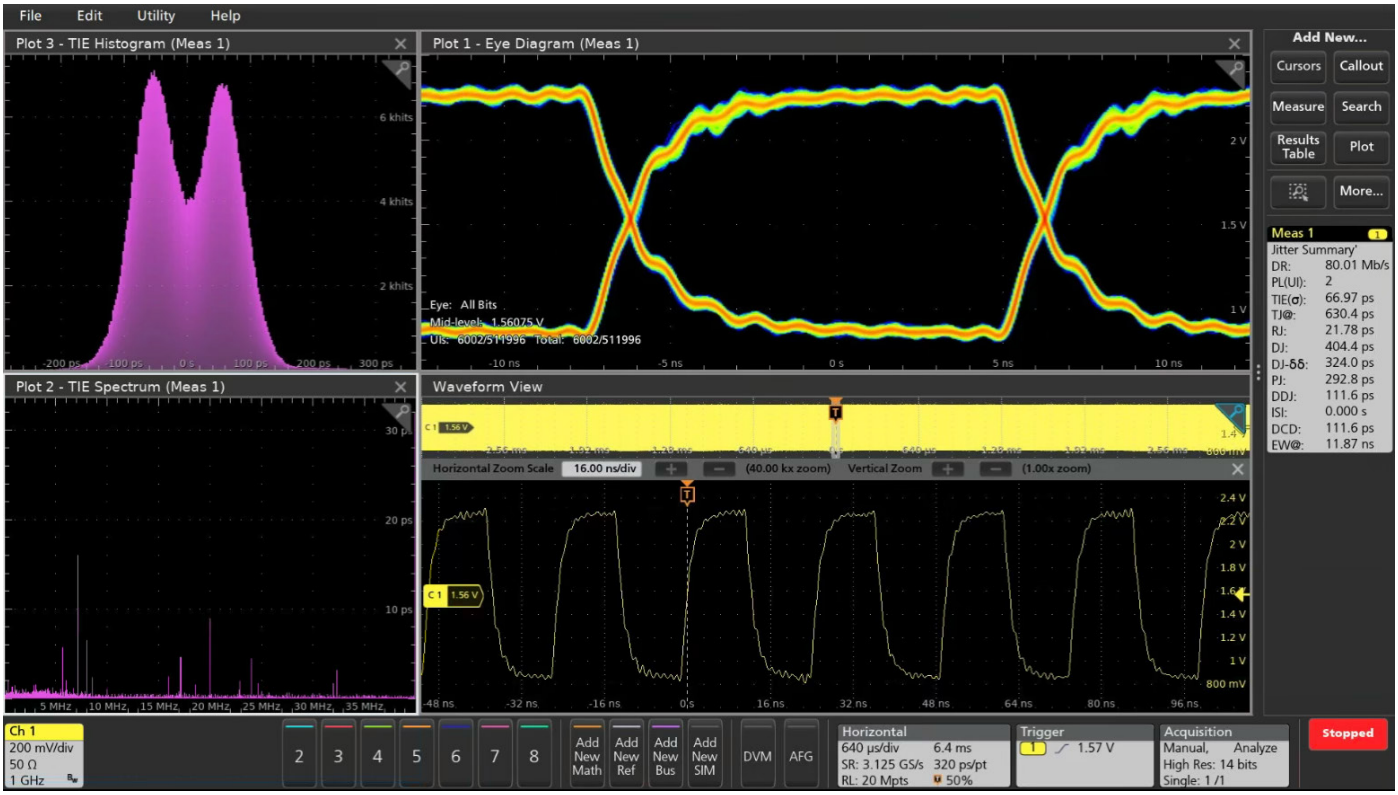

Figure 3. Jitter Summary measurement of a 40 MHz clock using Advanced Jitter Analysis software (option DJA).

40 MHz Non-modulated Clock Revisited

Applying the Jitter Summary measurement group in the optional Advanced Jitter Analysis software (option DJA) to the 40 MHz clock reveals some new clues. The Jitter Summary measurement in **Figure 3** renders an eye diagram of the signal, measures TIE, plots the histogram and spectrum of the TIE measurement, and decomposes the jitter into its individual components. Analysis is set to use both edges; this is why you see an eye diagram on a clock signal.

At first glance, the open eye in the eye diagram in **Figure 3** suggests that the clock signal has fairly low jitter based on the thickness of the eye edges. Indeed, the Total Jitter (TJ@BER) measurement value of about ~600ps is about 2% of the 40 MHz clock period. The jitter decomposition shows that the Random Jitter (RJ) component is very small relative to the period of 25 ns.

Therefore, the Deterministic Jitter (DJ) is the dominant component. The bi-modal nature of the TIE histogram also suggests a strong DJ component. The DJ is further decomposed into Periodic Jitter, Data Dependent Jitter, ISI and Duty Cycle Distortion. The difference between DJ and DJ $\sigma-\sigma$ shows the error in the model to fit this dataset to a dual dirac when the histogram, while close, is not that distribution.

The Periodic Jitter (PJ) is over half of the deterministic jitter. There are clear spectral components in the TIE Spectrum plot, indicating strong peaks at 7, 20, and 17 MHz. This suggests that the jitter has significant uncorrelated deterministic jitter, perhaps caused by signal crosstalk on the circuit board or within the FPGA. Since this is a clock signal rather than a data signal, by definition the Inter Symbol Interference (ISI) is zero. As you can see from the waveform, the asymmetry of the rising edges versus the falling edges leads to Duty Cycle Distortion (DCD) jitter. This suggests that the clock shaping circuit deserves further analysis and optimization.

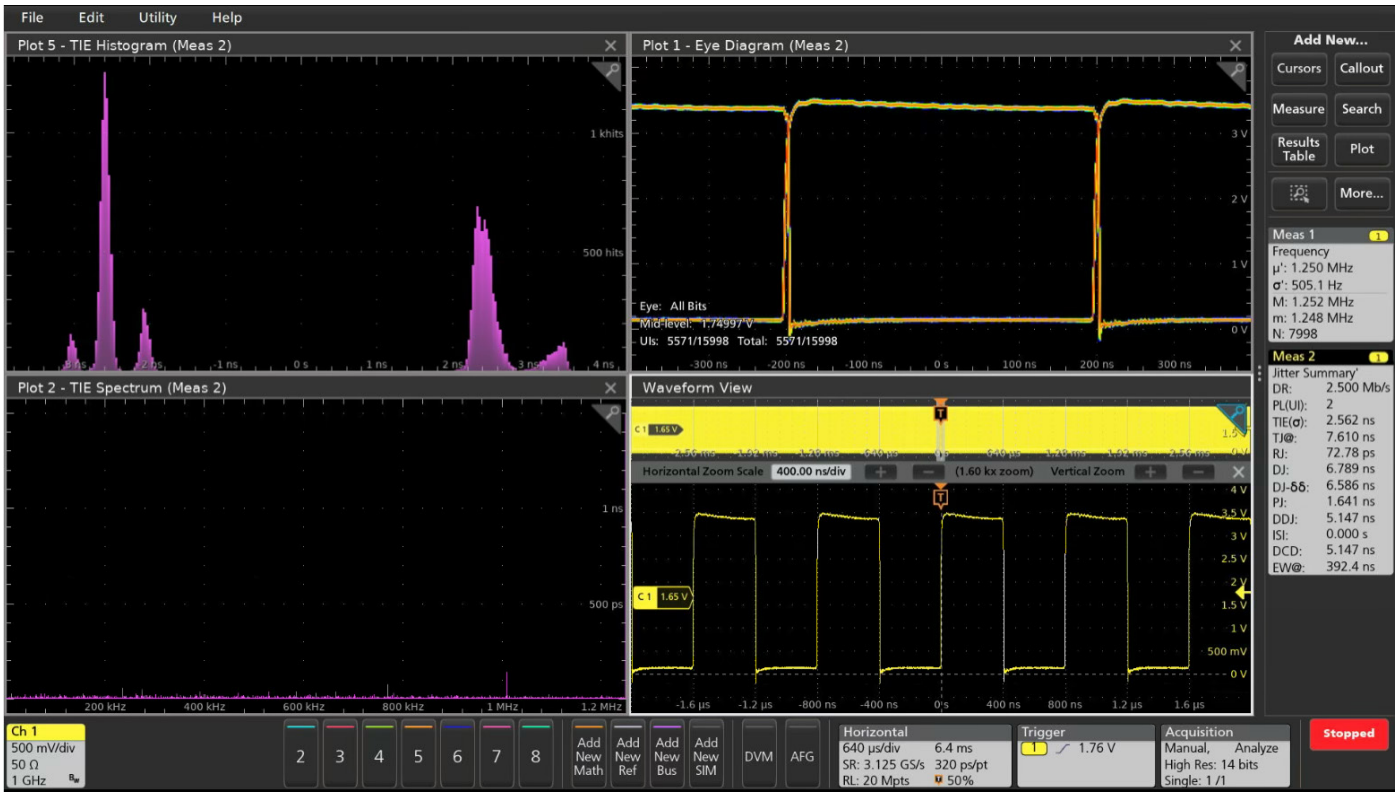

Figure 4. Jitter Summary analysis of a 1.25 MHz clock.

Figure 4 shows the analysis of another clock signal in the system, and it exhibits some different jitter characteristics. From the open eye in the eye diagram, you can conclude that the jitter on the clock signal is small. This is verified by the Total Jitter measurement value of about 7.6 ns, which is less than 0.95% of the clock period. The jitter decomposition shows that the Random Jitter component is very small at 73ps, an order of magnitude lower and not a problem.

The Periodic Jitter is also relatively small, and there are no clear spectral components in the TIE Spectrum plot, indicating that the jitter on the signal is not significantly related to uncorrelated components of the deterministic jitter. Because this is a clock signal rather than a data signal, the ISI is zero. However, the Duty Cycle Distortion causes a significant portion of the jitter. Why is this the case? Let's look at it in a different way.

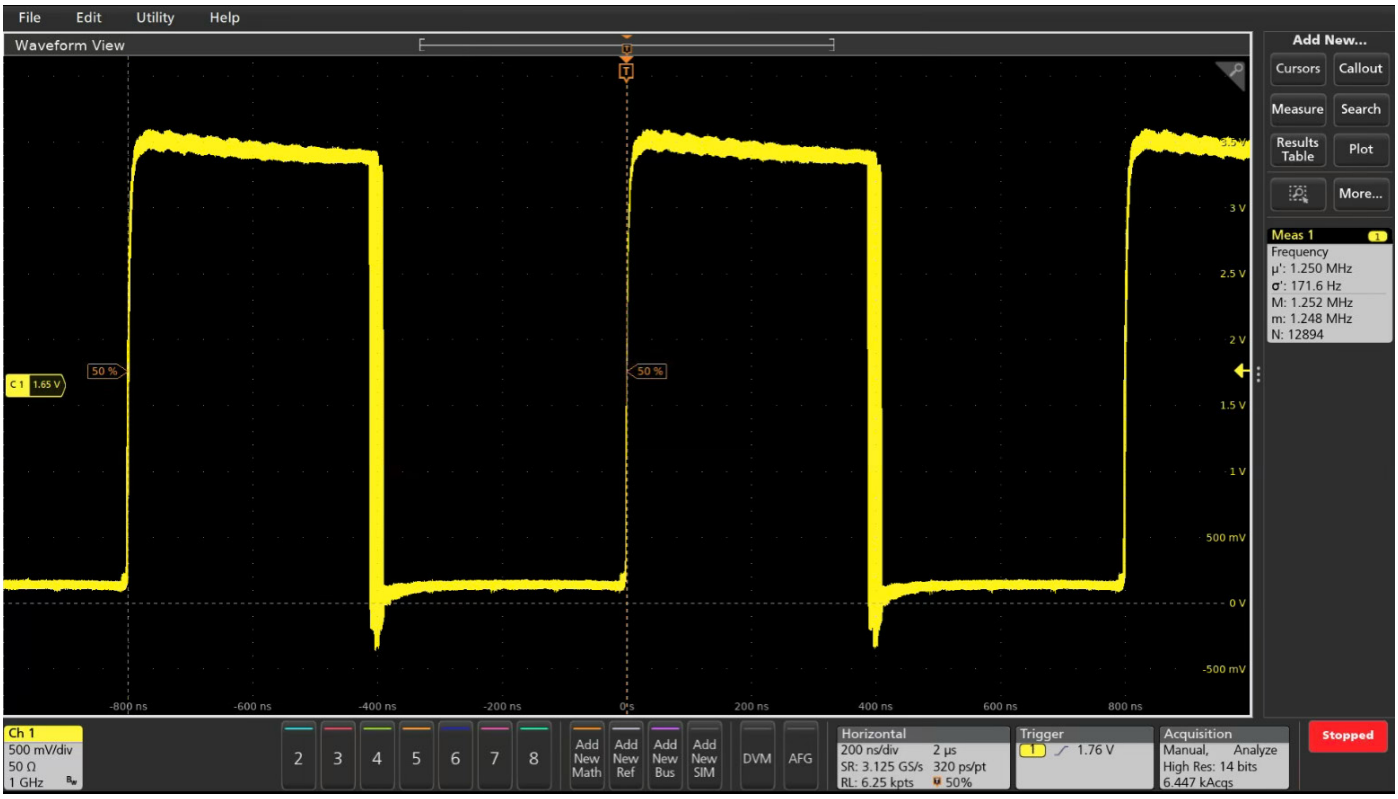

Figure 5. Duty Cycle variations are visible on the falling edges of the 1.25 MHz clock.

Armed with the clue that DCD is a major contributor, **Figure 5** shows a persistence display of the clock signal. The wide falling edges of the signal clearly show that the duty cycle is varying significantly relative to the rising edges being stable. If the embedded system uses the rising edge of the clock throughout, this duty cycle variation may not present a problem. However, if some of the circuits depend on the falling edge or both edges of the clock, this jitter behavior may cause the system to behave incorrectly or unreliably.

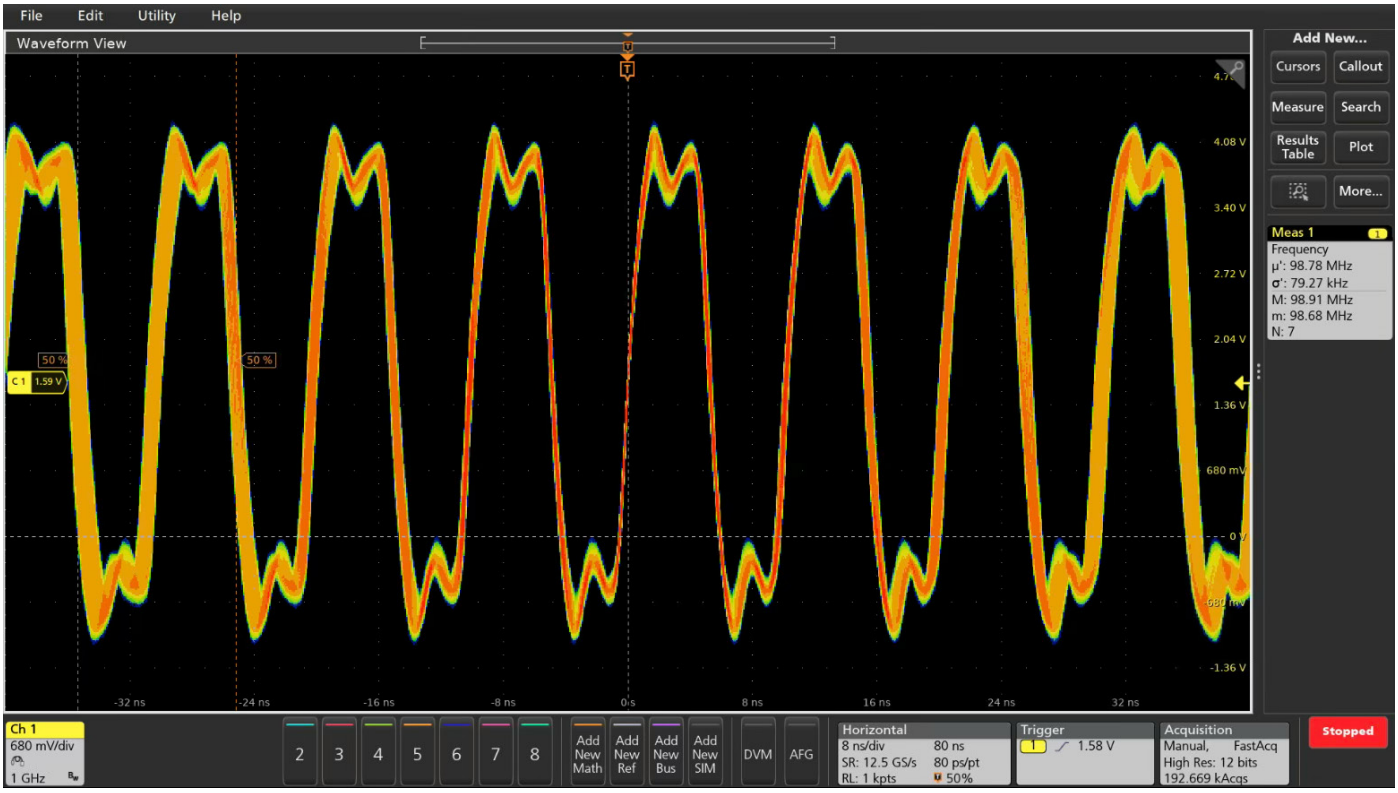

Figure 6. FastAcq capture time-domain of a 98 MHz clock.

Spread Spectrum Clock Characterization

The final example of clock analysis in this design is shown in **Figure 6**. The frequency measurement varies over time around the 98 MHz mean value. The clock period is varying, as indicated by the horizontal smearing in the waveform edges away from the trigger point.

Measurement statistics quantify frequency variation when captured over sufficient time and edge count. A FastAcq capture or infinite persistence capture gives a useful first look, yet a longer acquisition is needed to build the statistical confidence that reveals the full extent of the spread. The statistics from a frequency measurement could help verify that the clock is within design specifications, but it would not help in understanding how frequency is varying. In this case, the signal is a spread-spectrum clock (SSC) where the frequency is intentionally modulated. But is the design working as expected?

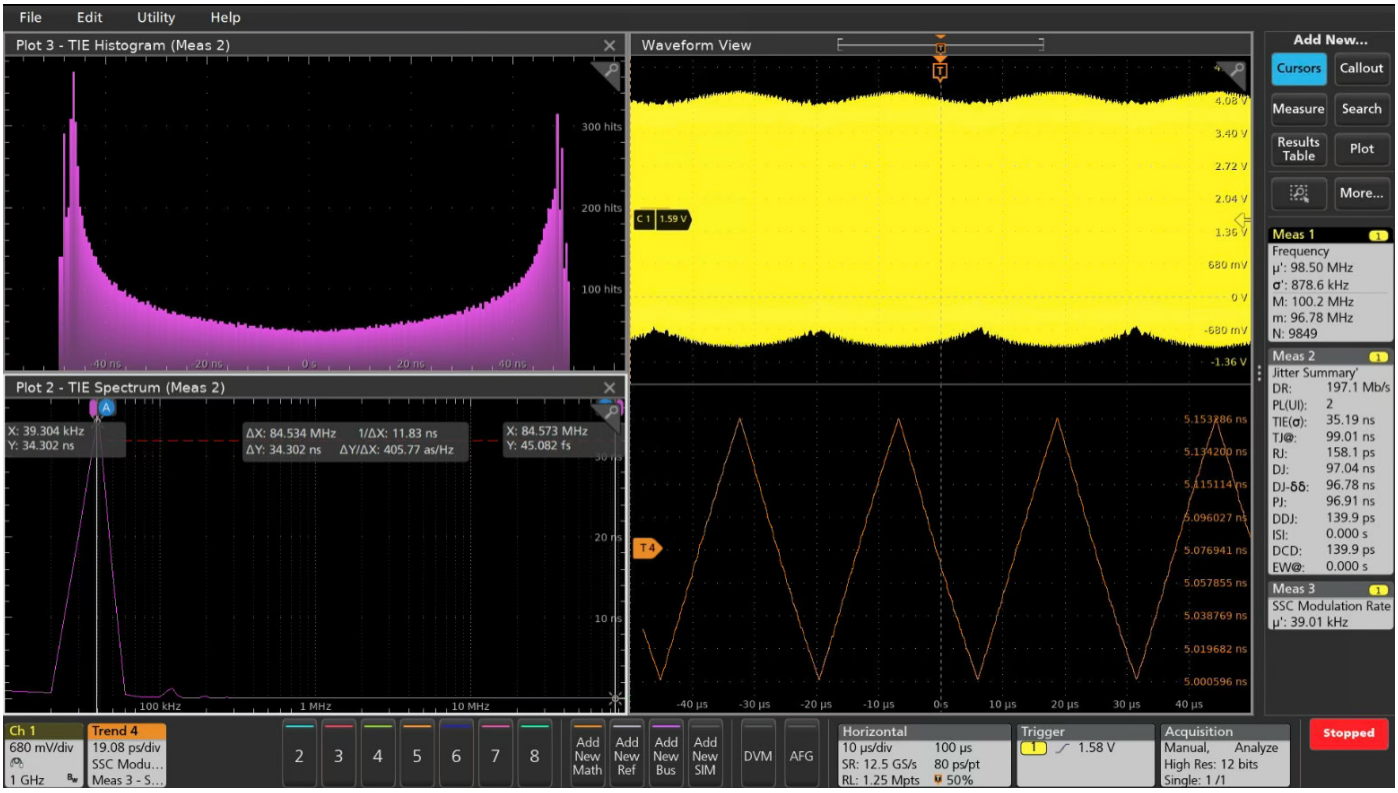

Figure 7. Jitter Summary of a 98 MHz spread spectrum clock.

Again, the Jitter Summary provides a wealth of information. The frequency variations (jitter) are dominated by Periodic Jitter. This is reflected in the measurement results and in the saddle-shaped TIE histogram. This U or saddle shape results from a single dominant PJ component in the signal.

In addition to jitter separation and eye diagrams, the Advanced Jitter Analysis software also has SSC measurements like Modulation Rate, SSC Freq Dev, Slew Rate and can plot the SSC profile. Having turned on the Mod Rate measurement, we can see that the modulation rate is about 39 kHz in the right hand side of the display.

Again we can use the plots provided to see where the results come from in the waveform and measurements. The TIE spectrum shows a single dominant spike at 39kHz. The orange T4 trend plot shows the SSC profile, a 39 kHz triangle wave.

Since we have a long-time capture, we can use the statistics of the Frequency measurement to see how much spread there is on the clock. From the min and max values, you can see the clock is modulating from 97 MHz to 100 MHz.

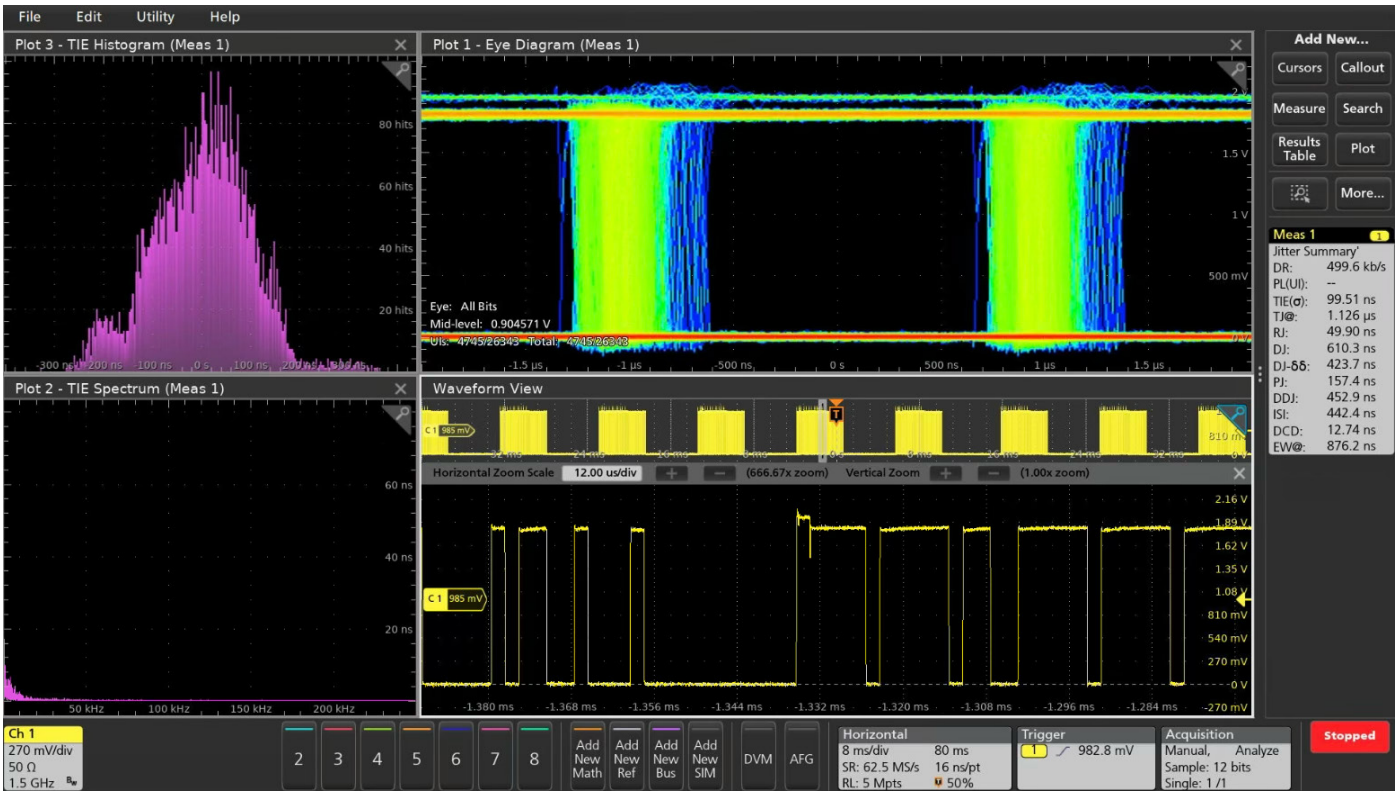

Figure 8. Jitter Summary analysis of a differential CAN bus signal at the transmitter, showing wide eye opening.

Low-speed Serial Bus Jitter Measurements

Jitter also affects the performance of serial buses, including self-clocking buses. **Figure 8** shows the Jitter Summary analysis of a 500 kb/s differential CAN bus signal at the transmitter. Similar measurement techniques can be used on other serial buses at the transmitter and the receiver.

The first step in this analysis is to recover a clock signal from the serial data signal. In this case, the software is performing a clock recovery using a Phase Locked Loop (PLL) with a narrow loop bandwidth to remain locked between data bursts. This recovered clock is then used as the reference for the jitter analysis.

The jitter decomposition shows that the majority of the total jitter at the transmitter is due to ISI. That means it is correlated jitter from **Figure 2** above. It correlates to the data rate and pattern repeat of the signal. Things like impedance mismatches on the transmission cables or traces often come into play.

Another great feature you can use for these bursts or multi-member buses is gating. Tektronix can gate per bus member, showing you an eye diagram for only one member of the bus. This enables debugging and identifying who is messing up signal quality of a bus like CAN.

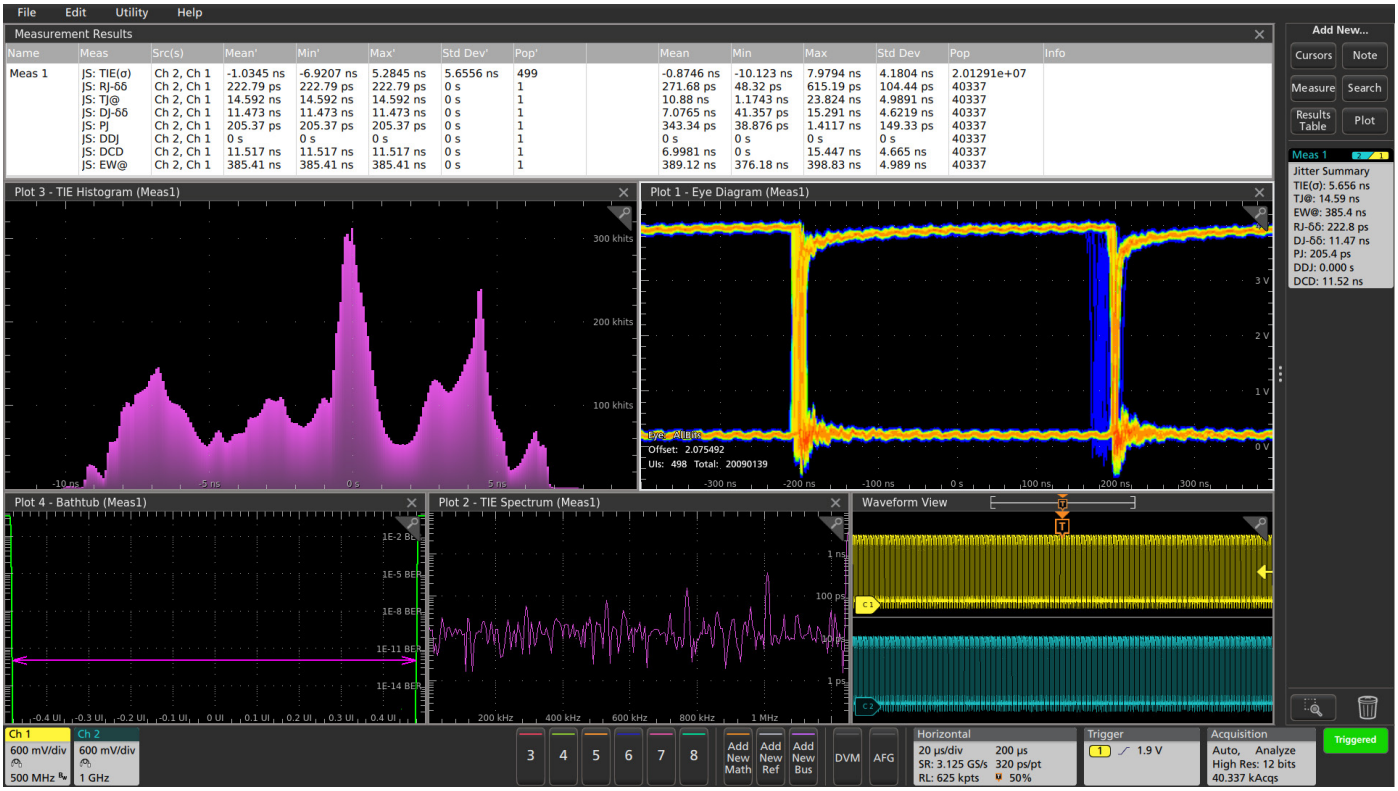

Figure 9. Jitter analysis of a synchronous logic circuit.

Clocked Data Jitter Measurements

The final example of jitter analysis is on a synchronous logic circuit. Unlike the previous examples, this circuit has an explicit clock signal, so the jitter measurements are made on the cyan data signal on channel 2 relative to the yellow clock signal on channel 1 (shown in the lower right corner of **Figure 9**).

The clock rate is just 1.25 MHz and the circuit board traces are short, so the signals are fairly clean, as indicated by the low random jitter and wide eye pattern. Because this circuit is using a separate clock signal, we would not expect that the jitter would be data-dependent.

In this case, the jitter seems to be dominated by duty cycle distortion. Further analysis of the circuit shows that the clock for this circuit was derived from the clock that was shown in **Figure 5**. Not coincidentally, a significant portion of this circuit's total jitter is due to the duty cycle distortion of the clock signal.

Achieve Reliable Embedded Design

Jitter is an unavoidable reality in every digital system. Pinpointing its sources is fundamental to achieving reliable, robust embedded designs. As the examples in this application note demonstrate, Tektronix provides an industry-leading approach to jitter analysis: from characterizing frequency stability with standard measurements and statistics, through full decomposition using Tektronix's patented spectral analysis method that measures jitter components directly from the signal. Where needed, industry-standard statistical modeling techniques such as dual Dirac are also supported, enabling compliance-driven evaluation alongside hands-on debug.

Whether the challenge is a clock with unexpected duty cycle distortion, a spread-spectrum source that needs modulation verification, or a serial bus with ISI at the receiver, the Advanced Jitter Analysis software (option DJA) provides the decomposition and visualization tools to move quickly from symptom to root cause. The result is shorter debug cycles, greater confidence in timing margins, and designs that reach the market faster.

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