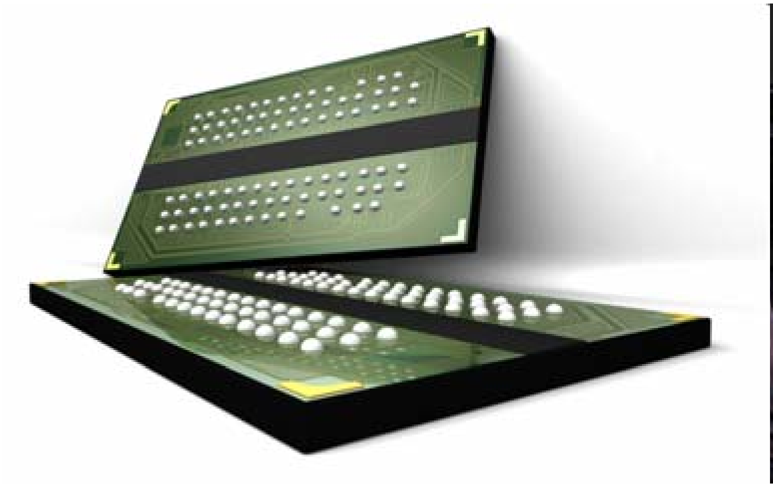
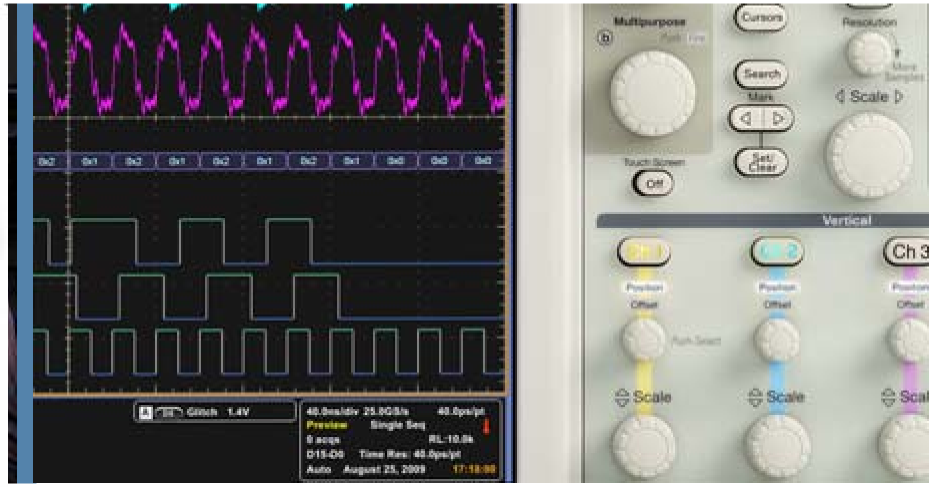
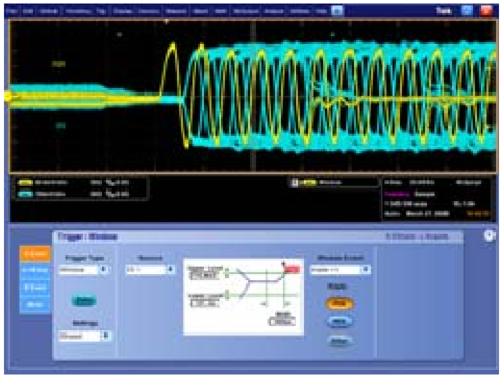
DDR Verification Approaches

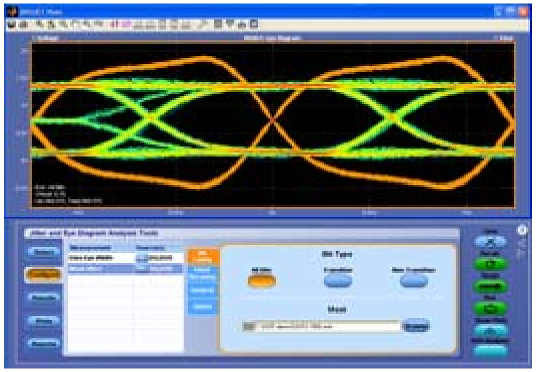




DDR Test Challenges

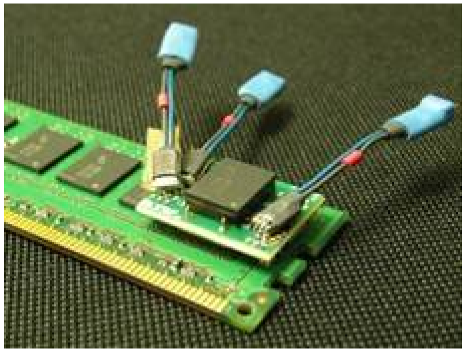
- Signal Access & Probing
  - Easy-to-use / reliable connections
  - Bandwidth & Signal Integrity
  - Affordable
- Isolation of Read/Write bursts
  - Triggering or Post-Processing (ASM)
- Complexity of JEDEC Conformance Tests
  - Vref / Vih / Vil
  - Derating
- Results Validity / Statistics
- Effective Reporting / Archiving
- Advanced Analysis
  - Characterization
  - Debug

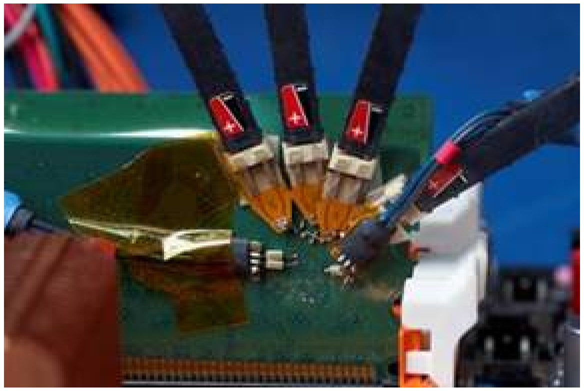


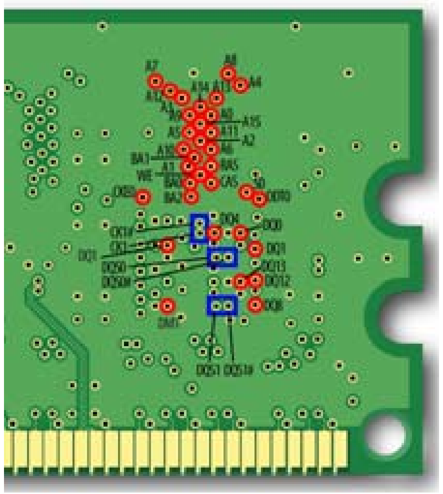


Challenge 1: Probing DDR Memory

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB
- All DDR2 & DDR3 Components use BGA Packages
- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device
- Signal Access Solutions
  - Component Interposers
  - Direct Probing
  - Analog Probing
    - DQ, DQS, Clock
  - Digital Probing
    - Address
    - Command
    - Power, Reset, and Reference


Component Interposer

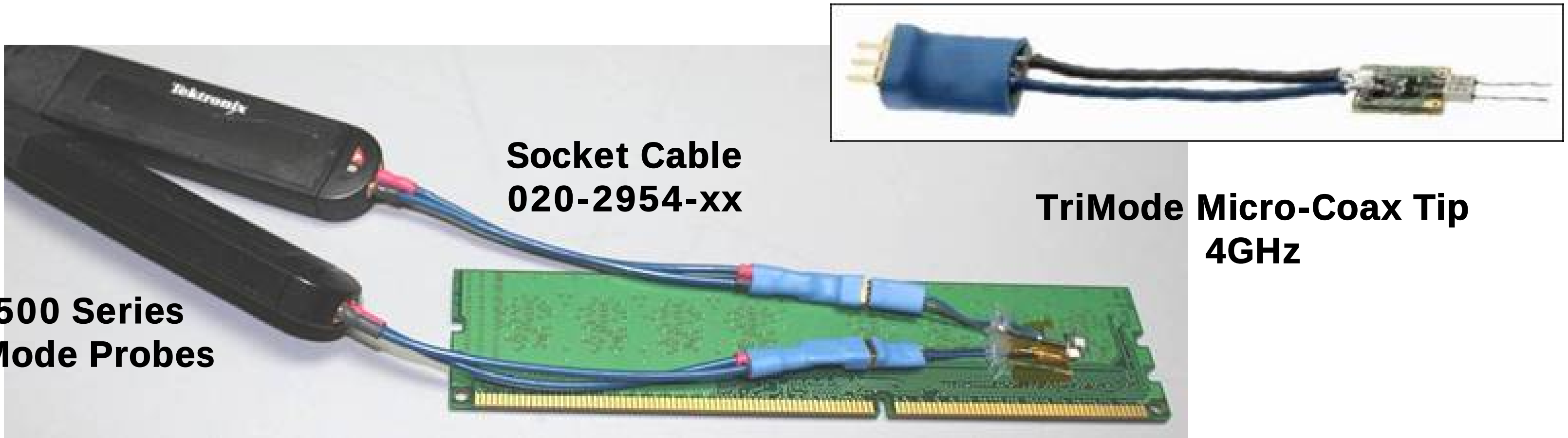

Analog and Digital Probing




Direct Probing

*Courtesy Micron Technologies

Analog Solder-In Probing Solutions for DDR



Socket Cable
020-2954-xx

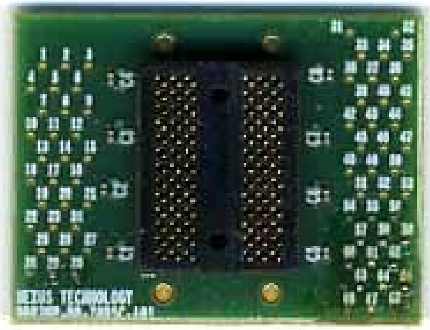
TriMode Micro-Coax Tip
4GHz

P7500 Series
Tri-Mode Probes

P75TRLST Solder Tip
up to 20GHz

Nexus DDR3 BGA Chip Interposers For Oscilloscopes

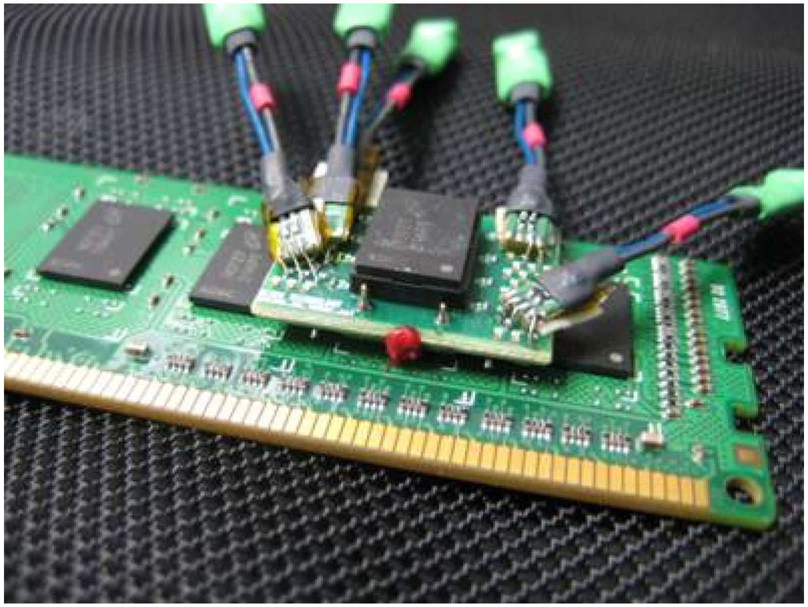
Retention Socket

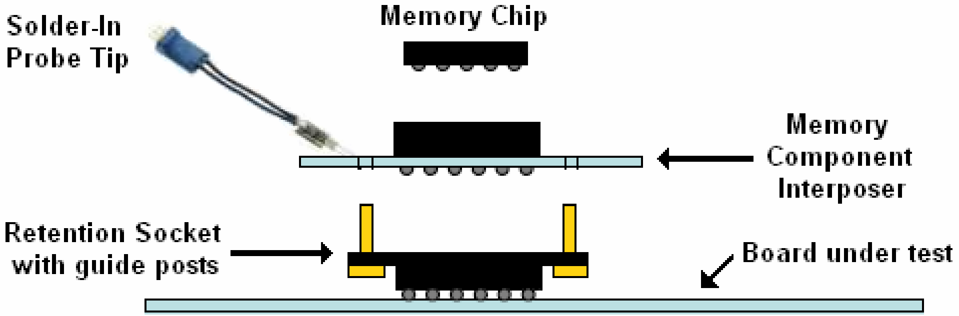


BGA Chip Interposer

BGA Chip Access For DDR2, DDR3

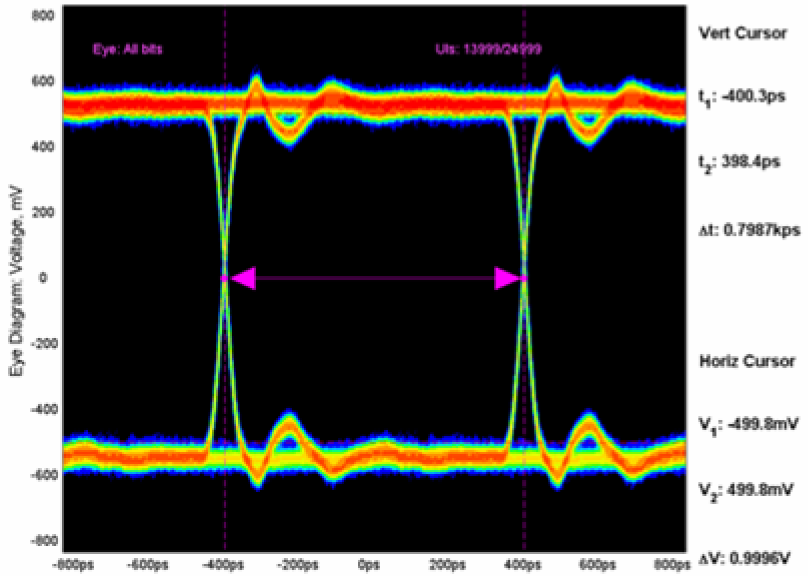
- Unique, reusable socket design allows for multiple chip exchanges
- Able to use both analog and digital probes
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models (See MSR for details)



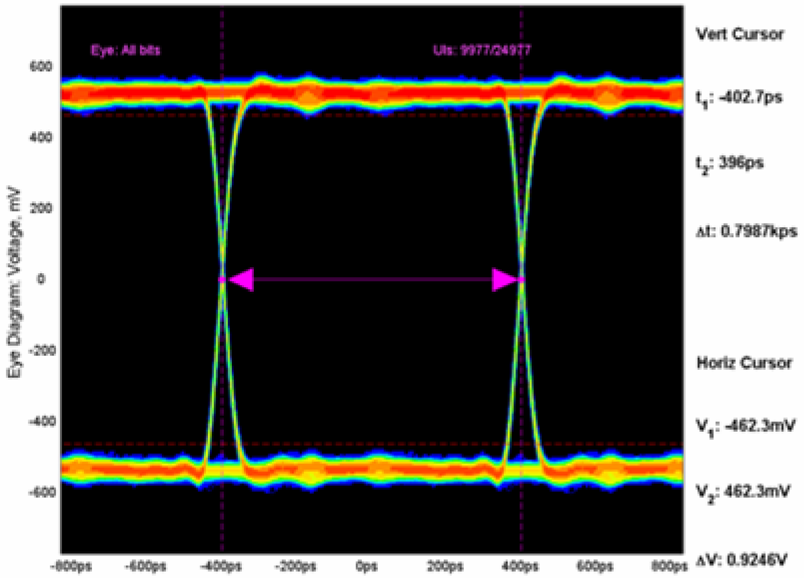


BGA Chip Interposer – Signal Fidelity

- Filters are available to de-embed analog effects
  - Library of filters is provided with the interposer
  - Filters were developed based on the actual S-parameters of the interposer + probe tip
  - Available for DPO/DSA/MSO70000 and DPO7000 scopes



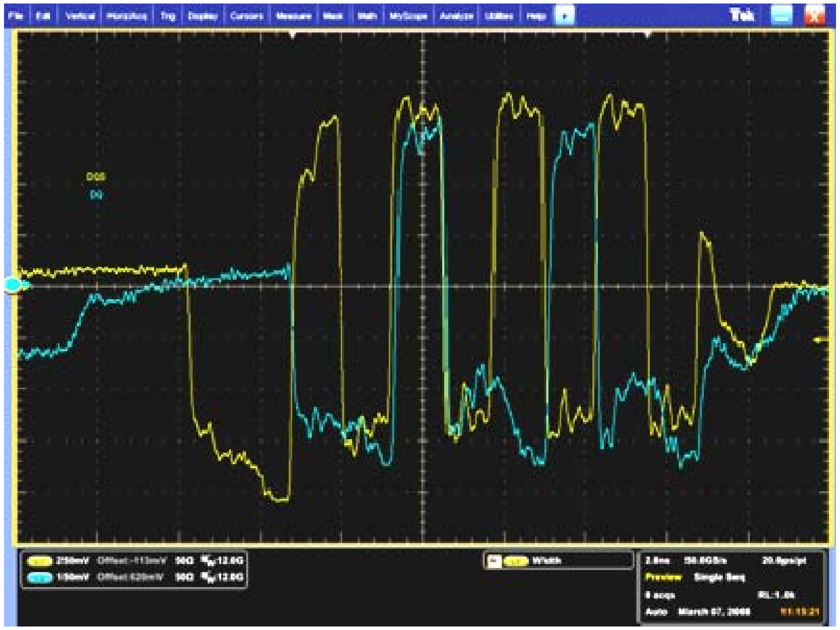
Eye - unfiltered



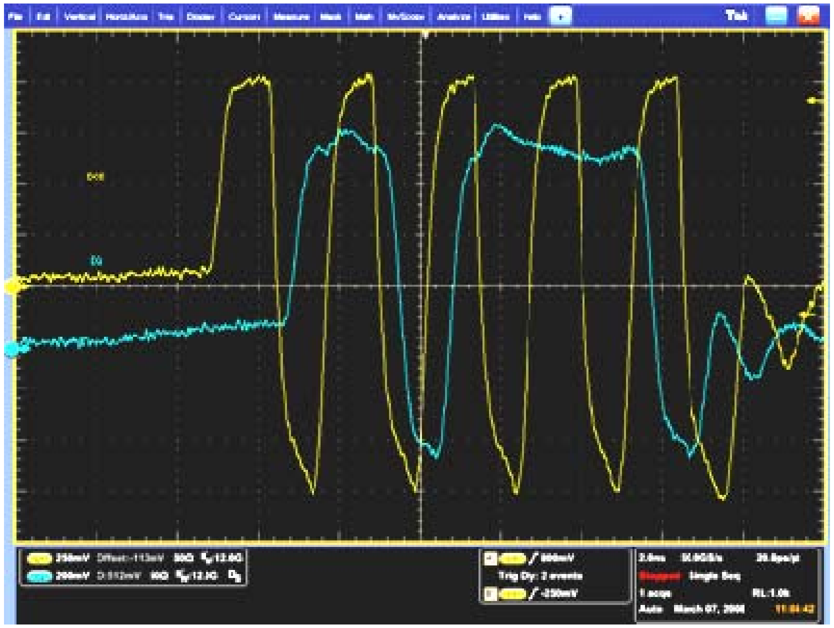
Eye – with filter

Challenge 2: Burst Identification

- Locate the right kind of bursts (read vs write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc)



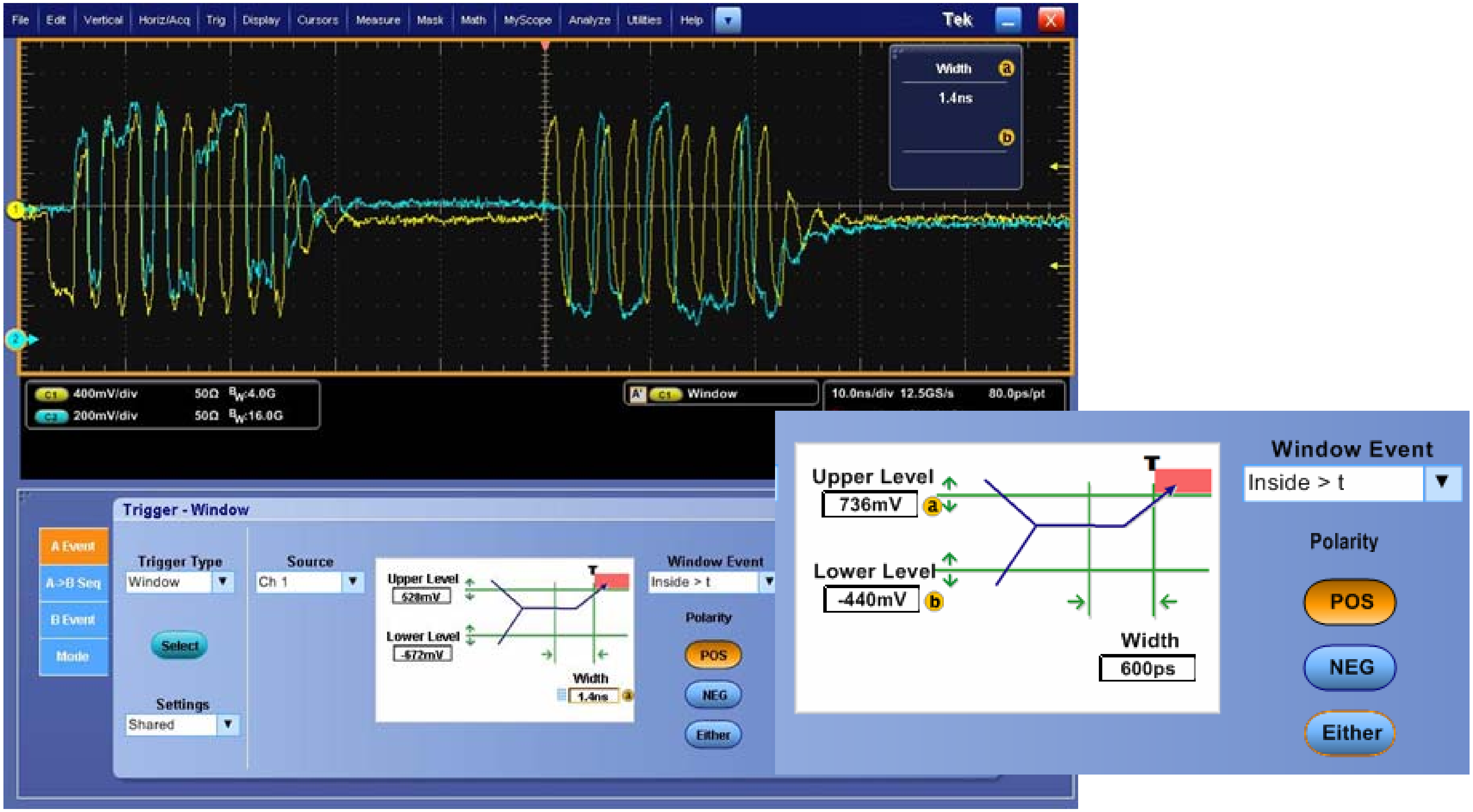
DDR3 Read Burst



DDR3 Write Burst

HW Triggering on DDR Reads / Writes

- Window Trigger - useful for real-time DDR read /write isolation
  - DQS goes high for writes, low for reads (DDR3)



Width ⓐ 1.4ns ⓑ

C1 400mV/div 50Ω B_W:4.0G
C2 200mV/div 50Ω B_W:16.0G

A' C1 Window

10.0ns/div 12.5GS/s 80.0ps/pt

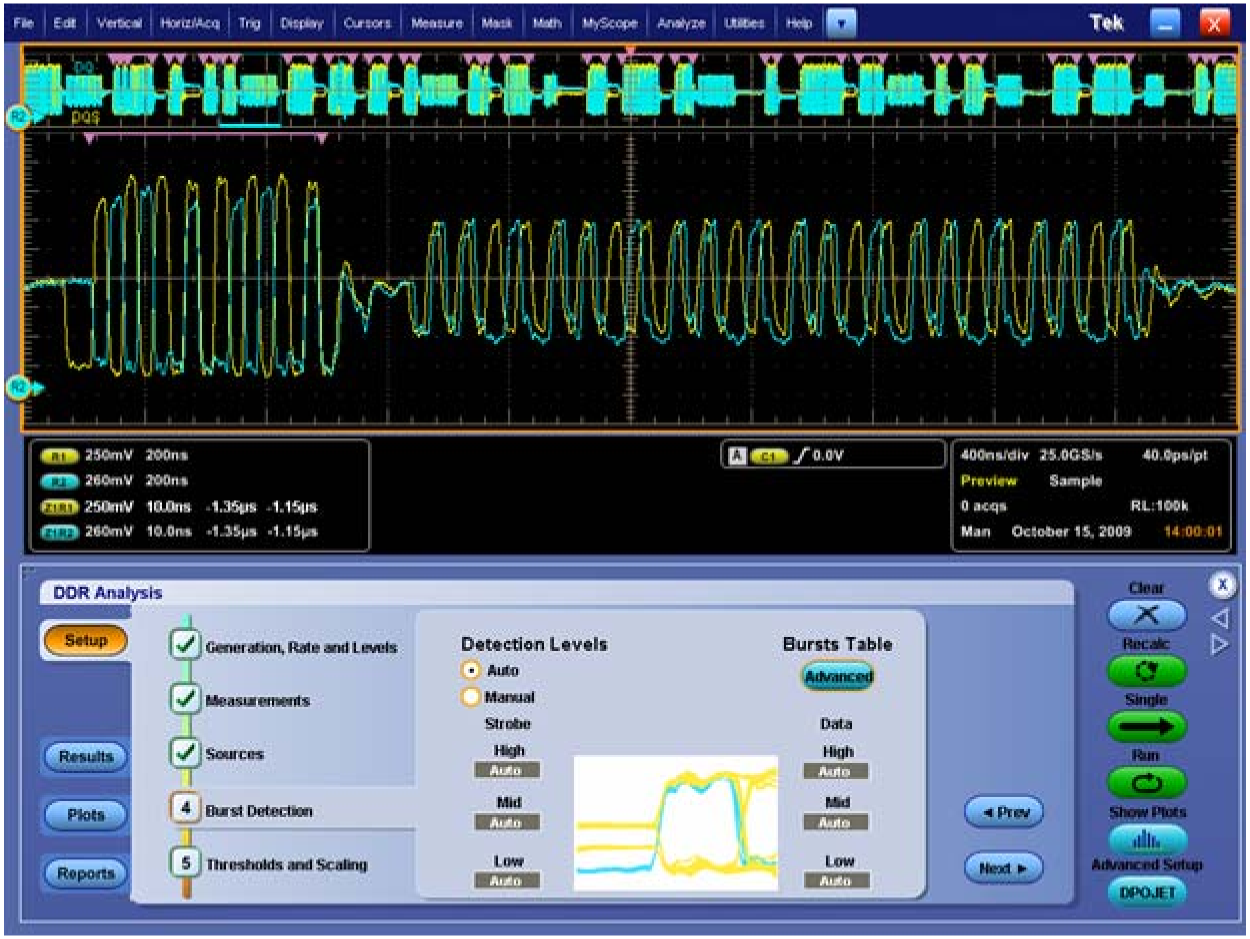
Trigger - Window

Trigger Type: Window
Source: Ch 1
Upper Level: 528mV
Lower Level: -672mV
Width: 1.4ns
Window Event: Inside > t
Polarity
Settings: Shared

Upper Level: 736mV ⓐ
Lower Level: -440mV ⓑ
Width: 600ps
Window Event: Inside > t
Polarity

Advanced Search & Mark (ASM) and Long Records

- Easily identify & measure all Read / Write bursts in the acquisition
  - Based on the Advanced Search & Mark feature
  - Scroll through marked reads / writes across the entire waveform record



R1 250mV 200ns
R2 260mV 200ns
Z1R1 250mV 10.0ns -1.35μs -1.15μs
Z1R2 260mV 10.0ns -1.35μs -1.15μs

A C1 ⨍ 0.0V

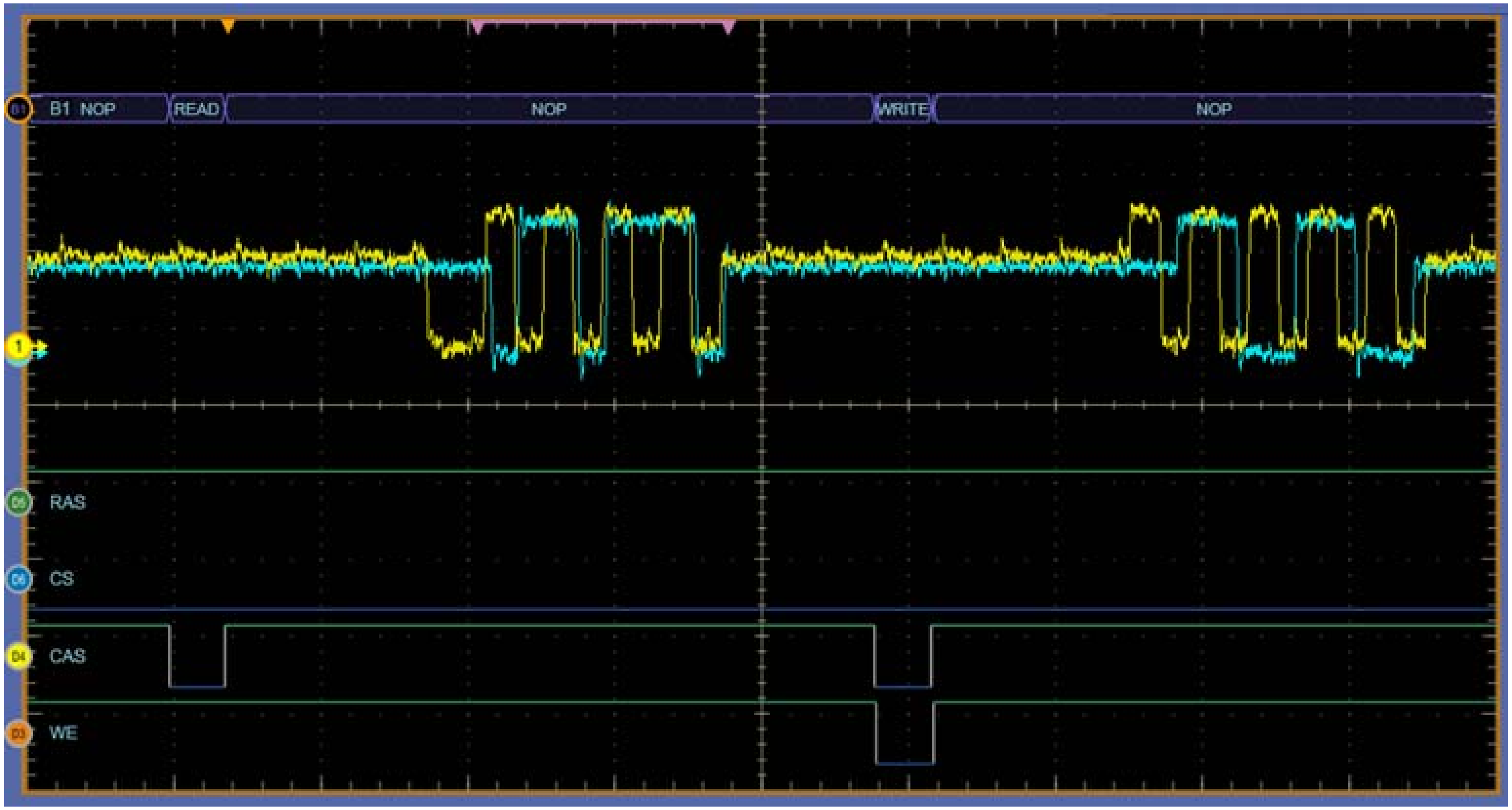
400ns/div 25.0GS/s 40.0ps/pt
Preview Sample
0 acqs RL:100k
Man October 15, 2009 14:00:01

Detection Levels
● Auto
○ Manual

Strobe	Data
High Auto	High Auto
Mid Auto	Mid Auto
Low Auto	Low Auto

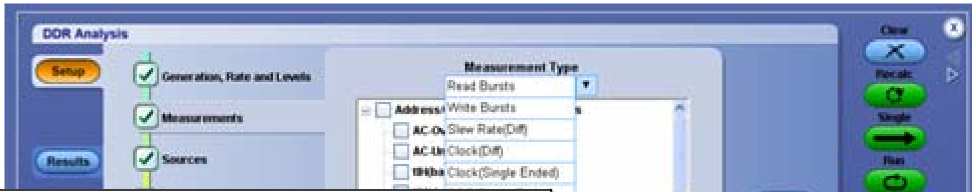
Burst Identification on an MSO

- Using bus state, specific transactions can be isolated
  - For example, locate only Reads from a specific memory rank
  - Advanced Search & Mark is used for fine burst positioning



Challenge 3: Measurement Setup

- JEDEC Standards specify measurements & methods



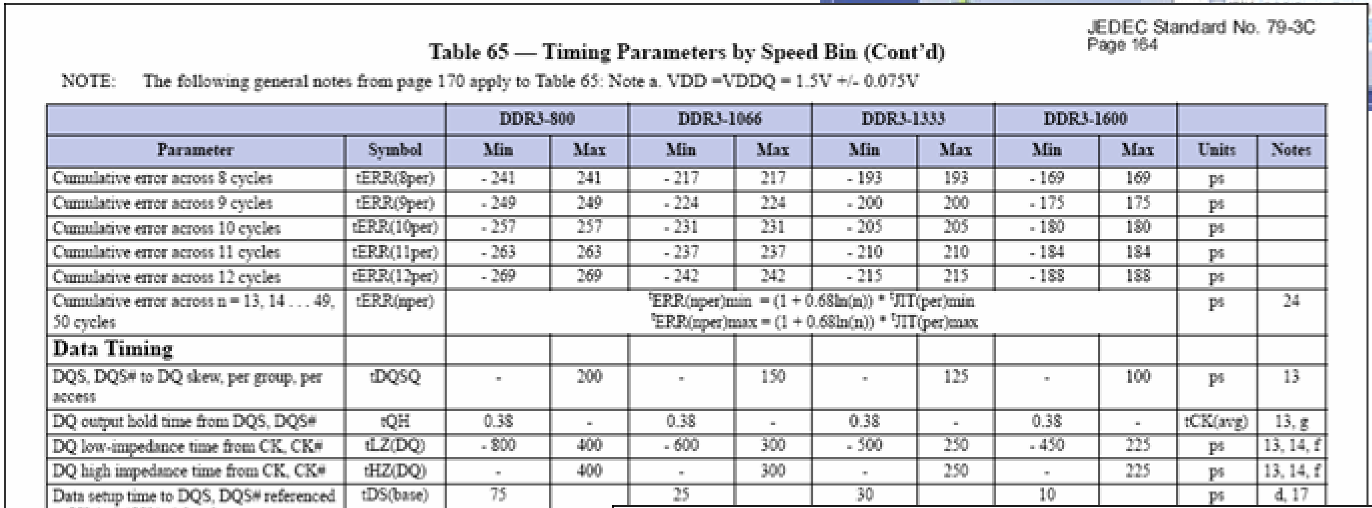


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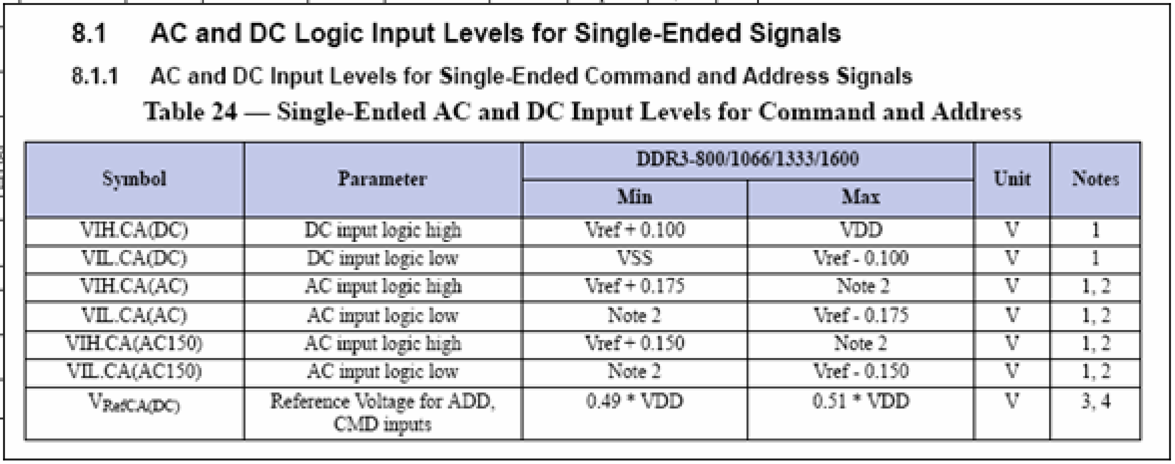
Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	- 169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	- 175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	- 180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	- 184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	- 188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$^{t}ERR(nper)min = (1 + 0.68ln(n)) * {}^{t}JIT(per)min$ $^{t}ERR(nper)max = (1 + 0.68ln(n)) * {}^{t}JIT(per)max$								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK#	tLZ(DQ)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75		25		30		10		ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150									
DQ and DM Input pulse width for each input	tDIPW	600	-								
Data Strobe Timing											
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 1								
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 1								
DQS, DQS# differential output high time	tQSH	0.38	-								
DQS, DQS# differential output low time	tQSL	0.38	-								
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-								
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-								
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	- 400	400								



8.1 AC and DC Logic Input Levels for Single-Ended Signals

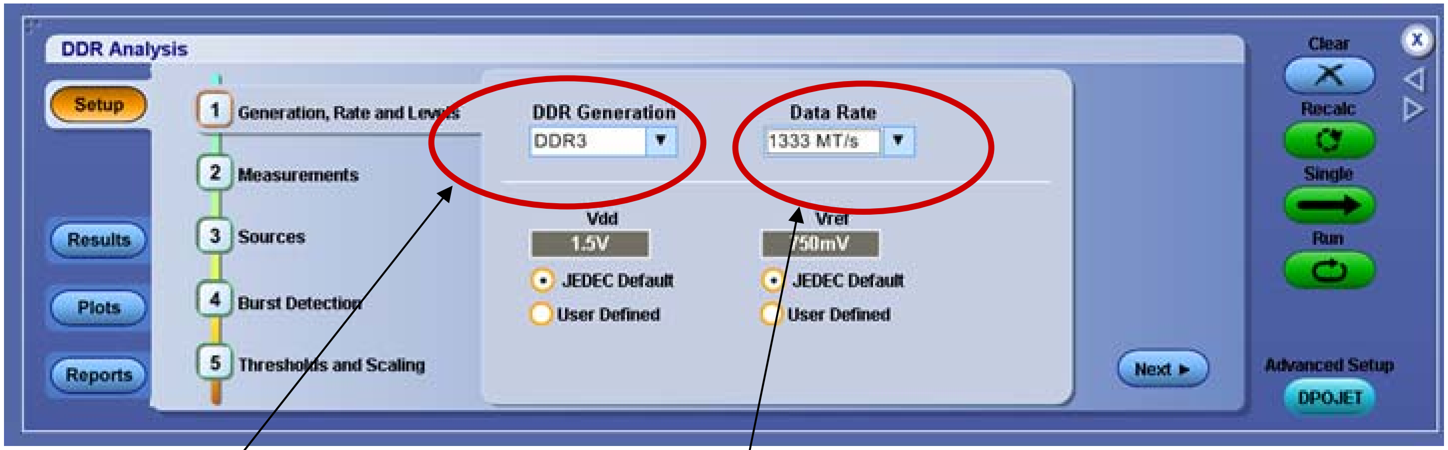
8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 24 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Notes
		Min	Max		
VIH.CA(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC input logic high	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC input logic low	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Ease of Use - DDRA Wizard

Step #1



DDR Generation: DDR3 ▼

Data Rate: 1333 MT/s ▼

Vdd: 1.5V

● JEDEC Default

○ User Defined

Vref: 750mV

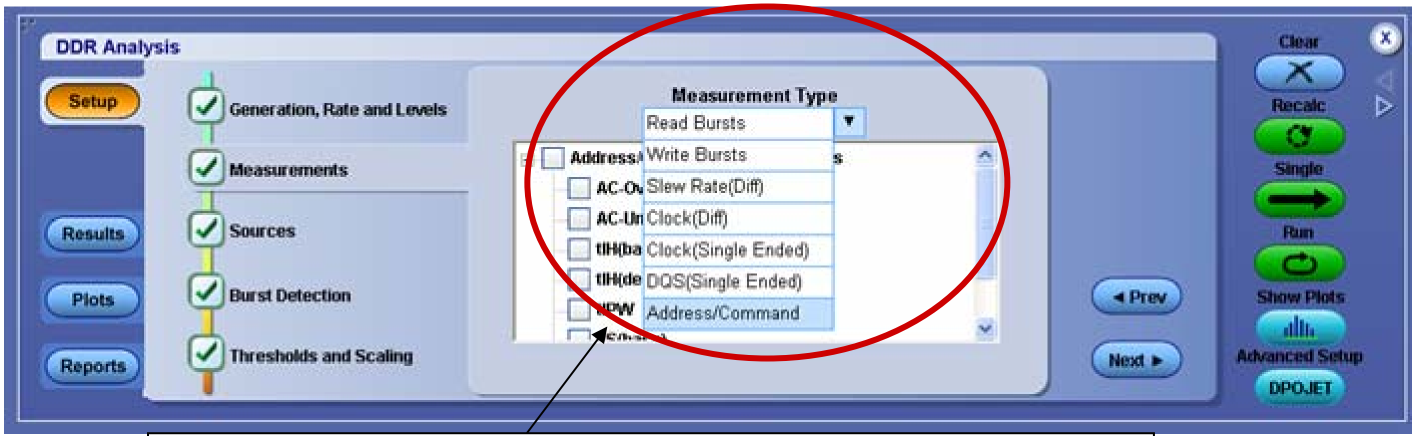
● JEDEC Default

○ User Defined

Select DDR Generation

Select DDR Rate

Step #2



Measurement Type: Read Bursts ▼

- Write Bursts
- Slew Rate(Diff)
- Clock(Diff)
- Clock(Single Ended)
- DQS(Single Ended)
- Address/Command

Choose measurements (Read / Write / CLK / Addr & Command)

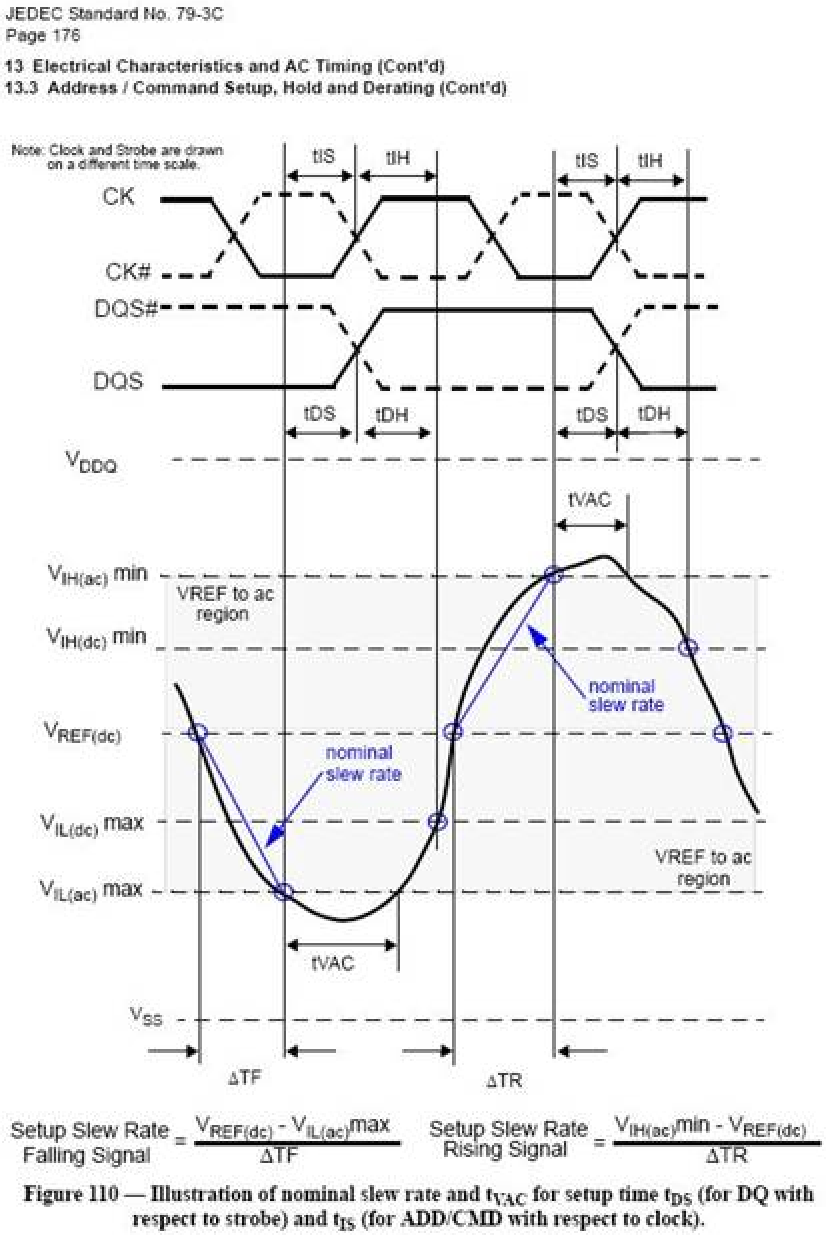
Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, LP-DDR

- Example measurements list for DDR2 :
  - tCK(avg)
  - tCK(abs)
  - tCH(avg)
  - tCH(abs)
  - tCL(avg)
  - tCL(abs)
  - tHP
  - tJIT(duty)
  - tJIT(per)
  - tJIT(cc)
  - tERR(02)
  - tERR(03)
  - tERR(04)
  - tERR(05)
  - tERR(6 - 10 per)
  - tERR(11 - 50 per)
  - tDQSH
  - tDS - diff (base)
  - tDS - SE (base)
  - tDS -diff - DERATED
  - tDS -SE - DERATED
  - tDH - diff (base)
  - tDH - SE (base)
  - tDH -diff - DERATED
  - tDH -SE - DERATED
  - tDIPW
  - tAC - diff
  - tDQSCK -diff
  - tDQSCK - SE
  - tDQSQ - diff
  - tDQSQ - SE
  - tQH
  - tDQSS
  - tDSS
  - tDSH
  - tIPW
  - tIS (base)
  - tIH (base)
  - tIS - DERATED
  - tIH - DERATED
  - Vid - diff (AC)
  - Vix (AC) - DQS
  - Vix (AC) - CLK
  - Vox (AC) - DQS
  - Vox (AC) - CLK
  - Input Slew-Rise (DQS),
  - Input Slew-Fall (DQS),
  - Input Slew-Rise (CLK),
  - Input Slew-Fall (CLK),
  - AC - Overshoot Amplitude - diff
  - AC -Undershoot Amplitude - diff
  - AC - Overshoot Amplitude - SE
  - AC - Undershoot Amplitude - SE
  - Data Eye Width

Measurement De-rating

- JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*
- Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.
  - tDS - diff (base)
  - tDS -diff - DERATED
  - tDS - SE (base)
  - tDS -SE - DERATED
  - tDH - diff (base)
  - tDH -diff - DERATED
  - tDH - SE (base)
  - tDH -SE - DERATED
  - tIS (base)
  - tIS - DERATED
  - tIH (base)
  - tIH - DERATED



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13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

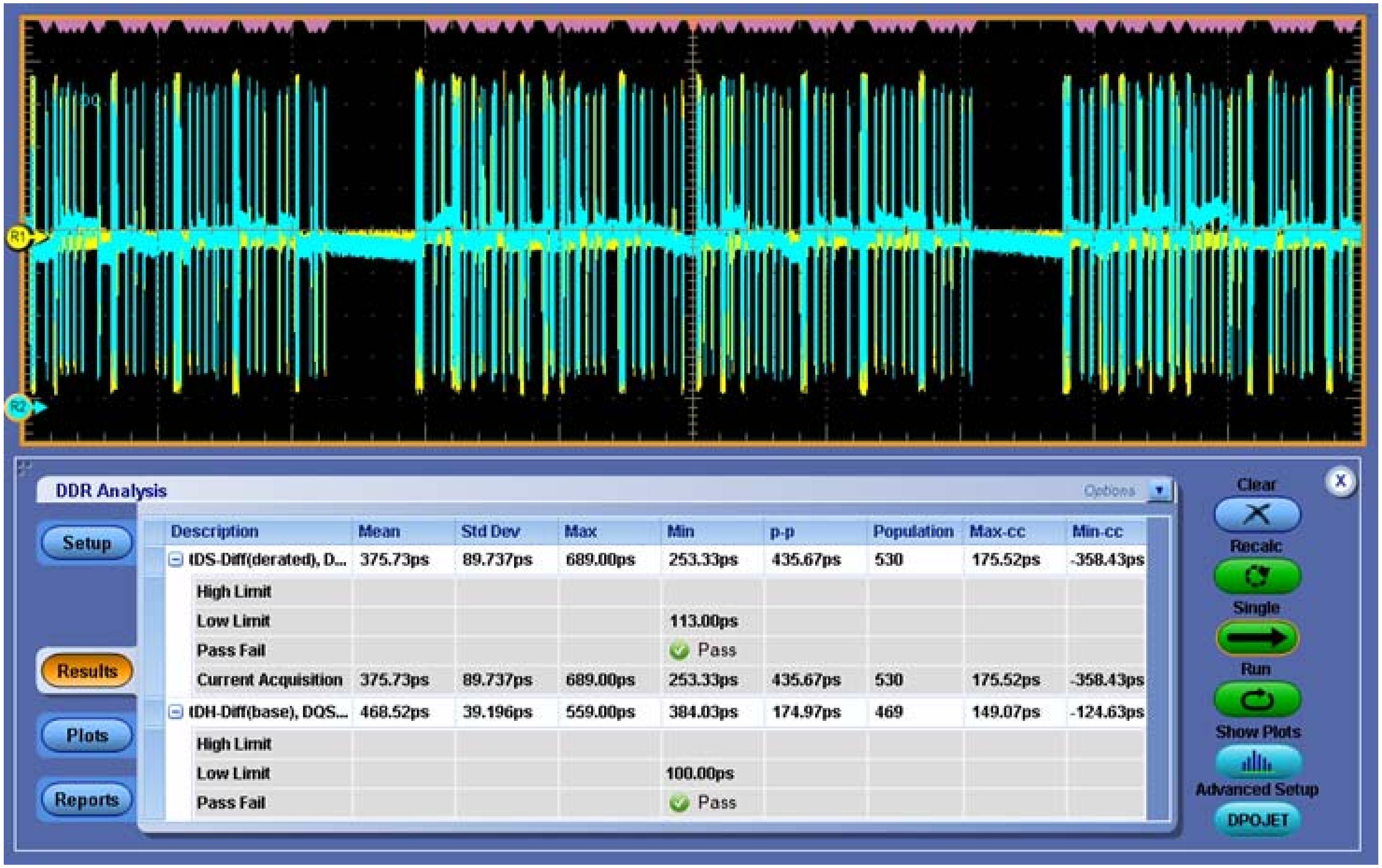
$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 110 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

* JESD79-2E, JESD79-3C specifications

Challenge 4: Results and Statistical Validity

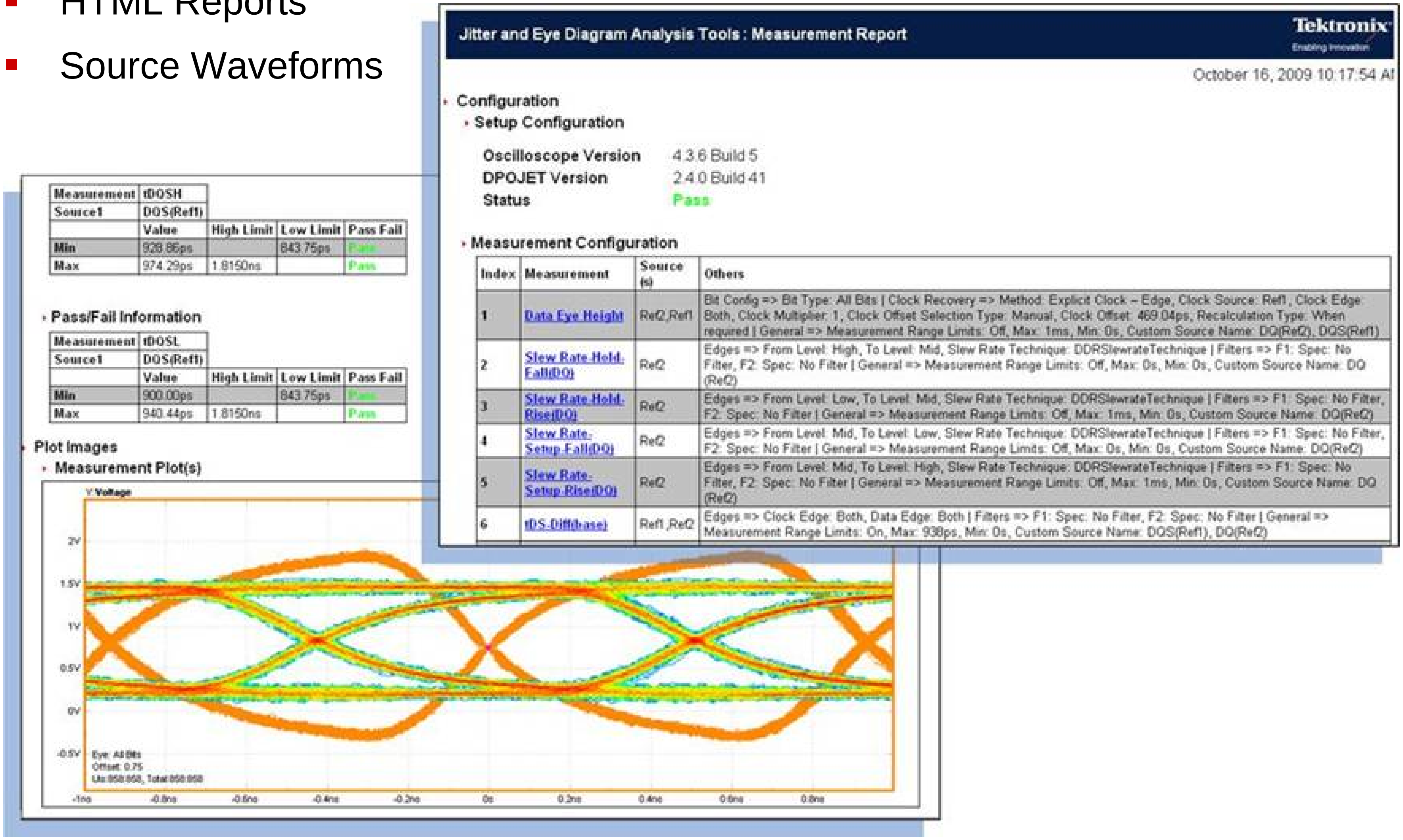
- To have confidence in your test results, you need 100’s, 1000’s or even more observations of each measurement
- As a practical matter, measurement throughput is essential



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
⊟ tDS-Diff(derated), D...	375.73ps	89.737ps	689.00ps	253.33ps	435.67ps	530	175.52ps	-358.43ps
High Limit								
Low Limit				113.00ps				
Pass Fail				✓ Pass				
Current Acquisition	375.73ps	89.737ps	689.00ps	253.33ps	435.67ps	530	175.52ps	-358.43ps
⊟ tDH-Diff(base), DQS...	468.52ps	39.196ps	559.00ps	384.03ps	174.97ps	469	149.07ps	-124.63ps
High Limit								
Low Limit				100.00ps				
Pass Fail				✓ Pass				

Challenge 5: Reporting and Archiving

- HTML Reports
- Source Waveforms



Jitter and Eye Diagram Analysis Tools : Measurement Report

Tektronix
Enabling Innovation

October 16, 2009 10:17:54 AM

- Configuration
  - Setup Configuration

Oscilloscope Version	4.3.6 Build 5
DPOJET Version	2.4.0 Build 41
Status	Pass

- Measurement Configuration

Index	Measurement	Source (s)	Others
1	Data Eye Height	Ref2,Ref1	Bit Config => Bit Type: All Bits | Clock Recovery => Method: Explicit Clock – Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 469.04ps, Recalculation Type: When required | General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(Ref2), DQS(Ref1)
2	Slew Rate Hold-Fall(DQ)	Ref2	Edges => From Level: High, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ (Ref2)
3	Slew Rate Hold-Rise(DQ)	Ref2	Edges => From Level: Low, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(Ref2)
4	Slew Rate-Setup-Fall(DQ)	Ref2	Edges => From Level: Mid, To Level: Low, Slew Rate Technique: DDRSlewrateTechnique | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(Ref2)
5	Slew Rate-Setup-Rise(DQ)	Ref2	Edges => From Level: Mid, To Level: High, Slew Rate Technique: DDRSlewrateTechnique | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ (Ref2)
6	tDS-Diff(base)	Ref1,Ref2	Edges => Clock Edge: Both, Data Edge: Both | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: On, Max: 938ps, Min: 0s, Custom Source Name: DQS(Ref1), DQ(Ref2)

Measurement	tDQSH			
Source1	DQS(Ref1)			
	Value	High Limit	Low Limit	Pass Fail
Min	928.86ps		843.75ps	Pass
Max	974.29ps	1.8150ns		Pass

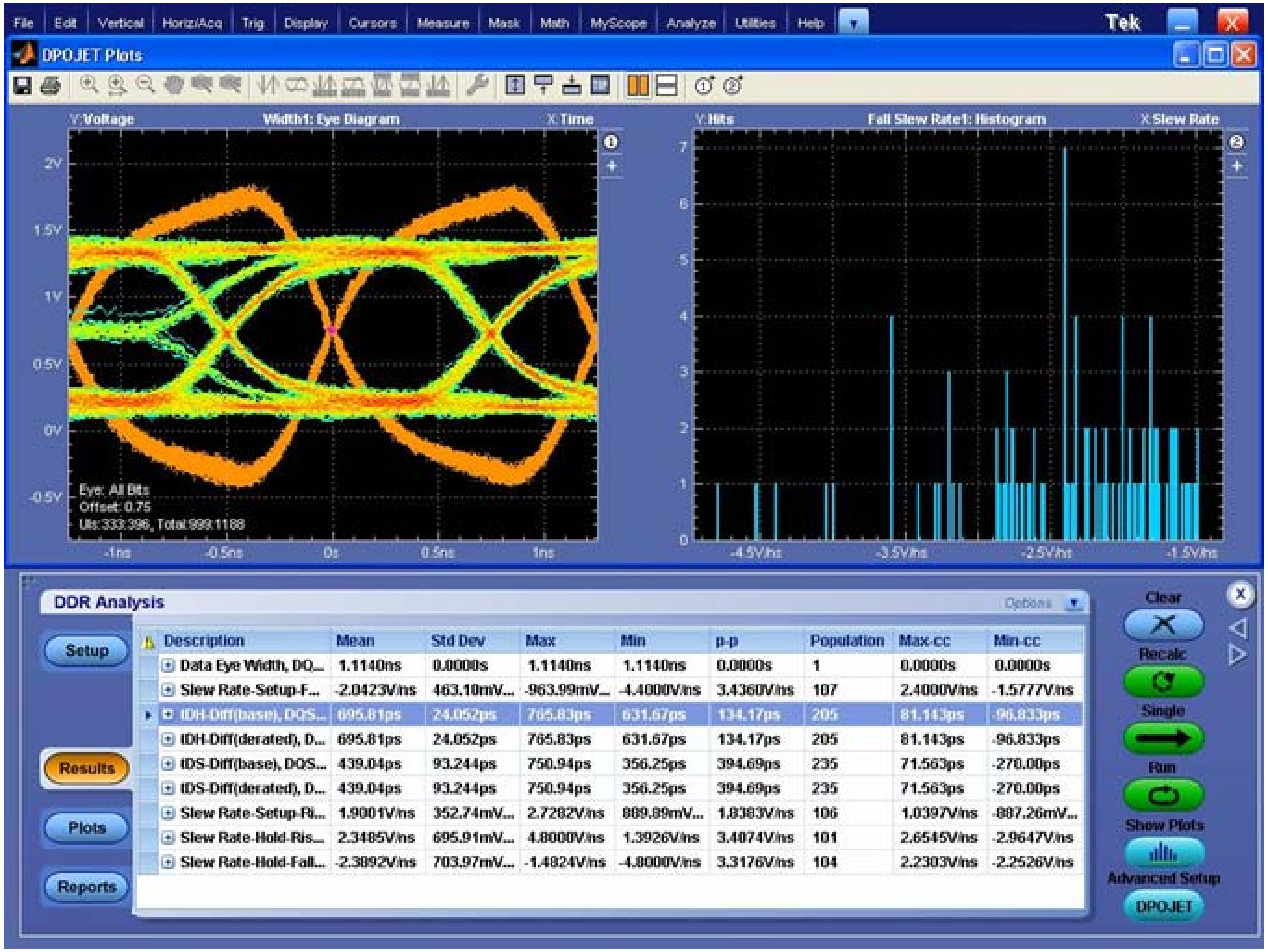
- Pass/Fail Information

Measurement	tDQSL			
Source1	DQS(Ref1)			
	Value	High Limit	Low Limit	Pass Fail
Min	900.00ps		843.75ps	Pass
Max	940.44ps	1.8150ns		Pass

- Plot Images
  - Measurement Plot(s)

Challenge 6: Advanced Analysis and Debug

- DDRA has access to all plotting & debug tools in DPOJET

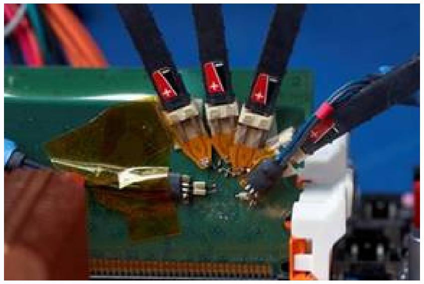


Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Data Eye Width, DQ...	1.1140ns	0.0000s	1.1140ns	1.1140ns	0.0000s	1	0.0000s	0.0000s
Slew Rate-Setup-F...	-2.0423V/ns	463.10mV...	-963.99mV...	-4.4000V/ns	3.4360V/ns	107	2.4000V/ns	-1.5777V/ns
tDH-Diff(base), DQS...	695.81ps	24.052ps	765.83ps	631.67ps	134.17ps	205	81.143ps	-96.833ps
tDH-Diff(derated), D...	695.81ps	24.052ps	765.83ps	631.67ps	134.17ps	205	81.143ps	-96.833ps
tDS-Diff(base), DQS...	439.04ps	93.244ps	750.94ps	356.25ps	394.69ps	235	71.563ps	-270.00ps
tDS-Diff(derated), D...	439.04ps	93.244ps	750.94ps	356.25ps	394.69ps	235	71.563ps	-270.00ps
Slew Rate-Setup-Ri...	1.9001V/ns	352.74mV...	2.7282V/ns	889.89mV...	1.8383V/ns	106	1.0397V/ns	-887.26mV...
Slew Rate-Hold-Ris...	2.3485V/ns	695.91mV...	4.8000V/ns	1.3926V/ns	3.4074V/ns	101	2.6545V/ns	-2.9647V/ns
Slew Rate-Hold-Fall...	-2.3892V/ns	703.97mV...	-1.4824V/ns	-4.8000V/ns	3.3176V/ns	104	2.2303V/ns	-2.2526V/ns

DDR Analog Validation & Debug – Tektronix Solutions

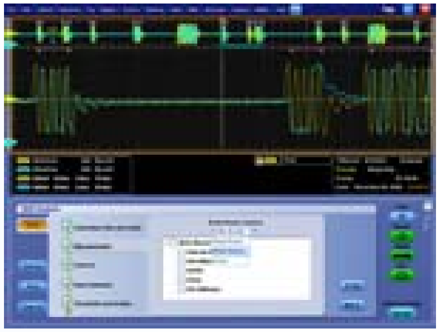
Signal Access - Probing

- P7500 TriMode Probing
  - Single probe for diff, CM and single-ended measurements
  - Up to 20 GHz bandwidth to the probe tip
- P6780 Logic Probe
  - 16 channel Active Differential probe with 2.5 GHz bandwidth
- Socketed BGA interposers for multiple exchanges



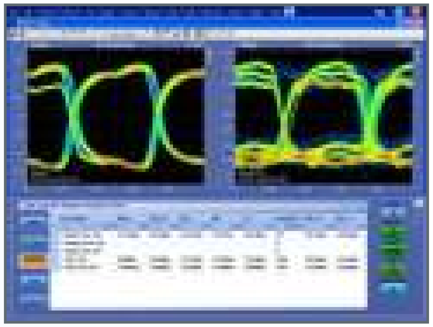
Signal Acquisition

- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Command Bus triggering with user-defined decode files
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis
  - Time trend view for analysis of low frequency effects



Signal Analysis

- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator



Resources

- Tektronix Knowledge Center: www.tektronix.com/memory
- DDR Application Note: www.tektronix.com/ddr