DDR Verification Approaches
DDR Test Challenges

- Signal Access & Probing
  - Easy-to-use / reliable connections
  - Bandwidth & Signal Integrity
  - Affordable

- Isolation of Read/Write bursts
  - Triggering or Post-Processing (ASM)

- Complexity of JEDEC Conformance Tests
  - Vref / Vih / Vil
  - Derating

- Results Validity / Statistics

- Effective Reporting / Archiving

- Advanced Analysis
  - Characterization
  - Debug
Challenge 1: Probing DDR Memory

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB
- All DDR2 & DDR3 Components use BGA Packages
- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device
- Signal Access Solutions
  - Component Interposers
  - Direct Probing
  - Analog Probing
    - DQ, DQS, Clock
  - Digital Probing
    - Address
    - Command
    - Power, Reset, and Reference

*Courtesy Micron Technologies*
Analog Solder-In Probing Solutions for DDR
Nexus DDR3 BGA Chip Interposers For Oscilloscopes

Retention Socket

BGA Chip Interposer
BGA Chip Access For DDR2, DDR3

- Unique, reusable socket design allows for multiple chip exchanges
- Able to use both analog and digital probes
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models
    (See MSR for details)
Filters are available to de-embed analog effects
- Library of filters is provided with the interposer
- Filters were developed based on the actual S-parameters of the interposer + probe tip
- Available for DPO/DSA/MSO70000 and DPO7000 scopes
Challenge 2: Burst Identification

- Locate the right kind of bursts (read vs write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc)
HW Triggering on DDR Reads / Writes

- Window Trigger - useful for real-time DDR read/write isolation
  - DQS goes high for writes, low for reads (DDR3)
Advanced Search & Mark (ASM) and Long Records

- Easily identify & measure all Read / Write bursts in the acquisition
  - Based on the Advanced Search & Mark feature
  - Scroll through marked reads / writes across the entire waveform record
Burst Identification on an MSO

- Using bus state, specific transactions can be isolated
  - For example, locate only Reads from a specific memory rank
  - Advanced Search & Mark is used for fine burst positioning
Challenge 3: Measurement Setup

- JEDEC Standards specify measurements & methods

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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>DDR3-800</th>
<th>DDR3-1066</th>
<th>DDR3-1333</th>
<th>DDR3-1600</th>
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</thead>
<tbody>
<tr>
<td>Cumulative error across 8 cycles</td>
<td>ERR(8er)</td>
<td>-241</td>
<td>241</td>
<td>-217</td>
<td>217</td>
</tr>
<tr>
<td>Cumulative error across 9 cycles</td>
<td>ERR(9er)</td>
<td>-250</td>
<td>249</td>
<td>-224</td>
<td>224</td>
</tr>
<tr>
<td>Cumulative error across 10 cycles</td>
<td>ERR(10er)</td>
<td>-307</td>
<td>367</td>
<td>-231</td>
<td>233</td>
</tr>
<tr>
<td>Cumulative error across 11 cycles</td>
<td>ERR(11er)</td>
<td>-263</td>
<td>256</td>
<td>-237</td>
<td>237</td>
</tr>
<tr>
<td>Cumulative error across 12 cycles</td>
<td>ERR(12er)</td>
<td>-269</td>
<td>259</td>
<td>-242</td>
<td>242</td>
</tr>
</tbody>
</table>

**Data Timing**

- DQS, DQS# to DQ skew, per group, per access: &DQSQ
- DQ output hold time from DQS, DQS#: &QH
- DQ low-impedance time from CK, CK#: &LZ(DQ)
- DQ high-impedance time from CK, CK#: &HZ(DQ)
- Data setup time to DQS, DQS# referenced to Vih(ck) / Vih(ck) levels: (DS(base)
- Data hold time from DQS, DQS# referenced to Vih(ck) / Vih(ck) levels: (DH(base)
- DQ and DM input pulse width for each signal: &DPW

**Data Strobe Timing**

- DQS, DQS# differential READ Preamble: &PRE
- DQS, DQS# differential READ Postamble: &RPST
- DQS, DQS# differential output high time: &QS
- DQS, DQS# differential output low time: &QSL
- DQS, DQS# differential WRITE Preamble: &WPRE
- DQS, DQS# differential WRITE Postamble: &WPST
- DQS, DQS# rising edge output access time from rising CK, CK#: &QSCK

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### 8.1 AC and DC Logic Input Levels for Single-Ended Signals

#### 8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>DDR3-800/1066/1333/1600</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH.CA(ADC)</td>
<td>DC input logic high</td>
<td>Vref + 0.100</td>
<td>VDD</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>VIL.CA(ADC)</td>
<td>DC input logic low</td>
<td>VDD</td>
<td>V</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>VIH.CA(AC)</td>
<td>AC input logic high</td>
<td>Vref + 0.175</td>
<td>Note 2</td>
<td>V</td>
<td>1,2</td>
<td></td>
</tr>
<tr>
<td>VIL.CA(AC)</td>
<td>AC input logic low</td>
<td>VDD</td>
<td>V</td>
<td>V</td>
<td>1,2</td>
<td></td>
</tr>
<tr>
<td>VIH.CA(AC150)</td>
<td>AC input logic high</td>
<td>Vref + 0.150</td>
<td>Note 2</td>
<td>V</td>
<td>1,2</td>
<td></td>
</tr>
<tr>
<td>VIL.CA(AC150)</td>
<td>AC input logic low</td>
<td>VDD</td>
<td>V</td>
<td>V</td>
<td>1,2</td>
<td></td>
</tr>
</tbody>
</table>
Ease of Use - DDRA Wizard

Step #1

Select DDR Generation

Select DDR Rate

Step #2

Choose measurements (Read / Write / CLK / Addr & Command)
Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, LP-DDR

- Example measurements list for DDR2:
  - tCK(avg)
  - tCK(abs)
  - tCH(avg)
  - tCH(abs)
  - tCL(avg)
  - tCL(abs)
  - tHP
  - tJIT(duty)
  - tJIT(per)
  - tJIT(cc)
  - tERR(02)
  - tERR(03)
  - tERR(04)
  - tERR(05)
  - tERR(6 - 10 per)
  - tERR(11 - 50 per)
  - tDQSH
  - tIPW
  - tS (base)
  - tH (base)
  - tS - DERATED
  - tH - DERATED
  - Vid - diff (AC)
  - Vix (AC) - DQS
  - Vix (AC) - CLK
  - Vox (AC) - DQS
  - Vox (AC) - CLK
  - Input Slew-Rise (DQS),
  - Input Slew-Fall (DQS),
  - Input Slew-Rise (CLK),
  - Input Slew-Fall (CLK),
  - AC - Overshoot Amplitude - diff
  - AC - Undershoot Amplitude - diff
  - AC - Overshoot Amplitude - SE
  - AC - Undershoot Amplitude - SE
  - Data Eye Width
Measurement De-rating

- JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*
- Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.

- tDS - diff (base)
- tDS -diff - DERATED
- tDS - SE (base)
- tDS -SE - DERATED
- tDH - diff (base)
- tDH -diff - DERATED
- tDH - SE (base)
- tDH -SE - DERATED
- tIS (base)
- tIS - DERATED
- tIH (base)
- tIH - DERATED
Challenge 4: Results and Statistical Validity

- To have confidence in your test results, you need 100’s, 1000’s or even more observations of each measurement
- As a practical matter, measurement throughput is essential
Challenge 5: Reporting and Archiving

- HTML Reports
- Source Waveforms
Challenge 6: Advanced Analysis and Debug

- DDRA has access to all plotting & debug tools in DPOJET
DDR Analog Validation & Debug – Tektronix Solutions

**Signal Access - Probing**
- P7500 TriMode Probing
  - Single probe for diff, CM and single-ended measurements
  - Up to 20 GHz bandwidth to the probe tip
- P6780 Logic Probe
  - 16 channel Active Differential probe with 2.5 GHz bandwidth
- Socketed BGA interposers for multiple exchanges

**Signal Acquisition**
- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Command Bus triggering with user-defined decode files
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis
  - Time trend view for analysis of low frequency effects

**Signal Analysis**
- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator
Resources

- Tektronix Knowledge Center: [www.tektronix.com/memory](http://www.tektronix.com/memory)
- DDR Application Note: [www.tektronix.com/ddr](http://www.tektronix.com/ddr)