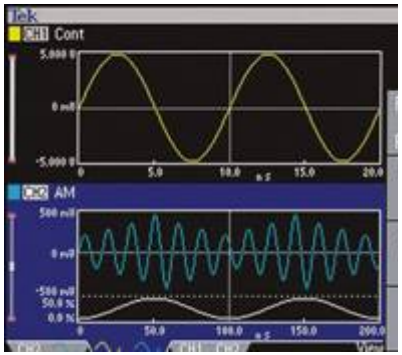
Compliance and Validation of SuperSpeed USB/PCIe Gen 3

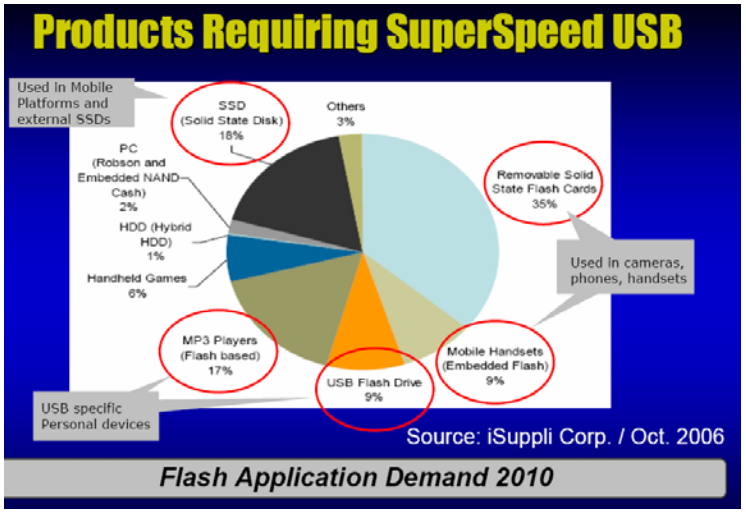


Agenda

- SuperSpeed USB
  - Technology Timeline
  - Transmitter
  - Receiver
  - Cable
  - Protocol
- PCI Express Electrical Testing
  - PCI Express Requirements
  - Solutions

Why SuperSpeed USB?

- USB 2.0 is adequate for many products…
- Emerging applications will benefit from higher performance.
- Something faster is needed for large digital multi-media files



Source: USB-IF

- **User wait time requirement is 1½ minutes to synchronize**

	Song /Pic	256 Flash	USB Flash	SD-Movie	USB Flash	HD-Movie
	4 MB	256 MB	1 GB	6 GB	16 GB	25 GB
USB 1.0	5.3 sec	5.7 min	22 min	2.2 hr	5.9 hr	9.3 hr
USB 2.0	0.1 sec	8.5 sec	33 sec	3.3 min	8.9 min	13.9 min
USB 3.0	0.01 sec	0.8 sec	3.3 sec	20 sec	53.3 sec	70 sec

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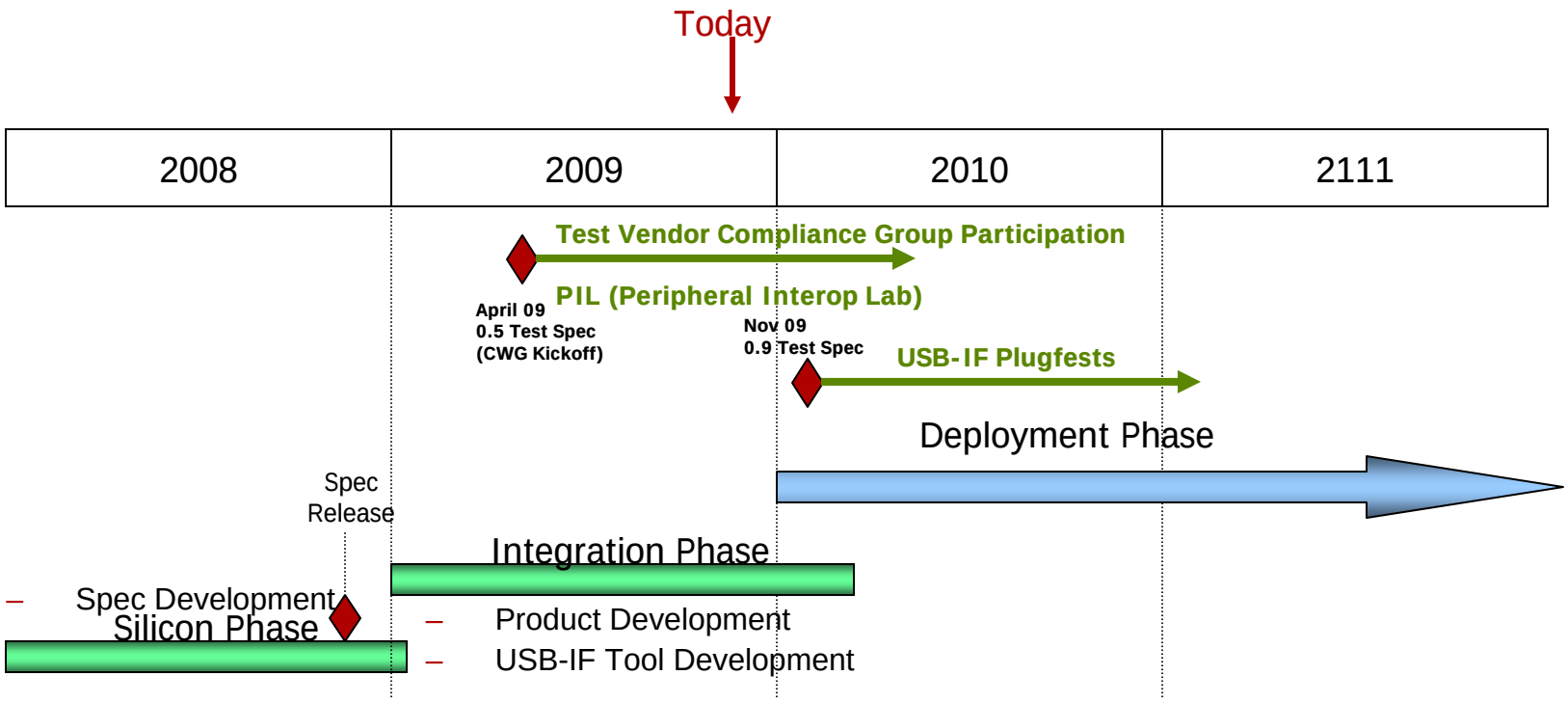
USB 3.0 Technology Timeline & Tektronix Involvement



Tektronix Test Solution Updates

- Chapter 5 - Cable
- Chapter 6 - Transmitter, Receiver, Channel
- Chapter 7 - Protocol (Partner Solution)

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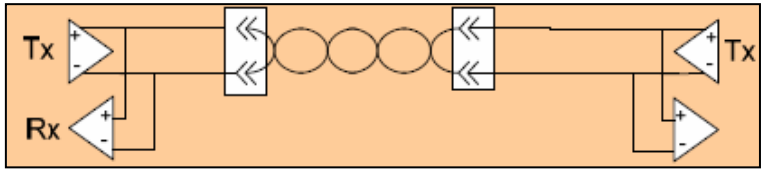
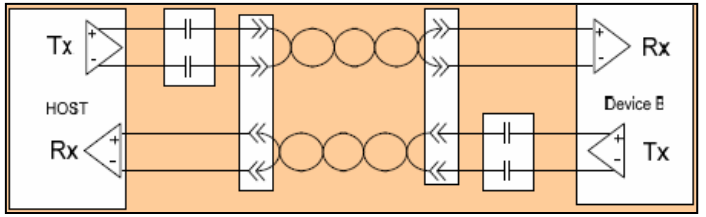
Differences from High-Speed Electricals

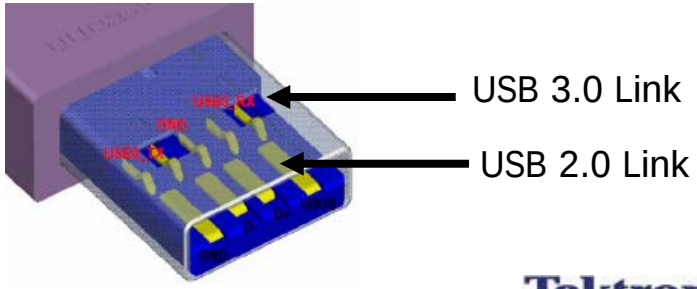
- High-Speed
  - 480MT/s
  - No-SSC
  - 2 wires for signaling
    - Tx and Rx use the same wire
    - 1 bi-directional link
  - DC coupled bus
  - NRZ encoding



- SuperSpeed
  - 5.0GT/s (10X speed increase)
  - SSC is required
  - 4 wires for signaling
    - 2 for Tx and 2 for Rx
    - Each Uni-directional
  - AC Coupled bus
  - Scrambled 8b/10b



- Backwards Compatibility
  - SuperSpeed incorporates both USB 2.0 and USB 3.0 in the same cable



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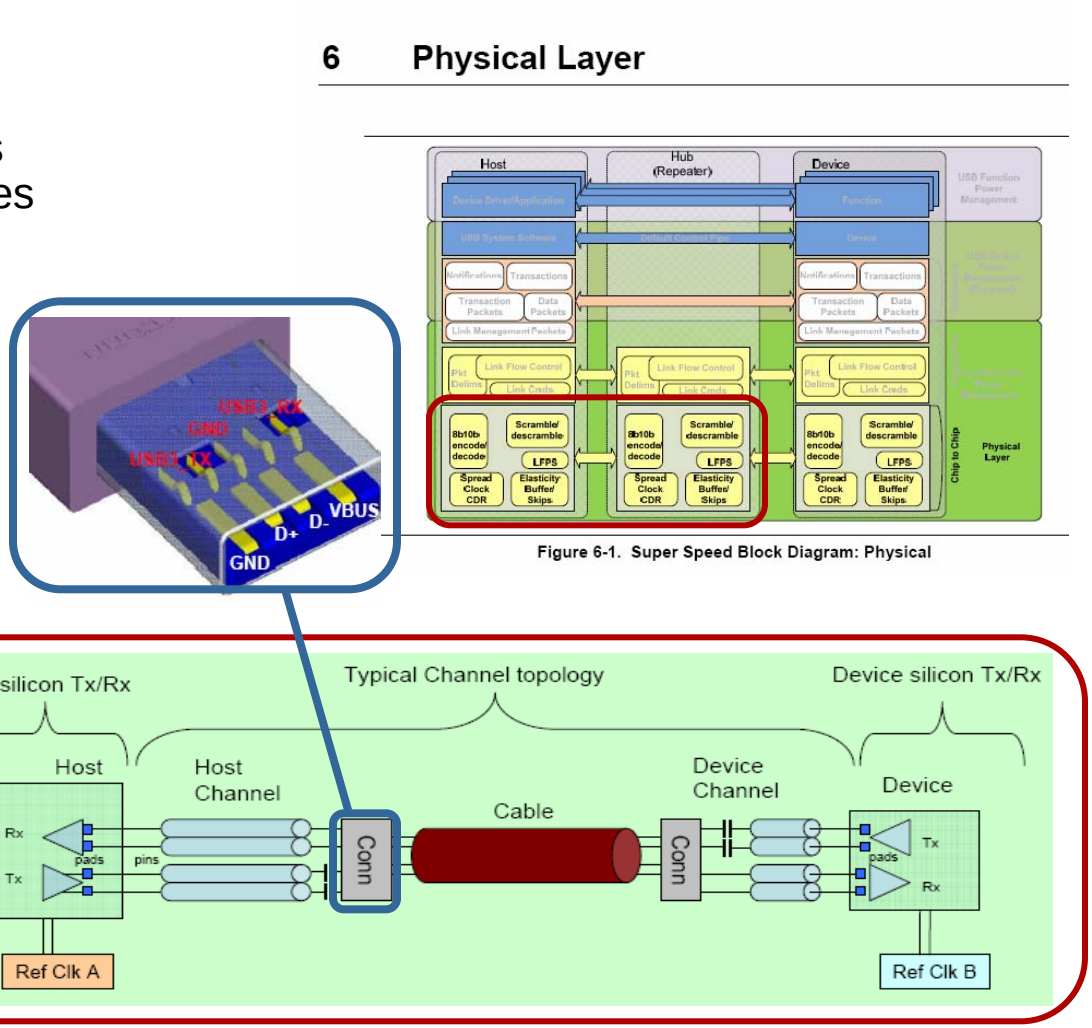
USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Test strategy
  - Cost-effective tools
  - Flexible solutions



Source: USB 3.0 Rev 1.0 Specification

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USB Channel Modeling

- Understand transmitter margin given worst case channels
- Model channel and cable combinations beyond compliance requirements
- Easily create interconnect models with SDLA software to analyze channel effects

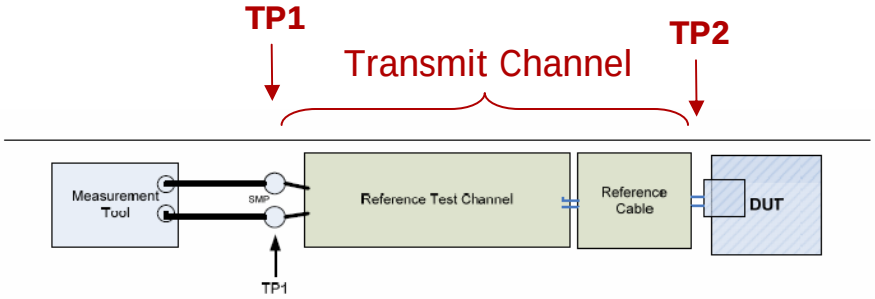
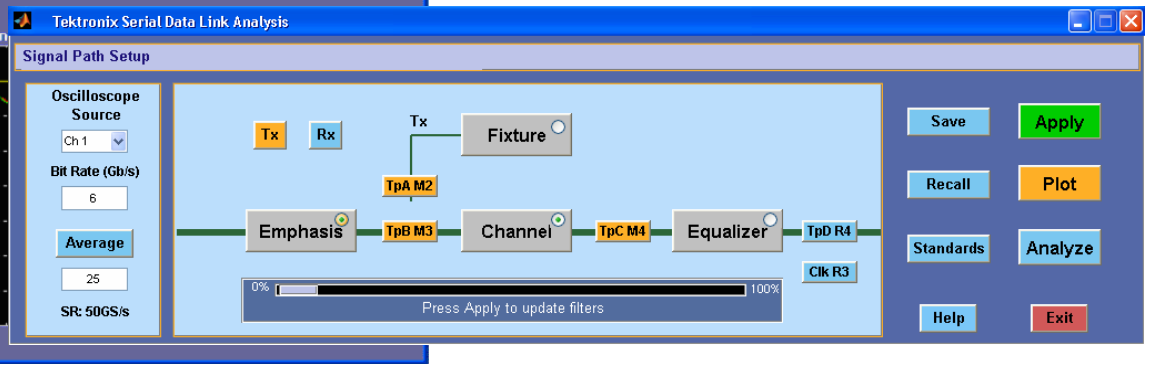


Figure 6-14. Tx Normative Setup with Reference Channel

USB-IF HW Channel Prototypes



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Custom Equalization Analysis

- Equalizer models
  - Pole, Zero, and Frequencies for Continuous Time Linear Equalizer (CTLE)
  - Feed-Forward (FFE) and Decision-Feedback (DFE) Equalizers

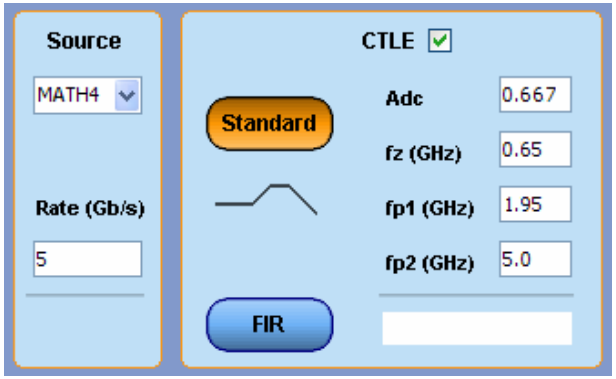
$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

$$A_{dc} = 0.667$$

$$\omega_z = 2\pi(650x10^6)$$

$$\omega_{p1} = 2\pi(1.95x10^9)$$

$$\omega_{p2} = 2\pi(5x10^9)$$



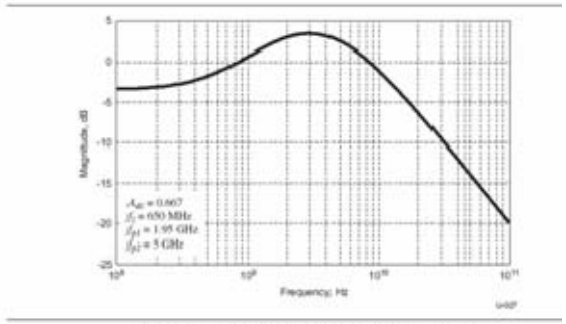
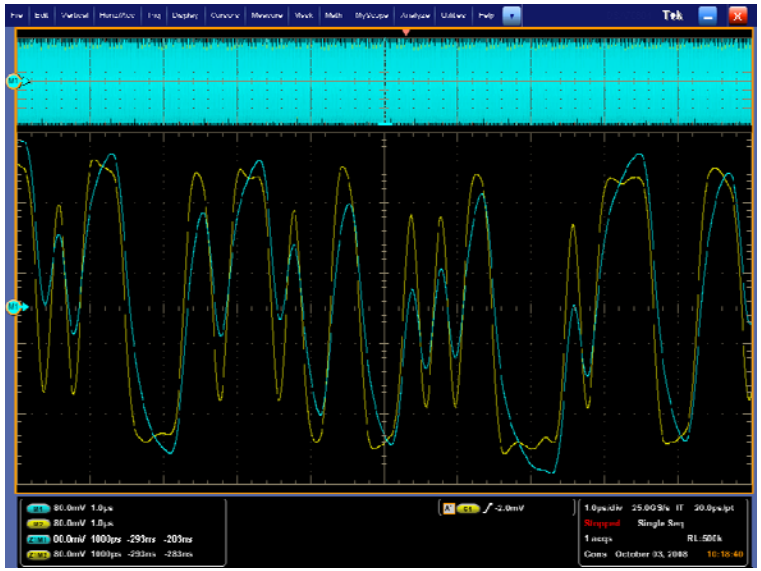
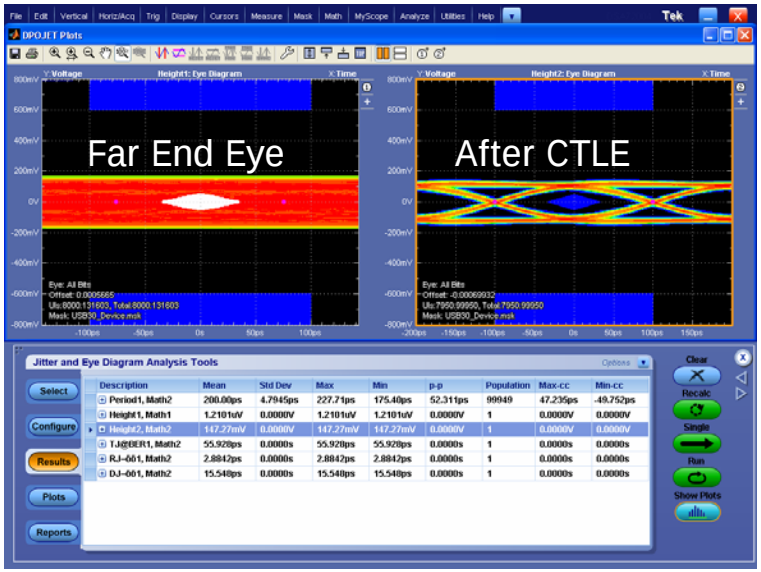


Figure 6-17. Tx Compliance Rx EQ Transfer Function





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Transmitter Compliance Testing (Normative Testing)

Channel Embedding

- Measurements at TP1
- HW Channel Probed at TP1
  - CTLE applied in SW
- SW Channel Probed at TP2
  - CTLE combined with Channel

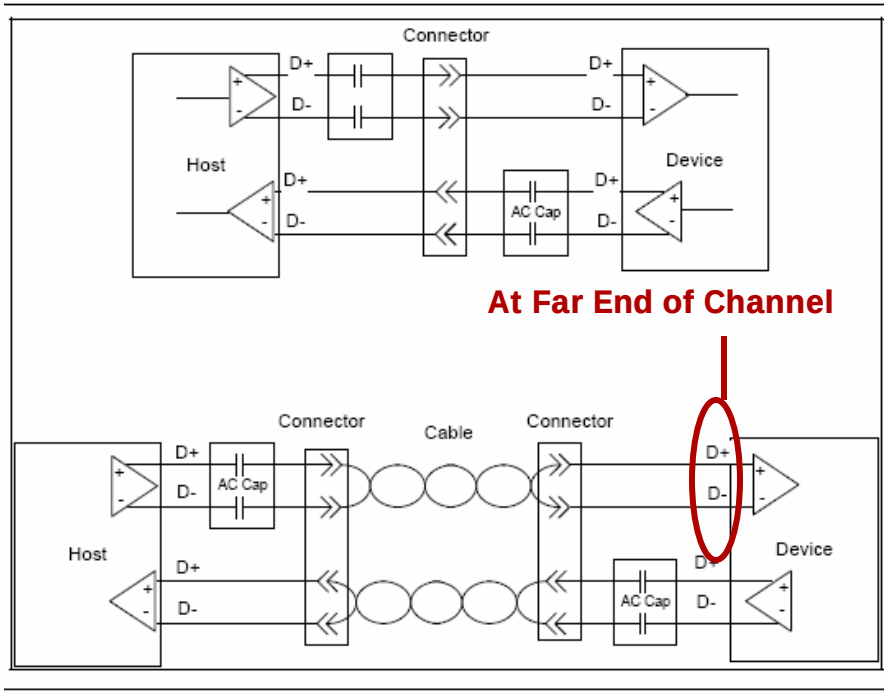


Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)

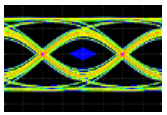
6.7.2 Transmitter Eye

The eye mask is measured using the compliance data pattern CD1 described in Section 6.4.4. Eye Height is measured from 10^{6} UI. Jitter is extrapolated from 10^{6} UI to 10^{-12}.

Table 6-12. Normative Transmitter Eye Mask

Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2
Dj			93	ps	1,2,3
Rj			60	ps	1,2,3
Tj			132	ps	1,2,3

Notes:
1. Measured over 10^{6} UI and extrapolated to 10^{-12} BER
2. Measured after receiver equalization function
3. Measured at end of reference channel and cables at TP1 figure 6-14



CTLE

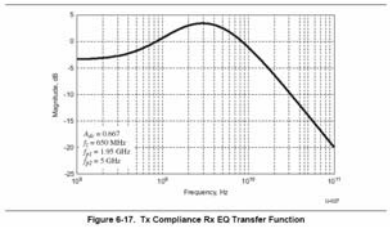


Figure 6-17. Tx Compliance Rx EQ Transfer Function

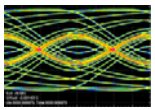


Figure 6-14. Tx Normative Setup with Reference Channel

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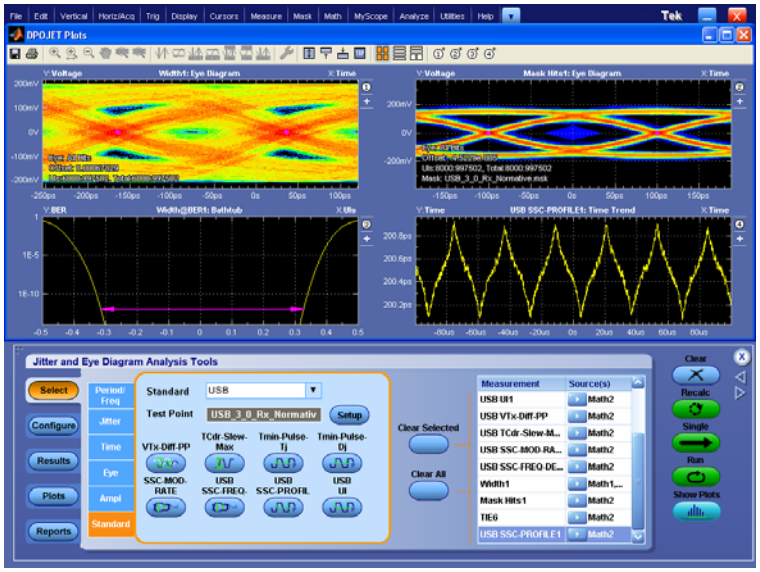
Complete USB 3.0 Transmitter Solution

DPO/DSA70000B Series Oscilloscopes

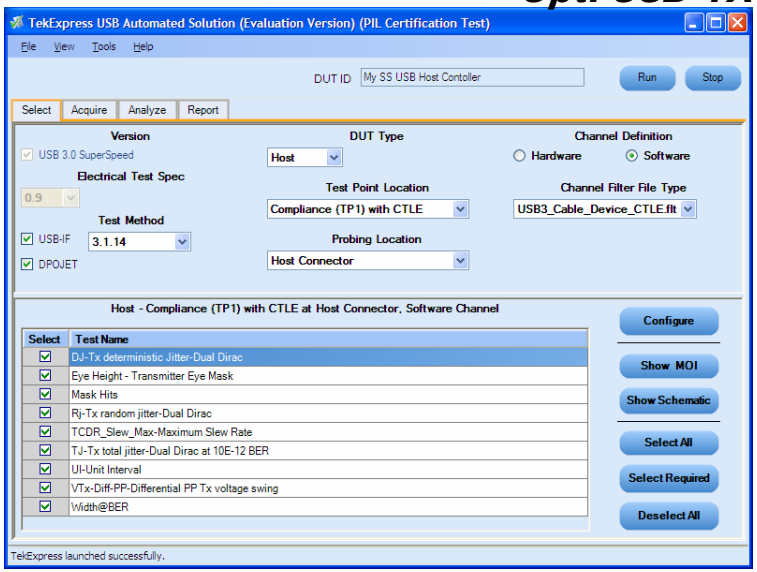
- Tektronix Super Speed USB Fixtures
- 12.5 GHz Real-Time Scope
  - 5th Harmonic Performance
  - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)
- Analysis software for validation and debug
  - Serial Data Link Analysis SW (Optional)
  - DPOJET with option USB3
- Automation software for characterization and compliance
  - TekExpress with option USB-TX

TF-USB3-AB-KIT

Opt. USB3



Opt. USB-TX



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Normative Receiver Tolerance Test

- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- De-Emphasis Level is set to -3dB
- Voltage Level is set to 0.75V
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

Frequency	SJ	RJ
500kHz	400ps	2.42ps
1MHz	200ps	2.42ps
2MHz	100ps	2.42ps
4.9MHz	40ps	2.42ps
50MHz	40ps	2.42ps

Normative Receiver Testing

- Receiver processes the BERT Ordered Sets using ‘built-in BERT’ feature
- Impairment at TP1
- HW Channel Attached at TP1
- SW Channel Attached at TP2

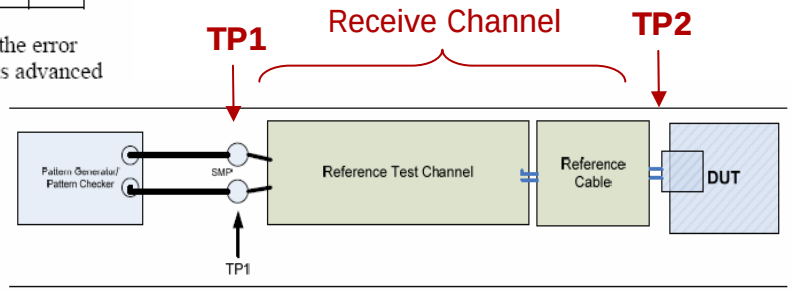
6.7.4.1 Loopback BERT

During loopback the receiver processes the BERT ordered sets BRST, BDAT, and BERC. These ordered sets are given in Table 6-14 through Table 6-17. BRST and BDAT are looped back as received. BERC ordered sets are not looped back but are replaced with BCNT ordered sets. Anytime a BRST is received the error count register EC is set to 0 and the scrambling LFSR is set to 0FFFF h. Any number of consecutive BRST ordered sets may be received.

BRST followed by BDAT starts the bit error rate test. BDAT sequence is the output of the scrambler and is equivalent to the logical idle sequence. It consists of scrambled 0 as described in Appendix B. As listed in Appendix B, the first 16 characters of the sequence are reprinted here:

FF	17	C0	14	B2	E7	02	82	72	6E	28	A6	BE	6D	BF	8D

The receiver must compare the received data to the BDAT sequence. Errors increment the error count register (EC) by 1. EC may not rollover but must be held at FFFF h. The LFSR is advanced once for every character except SKPs. The LFSR rolls over after 2^16 symbols. SKPs inserted or deleted as necessary for clock tolerance compensation.



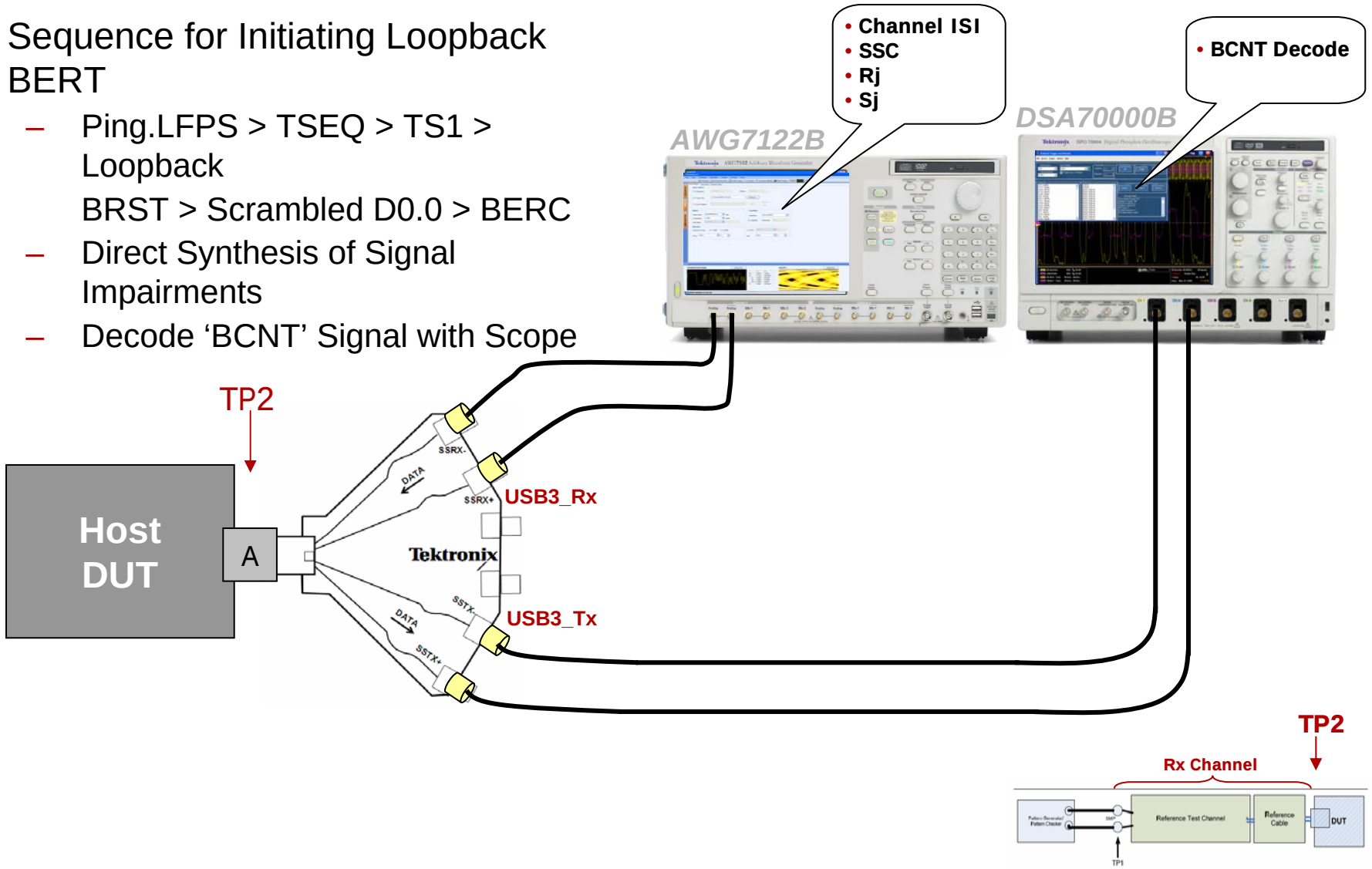
Source: USB 3.0 Specification Figure 6-18. Rx Tolerance Setup

Tektronix

Receiver Testing MOI (with SW Channel Emulation)

If DUT supports 'Loopback BERT'

- Sequence for Initiating Loopback BERT
  - Ping.LFPS > TSEQ > TS1 > Loopback
    BRST > Scrambled D0.0 > BERC
  - Direct Synthesis of Signal Impairments
  - Decode 'BCNT' Signal with Scope



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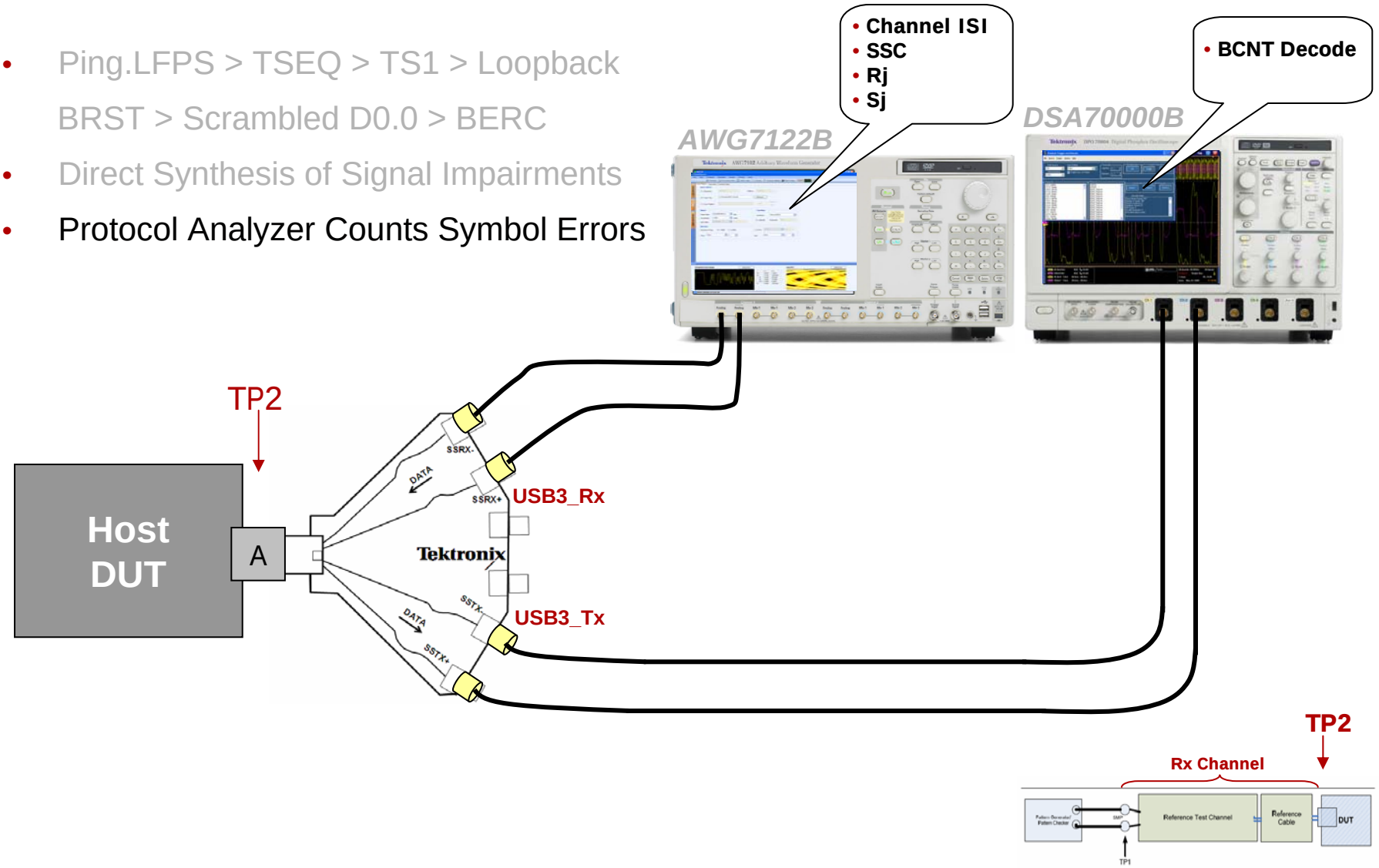
Tx and Rx MOI (with SW Channel Emulation)

If DUT does not support 'Loopback BERT'

- Ping.LFPS > TSEQ > TS1 > Loopback
  BRST > Scrambled D0.0 > BERC
- Direct Synthesis of Signal Impairments
- Protocol Analyzer Counts Symbol Errors

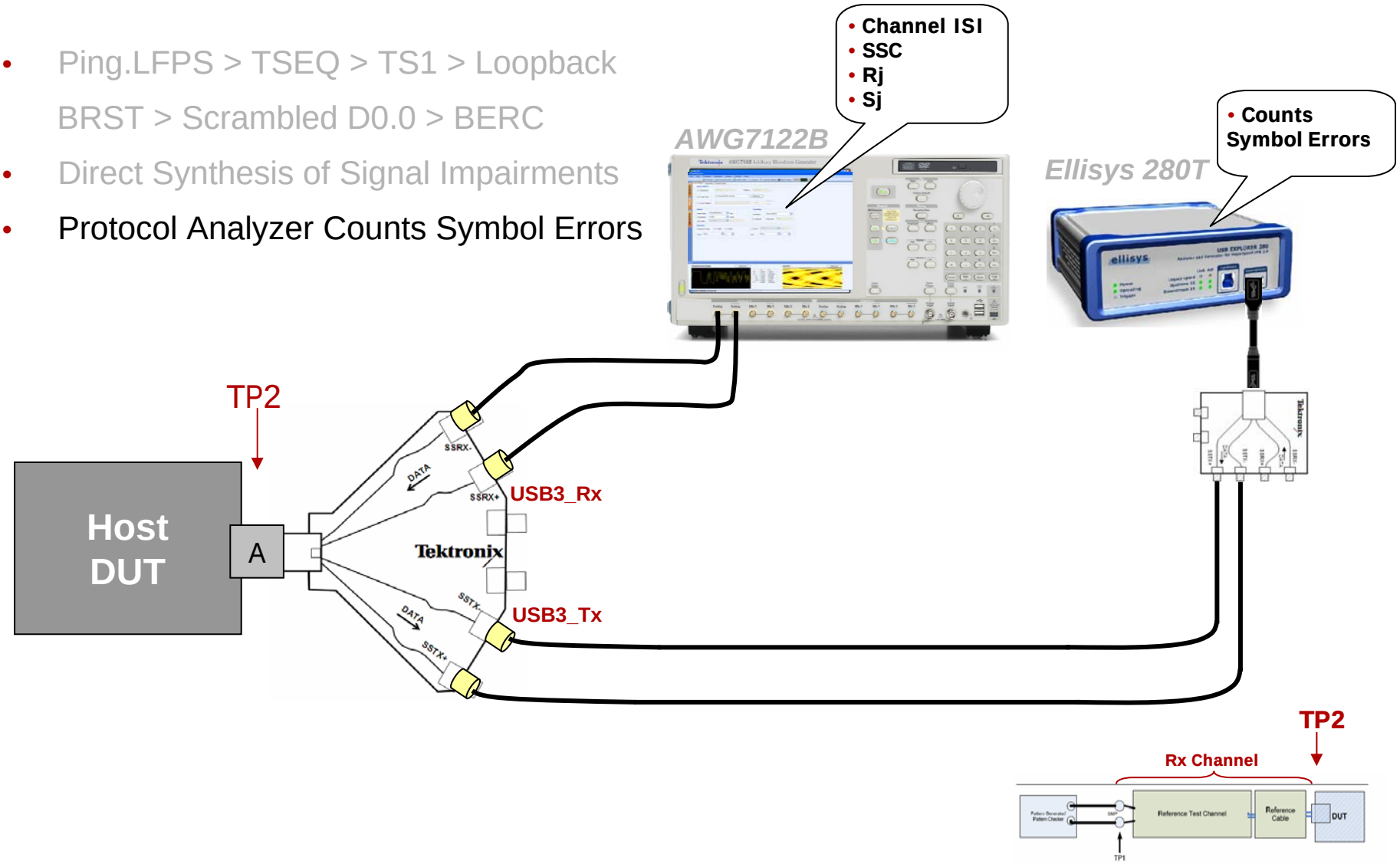


Tektronix

Receiver Test MOI (with SW Channel Emulation)

If DUT does not support 'Loopback BERT'

- Ping.LFPS > TSEQ > TS1 > Loopback
  BRST > Scrambled D0.0 > BERC
- Direct Synthesis of Signal Impairments
- Protocol Analyzer Counts Symbol Errors



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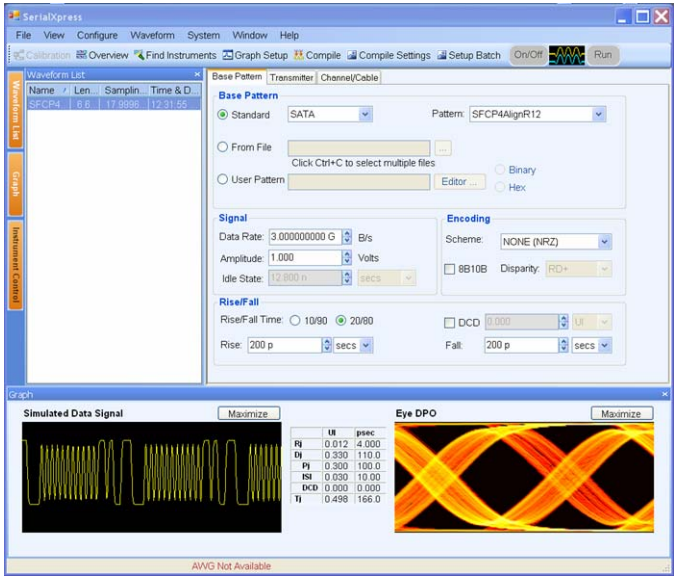
Key Advantages of the AWG for USB Receiver Testing

AWG7000 Arbitrary Waveform Generators with SerialXpress®

- Flexibility to support all signal impairments required for jitter tolerance testing
- Model real-world complexities of SSC profiles to avoid system interoperability issues
- No tradeoffs between any signal impairments - No limitations in generating SSC and SJ at the same time
- Multiple SJ tones can be generated at one time
- Flexible ISI generation enables customers to test ISI models that exceed the test specification
  - No need to wait for USB hardware compliance channels
- Minimize time needed for re-cabling
- Improved repeatability and portability of Receiver test configurations with setup files

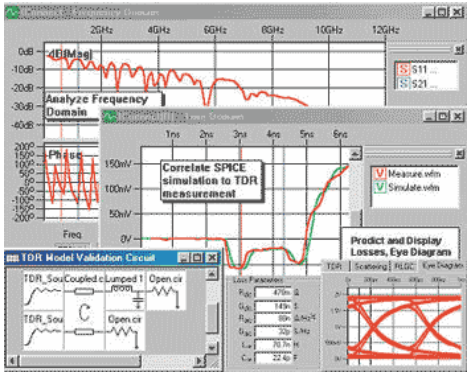


Tektronix

Cable Testing

DSA8200 Sampling Oscilloscope with IConnect®

- Test Fixtures
  - A Receptacle
  - B Receptacle
  - USB2/USB3 Connectors Available for Crosstalk measurements
- Using Sampling Oscilloscope & S-Parameter SW
- Measurements:
  - Impedance
  - Intra-Pair Skew
  - Differential Insertion Loss
  - Differential Return Loss
  - Differential Near-End Crosstalk
  - Differential Crosstalk between USB3.0 and USB2.0 Pairs
  - Differential to CM Conversion



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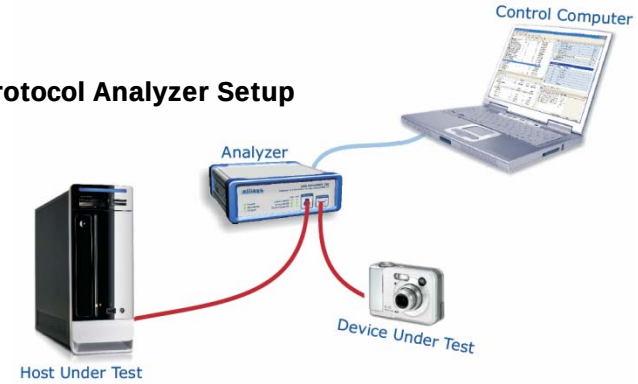
Tektronix Partner Solution

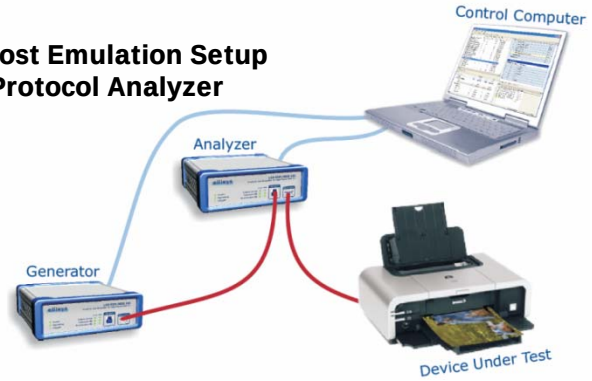
Ellisys EX280 Explorer- USB 3.0 Analyzer/Exerciser

- Analyzer Applications
  - USB host & device monitoring
  - Performance analysis
  - Debug of drivers & software stacks
  - Link state analysis
  - Protocol errors checks
- Generator Applications
  - USB host & device emulation
  - Testing error recovery mechanisms
  - Performance stress testing
  - Compliance verification
  - Link state analysis

Typical Protocol Analyzer Setup



Typical Host Emulation Setup with Protocol Analyzer



www.ellisys.com

Tektronix

Tektronix USB Solution

Complete solution: from PHY layer to Protocol for USB 2.0, 3.0 and Wireless USB

Cost Effective: Automation with a single box solution

Connectivity: Measure closest to Tx output for true performance of USB 3.0 device/host

Flexibility: Compliance, debug, characterization with software channel emulation

USB leadership:

1. Tektronix 1st to market for USB 2.0
2. Tektronix is active in USB-IF Compliance Group and USB 3.0 PIL and contributes to USB 3.0 specification (only T&M Technical Contributor in the USB 3.0 specification)

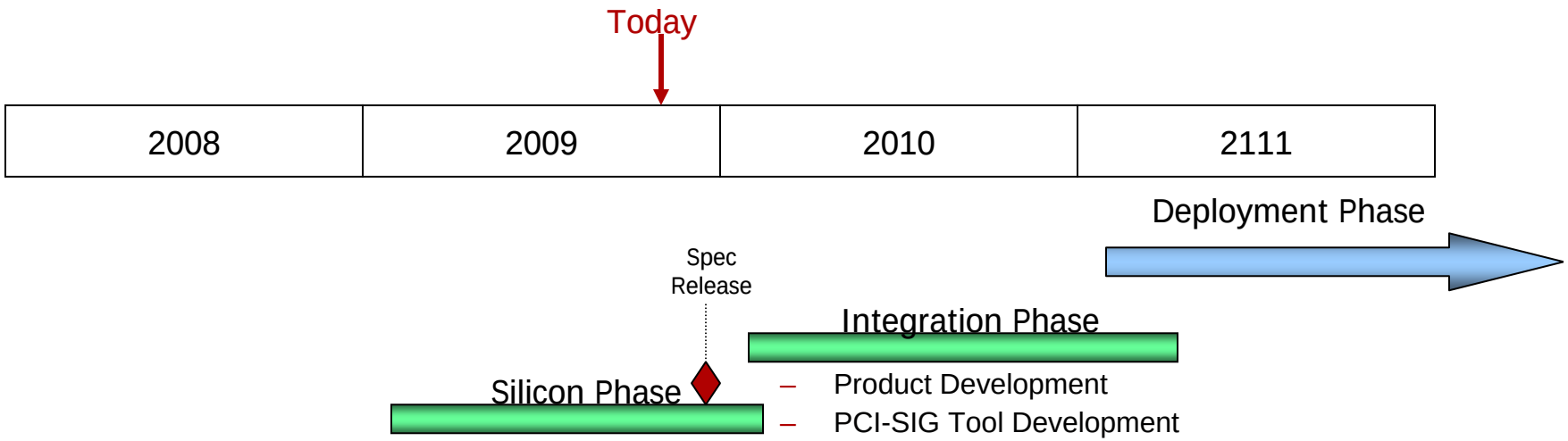
DSA70000B

AWG7122B

CSA8200

Tektronix in PCI Express

- PCI Express
  - Tektronix is market leader in scopes for PCIe validation, debug, and signal quality compliance testing
  - 1st to market with Rev1.0, Rev2.0, Rev3.0 Scope Performance!
  - Member of PCI-SIG EWG (Electrical Working Group) and SEG (Serial Enabling Group)
  - Primary vendor PCIe 2.0 'Gold' System Testing at PCI-SIG workshops.
  - PCI Express 3.0 Timeline



PCI Express Test Methodologies

- Rev 1.1 Testing (2.5GT/s)
  - Eye height of transition/non-transition bits
  - Common mode measurements
  - 1st Order PLL for Clean Clock
  - 3500:250 Scanning for Systems (3rd Order Filter Function)
  - Median-Max Jitter
  - 40-320Bit Compliance Pattern
- Rev 2.0 Testing (5GT/s)
  - Measurement Channel De-convolution
  - DeEmphasis removal
  - 2nd Order PLL, Dual-Dirac Jitter @ 10^{-12} BER
  - Signal Quality Eye and Jitter Testing
    - 1 Million UI Capture (10Million Samples)
    - Dual-Dirac Jitter @ 10^{-12} BER
  - Loop BW Test for Add-In Cards
  - Dual-Port Test for Systems
- Rev 3.0 Testing (8GT/s) – Rev 0.7 Base Spec under review
  - 128B/130B Encoding
  - Testing through Replica Channel
  - De-Embed to Tx Pins
  - Amplitude measured at low frequency
  - New Uncorrelated Jitter Terms
  - 4290 (PRBS-23) UI Repeating Compliance Pattern
  - CEM Spec. not defined yet

DSA70000B

Serial Bus Data Rate	Fundamental Frequency	3rd Harmonic	5th Harmonic
2.5 Gb/s (PCI Express 1.1)	1.25GHz	3.75GHz	6.25GHz
3.0 Gb/s (SATA Gen 2)	1.5GHz	4.5GHz	7.5GHz
5.0 Gb/s (PCI-Express 2.0)	2.5GHz	7.5GHz	12.5GHz
6.0 Gb/s (SATA Gen 3)	3.0GHz	9.0GHz	15 GHz
8.0 Gb/s (PCI Express 3.0)	4.0GHz	12GHz	20 GHz

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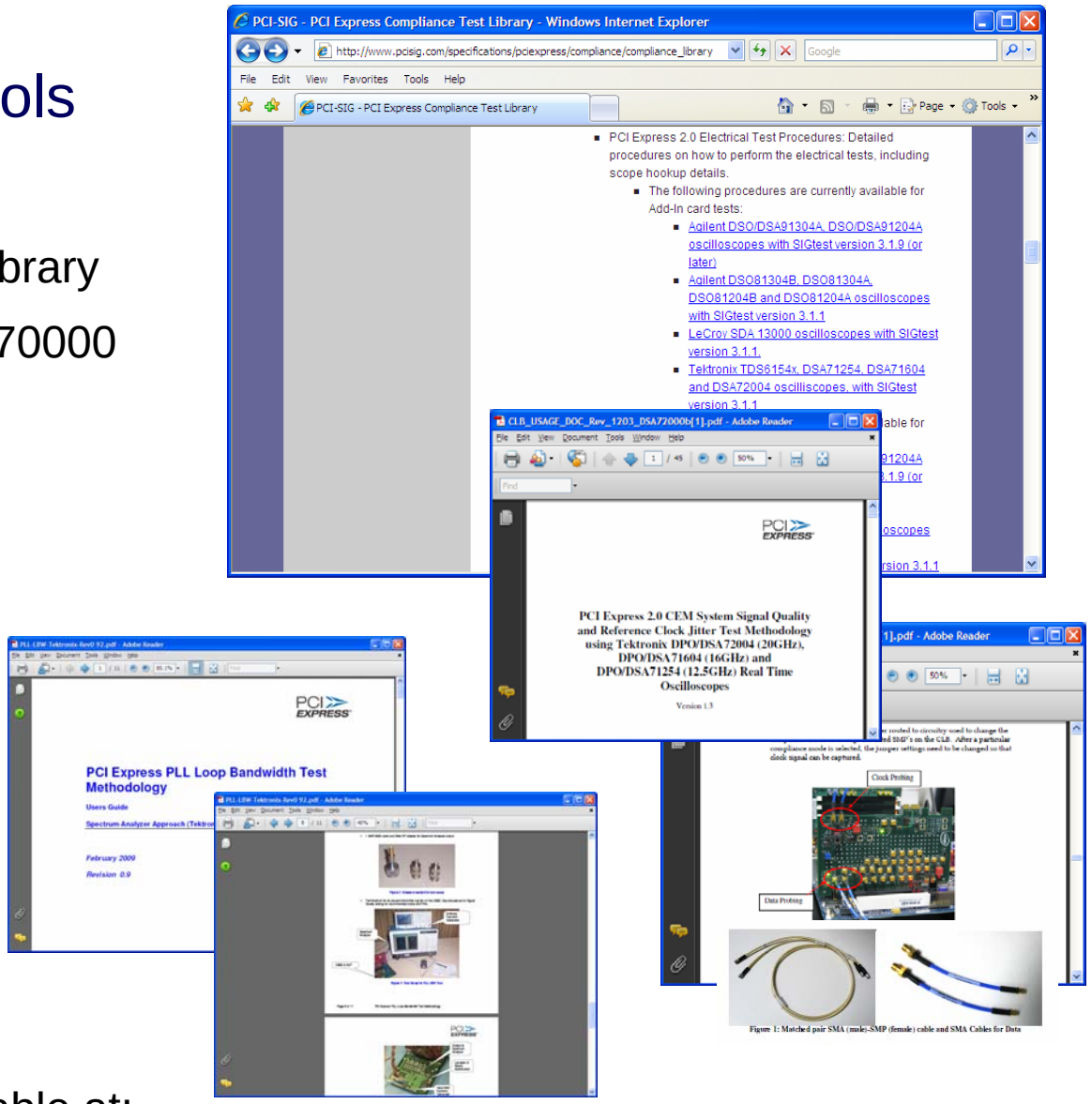
PCI-SIG Compliance Tools

- PCI Express Compliance Library
- Signal Quality Testing DSA70000
  - Add-In Cards*
  - System*
- SigTest & RefClk SW
- PLL LBW Testing
  - RSA6000/AFG3000*
  - AWG7000/DPOJET
- Serial Enabling Group
- Plugfests
  - IL Certification Available

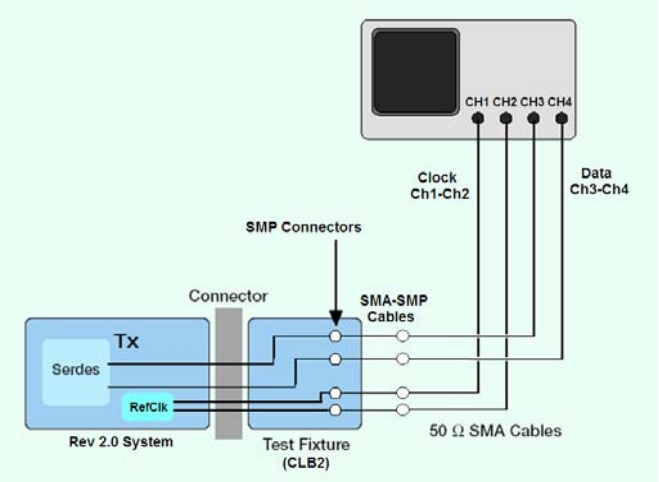


*Tektronix Procedures Available at:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library

Tektronix

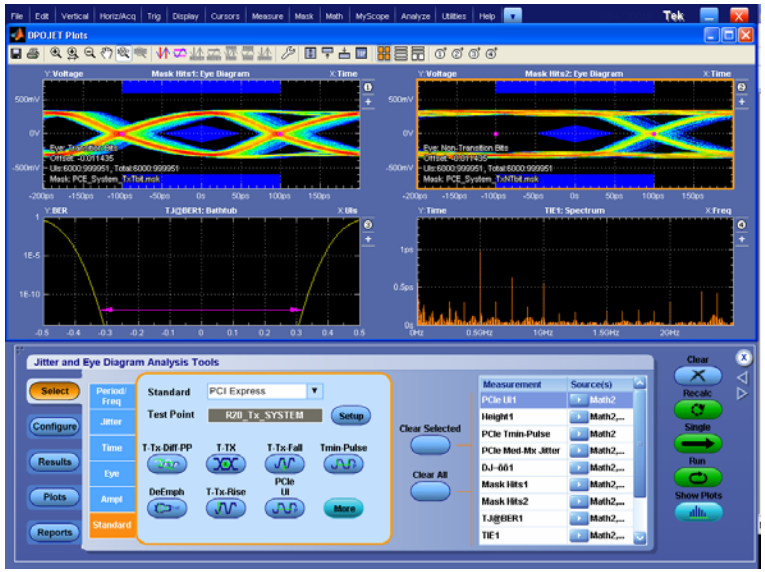
PCI Express Transmitter Validation & Debug

DPO/DSA70000B Series Oscilloscopes



- Fixtures Available from PCI-SIG
- 20 GHz Real-Time Scope
  - 5th Harmonic Performance
  - 50GS/s Sample Rate
- Analysis software for validation and debug
  - Serial Data Link Analysis SW (Optional)
  - DPOJET with option PCE
- New features added in Latest Release
  - Dual Port System Testing
  - Test Point Browser Button
  - RefClk phase Jitter testing
  - MXM CEM support
  - 'Preliminary' PCIe3
- PCI Express 3.0 – Under Development

Opt. PCE



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PCI Express DPOJET and PCI-SIG SigTest Comparison

Function	DPOJET (PCE)	PCI-SIG SigTest & RefClk Tools
Measurements Integrated In Scope Menu/Display	Yes	No
Flexible Integrated Analysis Tools for Validation & Debug	Yes	No
Setup Wizard	Setup Library	No
Single Acquisition & Free Run with Statistical Analysis for Characterization	Yes	Single Acquisition Only
Number of Unique Test Points (Base Tx/Rx, CEM, Cable, ExpressModule, ExpressCard, Rev1.1, Rev2.0, MXM, PCIe3 Preliminary)	18	Rev1.1/2.0 CEM Only
Base Spec. Measurements Supported	20+	0
Documented MOI with measurement algorithms	Yes	No
Test Point Selection through GUI	Yes	Yes
CEM*** Spec. Support	Yes	Yes
Support for PCIe 1.0a, 1.1, 2.0	Yes	Yes
Preliminary Support for Rev3.0	Yes	No
Reference clock tests	Yes	Yes*
Automatic Scope Setup	Yes	No
Clock Recovery/Jitter Filtering for Rev1.1, 2.0, 3.0	Yes**	Yes
HTML Report With Screenshots and Pass/Fail Results	Yes	Yes
Selectable Number of Tests Performed	Yes	No

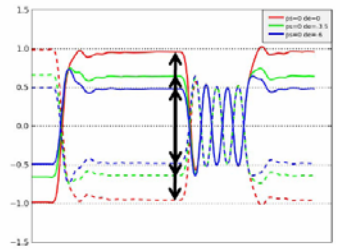
*PCI-SIG RefClk Jitter Tool (separate SW than SigTest)
**Rev 2.0 Brick Wall Emulated through 5th Order Filter (2nd Order PLL + 3rd Order LP Filter)
***CEM (Card Electro-Mechanical)

PCIe3 Transmitter Specifications

- Total pattern length 4290 UI
  - ✓ Repeated sequence allows DDJ separation

Requires De-Embed of Breakout Channel

Voltage



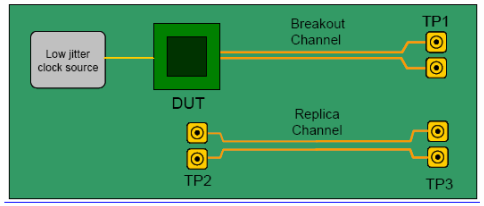


Figure 4-64: Tx Test Board Example

Table 4-29: 8.0 GT/s Tx Voltage and Jitter Parameters

Symbol	Parameter	Value	Units	Notes
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxLE	1200 (max) 800 (min)	mVPP	Note 1
$V_{TX-RS-NO-EQ}$	Reduced swing Tx voltage with no TxLE	1200 (max) 400 (min)	mVPP	Note 1
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	125 (min)	mV	Note 2
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	105 (min)	mV	Note 2
T_{TX-UTJ}	Tx uncorrelated total jitter	31.25 (max)	ps @ 10^{-12}	Note 3
$T_{TX-UDJ-DD}$	Tx uncorrelated deterministic jitter	12 (max)	ps PP	Note 3
$T_{TX-UPWJ-TJ}$	Total uncorrelated PWJ	24 (max)	ps PP	Note 3
$T_{TX-UPWJ-DJDD}$	Deterministic DjDD uncorrelated PWJ	10 (max)	ps PP	Note 3
T_{TX-DDJ}	Data dependent jitter	15 (max)	ps PP	Measured with optimized preset value after de-embedding to Tx pin.
$ps21_{TX}$	Pseudo package loss	TBD	dB	PP ratio of 64 ones/64 zeroes pattern vs. 0101 pattern. No Tx equalization.

Notes:

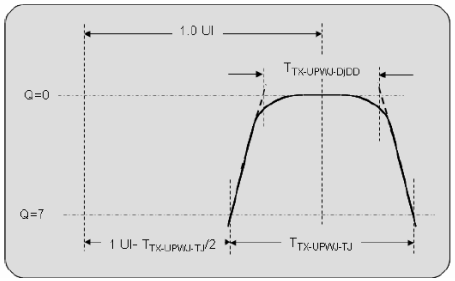
1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64 zeroes/64 ones pattern in the compliance pattern
2. Voltage limits comprehend both full swing and reduced swing modes. The Tx must reject any changes that would violate this spec. The maximum level is covered in the $V_{TX-NO-EQ}$ measurement which represents the maximum peak voltage the Tx can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mVPP at the Rx pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel. The transmitter must advertise a value for LF during TS1 at 8GT/s that ensures that these parameters are met.
3. PWJ parameters shall be measured after DDJ separation.

4.4.1.1.1. Breakout and Replica channels

In order to specify a transmitter with a uniform set of Tx parameters it is necessary to establish a one-to-one correspondence between what is measurable at TP1 and the corresponding Tx voltage or jitter parameter at the pin. This may be achieved by means of a breakout channel and a replica channel. The replica channel reproduces the breakout channel as closely as possible, matching its length, layer transitions, etc, making it possible to de-embed Tx measurements to the pin of the DUT. While the specification does not define precise electrical characteristics for the replica and breakout channels, it is advisable to adhere to the following guidelines:

- Breakout channels should be as short as feasible, less than 6 inches if possible. The longer the channel the more HF information will be lost.
- Breakout channels should be the same length and routed on as few layers as possible, thereby reducing the number of replica channels that need to be built and measured.
- Each routing layer on a testboard should have a separate breakout channel where the via and pad structures of the breakout and replica channels on respective layers match as closely as possible

PWJ



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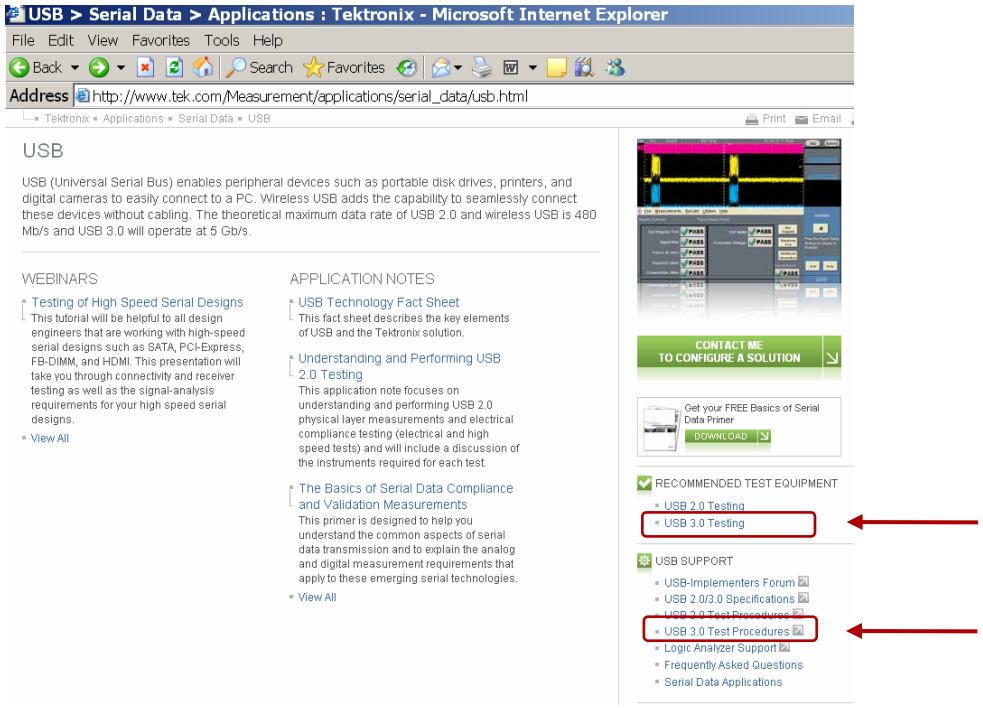
Resources

USB

- Specifications
  - http://www.usb.org/developers/docs/
- Tektronix USB Solutions
  - www.tektronix.com/usb
- Ellisys Protocol Analysis
  - www.ellisys.com

PCI Express

- Specifications
  - http://www.pcisig.com/specifications/pciexpress/
- Tektronix PCI Express Solutions
  - www.tektronix.com/pci_express



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