USB 3.0 Receiver Compliance Testing

Application Note

Tektronix®

Contents

Abstract

SuperSpeed USB (USB 3.0) is poised to become as popular and widespread as its predecessors. At 5 Gb/s, however, it is more than an order of magnitude faster than USB 2.0, posing challenges for physical layer testing and requiring bit error ratio (BER) testing for receivers. This paper reviews the requirements for receiver compliance testing with a comprehensive example using the Tektronix BERTScope family of products.

Introduction

The Universal Serial Bus (USB) is probably the best known computer peripheral interface today. It is ubiquitous in modern everyday life, connecting our various electronic devices such as mobile communication devices, external FLASH drives, digital cameras, etc. to our computers.

As with any serial bus standard, it is evolving to accommodate the growing need for faster data transfer and more intelligent power consumption. For example, USB external storage devices are reaching into the terabytes in size, and consumers' expectations of the speed at which large files, such as full resolution digital photos or entire movies, can be transferred to a host computer are rising.

The latest incarnation, USB 3.0, or "SuperSpeed USB," was designed to address such needs. Specifications[i] for USB 3.0[ii] were completed on November 17, 2008, and vendors are gearing up to introduce products compliant with the new standard. Improvements from USB 2.0 include:

- Faster data rate (5 Gb/s vs. 480 MB/s in USB 2.0). This has a big impact on USB 3.0 receiver testing, as the higher data rate means a higher burden on the physical layer and more stringent compliance testing compared to USB 2.0. For example, receiver testing now requires bit error ratio (BER) testing.

- More power when needed and more power saving when not needed.

- Full duplex data transfers (vs. half duplex in USB 2.0).

- New connectors and cables, with backward compatibility to USB 2.0.

The higher performance of the USB 3.0 standard has resulted in significant changes to the test requirement, including the addition of receiver testing as detailed in the following sections.
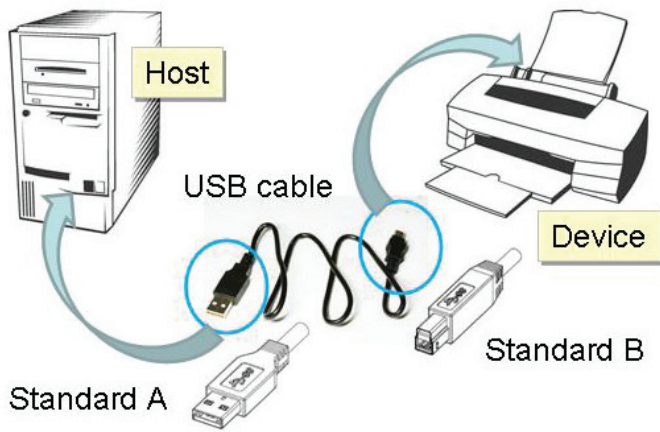
Figure 1. Standard A and Standard B USB connectors connect USB Hosts such as a PC to Devices such as a printer via a USB cable.

USB 3.0 Devices and Connectors

USB 3.0 devices come in two flavors – Hosts and Devices.

- **Hosts** are where the USB controller resides, for example, on a Personal Computer (PC). It includes the CPU, buses, and operating system.

- **Devices** are USB hubs or peripheral devices, for example memory sticks, external disk drives, printers, digital cameras, cellular telephones/PDAs, etc.

The receiver test requirements are the same for both, but as we will see, the adapters and cabling needed for testing differ.

There are four types of connectors defined in the USB 3.0 specification.

- The **Standard A** connector connects to the Host, and is the type of connector that is most familiar to consumers, as it is the type of USB port found on PCs and is the connector type found on the ubiquitous USB memory stick.

- The **Standard B** type of connector is typically used for large stationary USB peripherals such as printers and external hard drives. It is usually found at the other end of a USB cable connecting the peripheral to the PC.

- The **Power B** connector is the same form factor as the Standard B, with extra pins for power and ground.

- The **Micro** connectors are used for small peripherals, such as digital cameras.

While the SuperSpeed B side connectors on the cables (plugs) are incompatible with USB 2.0 B receptacles, the A side connectors are fully compatible. This allows USB 3.0 devices to plug into USB 2.0 hosts. All USB 3.0 receptacles accept both USB 2.0 and 3.0 plugs, so that USB 2.0 cables and devices can be used with USB 3.0 hosts.

The Standard A and Standard B connectors are used for receiver compliance testing.
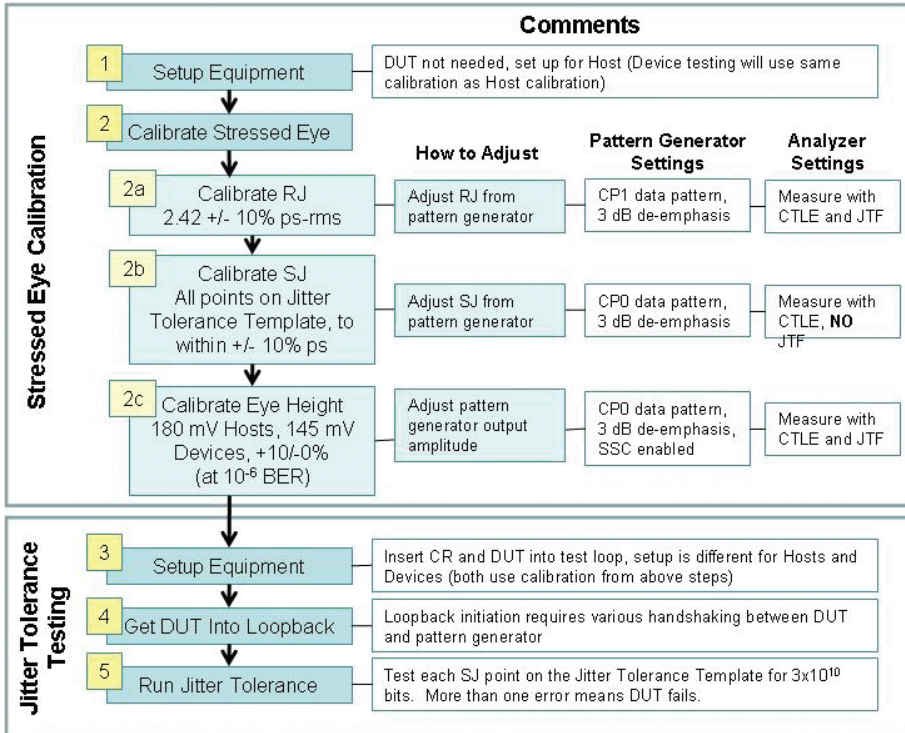
Figure 2. Steps 1 and 2 of Stressed Eye Calibration will be covered in Section 2.1. Steps 3-5 of Jitter Tolerance Testing will be covered in Section 2.2. All steps will be covered in the example in Section 3.

USB 3.0 Receiver Testing

Receiver testing for USB 3.0 is similar to other high speed serial bus receiver compliance testing, and is generally split up into two phases.

■ **Stressed eye calibration** is the industry name for the procedure to create a worst case signal condition to test receivers. This worst case signal is usually impaired both horizontally by added jitter, and vertically, by setting the amplitude to the lowest a receiver would see when deployed. Stressed eye calibration must be performed when any of the test fixtures, cabling, or instrumentation have been changed.

■ **Jitter tolerance** tests the receiver by using the calibrated stressed eye as input, and then applies additional sinusoidal jitter (SJ) of increasing frequency. This applied SJ exercises the clock recovery circuitry inside the receiver, so not only is the receiver being tested using worst case signal conditions, but its clock recovery is also explicitly tested. The magnitude and frequency of the applied SJ follows a template as prescribed by the standard. This jitter tolerance template covers the bandwidth of the clock recovery PLL; high amounts of applied SJ should be tolerated within the loop bandwidth since the clock recovery will track out this sinusoidal jitter, but only small amounts can be withstood beyond the loop bandwidth, since this jitter is not tracked out, and will affect the downstream receiver circuit.

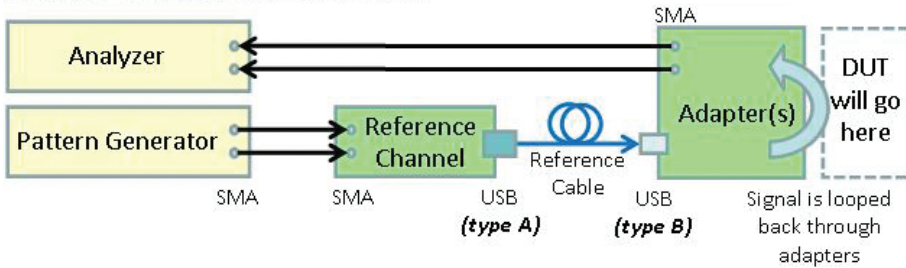## Host Receiver Calibration
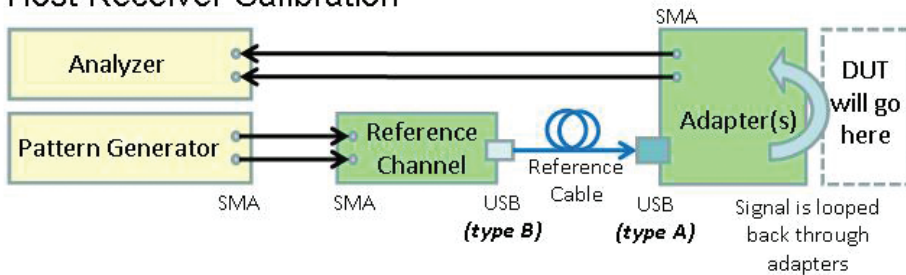
Device Receiver Calibration

Figure 3. Setup for Stressed Eye Calibration for Hosts (top) and Devices (bottom).

Stressed Eye Calibration

Stressed eye calibration involves first setting up the test equipment with compliant fixtures, cables, and channels, and then iteratively measuring and adjusting various types of applied stresses such as jitter. The calibration step is performed without the DUT, with compliant test fixtures and channels, and with specific data patterns generated by the test equipment.

Equipment Setup

The setup for stressed eye calibration is shown in Figure 3 for Hosts and Devices. The DUT is not needed for stressed eye calibration, but Figure 3 shows where the DUT would be placed during testing. Instead, the signal is looped back to the analyzer through the adapters and cabling. The goal is to calibrate the signal as close to the input of the DUT when it is placed in the test loop. Note that the polarity of the reference cable is reversed
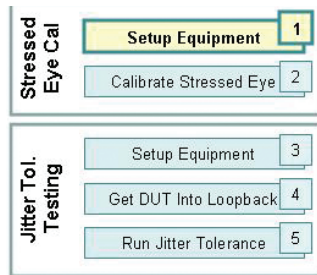
between the two, whereas for Host testing, the Standard A type connector is connected to the adapter of the Host DUT, but the Standard B type connector is connected to the adapter of the Device DUT. There are different test fixtures for Hosts and Devices, and several adapters may be necessary to loop the generated signal back to the measurement instrument, as will be shown in the example. The connection to the analyzer should be as high quality as possible.

The test instrumentation should be capable of performing two functions – pattern generation with the ability to add various types of stresses, and signal analysis such as jitter and eye measurements.
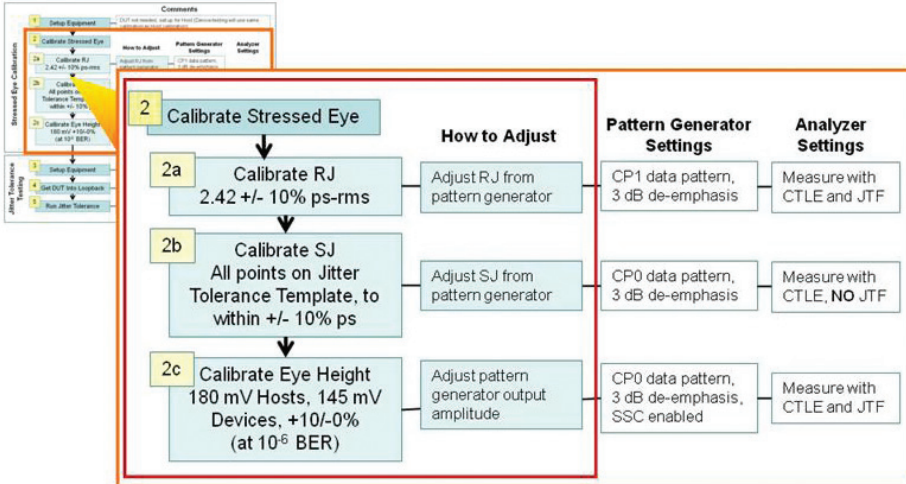
Figure 4. This figure shows the Stressed Eye Calibration (Step 2) of the overall flowchart in Figure 2.

How to Calibrate the Stressed Eye

The stressed eye recipe and how it can be achieved will be covered in this section. There are three impairment calibrations that must be made to calibrate the stressed eye, Random Jitter (RJ), Sinusoidal Jitter (SJ), and eye height. Each of these requires

particular settings on the pattern generator and analyzer, as listed in the flowchart in Figure 2. In this section, the stress components, the pattern generator settings, and the analyzer settings will be covered.

Stressed eye calibration must be performed once per set of cables, adapters, and instrumentation. Because they use different sets of adapters and reference channels, Hosts and Devices will have different stressed eye calibrations. Once complete, the settings for the calibrated eye can be re-used and must be re-calibrated only if the equipment setup changes.
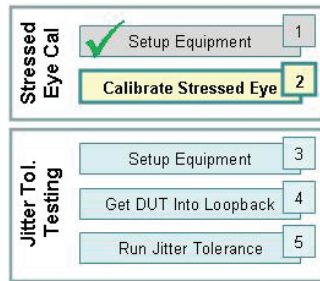
Stressed Eye Recipe Components

There are three "ingredients" in the stressed eye recipe, as shown in Figure 4. Each stress component should be calibrated in the order shown.

1. Random Jitter (RJ)

- **Definition:** RJ is unbounded jitter that is not correlated to the data pattern, which means that its measurement should be the same regardless of the data pattern used. Because it is unbounded, it grows with measurement depth; the deeper the measurement in terms of number of waveforms or BER measured, the larger the peak-peak RJ measurement becomes.

- **How to adjust:** To achieve the proper amount of RJ, the pattern generator must be able to adjust the amount of injected RJ.

- **How to measure:** Most analyzers (i.e. BERTs and oscilloscopes) provide automated RJ measurements.
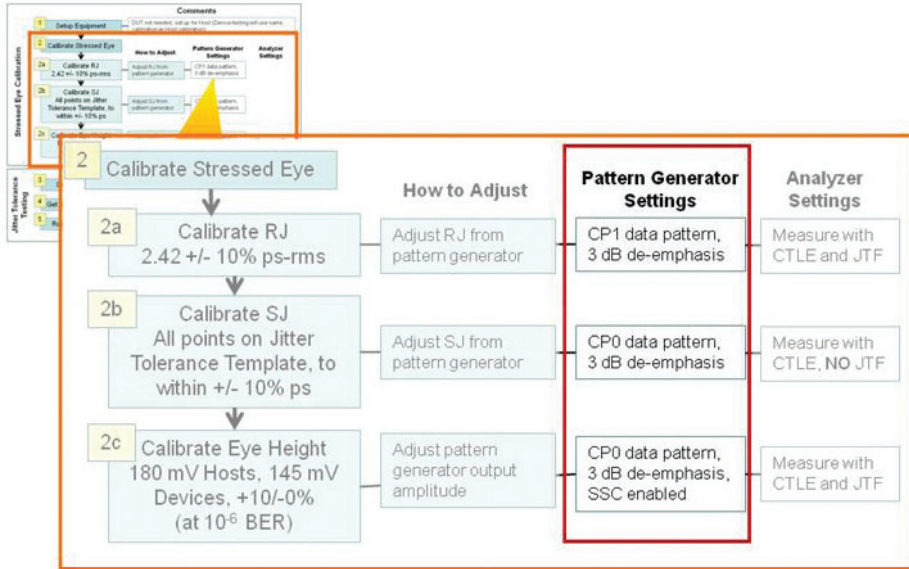
Figure 5. Pattern Generator Settings used for Stressed Eye Calibration, including specifications for data pattern, de-emphasis level, and spread spectrum clocking (SSC).

Sinusoidal Jitter (SJ)

- **Definition:** SJ is bounded jitter that is periodic in nature, but usually not correlated to the data pattern (unless the SJ frequency just happens to be a multiple of the pattern repetition frequency), so like RJ, its measurement is the same regardless of data pattern. Unlike RJ, it does not grow with measurement depth due to its bounded nature.

- **How to adjust:** Like RJ, the pattern generator must be able to adjust the amount of injected SJ to achieve the desired amount. The injected SJ must be of a particular frequency, with adjustable amplitude. All SJ frequencies and amplitudes in the USB 3.0 Jitter Tolerance Mask (above right) need to be calibrated.

- **How to measure:** The USB 3.0 compliance test procedures specify that the amount of SJ should be measured by taking the difference in Total Jitter (TJ) between a signal with 0 amplitude of injected SJ, and the desired amount of injected SJ. TJ measurements can be found on most oscilloscopes.
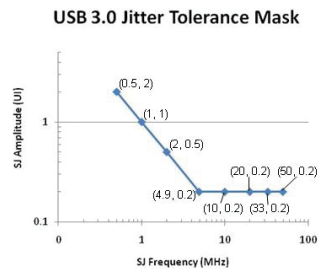
Eye Height

- **Definition:** Eye height is the opening of the eye in the center of the unit interval and is accompanied by a measurement depth, in this case, 10^6 waveforms. The eye height is data pattern dependent because it is impacted by the amount of Data Dependent Jitter (DDJ) in the signal. The eye height specification is different for Hosts (180 mV) and Devices (145 mV).

- **How to adjust:** The eye height is adjusted via the output amplitude of the pattern generator.

- **How to measure:** Eye height can be measured on oscilloscopes, and should meet the 10^6 waveforms requirement.

Pattern Generator Settings

Now that we have covered "what" needs to be calibrated, we will discuss the additional requirements of the pattern generator for each step of the calibration, including:

1. The data pattern to be used.

2. The amount of de-emphasis.

3. Whether or not spread spectrum clocking (SSC) should be enabled.

Compliance Pattern	Value	Bit Sequence Description
CP0	Scrambled D0.0	8b/10b encoded PRBS-16
CP1	D10.2	Repeating 1010 (Nyquist frequency)
CP2	D24.3	Repeating 1100 (Nyquist frequency / 2)
CP3	K28.5	Repeating 0011111010110000010, contains runs of 5 ones and zeroes and lone bit sequences, representative of longest and shortest runs in 8b/10b system
CP4	LFPS	Low Frequency Periodic Signaling (refer to standard for more on LFPS)
CP5	K28.7	Repeating 0011111000 (for use with de-emphasis)
CP6	K28.7	Repeating 0011111000 (for use without de-emphasis)
CP7	50-250 1's and 0's	Repeating 50-250 1's followed by 50-250 0's (for use with de-emphasis)
CP8	50-250 1's and 0's	Repeating 50-250 1's followed by 50-250 0's (for use without de-emphasis)

Table 1. USB 3.0 Compliance Patterns (from table 6-7 of standard).

Data Pattern

There are two patterns, CP0 and CP1 listed in the stressed eye calibration recipe. For reference, all USB 3.0 compliance patterns are listed in Table 1.

- **CP0** is an 8b/10b encoded PRBS-16 data pattern (the result of subjecting the D0.0 character to scrambling and encoding in a USB 3.0 transmitter). After 8b/10b encoding, the longest run length of ones or zeros is 5 bits, reduced from the longest run length of 16 bits in a PRBS-16 pattern. CP3 (see Table 1) is a pattern similar to the 8b/10b encoded PRBS-16 in that it contains both the shortest (lone bit) and longest sequences of identical bits.

- **CP1** is a clock pattern used for the RJ calibration. Many instruments implement a dual-Dirac method of random and deterministic jitter separation for the RJ measurement. Using a clock pattern circumvents one of the drawbacks of the dual-Dirac method, which is the tendency to report data dependent jitter (DDJ) as RJ, especially on long patterns. By using a clock pattern, DDJ as a result of Inter-symbol Interference (ISI) is eliminated from the jitter measurement, resulting in a more accurate RJ measurement. The CP2 pattern, which is an 1100 clock pattern, could also be used for RJ measurement.
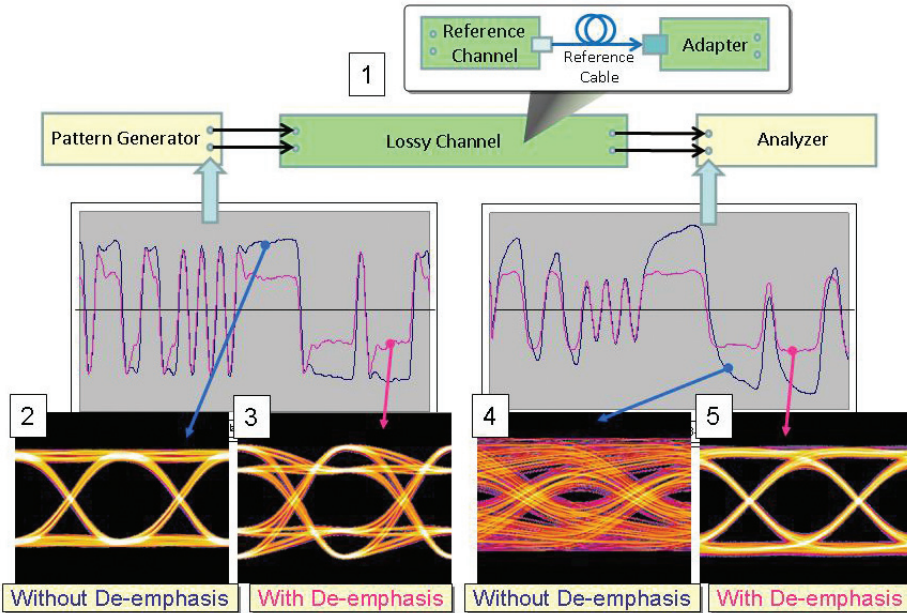
Figure 6. An example showing waveforms and eye diagrams demonstrating the effects of de-emphasis, using a PRBS-7 data pattern.

De-Emphasis

As shown in Figure 3 and replicated in Figure 6, there is a lossy channel (i.e. a USB 3.0 reference channel and cable) in between the pattern generator (transmitter) and the analyzer (receiver). This causes frequency dependent loss in the form of eye closure, both vertically and horizontally. To combat this loss, transmitter de-emphasis is used to boost the high frequency components of the signal so that the received eye is good enough for an operational link at a BER of 10^{-12} or better.

In Figure 6:

1. A typical setup for measuring signals is shown, with a lossy channel in between the transmitter and receiver. The USB 3.0 reference channel, reference cable, and adapter are examples of components that constitute a lossy channel.

2. Without de-emphasis, all amplitudes are nominally the same.

3. With de-emphasis, transition bits have higher amplitude relative to non-transition bits, effectively boosting the high frequency components of the signal.

4. After passing through lossy channels and cables, the signal without de-emphasis suffers from Inter-Symbol Interference (ISI) and has more eye closure then the signal without de-emphasis.

5. The signal with de-emphasis is fully open.

As shown here, the amount of de-emphasis affects the amount of ISI and DDJ and therefore impacts the eye opening at the receiver.
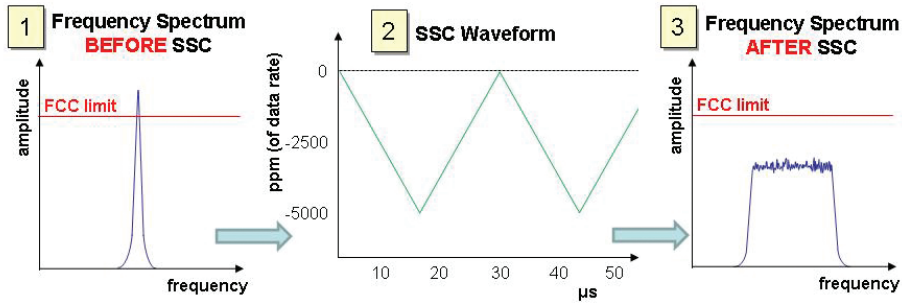
Figure 7. The effect of SSC on a frequency spectrum (single tone shown).

Spread Spectrum Clocking (SSC)

Spread spectrum clocking (SSC) is commonly used in synchronous digital systems (USB 3.0 included) to reduce electromagnetic interference (EMI). Shown in Figure 7:

1. Without SSC, the frequency spectrum of the digital stream would have a high magnitude sharp peak at the carrier frequency (i.e. 5 Gb/s) and its harmonics, possibly exceeding limits set by federal regulatory bodies such as the Federal Communications Commission (FCC) (in the United States).

2. To prevent this problem, SSC is used to spread out the energy of the frequency spectrum, keeping within the FCC limits. The carrier frequency is modulated, in this case by a triangle wave. The amount of frequency "spreading" for receiver testing is 5000 ppm, or 25 MHz, with the frequency modulation cycling at 33 kHz, or every 30 μs, shown as one period of the triangle wave.

3. After SSC, the energy in the frequency spectrum is spread out, and no single frequency violates the FCC limits.
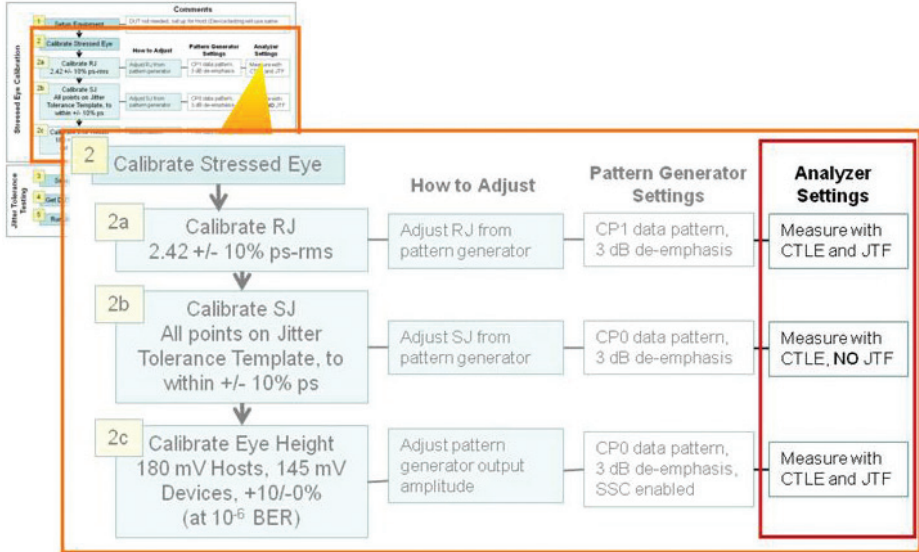
Figure 8. Analyzer Settings used for stressed eye calibration, including required use of the Continuous Time Linear Equalizer (CTLE) and Jitter Transfer Function (JTF).

Analyzer Settings

We have covered the stress recipe components, and the requirements of the pattern generator when calibrating the various stress components. This section covers the requirements of the analyzer, specifically the use of the Continuous Time Linear Equalizer and Jitter Transfer Function when making jitter and eye opening measurements.
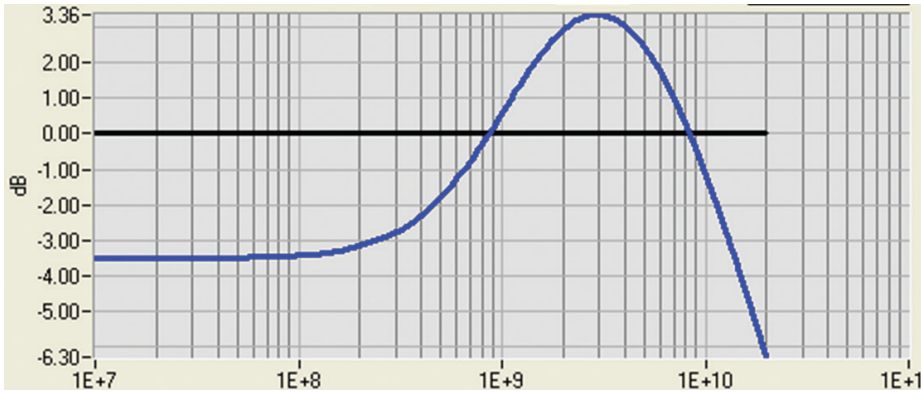
Figure 9. The CTLE function, from the USB 3.0 specification.

Continuous Time Linear Equalizer (CTLE) Function

In addition to transmitter de-emphasis, receiver-side equalization is used to improve signals that have been impaired by ISI caused by frequency dependent loss from such elements as the reference channel and cabling. The concept is the same as for de-emphasis – the high frequency components of the signal are boosted via signal processing methods.

Although receiver equalization circuitry in a Device or Host is implementation specific, the USB 3.0 standard specifies a Continuous Time Linear Equalizer (CTLE) to be used for compliance testing (Figure 9). This CTLE must be implemented by the reference receiver such as a BERT or oscilloscope prior to making compliance test measurements (both for transmitter testing, and in this case, receiver stressed eye calibration), often in the form of software emulation.

The use of CTLE emulation for jitter measurements mainly impacts jitter that is affected by signal processing methods, namely ISI. Jitter components that are not correlated to the data pattern such as RJ and SJ are not impacted by CTLE emulation, although the use of the CTLE is required for both of these measurements according to the CTS. On the other hand, eye height is directly impacted, since ISI contributes to its measurement.
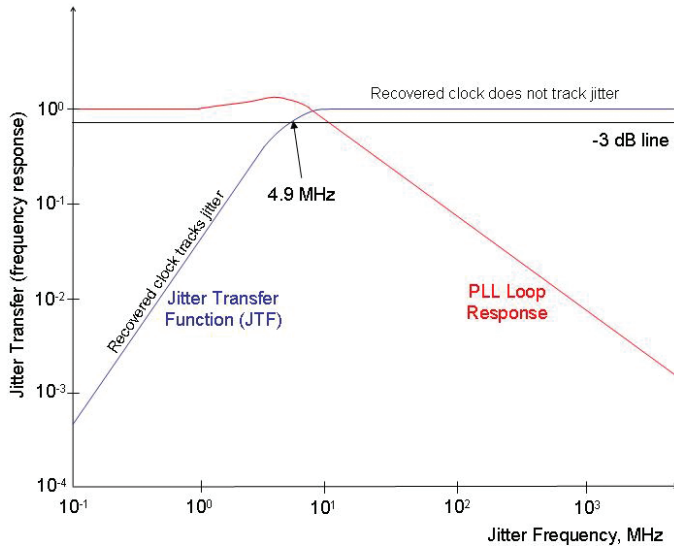
Figure 10. The JTF of the Golden PLL, adapted from figure 6-9 of the USB 3.0 standard.

Figure 11. After Stressed Eye Calibration is complete, Jitter Tolerance tests the receiver using worst case signal conditions.

Jitter Transfer Function (JTF)

Jitter calibration measurements must be made using a clock recovery Golden PLL with a compliant Jitter Transfer Function (JTF), as shown in Figure 10 (blue trace). The JTF dictates how much jitter is transferred from the incoming signal to the downstream analyzer. In this case, the -3 dB cutoff is 4.9 MHz.

- At lower SJ frequencies (along the sloped part of the JTF, and where the PLL Loop Response is flat), the recovered clock tracks the jitter on the data signal, and thus, the jitter in the data **relative** to the clock is attenuated according to the JTF.

- At higher SJ frequencies (where the JTF flattens out and the PLL Loop Response slopes downward), the SJ present in the signal is transferred to the downstream analyzer because the clock is a "clean" clock and does not track the jitter on the incoming data signal.

The use of a compliant JTF is specified for all measurements except for SJ during stressed eye calibration.
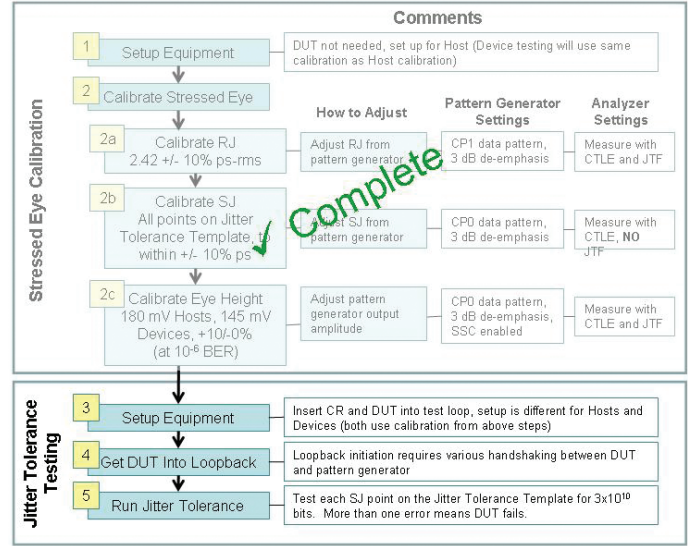
Jitter Tolerance Testing

Once the stressed eye has been calibrated, testing of the receiver can commence. As mentioned in the Introduction, USB 3.0 requires BER testing, unlike its 2.0 predecessor. Bit error ratio (BER) testing in the form of a Jitter Tolerance test is the **only** test required for receiver testing.

The Jitter Tolerance test exercises the receiver using worst case input signal conditions (the stressed eye calibrated in the previous section). On top of the stressed eye, a series of SJ frequencies and amplitudes covering the frequency range surrounding the -3 dB cutoff frequency of the JTF are injected into the test signal while the error detector monitors the receiver for mistakes or bit errors, and calculates the BER. Jitter Tolerance will be covered in detail after a review of the equipment setup and receiver loopback mode, a state in which the DUT's transmitter re-sends the bits it receives.

Host Receiver Test
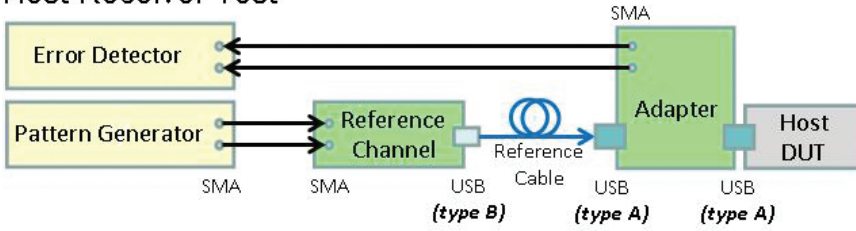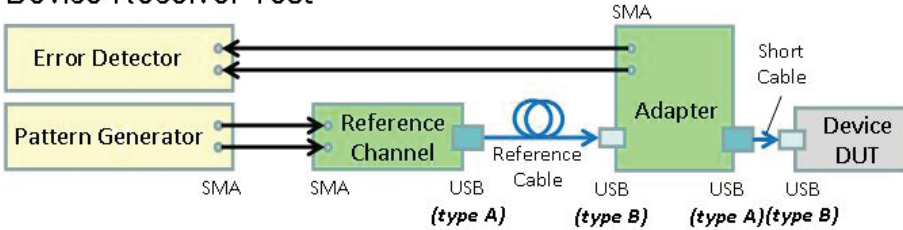

Device Receiver Test

Figure 12. Setup for USB 3.0 Receiver Test.

Equipment Setup

The setup of equipment for receiver testing is similar to that of stressed eye calibration, with the DUT now inserted into the test loop, as shown in Figure 12. The Host or Device DUT is connected to the adapter as displayed. Instead of the signal being routed straight back to the analyzer, the test signal from the pattern generator passes through the DUT's receiver, is "looped back" through its transmitter (hence, the term "loopback"), back through the adapter, and to the error detector. The connection to the error detector should be as high quality as possible.
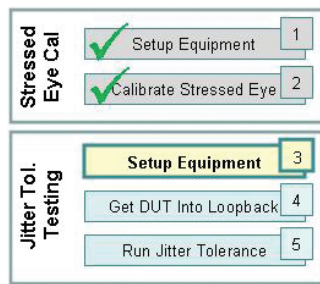
For Jitter Tolerance testing, the test instrumentation must be able to perform error detection and keep track of the BER. Instruments such as BERTs and oscilloscopes are capable of this function.

Receiver Loopback

Loopback is one of the USB 3.0 link states in which the device sends the bits it receives back through its transmitter. If the receiver makes a mistake, the bit in error will be sent back through the transmitter and to the downstream analyzer for detection. To initiate loopback, a series of handshakes[1] must be performed between the pattern generator and DUT.

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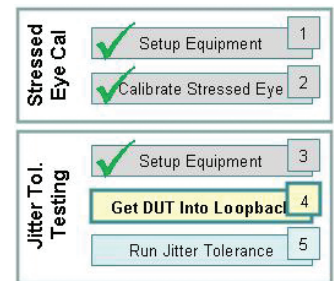
[1] A detailed description of loopback initiation is beyond the scope of this paper. See the USB 3.0 Specification, which includes link state diagrams and details on the bit sequences required for loopback initiation handshaking.
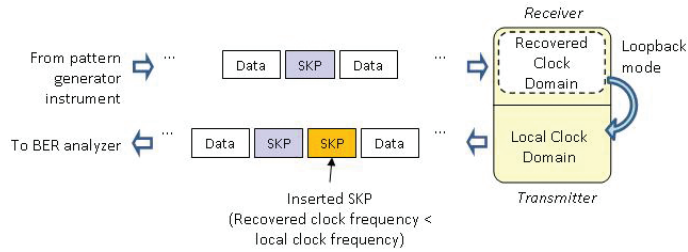
Figure 13. Example showing an inserted SKP when DUT is in loopback mode.

Asynchronous BER Testing

USB 3.0 uses 8b/10 encoding, and as is common in 8b/10b encoded systems, the receiver and transmitter may be on slightly different clock frequencies – the recovered clock of the received data stream may not be exactly equal to the clock frequency of the transmitter. When in loopback mode for receiver testing, this mismatch in frequencies poses a problem for the DUT; bits may be coming in faster than they can be sent back out, or vice versa. To compensate for the frequency mismatch, clock compensation symbols are used and either deleted or inserted into the data stream as it is passed from the receiver back through the transmitter. For example, symbols are added if the recovered clock frequency is less than (slower than) the transmitter clock frequency (as shown in Figure 13), and vice versa. USB 3.0 uses SKP symbols for clock compensation.

The test equipment must be able to handle this non-deterministic number of clock compensation symbols in the incoming data stream, commonly termed **asynchronous BER testing.**
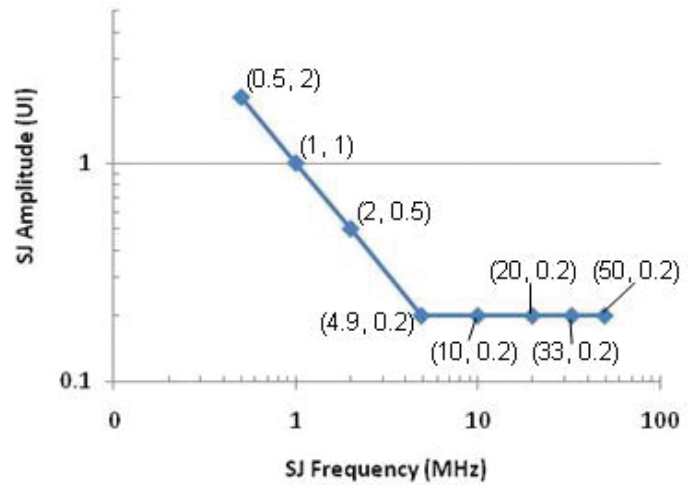

Figure 14. The USB 3.0 Jitter Tolerance Mask.

As a final note, the USB 3.0 specification includes two types of loopback for BER testing. The first is as described above, where the bits received are re-transmitted back to the analyzer for BER testing. The second relies on the DUT to keep track of its own BER, and report this back in bits embedded in special symbols called ordered sets. However, the second method is not included in the latest Compliance Test Specification.

Stepping Through the Tolerance Mask

Once the stressed eye has been calibrated, the DUT and equipment have been set up for testing, and the DUT has been put into loopback mode, the DUT's receiver is ready to be tested.

Stressed Eye Cal	Setup Equipment	1
	Calibrate Stressed Eye	2
Jitter Tol. Testing	Setup Equipment	3
	Get DUT Into Loopback	4
	Run Jitter Tolerance	5

Jitter tolerance testing applies varying levels of SJ amplitude at specific SJ frequencies to test the receiver. As shown in Figure 14, the lower SJ frequencies tend to have higher SJ amplitude, as these frequencies are well within the loop bandwidth of the receiver CR and will thus get tracked out. As the SJ frequency approaches the loop bandwidth and surpasses it, the SJ amplitude levels out at an amplitude less than 1 UI. Jitter above the loop bandwidth of the receiver will not get tracked out, and will be passed down to the receiver's decision circuit.

The USB 3.0 CTS specifies that each SJ point on the tolerance curve be tested using 3×10^{10} bits. The DUT fails if more than one error is detected at any SJ test point.
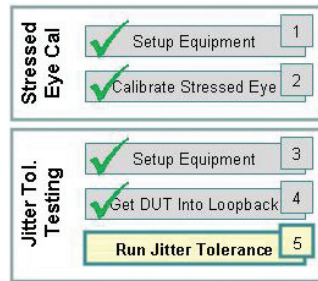
Summary

USB 3.0 promises to become a dominant computer peripheral bus standard, just as USB 2.0 is today. Its signaling speed of 5 Gb/s is more than a magnitude faster than USB 2.0, and thus, signal integrity challenges cause a higher bar to be set for testing SuperSpeed USB devices over the previous generation. For receiver testing, the test regimen is wholly based on Jitter Tolerance using a calibrated stressed eye input.

In this application note, all aspects of USB 3.0 receiver testing have been covered, including stressed eye calibration and jitter tolerance testing with measured device margin. An MOI demonstrating receiver testing using the BERTScope Family of Products is available on www.tektronix.com/usb. In this MOI, you'll see how the USB 3.0 Automation Software coordinates the operation of the following equipment to lead you through the receiver set-up and test process, including loopback initiation with a simple button click.

- BERTScope
- USB Switch
- De-emphasis Processor
- Clock Recovery

The BERTScope not only provides a straightforward solution for compliance testing, but also has the flexibility to troubleshoot difficult engineering problems if compliance tests fail.

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