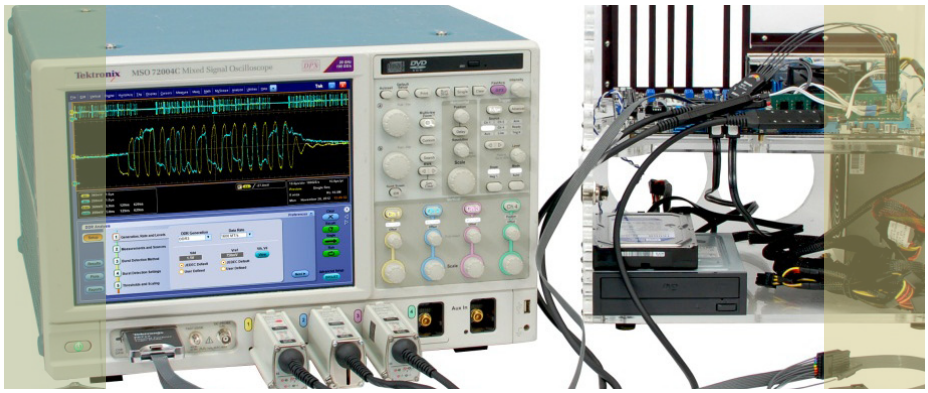

Debugging Memory Interfaces using Visual Trigger on Tektronix Oscilloscopes

Application Note

What you will learn:

This document focuses on how Visual Triggering, Pinpoint™ Triggering, and Advanced Search & Mark to set up triggers to easily capture events of interest.

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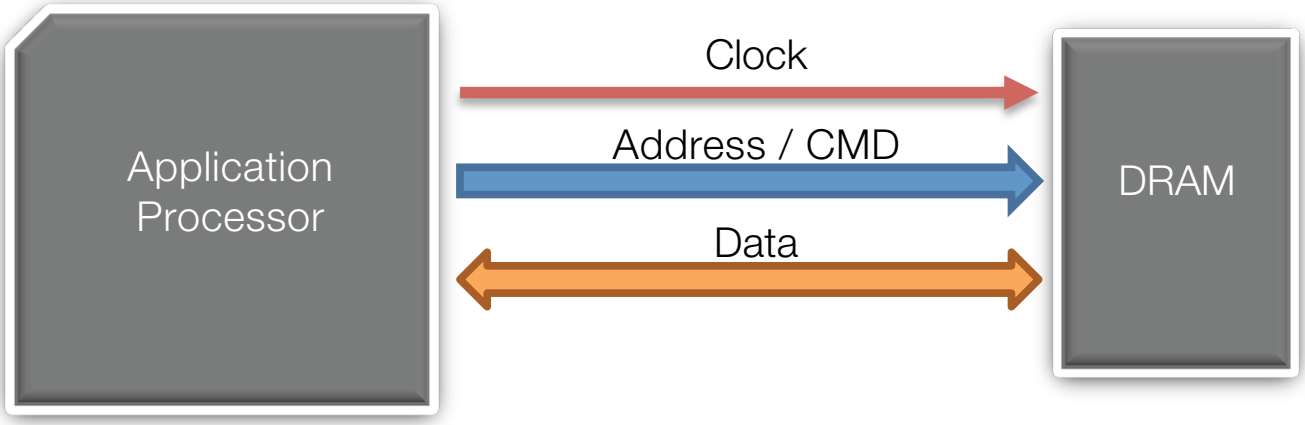


Introduction

Virtually every electronic device uses some form of memory. As applications become more complex and media-oriented, they drive the need for higher performance along with the need for improved efficiency and reliability at lower cost. JEDEC has evolved technical standards to support these requirements making DDR memory the most widely used memory technology in all electronic devices, i.e., computer systems, consumer electronics, industrial applications or mobile products. JEDEC recently published the fourth generation (DDR4) memory standard, as well as the third generation low power (LPDDR3) memory standard.

The DDR interface can be divided into three separate groups of signals:

- Clock:
  - All transactions on the bus occur with reference to the clock signal. The clock is provided by the Application Processor.
- Address/Command Bus:
  - Signals are uni-directional and are driven by the application processor to the DRAM at the speed of the clock signal. This carries Address as well as Commands to the DRAM.
- Data Bus:
  - Signals are bi-directional and are Command bus driven by either the DRAM Chip (READ Command) or the Application processor (WRITE Command) at twice the speed of the clock signal.

DDR bus protocol allows signals to go idle, or tri-state when they are not active. When debugging or performing JEDEC conformance measurements on the DDR interface, it is necessary to perform certain measurements only on qualified portions of the signal acquired using an Oscilloscope, such as during Read or Write bursts or on bus transactions to a specific Rank.

Capturing and finding the correct sections of the waveform for analysis on the DDR interface is challenging; this requires collecting and sorting through thousands of acquisitions for the event of interest. Defining a trigger that isolates the desired event and shows only asserted signal states; speeds up the debug/characterization of the memory interface.

Tektronix Oscilloscope Capabilities for Memory Validation

Tektronix Oscilloscopes provide a variety of ways to trigger, isolate and capture events of interest making them an indispensable tool for debug, validation and characterization of memory interfaces. Some of the capabilities that are most useful for memory interface validation are Visual Triggering, Pinpoint Triggering, and Advanced Search & Mark. This document focuses on how the Visual Trigger capabilities on Tektronix Oscilloscopes can be used to setup different types of triggers in order to capture different events on the Memory Interface.

Visual Trigger

- Visual Trigger feature provides customized qualification of PinPoint hardware trigger events by using user-defined qualification areas drawn on the scope display. By discarding acquired waveforms which do not meet the graphical definition, Visual Trigger extends the oscilloscope's trigger capabilities beyond the traditional hardware trigger system.

Pinpoint® Triggering

- Tektronix PinPoint® trigger is the industry's highest performance scope trigger system. The PinPoint trigger system encompasses Dual A- and B-Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering apart from the usual range of threshold and timing related triggers.

Advanced Search & Mark

- Advanced Search & Mark (ASM) scans acquired waveform data for multiple occurrences of an event and marks each occurrence. Search and Mark extends across live channels, stored data and math waveforms. The results of ASM can be viewed in a table making it easy to navigate to a particular occurrence of the event in a long record.

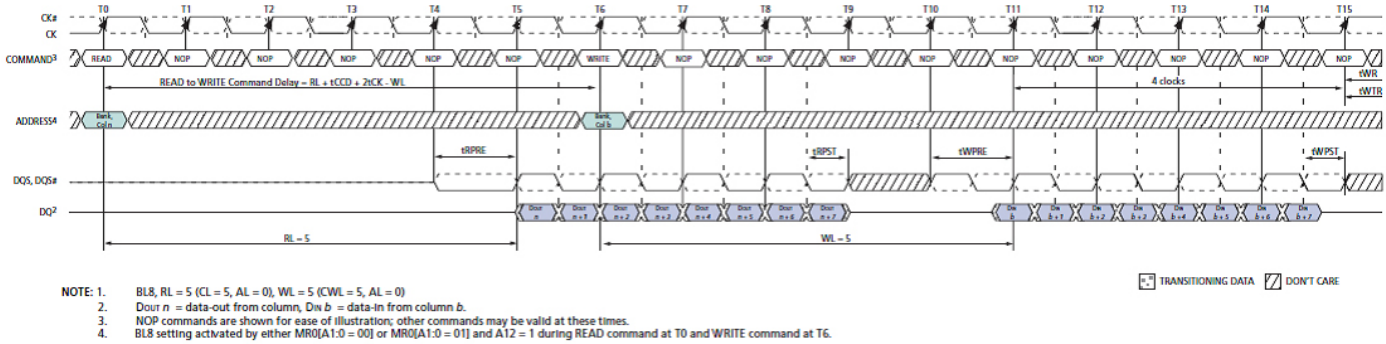
Advanced Search & Mark and Visual Trigger can be used in combination with PinPoint® triggering to trigger and isolate READ and WRITE bursts, detecting patterns as well as building eye diagrams of specific events. This document focuses on how these capabilities on Tektronix Oscilloscopes can be used to setup different types of triggers in order to capture different events on the Memory Interface.

Feature	Description
Number of areas	8
Area shapes supported	Rectangle, Triangle, Trapezoid, Hexagon, User Defined (48 vertices)
Area operations	Move, Resize, Duplicate, Flip, Rotate and add/delete/edit vertices
Area Colors	1 per channel
Long Record length and zoom	Supported
Triggers qualification	A, B, A+B, B event scan, trigger reset and trigger delay
Logic Operators	In/Out, AND, OR, XOR
Acquisition Modes	Real-time, Equivalent time
Programmable Interface	Yes
Save/Recall setup	All settings or only Visual Trigger
Supported Models	MSO/DPO/DSA70000C/D, DPO7000C, MSO/DPO5000

Table 1. Visual Trigger Capabilities.

Feature	Description
A-Event Trigger Types	Edge, Glitch, Runt, Width, Transition Time, Timeout, Pattern, State, Setup/Hold, Window, Selectable logic qualification up to 20 bits wide on MSO
B-Event Trigger Types	Same as A-Event Trigger Types
Trigger Sequences	Main, Delayed by Time, Delayed by Events, Reset by Time, State, Transition
Application Specific Triggers	Communication, Video, Serial Pattern, 8b/10b, Low Speed Standard Protocol Triggers
Search and Mark Events	Search glitches or runts, as well as transition rate, pulse width, setup and hold, timeout, window violations or find any logic or state pattern on any number of channels. Search DDR read or write bursts with Opt. DDRA.
Supported Models	MSO/DPO/DSA70000C/D, DPO7000C, MSO/DPO5000

Table 2. Pinpoint Trigger Capabilities.



NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout *n* = data-out from column, Din *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0 and WRITE command at T6.

Figure 1. DDR3 READ and WRITE operations.

Isolating Read and Write Bursts on the DDR3 Bus

DDR READ and WRITE operations are burst oriented. The burst length is programmed during initialization by writing to the appropriate bit fields in the MRS registers.

A READ or a WRITE operation begins with a READ or a WRITE command along with the Column Address targeted at the active open Row. After a delay specified by Read/ Write Latency, the Data appears as done but there are several differences in the signaling between the two cycles that can be used to quickly setup trigger conditions to isolate and trigger on bus events of interest.

In this white paper, DDR3 will be used as the example to illustrate the different types of Visual Triggering setups.

- Polarity of the DQS pre-amble
  - For DDR3 and LPDDR3, negative on READ vs. positive on WRITE
  - For DDR4, both READ and WRITE positive
- DQS and DQ phase alignment differences
  - Edge aligned for READ vs. Center aligned for WRITE
- CS for Qualification of Bus transactions to a specific rank
- READ/WRITE commands on the command bus
- Signal Amplitude vs. scope probe point location

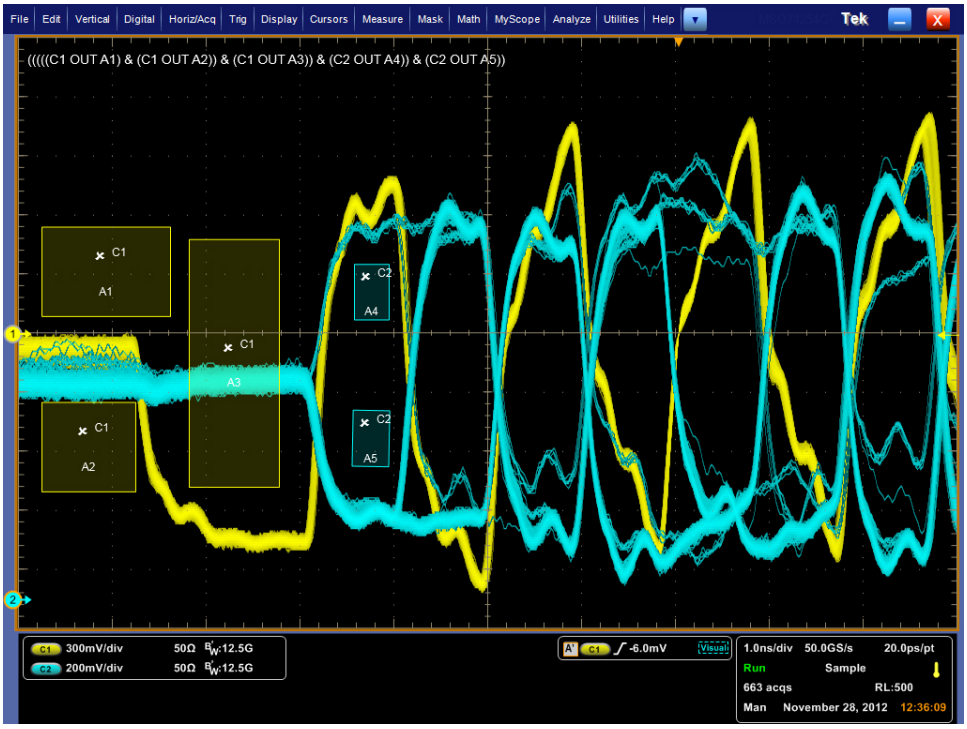


Figure 2. Read Burst.

Isolating Bursts Based on Pre-Amble Polarity and DQ/DQS Phase Alignment

In Figures 2 and 3, Channel 1 (Yellow) is DQS strobe and Channel 2 (Blue) is DQ data bit. A simple edge trigger is defined for the channel connected to the DQS strobe. Without any qualification, the hardware trigger will capture both Read and Write bursts. The user may configure screen areas to capture either Reads or Writes depending on which is desired.

To Trigger on READs (see Figure 2)

- Areas A1 and A2 are set so that when a signal is captured there is no DQS signal in these regions. This ensures that DQS is captured coming out of tri-state.
- Area A3 is set to filter out positive pre-amble events (Write), and only show negative polarity pre-amble events (Read).
- Areas A4 and A5 are set so that DQ signal does not to enter these regions, ensuring that the DQS and DQ are aligned.

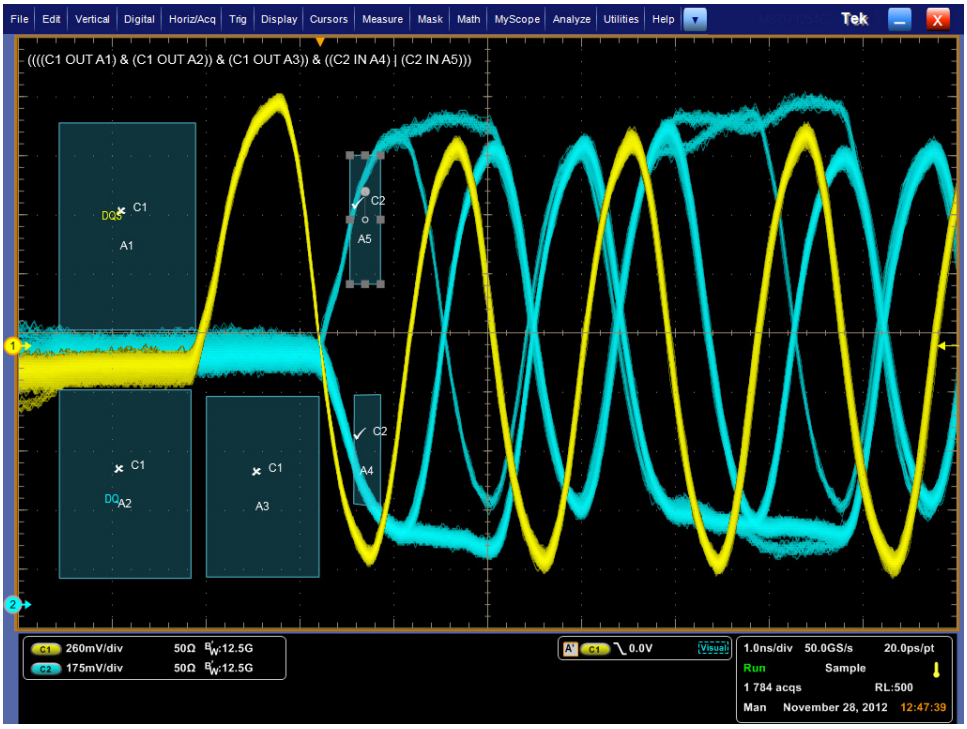


Figure 3. Write Burst.

To Trigger on WRITEs (see Figure 3)

- Areas A1 and A2 are set so that when a signal is captured there is no DQS signal in these regions. This ensures that DQS is captured coming out of tri-state.
- Area A3 is set to filter out negative pre-amble events (READ), and only show positive polarity pre-amble events (WRITE).
- Areas A4 and A5 are set so that DQ signal enters these regions, ensuring that the DQS and DQ are not aligned.

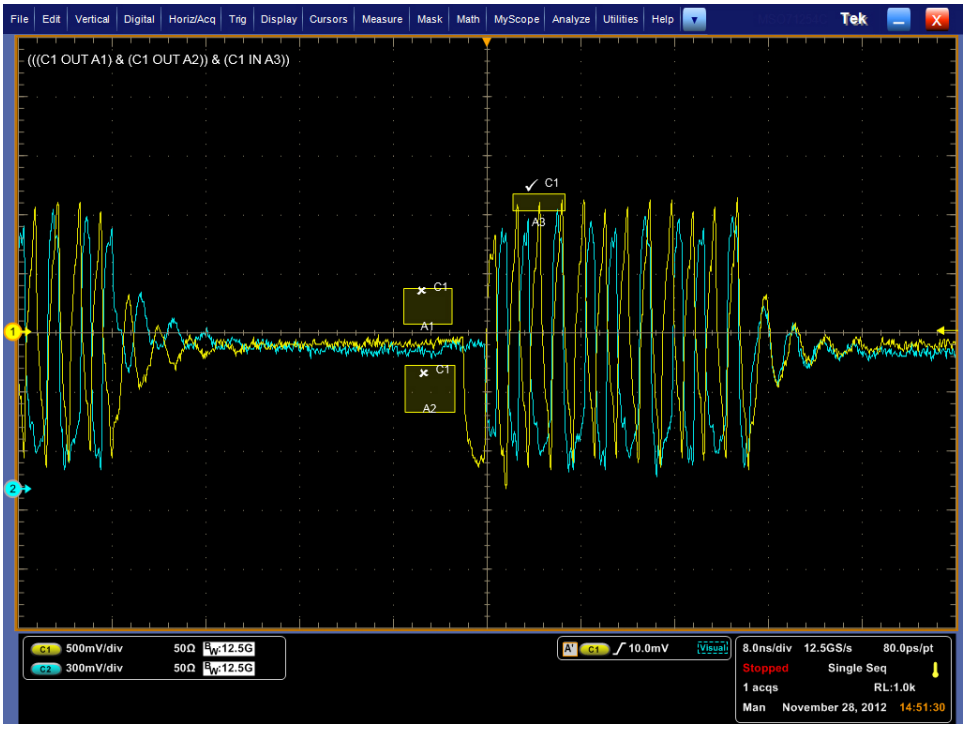


Figure 4. Read Burst based on Amplitude.

Isolating Read / Write Bursts Based on Amplitude

The application processor drives the DQ/DQS lines during WRITEs, and the DRAM memory drives the DQ/DQS lines during READs. The signals are usually probed as close as possible to the balls of the DRAM device. Due to this probing location, READs will have a higher amplitude compared to the WRITEs in this case. This difference in amplitude can be used to setup a Visual trigger to isolate READ from WRITE.

To Trigger on READs (See Figure 4)

- Areas A1 and A2 are set so that when a signal is captured there is no active DQS signal in these regions. This ensures that DQS is captured coming out of tri-state.
- Area A3 is set to “keep in” mode to detect higher DQS swing on the Read burst.

Because of higher amplitude on the Reads, DQS signals that do not pass through A3 (Writes) are filtered.

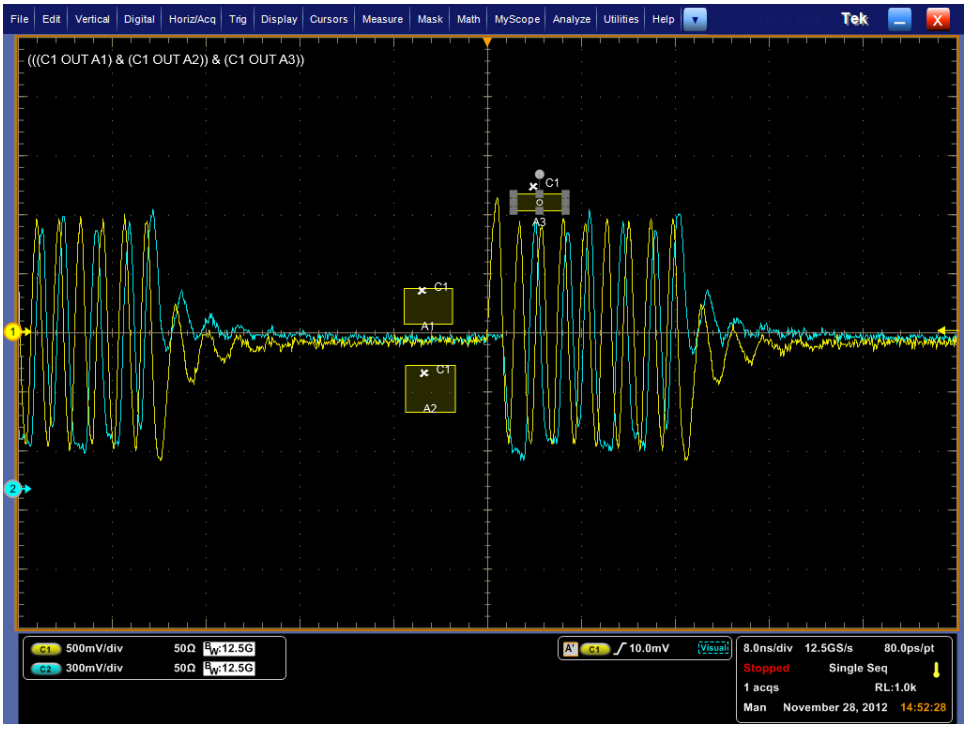


Figure 5. Write Burst based on Amplitude.

To Trigger on WRITEs (See Figure 5)

- Areas A1 and A2 is set so that when signal is captured there is no active DQS signal in these regions. This ensures that we capture signal coming out of tri-state.
- Area A3 is set to “keep out” mode to detect lower DQS swing on the Write burst.

Because of higher amplitude on the Reads, DQS signals that pass through A3 (Reads) are filtered.

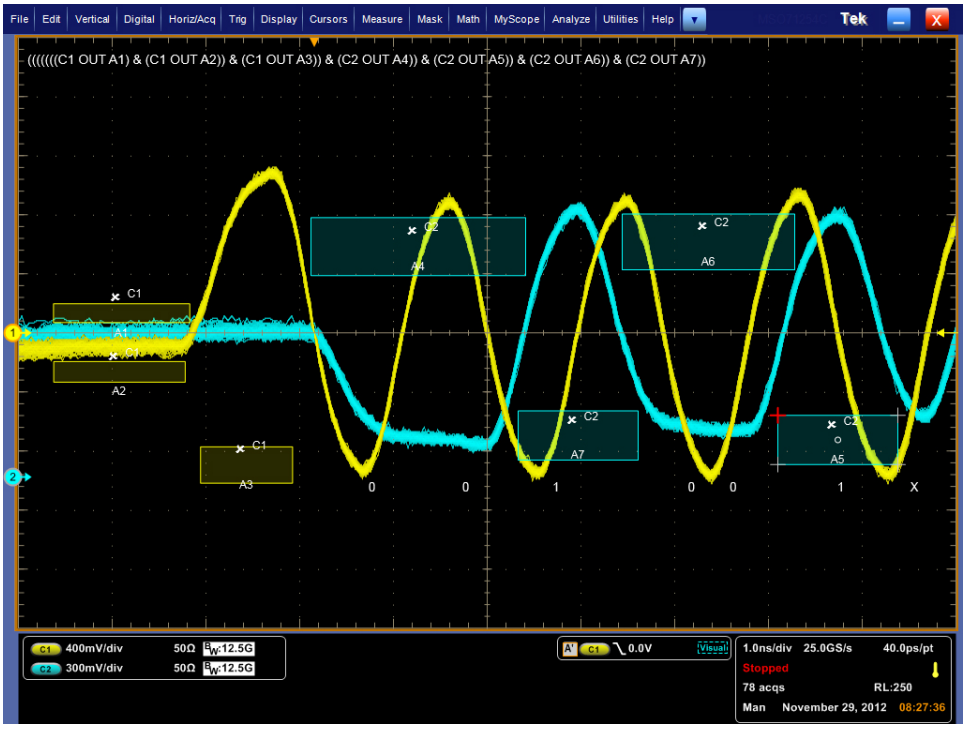


Figure 6. Visual Trigger for a Data pattern.

Isolating a Burst on a Specific Pattern

There are cases when it is necessary to trigger on and isolate a burst with a specific pattern such as debugging the crosstalk due to capacitive coupling on adjacent lines.

Figure 6 shows a Visual Trigger setup to isolate a Write burst with a DQ bit pattern of 001001X. The specific data pattern is defined using areas A4-A7 shown in blue. Figure 6 shows a capture based on the definition on the left.

Figure 7. Trigger on Data Pattern '11000000'.

Figure 8. Trigger on Data Pattern '01000001X'.

Figures 7 and 8 show the Visual Trigger custom shape feature, allowing the user to add additional vertices and move these vertices to make custom shapes. In both cases below, an “upper” and “lower” area have been created between which the DQ data signal must stay in order for the capture to be valid and thus shown on the display.

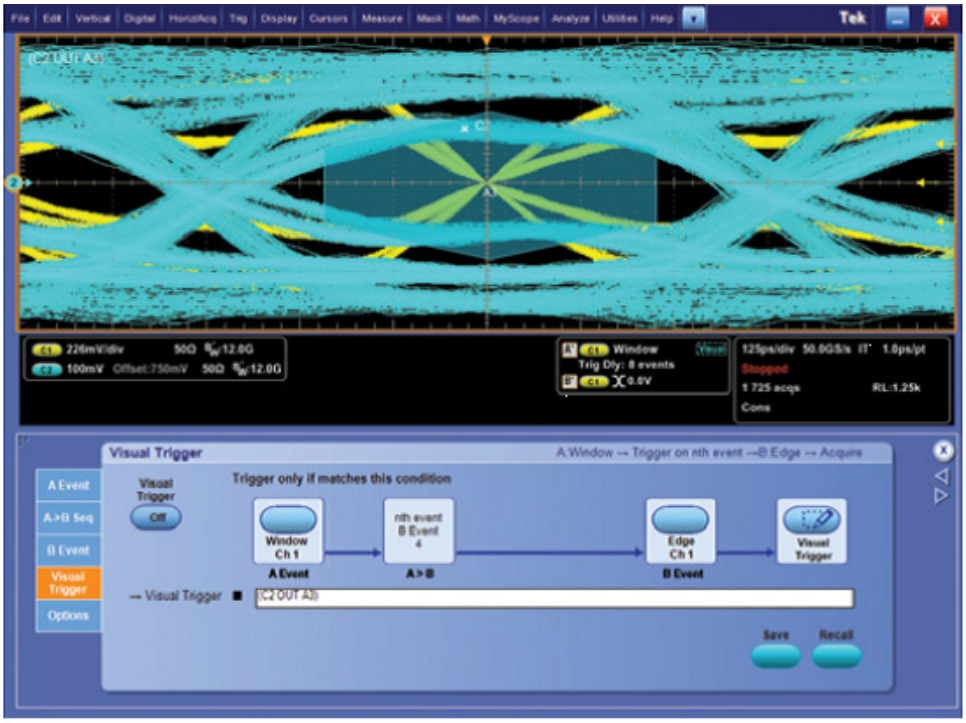


Figure 9. Eye Diagram before qualification.

Isolating Bursts Using the Digital Channels on the MSO

The digitals signals on the MSO can be connected to the command bus on the DDR interface and the digital pattern triggers can be setup to trigger the READ/WRITE commands. The information on the command bus acquired on the digital channels can be used for Isolating, Detecting, and Marking the bursts for further analysis.

Isolating and Rendering Eye Diagram Using Visual Trigger for Specific Rank

Visual Trigger can be helpful in distinguishing signals from multiple ranks or slots within a DDR memory array. Figure 9 is an eye diagram display of a DDR3 DQS strobe signal (Yellow) and DQ data signal (Blue). Because the DDR3 data and strobe lines are shared by multiple components on the bus, there are two distinct amplitude levels of both the strobe and data eyes. The higher amplitudes correspond to the target rank within the memory array, while the lower amplitudes correspond to another rank.

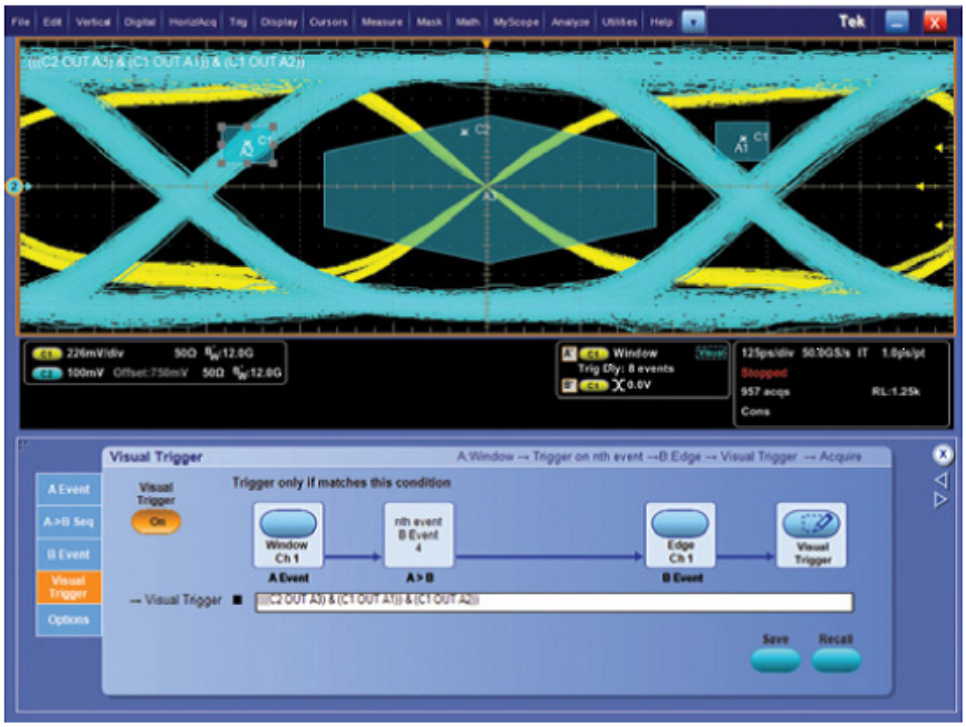


Figure 10. Eye diagram after Visual Trigger qualification.

In such a verification test, there is a need to acquire millions of data bits in the eye diagram, but only bits from the desired or target rank. To evaluate the eye diagrams of the target rank only, Visual Trigger is used to capture and display only the signals from the target rank.

As shown in Figure 10, square areas A1 and A2 are positioned to exclude the lower-amplitude strobe signals, and hexagonal area A3 is placed at the center of the eye and sized to exclude the lower-amplitude data signals. Using Visual Trigger, eye diagram analysis on the signals from the desired rank can be isolated and better targeted for analysis.

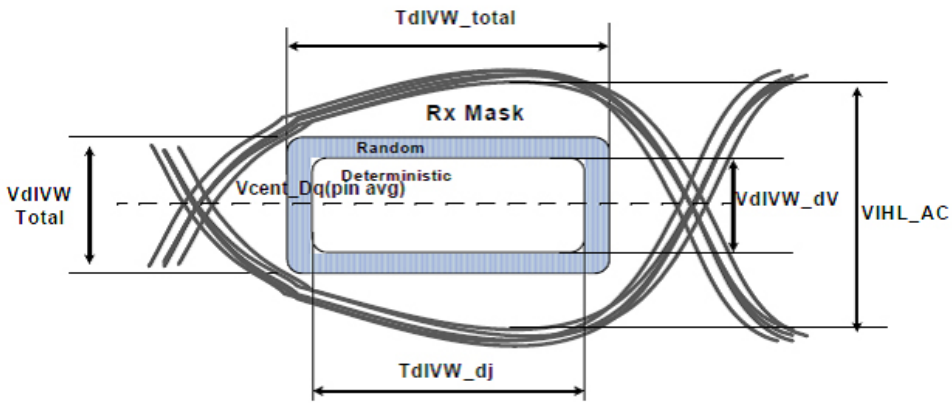


Figure 11. DDR4 mask based receiver testing.

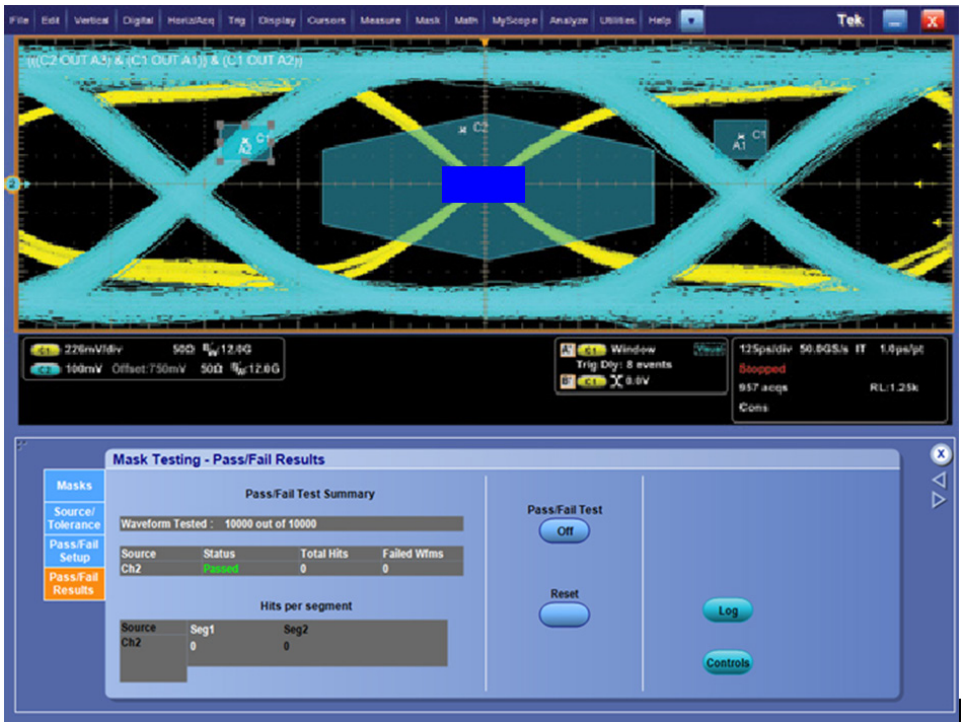
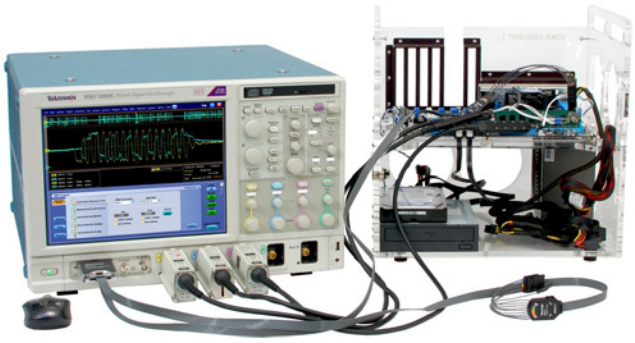


Figure 12. Built-in mask measurement capability.

For DDR4, JEDEC has specified a minimum mask area for DQ eye diagram specified at the input to the DRAM receiver (See Figure 11). The receiver mask defines the minimum area that the Write DQ signal must not encroach It is assumed that signals meeting the receiver mask will be correctly latched by the DRAM input buffers. The specification defines the mask size for each speed grade in the DDR4 Specification.

Once the persistence diagram is drawn for DQ with respect DQS, using the built-in mask measurement capability to measure PASS/FAIL results as well as margin can be obtained (see Figure 12).



Conclusion

The Visual Trigger capability on Tektronix Oscilloscopes take the action of isolating and capturing events of interest in order to root cause the reasons for failure on the memory interface to the next level. Combined with Pinpoint® triggering, Advanced Search & Mark and Visual Trigger provides unprecedented level of insight into signal behavior allowing isolation and analysis of hard to capture events of interest, eliminating hours of Oscilloscope setup time, capturing and manually searching through acquisitions thus speeding up debug and analysis of the Memory Interfaces.

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