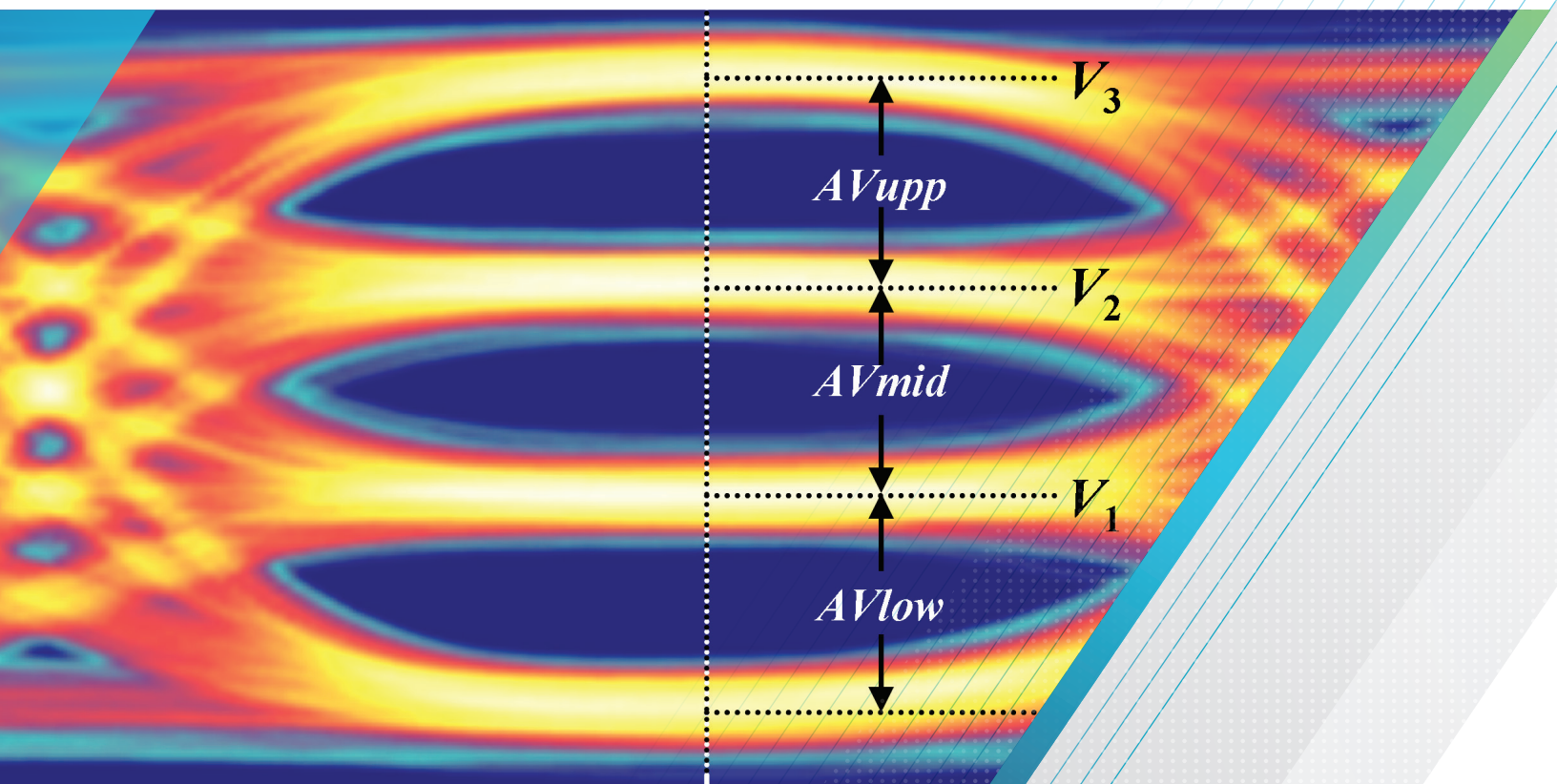


PAM4 Signaling in High Speed Serial Technology: Test, Analysis, and Debug

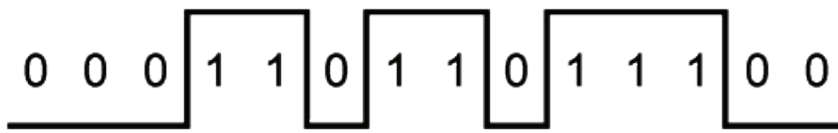
APPLICATION NOTE



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PAM2-NRZ



PAM4

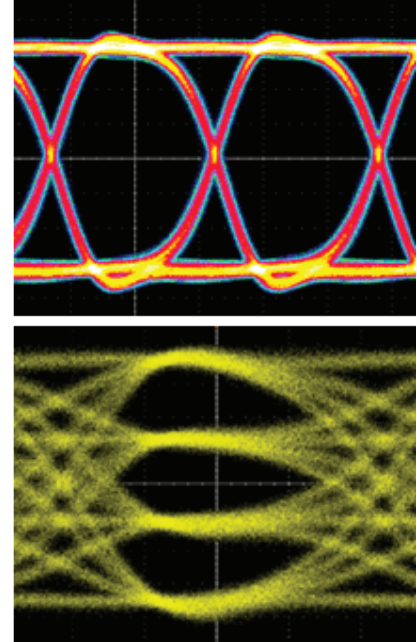
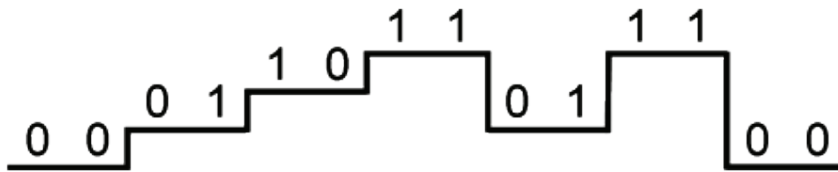


Figure 1. PAM2-NRZ and PAM4: baseband signaling and eye diagrams.

1. 4-Level Pulse Amplitude Modulation – PAM4

As serial data rates approach 56 Gb/s per channel, signal impairments caused by increasing bandwidth have compelled the high speed serial data industry to make a considerable shift in approach. Simple, baseband, NRZ (non-return to zero) signal modulation techniques are being left behind in favor of more bandwidth efficient PAM4 (4 level pulse amplitude modulation).

PAM4 cuts the bandwidth for a given data rate in half by transmitting two bits in each symbol, as indicated by Figure 1. We distinguish the PAM4 bit rate from its symbol rate, referred to as Bd (baud). For example, a 56 Gb/s PAM4 signal is transmitted at 28 GBd.

The abbreviation NRZ has been used informally to describe intuitive baseband high/low signaling, but the formal description is 2-level pulse amplitude modulation, or PAM2. Since PAM4 signals do not return-to-zero after each symbol, they are also an NRZ signaling scheme. In this paper, we'll refer to the two schemes as PAM2-NRZ and PAM4 to familiarize ourselves with the more accurate PAM2 terminology without any loss of clarity.

The eye diagrams in Figure 1 show that its multiple symbol levels make PAM4 more sensitive to amplitude noise than PAM2-NRZ. While PAM4 signals also suffer greater ISI than PAM2-NRZ at a given *baud* rate, they suffer much less at the same *data* rate. PAM4's greater resilience to ISI at a given data rate on lossy electrical channels like backplanes is the primary

reason for switching from PAM2-NRZ.

We'll see that PAM4 signal analysis borrows a great deal from the jitter and noise analysis developed for PAM2-NRZ and that PAM4 technology at 25+ GBd will continue to benefit from the innovations that got PAM2-NRZ so far: differential signaling, clock recovery, and equalization at both the transmitter and receiver.

Since fiber optic systems can operate above 25 Gbd with PAM2-NRZ the switch is less urgent—and this fact is reflected in the decreased rate of optical PAM4 development. For optical systems, the motivation to switch has to do with cost and power. Coherent modulation techniques, like DP-QPSK (dual-polarization quadrature phase shift key), can easily accommodate 50+ Gb/s signals across thousands of kilometers, but shorter reaches, like those within and between data centers, 500m-10 km, can be accommodated by optical PAM4 transceivers at a fraction of the cost and power consumption.

In this paper, we examine how PAM4 technology can be evaluated with emphasis on the performance requirements that enable SerDes and transceivers to operate and interoperate in PAM4 systems. In Section 2 we describe PAM4 technology for 50-400G applications. Section 3 goes into the details of PAM4 signaling, Section 4 and 5 cover electrical and optical transmitter evaluation, and Section 6 describes methods for evaluating PAM4 receivers. We conclude with a short discussion of the PAM2 PAM4 conversion and currently available analysis tools.

STANDARD		MEDIA	REACH	RATE	PRE-FEC BER
100 GbE	100GBASE-KP4	PCB	33 dB	4×13.6 GBd	≤ 10 ⁻⁶
400 GbE	400GBASE-FR8*	WDM SM	2 km	8×26.6 GBd	≤ 2×10 ⁻⁴
	400GBASE-LR8*	WDM SM	10 km	8×26.6 GBd	
	400GBASE-DR4*	4×SM	500 m	4×53 GBd	
OIF-CEI	CEI-56G-VSR*	PCB	100 mm host 50 mm module	19-29 GBd	≤ 10 ⁻⁶
	CEI-56G-MR*		500 mm	19-29 GBd	
	CEI-56G-LR*		1 m	19-29 GBd	

Table 1. Summary of expected PAM4 standards; those marked with an asterisk (*) have not been released as of September-2015. (Remember to refer only to the officially released specifications before making compliance tests!)

2. Emerging High Speed Serial PAM4 Technologies

As of September-2015, the only high speed serial PAM4 standard that has been released is IEEE 802.3bj 100 Gigabit Ethernet (GbE), 100GBASE-KP4. To reach 100 Gb/s total data rate, it combines four lanes at 13.6 GBd. The continued success of PAM2-NRZ has prevented extensive adoption of 100GBASE-KP4, but it provides a foothold for what we can expect from emerging PAM4 standards.

The so-far released and emerging PAM4 standards are summarized in Table 1.

Electrical PAM4 specifications will consist of multi-lane, hot plug, low voltage, balanced differential pairs with embedded

clocking and either transmitter or receiver equalization or both. Optical PAM4 can be used with SM (single mode) or MM (multi-mode) fibers—though MM poses extra difficulty. The length, or “reach,” of the lanes can be defined as physical distance or its engineering equivalent, loss and phase response.

Each standard applies to a particular purpose in a unique signal integrity environment. For example, 100 GbE has separate specifications for cables, backplanes, and both SM and MM fiber optics. In this paper, we quote ranges of performance parameters that span most applications guided by our experience in the field and ongoing contributions to the standards bodies. That said, prior to making any compliance test it is imperative that you double-check the specific interoperability standards that apply to the technology you’re developing!

	PAM2-NRZ	PAM4
Bits per symbol	1	2
Symbol levels	2	4
Rising/falling edges	2	6
Distinct transitions	2	12
Eye diagrams per UI	1	3
Average transition density	50%	75%

Table 2. Comparison of PAM2-NRZ and PAM4 signal traits.

3. Properties of PAM4 Signals

Table 2 and Figure 2 compare characteristics of PAM4 and PAM2-NRZ signals. If you’ve never drawn a PAM4 eye diagram, it’s a simple and effective way to grasp the complexity of PAM4’s four separate symbol levels, six rising and falling edges, twelve distinct transition possibilities, and four different non-transitions. Even the 50% bit transition density of PAM2-NRZ changes to 75% PAM4 symbol transition density.

Each of the PAM4 levels are specified as mean voltages, V_A , V_B , V_C , and V_D , for electrical signals and mean power for optical, P_A , P_B , P_C , and P_D . The four symbols are referred to as level 0, level 1, level 2, and level 3—so that the sequence shown in Figure 1 is described as {0, 1, 2, 3, 1, 3, 0}. Some of the literature also refers to them as {-3, -1, 1, 3} or {-1, -1/3, 1/3, 1}. As the technology evolves, the notation will converge. We’ll use {0, 1, 2, 3} in this paper.

Since PAM4 signals have four levels, they have three interdependent eye diagrams, Figure 3—interdependent because transitions from one symbol to another can affect more than one eye. Since noise affects each eye independently, PAM4 signals are at least three times more sensitive to amplitude noise than PAM2-NRZ. Each of the three eye diagrams can be analyzed the way that PAM2-NRZ eyes are analyzed. That is, we can measure EW (eye width) and EH (eye height) defined with respect to a BER separately for the lower, middle, and upper eye diagrams.

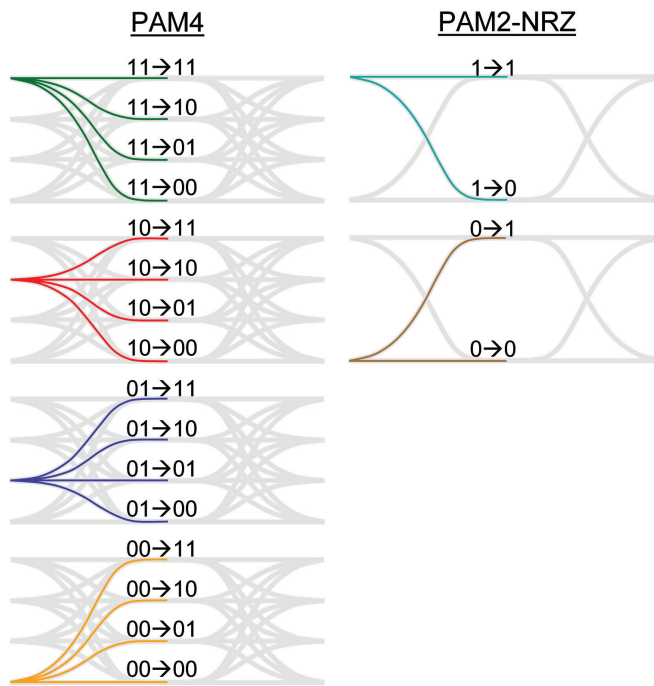


Figure 2. Properties of PAM4 signals.

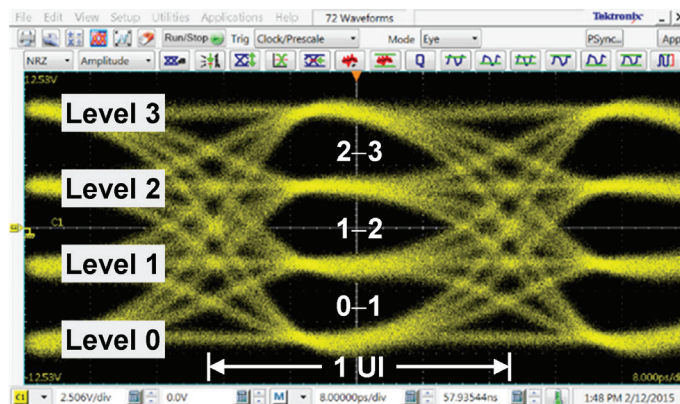


Figure 3. Some notation for PAM4 eye diagrams.

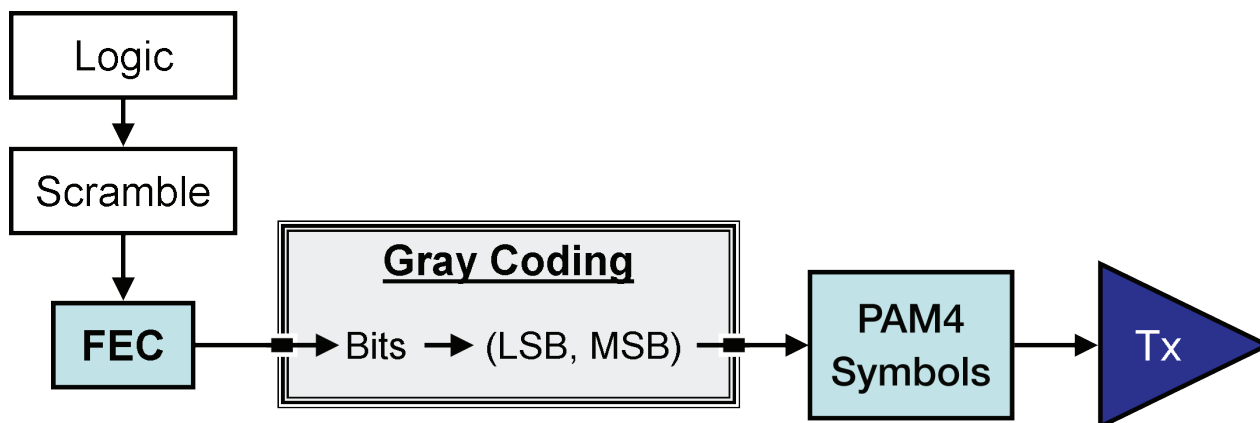


Figure 4. The Gray coding conversion from logic “bits” to FEC encoded PAM4 symbols.

3.1 FEC and Gray Coding

The increased impact of signal-to-noise ratio on PAM4 signals demands FEC (forward error correction). FEC allows the maximum uncorrected BER (bit error rate) to be increased to 10^{-6} for electrical signaling and even higher for optical. From the test perspective, this relaxed BER constraint is a huge advantage because it allows us to measure pre-FEC performance down to $BER \sim 10^{-6}$ in seconds. In the past, it either took a large fraction of an hour to reach down to $BER \sim 10^{-12}$ – 10^{-15} or we had to use risky extrapolation techniques.

Figure 4 shows how FEC encodes binary logic into a set of data bits that include the overhead of FEC’s parity-like bits. The resulting bit stream is then *Gray coded* and then formatted into the PAM4 symbols that are transmitted. The received data stream is Gray decoded back into a bit stream. This bit stream is then processed by FEC which is capable of correcting a limited number of bit errors.

The FEC schemes adopted for PAM4 are likely to require more overhead than the scheme used for PAM2-NRZ. For example, 100 GbE’s PAM4 100GBASE-KP4 standard uses the Reed-Solomon FEC scheme RS(544, 514) whereas its PAM2-NRZ counterparts all use RS(528, 514). RS(544, 514) can correct up to 150 bit errors, more than twice the capability of RS(528, 514) but with a corresponding increase in overhead.

The way that Gray coding combines the MSB (most significant bit) and LSB (least significant bit) in each PAM4 symbol assures that symbol errors caused by amplitude noise are more likely to cause one bit error than two. On the other hand, jitter is more likely to cause two bit errors per symbol error. In any case, the standards could specify either minimum acceptable BER before FEC or a raw SER (symbol error rate). In this paper, we follow the current practice of requiring minimal BER prior to FEC.

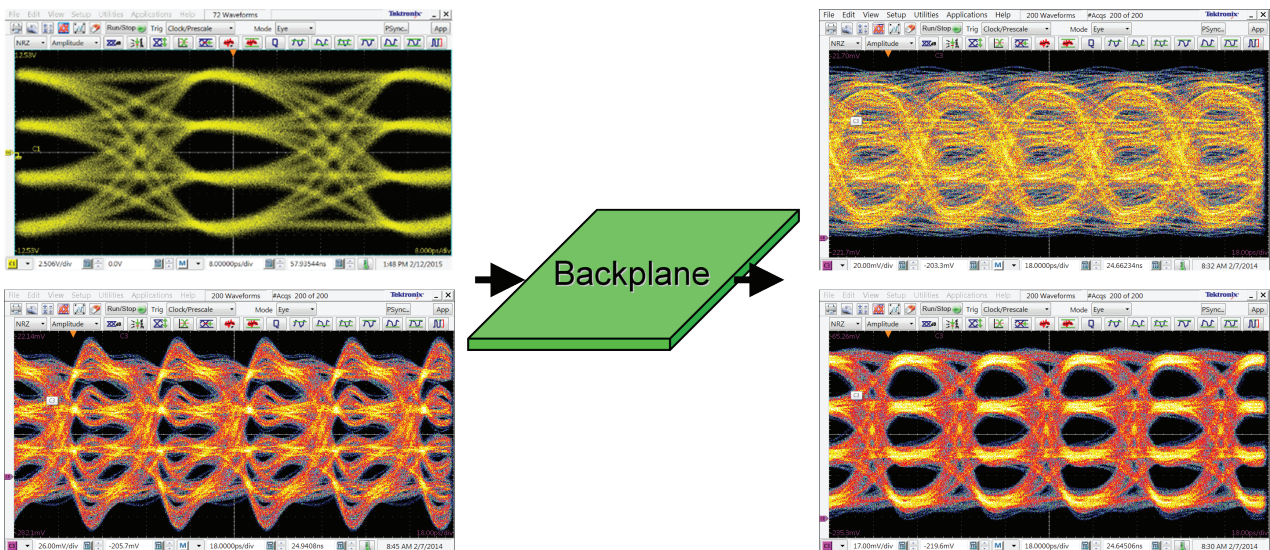


Figure 5. PAM4 eye diagrams prior to and after propagating through a backplane, top without transmitter FFE and, bottom, with transmitter FFE.

3.2 Equalization in PAM4 Systems

To open eye diagrams that have been closed by ISI, PAM4 systems must employ equalization. ISI is caused by the low-pass nature of the channel frequency response. Transmitter FFE (feed-forward equalization), which includes pre- and de-emphasis, and passive CTLE (continuous time linear equalization) at the receiver are techniques that boost the high frequency components of the waveform relative to its low frequency components in an effort to invert the effect of the channel. Unfortunately, increased high frequency content also aggravates crosstalk. DFE (decision feedback equalization) at the receiver is a nonlinear technique that helps invert the channel response but without amplifying crosstalk.

Figure 5 shows the eye diagram of a signal with 2 “taps” of transmitter FFE, i.e., de-emphasis. The voltage levels of symbols prior to transitions are boosted by a constant factor relative to the voltage levels of non-transition bits.

The de-emphasis concept is easily generalized to longer FFE filters. Symbol voltage levels are called “cursors” and their correction factors are constants called “taps.” Cursors that precede the bit being transmitted, $C(n)$, are called pre-cursors, e.g., $C(n-1)$, and those that follow are called post cursors, e.g., $C(n+1)$. Each cursor is multiplied by a tap and taps are chosen so as to cancel the frequency response of the channel to as great an extent as possible. Studies of PAM4 systems have shown little benefit to use of more than 3 taps, so we expect most 13+ GBd PAM4 systems to require 3 taps of transmitter FFE.

Since CTLEs are passive filters, they’re no different in PAM4 systems than in PAM2-NRZ systems, but with four symbol levels, the decisions that PAM4 DFEs feedback are more complicated.

While all three equalization techniques, transmitter FFE, CTLE, and DFE, are often combined to mitigate ISI in PAM2-NRZ systems, most PAM4 systems use only one or two of them: transmitter FFE or CTLE or FFE + DFE or CTLE + DFE, that is, (FFE XOR CTLE) OR DFE.

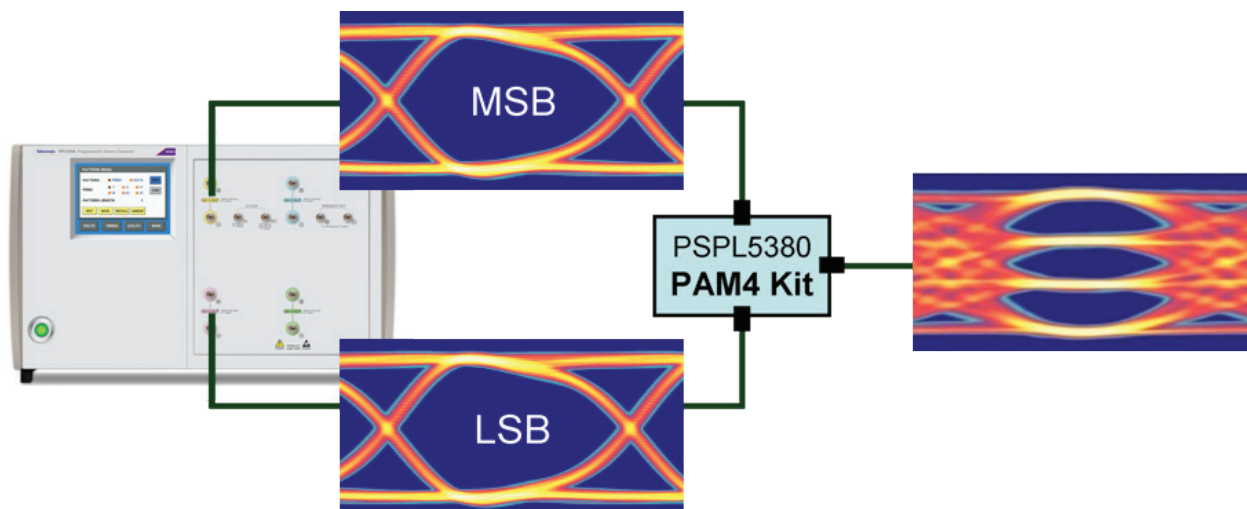


Figure 6. Generating PAM4 signals by combining two PPG channels.

3.3 PAM4 Test Signals

The PAM4 version of a PRBS n (pseudo-random binary sequence) pattern is called a quarternary PRBS pattern, QPBRBS n .

PRBS n patterns include 2^n-1 bits, every permutation of n consecutive bits. QPRBS n patterns are assembled by Gray coding a PRBS n pattern and its inverse. The inverse is included for balance, resulting in QPRBS n patterns with $2n$ symbols.

For example, QPRBS13 includes 8191 PAM4 symbols. For 100 GbE PAM4 100GBASE-KP4, a modified version of the QPRBS13 pattern is used that is composed of 15,548 symbols that include 338 training frame words.

Most transmitter tests should be performed with either a QPRBS9 or a QPRBS13 test pattern. Receiver tests should be set up and calibrated with QPRBS13 but performed with QPRBS31.

Figure 6 shows how PAM4 test patterns can be generated by combining the output of two channels of a Tektronix PatternPro [PPG3202](#) pattern generator with our [PSPL5380](#) PAM4 Kit. One PPG channel transmits the LSB and the other transmits the MSB. The LSB has half the amplitude of the MSB so that when the two are combined with an RF power divider, we get a proper PAM4 signal.

Electrical PAM4 Signaling & Transmitter Performance Parameters		
Baud rate	100GBASE-KP4 13.6 GBd	19-29 GBd PCB*
Differential peak-to-peak voltage	1200 mV	800-1200 mV
Level separation mismatch, R_{LM}	≥ 0.92	≥ 0.92
Clock RJ (CRJ_{rms})	≤ 0.005 UI	≤ 0.005 UI
Clock DJ (CDJ_{pp})	≤ 0.05 UI	≤ 0.05 UI
Even-odd jitter	≤ 0.019 UI	≤ 0.019 UI
Signal-to-noise-distortion-ratio (SNDR)	≥ 31 dB	≥ 31 dB
EW6		≥ 0.25 - 0.4 UI
EH6		≥ 50 - 120 mV
Eye linearity		≤ 1.5
VEC		≤ 5.8 dB
BER	$\leq 10^{-6}$	$\leq 10^{-6}$

Table 3. Performance criteria for electrical PAM4 signals and transmitters. *Since no 19-29 GBd standards have been released, please think of these as unofficial estimates. Ranges of values indicate how the parameters can differ according to application. Refer to the officially released specifications before making compliance tests.

4. Evaluating Electrical PAM4 Transmitters

Table 3 provides sample performance parameters. The range of values indicates the variation in performance requirements for different electrical subsystems: SerDes to SerDes, SerDes to transceiver, transceiver to SerDes and across different lengths of PCB, circuits, and backplanes.

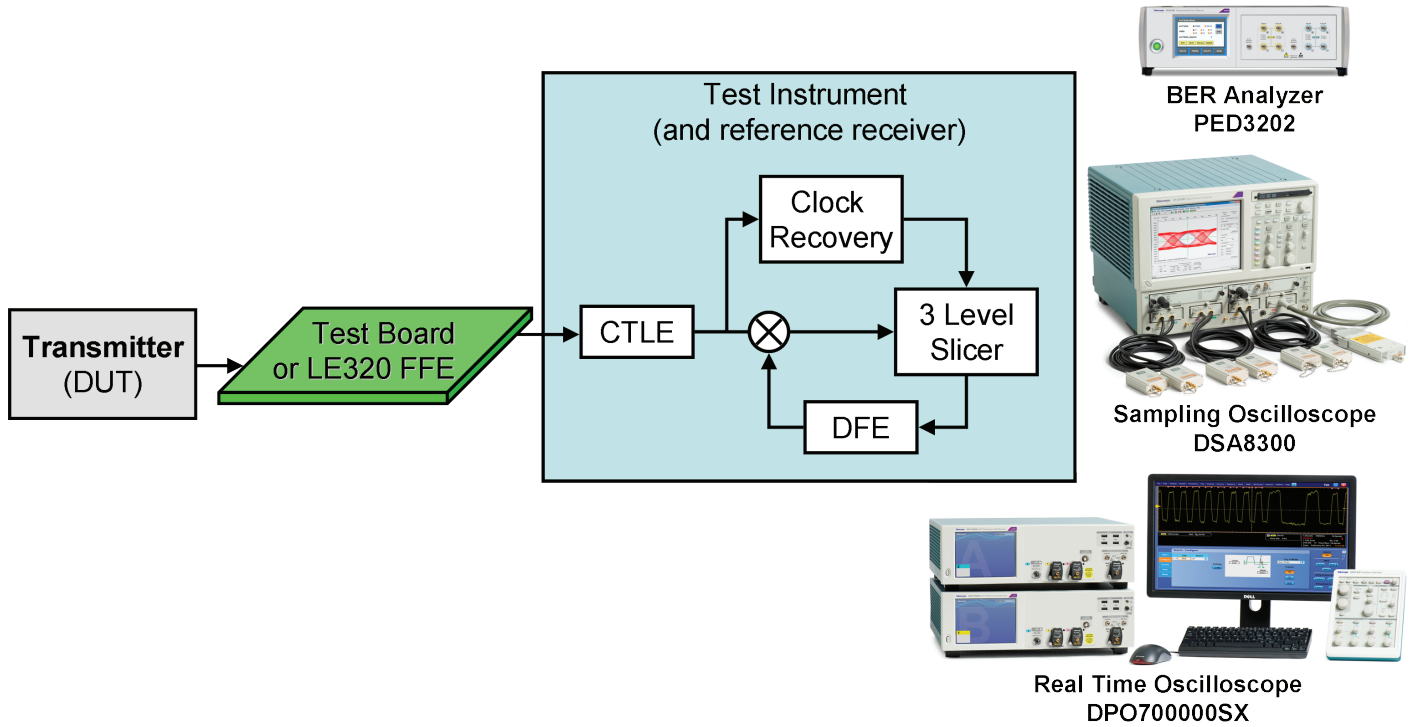


Figure 7. Electrical transmitter test setup.

Transmitter analysis, Figure 7, requires an instrument-quality reference receiver that doubles as a signal analyzer, like Tektronix's [DPO70000SX](#) 70 GHz bandwidth real time oscilloscope, [DSA8300](#) equivalent-time sampling scope, or our PAM4 BERT (bit error rate test) system [PED3202](#) Error Detector with PAM4DEC. In any case, the reference receiver should apply a fourth-order Bessel-Thomson filter with a bandwidth of about $1.25 \times f_b$ (depending on the application), where f_b is the symbol rate.

Many of these measurements are automated by Tektronix PAM4 analysis packages, but since PAM4 technology is still evolving, contact your [Tektronix representative](#) for an up to date list of automated measurements.

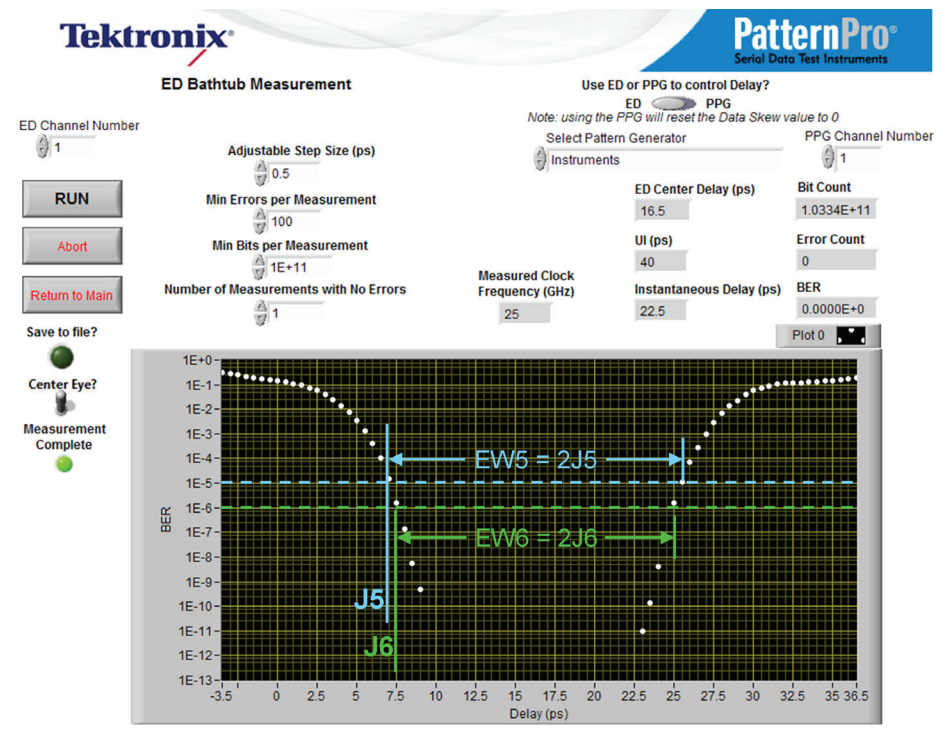


Figure 8. Extracting J5 and J6 from BER(*t*), the bathtub plot, from the test transmitter transmitting the JP03A clocklike pattern.

4.1 Transmitter Jitter: CRJ_{rms} and CDJ_{pp}

Measure *clock* jitter with a simple test pattern called JP03A: a clock-like sequence of alternating {0, 3} symbols.

By measuring CRJ_{rms} (rms clock random jitter), and CDJ_{pp} (clock deterministic jitter), on this clocklike square wave pattern, we can evaluate transmitter jitter independent of correlation to symbol sequences in the data; that is, we avoid contamination by ISI but retain random noise and other uncorrelated impairments like PJ (periodic jitter) and EMI (electromagnetic interference).

Measuring CRJ_{rms} and CDJ_{pp} requires two quantities called J5 and J6 that are related to the total jitter defined at BER=10⁻⁵ and 10⁻⁶, respectively. J5 and J6 are easy to extract from a bathtub plot, BER(*t*), where *t* is the time-delay position of the sampling point, Figure 8. J5 is the time interval that contains all but 10⁻⁵ of the distribution and J6 is the interval that covers all but 10⁻⁶ of the distribution.

The dual-Dirac model gives

$$TJ(BER=10^{-5}) = 8.83 \times CRJ_{rms} + CDJ_{pp}$$

$$TJ(BER=10^{-6}) = 9.78 \times CRJ_{rms} + CDJ_{pp}$$

and we get

$$CRJ_{rms} = 1.05 \times J6 - 1.05 \times J5$$

$$CDJ_{pp} = -9.3 \times J6 + 10.3 \times J5$$

Configure a JP03A clock-like pattern on the transmitter being tested. Make sure that your test equipment is equipped with clock recovery appropriate for your application. The current industry standard is the same 10 MHz PLL (phase locked loop) bandwidth used for 100 GbE's 25.78125 Gb/s PAM2-NRZ signals.

If you're using a real time scope, then the clock recovery can be emulated in software; if you're using a sampling scope, clock recovery is performed by the [82A04B](#) Phase Reference Module; if you're using an error detector, the PAM4DEC performs clock recovery.

Typical performance criteria restrict CRJ_{rms} < 0.005 UI and CDJ_{pp} < 0.05 UI. Remember, since CRJ is reported as an rms value, 0.005 UI of CRJ_{rms} closes the eyes about the same amount as 0.05 UI of CDJ_{pp}.

The combined clock jitter should not close the eye more than 10% at BER=10⁻⁶.

4.2 Even-Odd Jitter, EOJ

To measure EOJ, it's important that the test pattern include two pairs of consecutive identical symbols. The JP03B test pattern consists of 15 alternating {0, 3} symbols followed by 16 alternating {3, 0} symbols. Picture a {3, 3} sequence in the center of the pattern and a {0, 0} sequence as the end of one pattern connects to the beginning of the next.

EOJ is the difference between the average deviations of even-numbered and odd-numbered logic transitions. It is a type of DCD (duty-cycle distortion).

Remove uncorrelated noise and jitter by averaging the waveform. The JP03B waveform is 62 UI in length with 60 transitions. To calculate EOJ, measure the average widths of the 40 even pulses displaced from the double-width pulses by 10 UI. Then measure the average width of the 40 odd pulse widths similarly separated from the double-width pulses by 10 UI. EOJ is the difference between the averaged even and odd pulse widths.

Very little duty cycle distortion in the form of EOJ should be accepted of a high performance transmitter; expect the standards to require less than 0.02 UI of EOJ, perhaps as low as 0.015UI.

4.3 Signal to Noise and Distortion (SNDR)

Signal-to-noise-and-distortion ratio (SNDR) compares the signal strength to the combined random noise and harmonic distortion. SNDR is independent of insertion loss effects, like ISI, but includes all other sources of transmitter noise and distortion.

SNDR is derived from a linear fit to the transmitter pulse response with all transmitter lanes enabled and with each lane operating with identical transmitter FFE settings.

A linear fit is performed on an averaged QPRBS9 waveform, $w(k)$; where k runs from 1 to the product of the number of samples per symbol, at least 8, and the length of the test pattern, 512 for a QPRBS9. The fitted pulse response is given by $p(k)$ and the sample-by-sample fit error is given by $e(k) = p(k) - w(k)$.

SNDR is given by

$$SNDR = 10 \log \frac{P_{\max}^2}{\sigma_e^2 + \sigma_n^2}$$

where p_{\max} is the maximum of the fitted pulse response, $\max\{p(k); \text{ for all } k\}$, σ_e is the standard deviation of the fit error, $e(k)$, and σ_n is the rms deviation of the mean voltage. The maximum of the pulse response provides the signal magnitude. Since σ_e measures deviations in the fit to an averaged waveform, it accounts for harmonic distortion. The rms deviation of the mean voltage, σ_n , should be measured on a run of at least eight consecutive identical symbols; it accounts for random noise.

A transmitter of reasonable quality should have a healthy SNDR margin, certainly $SNDR \geq 31$ dB.

4.4 Level Thickness

Level thickness measures the average width of the four symbol levels due only to channel response and equalization; that is, due to the ISI and DCD that remain after equalization.

Remove signal impairments that are uncorrelated to the test pattern or data signal, like random noise, EMI (electromagnetic interference), and crosstalk, by averaging the eye diagram. Now calculate the standard deviations of each voltage rail, σ_i , by projecting vertical histograms around the narrowest parts of the rails.

$$\text{Level Thickness} = \frac{1}{4} \left(\sum_{i=0}^3 \frac{\sigma_i}{V_{pp}} \right) \times 100\%$$

where V_{pp} is the average swing voltage between the extreme symbols 0 and 3.

Level thickness is the average of the crest factors of the four symbol rails. It measures equalization effectiveness.

4.5 PAM4 Eye Height, EH6, and Eye Width, EW6

Eye height and eye width are the post-equalization eye opening measured with respect to BER along the vertical and horizontal axes. That is, EH6 is the vertical distance across the BER=10⁻⁶ contour—the “height” of the eye opening at BER=10⁻⁶; naturally, it’s measured in volts. Similarly, EW6 is the horizontal distance across the BER=10⁻⁶ contour and is measured in UI or ps.

The idea is to put transmitters in systems with lossy, ISI-inducing channels and crosstalk but with instrument-quality reference receivers. EH6 and EW6 are measured on all three PAM4 eyes after they’ve been opened by the appropriate combination of transmitter FFE, receiver CTLE, and/or DFE.

4.5.1 Apply Prescribed ISI Levels

To put your transmitter in a realistic setting, the signal has to propagate through a channel with appropriate insertion loss. Figure 9 shows examples of IL(*f*), or equivalently, S_{DD12} for two typical applications. The required insertion loss response can be achieved with either compliance test boards whose IL(*f*), has been calibrated and double-checked or with an appropriately adjusted FFE filter, like Tektronix’s [LE320](#) FFE (linear feed forward equalizer)—just as transmitter FFE can invert a channel’s frequency response, so can an FFE filter apply the equivalent frequency response.

PAM4 transmitters should have at least 3 taps of de-emphasis/FIR equalization. Optimize the taps as well as possible, within the restrictions of the technology standard, to compensate for the test channel’s loss and ISI.

Connect the output of the filter/compliance board to a reference receiver oscilloscope or BER analyzer. The reference receiver should include clock recovery with the appropriate bandwidth, e.g., 10 MHz. Set the CTLE peaking value to half the symbol rate frequency, $\frac{1}{2}f_b$ (a.k.a., the signal’s fundamental harmonic). The gain has integral values from 1 to 9 dB, Figure 10, set it at the value that optimizes the resulting eye diagram.

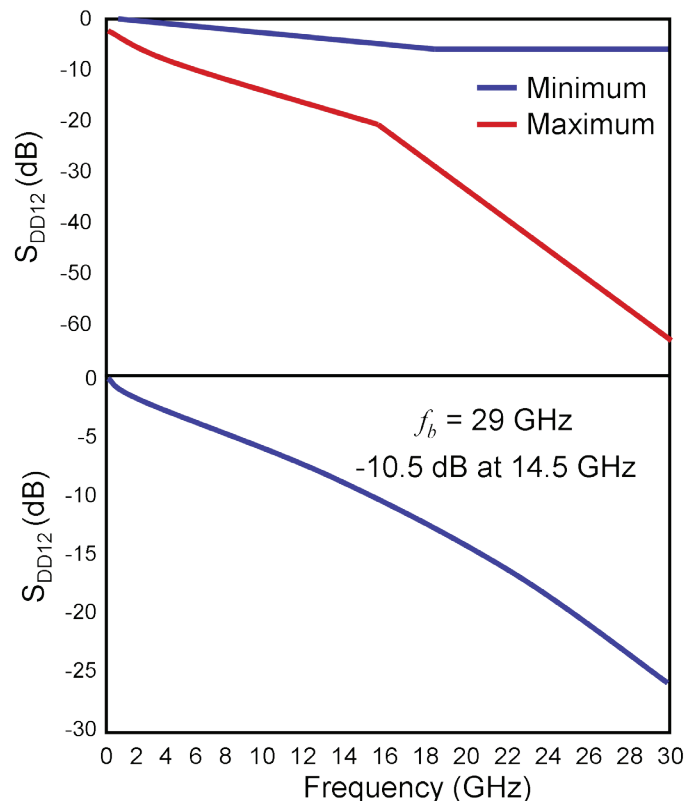


Figure 9. Examples of insertion loss response, IL(*f*) or S_{DD12}, for compliance test boards/ISI stressors.

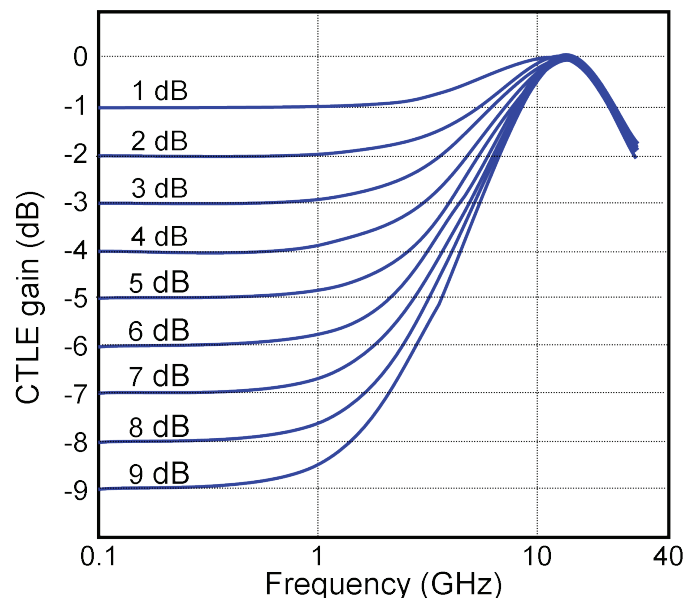


Figure 10. CTLE frequency response.

4.5.2 Apply Crosstalk

To include all reasonable sources of crosstalk interference, measure EH and EW with every system channel active in both directions. To prevent unrealistic data-dependent interference, patterns on the crosstalk channels should differ from the test signal pattern. If it's not possible for each aggressor to transmit a unique pattern, introduce sufficient delay between them so that the patterns aren't synchronized.

Setting the right levels of crosstalk can be tricky.

Compliance tests are likely to specify required levels of the somewhat arcane parameter, ICN (integrated crosstalk noise). ICN includes both NEXT (near end crosstalk) and FEXT (far end crosstalk) and is derived by combining measurements of the S-parameters for both the victim and crosstalk channels with specified aggressor signal amplitudes. ICN is given by

$$ICN \equiv \sigma_x \sqrt{\sigma_{NEXT}^2 + \sigma_{FEXT}^2}$$

where the calculated contributions from all NEXT and FEXT are weighted according to the receiver frequency response. A reasonable level of ICN is about 3 mV.

FEXT (also called MDFEXT for multi-disturber FEXT) should be about 3 times larger than NEXT; expect totals of about 1.3 mV rms NEXT and 3.5 mV rms FEXT. The latter value, 3.5 mV does not contradict the 3 mV ICN value because ICN includes the filtering effect of clock recovery.

The cumulative rms crosstalk amplitude of all NEXT and FEXT aggressors as measured on the victim lane, should be less than but close to 3.9 mV.

4.5.3 Measure EH6 and EW6

We refer to PAM4's three eye diagrams as low, middle, and upper. EH6 and EW6 are measured on each of the three. Since the smallest of each set, $\min(EW6_{low}, EW6_{mid}, EW6_{upp})$ and $\min(EH6_{low}, EH6_{mid}, EH6_{upp})$, limit transmitter performance, they are used as benchmarks.

Collect sufficient data to construct BER=10⁻⁶ contours.

Since there are three eye diagrams, we have to make some assumptions about the structure of the logic decision circuit. Ultimately, PAM4 receiver designers may implement three independent slicers, each with its own time-delay sampling point. The first PAM4 applications will use three slicers with a common time-delay sampling point, t_{center} , defined as the center of the middle eye.

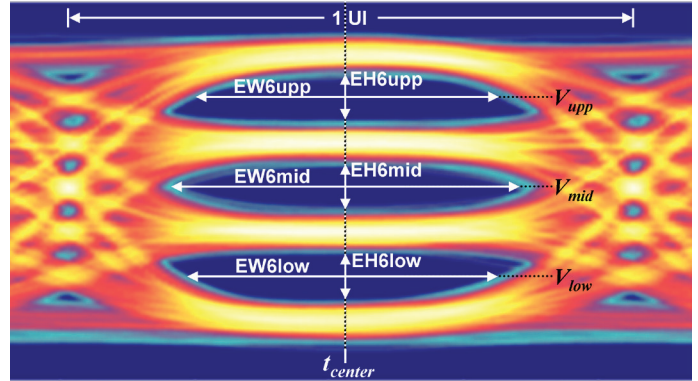


Figure 11. Measurement of EH6 and EW6 for each eye from the BER = 10⁻⁶ contours, definition of eye center and nominal slice thresholds, V_{low} , V_{mid} , and V_{upp}

To determine t_{center} , find the maximum EW6 for the middle eye as in Figure 11. Now bisect the line across the BER=10⁻⁶ contour that defines EW6mid. This vertical line is defined to be the PAM4 eye center, t_{center} .

The vertical eye openings for each eye, EH6low, EH6mid, EH6upp, are measured at the same time-delay, t_{center} . The vertical centers of the eyes—let's call them V_{low} , V_{mid} , and V_{upp} —are given by the midpoints of EH6low, EH6mid, EH6upp. V_{low} , V_{mid} , and V_{upp} also serve as the three nominal voltage slicer thresholds.

Notice that the somewhat arbitrary choice of defining the center of the eye by the midpoint of EW6mid, it's possible for the lower and upper eyes to be asymmetric about that center.

The three nominal eye centers are therefore given by (t_{center}, V_{low}) , (t_{center}, V_{mid}) , and (t_{center}, V_{upp}) .

Since the system BER is limited by the lowest performing signal, the standards will specify minimum acceptable values for:

$$EW6 = \min(EW6_{low}, EW6_{mid}, EW6_{upp}) \text{ and}$$

$$EH6 = \min(EH6_{low}, EH6_{mid}, EH6_{upp}).$$

Depending on application, after any receiver equalization, satisfactory transmitters should be capable of about:

$$EW6 \geq 0.25 \text{ UI and } EH6 \geq 50 \text{ mV.}$$

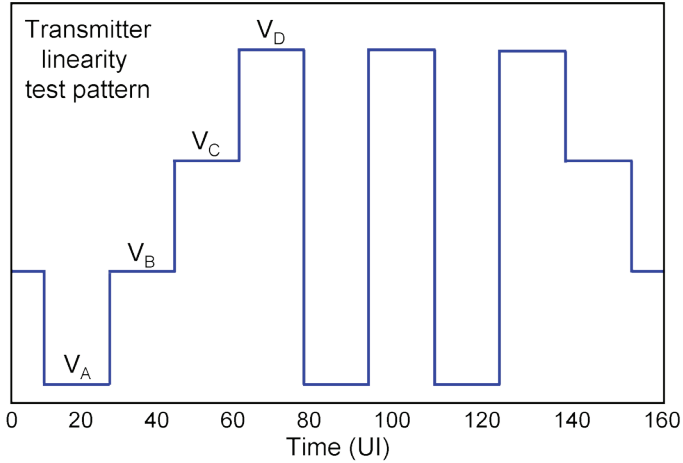


Figure 12. Transmitter linearity test pattern; each symbol level is maintained for 16 consecutive identical symbols.

4.6 PAM4 Eye Linearity

The relative dimensions and orientations of PAM4’s three eye diagrams present new challenges.

Different parameters are emerging to quantify variations in the centers, levels, heights, and widths of each eye. The technology has not converged, though an obvious transmitter design goal is to assure that each eye contributes equally to the BER.

In this section we present different approaches to analyzing nonlinearities in the vertical distributions of the three eyes.

4.6.1 Level Separation Mismatch Ratio, R_{LM}

The level separation mismatch ratio, R_{LM} , indicates the vertical linearity of the signal.

Use the linearity test pattern shown in Figure 12 to measure R_{LM} . Each level of this pattern is sustained for 16 UI. To assure that the level has settled, regardless of pre/de-emphasis scheme, measure the settled symbol levels, V_A , V_B , V_C , and V_D , over 2 UI starting 7 UI after the transition.

The average voltage is, of course, the average of the four levels:

$$V_{avg} = \frac{1}{4}(V_A + V_B + V_C + V_D).$$

The effective symbol levels, ES_1 and ES_2 , are the average levels of the two center symbols:

$$ES_1 = \frac{V_B - V_{avg}}{V_A - V_{avg}}$$

$$ES_2 = \frac{V_C - V_{avg}}{V_D - V_{avg}}$$

The minimum signal level, S_{min} , is half of the swing between the closest adjacent symbols:

$$S_{min} = \frac{1}{2} \min(V_D - V_C, V_C - V_B, V_B - V_A),$$

and the level separation mismatch ratio is:

$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A}.$$

A linear transmitter, should yield $ES_1 = ES_2 = 1/3$ and $R_{LM} = 1.0$.

Amplitude compression causes variations in the vertical eye opening, EH, of the three eye diagrams. The 100 GbE PAM4 spec 100GBASE-KP4 requires $R_{LM} \geq 0.92$ which we expect to serve as a performance benchmark going forward.

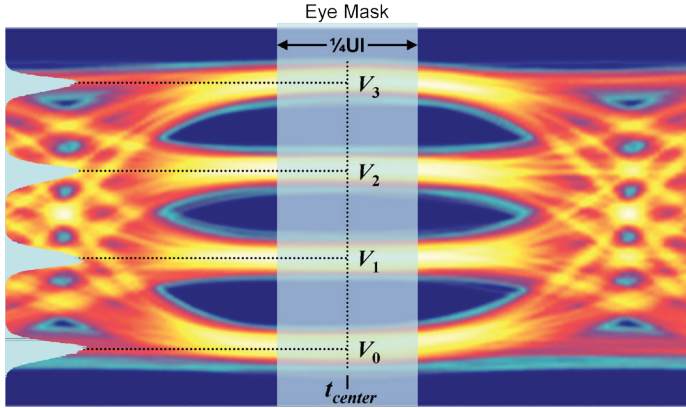


Figure 13. Measuring symbol levels with a horizontal eye mask.

4.6.2 Eye Linearity and Vertical Eye Closure, VEC

Another way to gauge the average symbol levels is to use a horizontal eye mask about t_{center} , Figure 13. The width of the mask is $\frac{1}{4}UI$ unless it extends beyond the horizontal eye opening, EW6, of any of the three eyes. If it does, then the mask width is limited to the extent of the smallest of (EW6low, EW6mid, EW6upp). In other words, the width of the horizontal eye mask is the smaller of $\frac{1}{4}UI$ and the extent of the eye with the smallest EW6, and must be symmetric about t_{center} .

The mean symbol levels measured on active data, V_0, V_1, V_2, V_3 , are given by the mean values of the four histograms formed by projecting the vertical data within the mask. Depending on the tap values, V_0, V_1, V_2, V_3 are likely to differ from the settled values V_A, V_B, V_C , and V_D , used to measure R_{LM} in Section 4.6.1 above, but the average inter-symbol voltage swings should be similar.

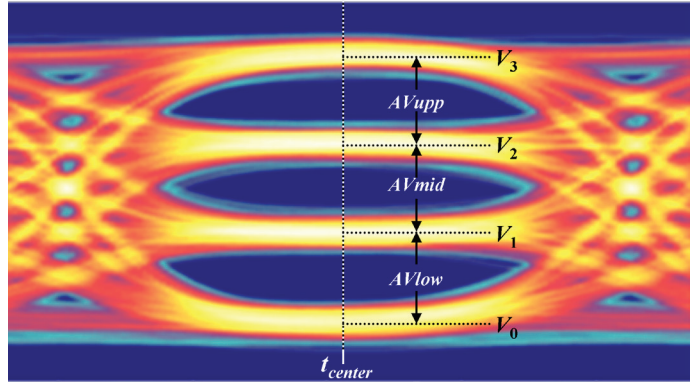


Figure 14. Using a horizontal mask to determine the symbol levels and their separations.

Eye linearity is a measure of vertical eye linearity that is similar to level separation mismatch ratio, R_{LM} , but rather than comparing settled inter-symbol voltage levels to the settled peak-to-peak PAM4 voltage swing, eye linearity is the ratio of the largest to smallest mean voltage swing between symbols with active data patterns.

The separations of the symbol levels are given by $AV_{low} = V_1 - V_0$, $AV_{mid} = V_2 - V_1$, and $AV_{upp} = V_3 - V_2$. Eye linearity is given by the ratio of the largest to smallest voltage swings between adjacent symbols:

$$\text{Eye linearity} = \frac{\max(AV_{low}, AV_{mid}, AV_{upp})}{\min(AV_{low}, AV_{mid}, AV_{upp})}$$

and vertical eye closure is given in dB by:

$$\text{VEC} = 20 \log \left(\min \left(\frac{AV_{low}}{EH6_{low}}, \frac{AV_{mid}}{EH6_{mid}}, \frac{AV_{upp}}{EH6_{upp}} \right) \right)$$

Eye linearity should be less than 1.5 and VEC less than 5.8 dB.

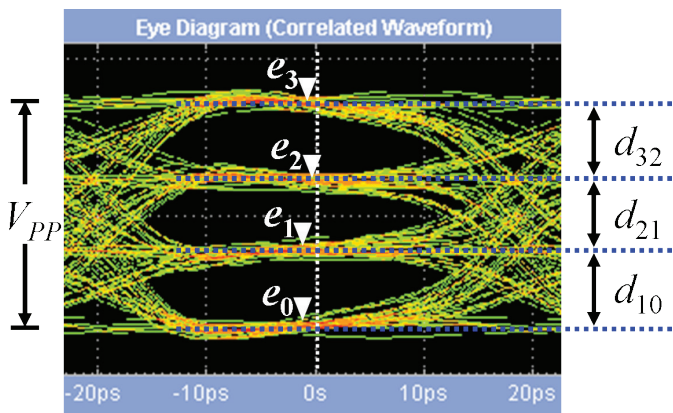


Figure 15. Measuring level and time deviation.

4.6.3 Level and Time Deviation

Like level separation mismatch ratio, R_{LM} , level deviation measures the relative variation of the four symbol levels but restricted to the response of the channel and equalization scheme. It includes the vertical voltage nonlinearities in the transmitter and how those nonlinearities are reflected in the ISI and DCD that remain after equalization. Similarly, time deviation measures the combination of transmitter timing nonlinearities, channel response, and equalization.

To measure level and time deviation, first remove signal impairments that are uncorrelated to the test pattern or data signal, like random noise and jitter, EMI (electromagnetic interference), and crosstalk, by averaging the eye diagram.

Determine the narrowest points in the symbol rails—these are the points in the eye diagram of minimum ISI as shown in Figure 15. Let’s call their time-delay positions with respect to the PAM4 eye center $e_0, e_1, e_2,$ and e_3 , and the voltage difference between them d_{10}, d_{21}, d_{32} .

Level deviation is the sum of symbol rail voltage deviations from their ideal values at the points of minimum ISI divided, V_{PP} , by the swing voltage between symbols 0 and 3:

$$\text{Level Deviation} = \left(\frac{\left|d_{10} - \frac{1}{3}V_{PP}\right|}{V_{PP}} + \frac{\left|d_{21} - \frac{1}{3}V_{PP}\right|}{V_{PP}} + \frac{\left|d_{32} - \frac{1}{3}V_{PP}\right|}{V_{PP}} \right) \times 100\%$$

Level deviation for a quality transmitter shouldn’t exceed several percent.

Time deviation is the average deviation of the points of minimum ISI with respect to the eye center in percent of a UI (unit interval):

$$\text{Time Deviation} = \frac{f_B}{4} \left(\sum_{i=0}^3 |e_i| \right) \times 100\%$$

where f_B is the baud rate. The amount of time delay that a system can tolerate depends on the symbol decision circuit. If all three slicers share a single time-delay, then time deviation should be under 10%. Time delay tends to be a greater problem in optical than electrical systems for reasons described below in Section 5.

5. Evaluating PAM4 Optical Transmitters

Specific techniques for evaluating optical PAM4 transceivers have not been formalized. Table 4 lists some performance parameters that should assure adequate PAM4 transmitter performance in most applications.

Optical signals should be analyzed with a measurement bandwidth slightly higher than the symbol rate. Unfortunately some specifications refer to this requirement as $0.75 \times f_B$ because early oscilloscopes used independent optical-electrical converters that had square-law detectors.

Unlike differential electrical transmitters, optical transmitters have physically distinct “on” and “off” states. Many of the standard characterization parameters for optical transmitters should be measured separately for both the inner eye structures and the outer structure. That is,

- OMA_{inner} , the optical modulation amplitude of the inner eye structures are given by the difference of high and low power for each eye: $OMA_{01} = P_1 - P_0$, $OMA_{12} = P_2 - P_1$, and $OMA_{23} = P_3 - P_2$. The inner OMA that has greatest effect on BER is called $OMA_{inner} = \min(OMA_{01}, OMA_{12}, OMA_{23})$.
- $OMA_{outer} = P_3 - P_0$.
- ER (extinction ratio) can be separated into inner and outer values, too, though it usually is only quoted for the outer eye, $ER = 10 \log(P_3/P_0)$.
- RIN (relative intensity noise) is the ratio of the rms noise of the unmodulated laser in the off state at a specific frequency per unit bandwidth to the total power of the unmodulated laser at any of the symbol levels. RIN of the outer eye structure is likely to be the only one specified.

PAM4 Optical Transmitter Performance Parameters*	
Total Average Launch Power	13 dBm
Outer OMA	≤ 6 dBm
Inner OMA	≥ -2.77 dBm
Extinction Ratio, ER	≥ 5.5 dB
Relative Intensity Noise, RIN	< -142 dB/Hz
RINxOMA	TBD dB/Hz

Table 4. Performance parameters for 13-29 GBd optical PAM4 transceivers. *Since no optical PAM4 standards have been released, please think of these as unofficial guidelines. Refer to the officially released specifications before making compliance tests.

Since RINxOMA, the relative intensity noise referred to the optical modulation amplitude, is the ratio of ambient light noise to the average modulated power per unit bandwidth. Tektronix application note, [“Performing RIN and RINxOMA Measurements on the DSA8300 Sampling Oscilloscope”](#) has a complete description of how to perform the measurement.

Optical transmitters have different linearity problems than differential electrical transmitters. In some modulation implementations, transitions from low to high power states occur faster than high to low. The result is a tendency for the three PAM4 optical eyes to be misaligned. The higher the baud rate, the greater the deviation. High rate optical receivers may require independent time-delay sampling points for each eye: (t_{low}, P_{low}) , (t_{mid}, P_{mid}) , and (t_{upp}, P_{upp}) .

Time deviation was defined in Section 4.6.3 with the help of Figure 15:

$$\text{Time Deviation} = \frac{f_B}{4} \left(\sum_{i=0}^3 |e_i| \right) \times 100\%$$

Time deviation requirements depend on the logic detection scheme, but if the decision circuits time-delay sampling point is the same for all three eye diagrams, time deviation should be less than 5-10%.

6. Evaluating PAM4 Receivers

The measure of a receiver's performance is how it does in the worst conditions it's likely to encounter. Stressed receiver tolerance tests measure a receiver's tolerance to signal impairments.

Like 25+ Gb/s PAM2-NRZ, both electrical and optical PAM4 receivers are subject to tolerance tests. The idea is to probe a receiver's weaknesses in a wide variety of difficult environments. Electrical PAM4 receivers are subject to jitter and noise tolerance tests plus separate interference and crosstalk tolerance tests.

When we say that a receiver "tolerates" a stressed signal, we mean that the receiver operates at or below the BER specified for the application before the signal is subjected to FEC.

6.1 Receiver Evaluation Test Pattern Pros and Cons

The test pattern is our first tool for determining receiver performance. The QPRBS13 and QPRBS31 patterns serve complementary purposes. QPRBS13 has 8192 symbols, short enough for both real-time and sampling oscilloscopes to analyze many pattern repetitions and perform their most accurate measurements.

On the other hand, to excite every possible ISI impairment, the test pattern should include every permutation of consecutive identical symbols that extends over the length of the pulse response. For example, if the pulse response extends over 7 UI, then the QPRBS13 test pattern will not provide a complete set of ISI impairments. The QPRBS31 pattern has over two billion unique sequences of 31 bits, enough to accommodate a pulse response that extends up to 15 UI. The problem, from the test perspective, is that both real-time and sampling oscilloscopes are less accurate when analyzing patterns that

are too long for them to capture and average. Think of the two primary test patterns as complementary tools for evaluating receivers: QPRBS13 allows you to make more accurate measurements at the expense of less complete ISI versus QPRBS31's less accurate measurements but exhaustive ISI.

A good way to optimize the performance of your test equipment and the stress from the test pattern is to calibrate the signal stress with the QPRBS13 pattern but test the receiver with a QPRBS31.

6.2 Evaluating Optical PAM4 Receivers

At the time of publication, September-2015, the optical PAM4 standards have not defined specific parameters for PAM4 optical receivers or tests unique to PAM4 modulation. To date, they outline test strategies based on PAM2-NRZ optical signaling at 25.8 Gb/s. These tests are covered in Tektronix application note, ["Physical Layer Tests of 100 Gb/s Communications Systems."](#) The reason that optical PAM4 technology lags electrical is a simple consequence of need; optical systems can use PAM2-NRZ at much higher rates than electrical.

To determine an optical receiver's performance margin, apply increasing levels of stress and determine the BER performance of the receiver in challenging conditions. For example, test the receiver's BER margin with decreasing inner and outer OMA and ER, increasing RIN and chromatic dispersion, and with signals that have increasing time deviation.

In the next section we'll discuss a variety of electrical stressed receiver tolerance tests. For the exception of crosstalk and ISI caused by channel insertion loss, these tests can be translated into the optical domain. For example, you can add SJ (sinusoidal jitter) to an optical signal to stress its clock recovery as is done in the electrical jitter and noise tolerance test described in Section 6.3 below.

Electrical PAM4 Receiver jitter and noise tolerance criteria		
Baud rate	13.6 GBd (100GBASE-KP4)	19-29 GBd*
Test pattern	Scrambled idle	QPRBS13 or QPRBS31
Low frequency SJ	5 UI at $f_{SJ} = 16$ kHz	5 UI for $CR-BW/100 < f_{SJ}$
High Frequency SJ	0.5 UI at $160 f_{SJ} =$ kHz	0.05 UI for $CR-BW \leq f_{SJ}$
Worst case channel		10.25 dB at Nyquist
Add UUGJ & reduce V_{pp} to give		
EW6		0.25 U
EH6		150 mV
VEC		5-6 dB
BER	$\leq 10^{-6}$	$\leq 10^{-6}$

Table 5. SerDes jitter and noise tolerance criteria. *Since no 19-29 GBd standards have been released, please think of these as unofficial estimates. Refer to the officially released specifications before making compliance tests.

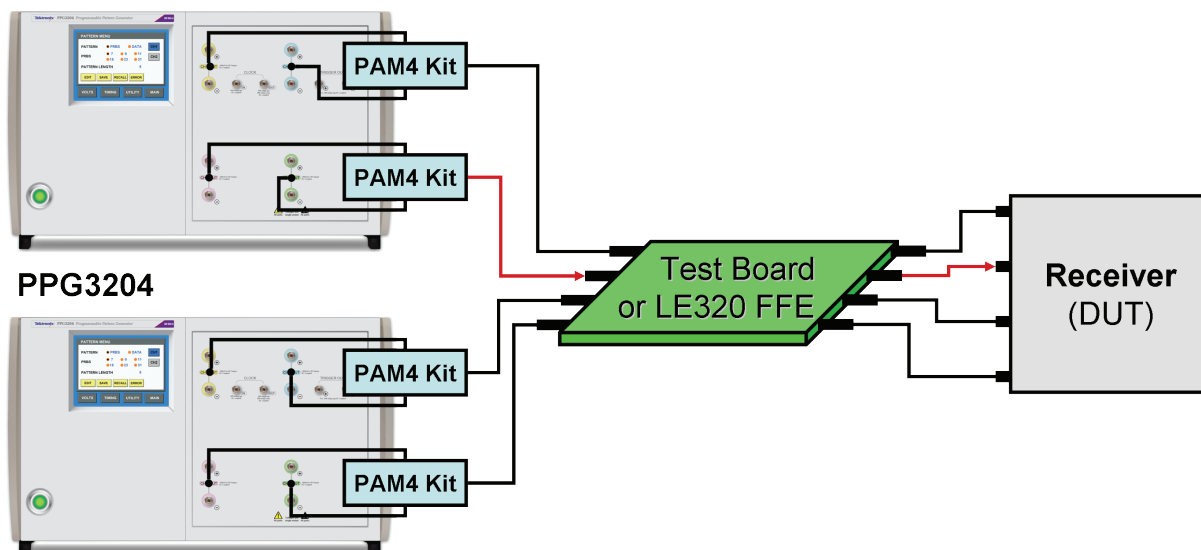


Figure 16. Electrical stressed receiver tolerance test setup.

6.3 PAM4 Electrical Receiver Jitter and Noise Tolerance

Table 5 lists jitter and noise stresses that PAM4 receivers should be able to tolerate.

Figure 16 shows a setup for receiver tolerance testing. PAM4 test patterns and stresses are generated by a PatternPro

PPG3202 pattern generator equipped with PSPL5380 PAM4 Kit. To meet requirements like those in Table 5, stresses have to be calibrated. Calibration can be performed with a DSA8300 Sampling Oscilloscope equipped with PAM4JARB PAM4 Analysis Application and/or a PED3202 Bit Error Rate Tester Error Detector with PAM4DEC reference receiver and Gray decoder.

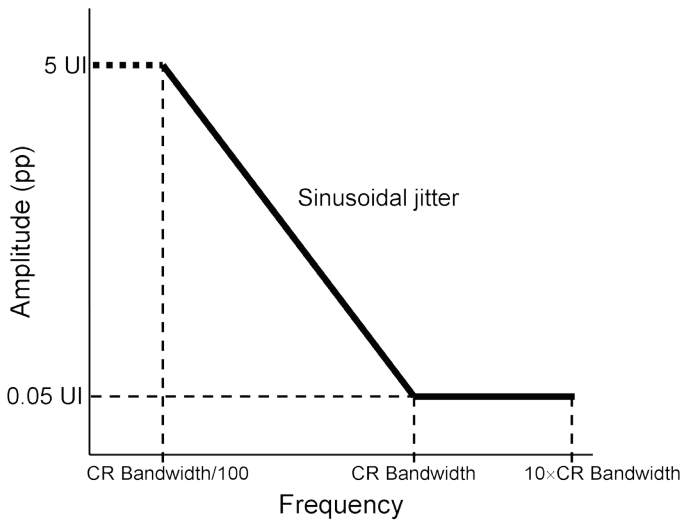


Figure 17. Sinusoidal jitter template. Receivers should tolerate high amplitude SJ below the clock recovery bandwidth and low amplitude SJ above.

6.3.1 Evaluating Clock Recovery

The use of embedded clocking and clock-data recovery effectively filters low frequency jitter from the decision circuit. An essential test of a SerDes’ clock recovery circuit consists of measuring SJ (sinusoidal jitter) tolerance across an amplitude-frequency SJ template. Receivers must tolerate both high amplitude SJ at SJ frequencies below the clock recovery bandwidth and low amplitude SJ for SJ frequencies above the clock recovery bandwidth, Figure 17.

If your receiver fails the SJ template test, determine the ranges in SJ amplitude and frequency where it works and where it doesn’t to acquire the information you need to diagnose clock recovery circuit problems.

6.3.2 Evaluating CTLE and DFE

We test a receiver’s CTLE and/or DFE by subjecting it to the maximum ISI of any compliant transmitter-channel combination.

Send the signal through the worst-case test board or equivalent FFE filter, like Tektronix’s [LE320](#) FFE. Frequency response is given by insertion loss as a function of frequency, $IL(f)$, the magnitude of the differential S -parameter, S_{DD12} . Different applications require different $IL(f)$ tolerances. Some standards specify $IL(f)$ with a simple loss requirement at the Nyquist frequency. At higher data rates, standards are more likely to specify $IL(f)$ with a set of constants, a_i ,

$$IL(f) = a_0 + a_1\sqrt{f} + a_2f + a_3f^2 + a_4f^3 \text{ (dB)}.$$

Figure 9, in Section 4 on transmitter testing, shows two examples from 29 GBd PAM4 applications.

To evaluate receiver equalization, optimize all equalization components at both the transmitter and receiver.

In testing receiver equalization we need to be careful about our choice of test pattern. Thorough evaluation with many repetitions of QPRBS13 accompanied by confirmation tests with QPRBS31 should suffice in most cases, but if your margin is small, say BER $\sim 10^{-7}$ - 10^{-6} , then the time investment of more careful analysis with many repetitions of QPRBS31 is warranted.

6.3.3 Evaluating a Receiver’s Tolerance to Jitter and Noise

With four symbol levels to discern, PAM4 receivers must tolerate comparatively poor signal-to-noise ratios and small symbol-to-symbol voltage swings. The easiest way to estimate a receiver’s sensitivity is to reduce the voltage swing until BER approaches 10^{-5} - 10^{-6} . A more comprehensive approach is to close the three PAM4 eye diagrams by

1. imposing ISI through test boards or a FFE filter,
2. applying UBHPJ (uncorrelated, bounded, high probability jitter, like SJ or crosstalk),
3. applying UUGJ (unbounded uncorrelated Gaussian jitter, essentially RJ), and
4. reducing the peak-to-peak voltage swing, V_{pp} ,

until EH6 and EW6 meet the target values, for example, EH6 = 50 mV and EW6 = 0.25 UI.

The resulting VEC (vertical eye closure, covered in Section 4.6.2 above) should be close to 5.5 dB. If it’s not in the range 5-6 dB, adjust V_{pp} , UBHPJ, and UUGJ until it is.

Since EH6, EW6, and VEC, are all derived from the worst of the three PAM4 eyes, the receiver might be particularly sensitive to the transmitter linearity or level separation mismatch, R_{LM} . To test the receiver’s performance on separate PAM4 eye diagrams and to determine its sensitivity to signal linearity, measure BER as a function of R_{LM} .

An acceptable receiver should operate under the combined stress with a BER $\leq 10^{-6}$ or 10^{-5} prior to FEC, depending on the standard.

Electrical PAM4 Receiver Interference and Crosstalk Tolerance Criteria				
Baud rate	13.6 GBd (100GBASE-KP4)		19-29 GBd*	
Test pattern	Scrambled idle		QPRBS13 or QPRBS31	
Low Pass B-T filter 3 dB BW	17 GHz		$1.5 \times f_B$	
Voltage swing, V_{pp}	≤ 800 mV		≤ 800 mV	
Level separation mismatch, R_{LM}	0.92		0.92	
Pre-cursor peaking	≥ 1.54		≥ 1.54	
Post-cursor peaking	≥ 4		≥ 4	
Insertion loss (dB), parameters	Test 1	Test 2	Test 1	Test 2
$IL(f) =$				
$a_0 +$	$-1.5 \leq a_0 \leq 1$	$-1.5 \leq a_0 \leq 2$	$-1 \leq a_0 \leq 1.5$	$-1 \leq a_0 \leq 2$
$a_1 \sqrt{f} +$	$0 \leq a_1 \leq 1.6$	$0 \leq a_1 \leq 3.8$	$0 \leq a_1 \leq 9.5$	$0 \leq a_1 \leq 15$
$a_2 f +$	$0 \leq a_2 \leq 1.6$	$0 \leq a_2 \leq 4.2$	$0 \leq a_2 \leq 31$	$0 \leq a_2 \leq 41$
$a_3 f^2 +$	$a_3 = 0$	$a_3 = 0$	$a_3 = 0$	$a_3 = 0$
$a_4 f^3$	$0 \leq a_4 \leq 0.03$	$0 \leq a_4 \leq 0.065$	$0 \leq a_4 \leq 14$	$0 \leq a_4 \leq 20$
Loss at Nyquist	≤ 14.4 dB	≥ 33 dB	≤ 10 dB	≥ 20 dB
Channel operating margin, COM parameters:				
R_{LM}	0.92		0.92	
Transmitter SNR	31 dB		31 dB	
DFE Taps	16 UI		5 UI	
CRJ	Measure CRJ_{rms}		Measured CRJ_{rms}	
DJ_{DD}	Measured CDJ_{PP}		$\frac{1}{2}$ measured CDJ_{PP}	
COM	< 3 dB		< 3 dB	
BER	$\leq 10^{-6}$		$\leq 10^{-6}$ or 10^{-5}	

Table 6. SerDes interference and crosstalk tolerance criteria. *Since no 19-29 GBd standards have been released, please think of these as unofficial estimates, refer to the officially released specifications before making compliance tests.

6.4 PAM4 Electrical Receiver Interference and Crosstalk Tolerance

Since a receiver’s tolerance to interference and crosstalk can vary in different situations so it makes sense to perform separate tests that span the worst-case possibilities. The emerging standards will require separate compliance tests for

cases of high interference/crosstalk with low ISI/insertion loss and low interference/crosstalk with high ISI/insertion loss. Table 6 lists parameters for creating the two test scenarios.

Acceptable receivers must operate at $BER \leq 10^{-6}$ or 10^{-5} prior to FEC, depending on the standard, under all conditions.

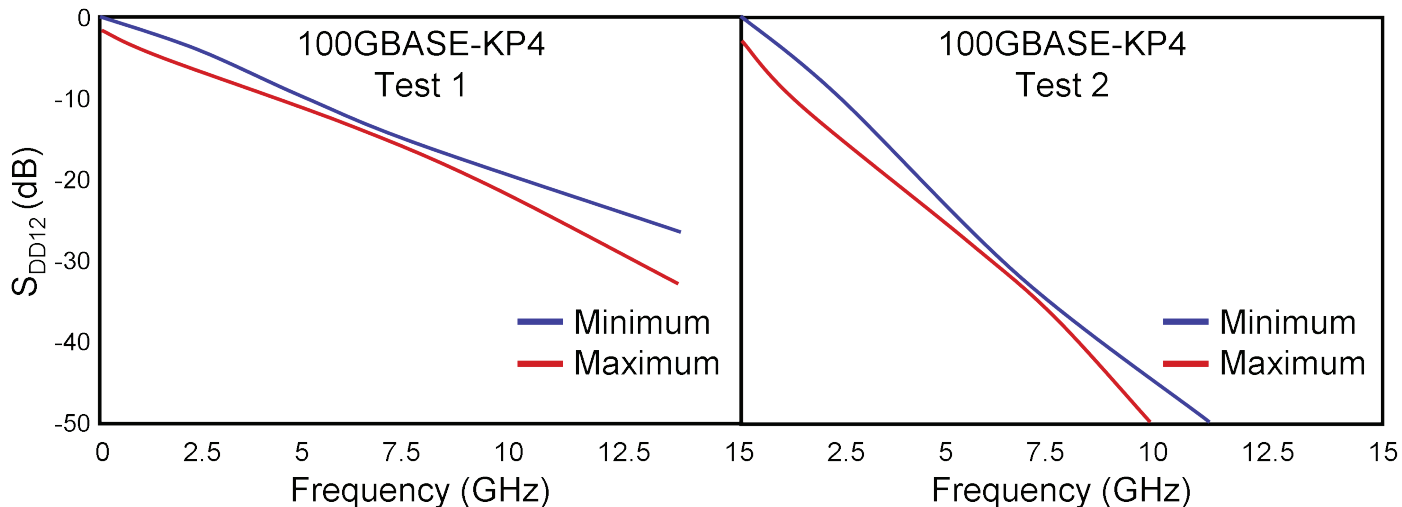


Figure 18. Examples of channel response, $IL(f) = S_{DD12}$, for Test 1 and Test 2 from 100 GbE 100GBASE-KP4.

Notice that Test 1 and Test 2 specified in Table 6 have separate channel responses, $IL(f)$, and the same COM (channel operating margin) requirement. Test 1 is a low loss/high interference test and Test 2 is a high loss/low interference test. Figure 18 shows examples for the two $IL(f)$ requirements from 100 GbE’s 13.6 GBd PAM4 100GBASE-KP4.

Where the low and high loss $IL(f)$ profiles are explicitly specified, the high and low interference conditions are implicitly specified by requiring $COM < 3$ dB for both tests.

COM, or channel operating margin, is a signal-to-noise like parameter: the ratio of the signal amplitude to the aggregate noise amplitude for the combination of the channel—the signal channel as well as all crosstalk aggressor channels—and every source of signal impairment.

You can derive COM by combining channel S -parameters with models of the transmitted and aggressor signals including transmitter de-emphasis and receiver CTLE, random and deterministic jitter, and voltage noise. Since COM is derived from channel S -parameters, it includes ISI and crosstalk.

Both Test 1 and Test 2 use signals with COM less than but close to 3 dB. To keep COM essentially constant for both tests, the low-loss Test 1 requires more crosstalk, ICN (integrated crosstalk noise, Section 4.5.2 above). Similarly, the high loss Test 2 has consequently lower ICN.

To perform the test, calibrate the stressed signals with an oscilloscope, including the standard fourth-order Bessel-Thomson low pass filter. Reduce the signal voltage swing to both close the eye vertically and to meet the COM requirement. Set the symbol levels of the stressed signal to give the worst case level separation mismatch, $R_{LM} = 0.92$, described in Section 4.6.1 above.

In the COM calculation, use R_{LM} , transmitter SNR, and DFE taps as specified in Table 6. For RJ and dual-Dirac DJ, use $R_J = CRJ_{rms}$ and $D_{JDD} = CD_{JPP}$ where CRJ_{rms} and CD_{JPP} are the test signal’s measured values as described in Section 4.1.

A good high speed PAM4 receiver should tolerate both Test 1 and Test 2 signals with BER below the minimum, 10^{-6} or 10^{-5} , depending on standard. Once you’ve set up COM and the two $IL(f)$ conditions by virtue of test boards or [LE320](#) FFE filter settings, you can gauge your receiver’s BER performance margin by increasing the aggressor amplitudes, reducing the signal peak-to-peak voltage, decreasing R_{LM} , and so on.



Figure 19. [DPO70000SX](#) 70 GHz bandwidth real time oscilloscope.

7. The NRZ-PAM4 Inflection Point

In advancing from 25 to 50 Gb/s, high speed serial data transmission technology has crossed an inflection point. The technical advances that have enabled multi-gigabit electrical data rates with PAM2-NRZ signal modulation on standard PCB (printed circuit board) can no longer economically produce the signal integrity required for reliable data transfer.

The situation is simple: Backplane loss at 12.5 GHz—the Nyquist rate for both PAM2-NRZ 25 Gb/s and PAM4 25 GBd (i.e., 50 Gb/s)—is about 40 dB, but at 25 GHz, backplane loss climbs to about 70 dB, well beyond the capability of any reasonable receiver technology. Plus, crosstalk gets disproportionately worse as we go from 12.5 to 25 GHz. Since no PCB medium can reduce loss by a factor of two, the only solution is to double the data rate without changing the symbol rate, that is, switch from PAM2-NRZ to PAM4. The drawback is reduced signal-to-noise ratio and increased signaling complexity.

With PAM4’s four symbol levels we have to develop techniques that account for new signal properties like the relative orientation and proportions of the three eye diagrams. High speed serial PAM4 technology is being developed as this paper is written in September-2015. We’ve reported the tests currently being used in the notation that is common among

standards groups. Both the tests and notation will evolve quickly in the coming months.

Tektronix will continue to provide all of the tools and measurement expertise you need to design, test, and manufacture this exciting new technology through both instrumentation and applications support. We have representatives of the OIF and IEEE 400G standards bodies and local AEs steeped in high speed serial technology experience available to help.

We provide multiple approaches to analyze and produce PAM4 signals to fit your application:

- The [DPO70000SX](#) 70 GHz bandwidth real time oscilloscope has the lowest noise in the industry and emulates the clock recovery, receiver equalization, and filtering required of an electrical reference receiver and signal analyzer. It provides all the tools you need to make the transmitter measurements and calibrate the stressed receiver tolerance tests we’ve described. When equipped with our PAM4JARB PAM4 Analysis Application it can make many of the measurements automatically.



Figure 20. [DSA8300](#) equivalent time sampling oscilloscope.

- The [DSA8300](#) equivalent time sampling oscilloscope analyzes both electrical and optical signals. When properly equipped, it serves as an excellent reference receiver that can perform all required transmitter measurements and stressed receiver tolerance test calibrations. The PAM4 software analysis package, [80SJNB Advanced](#), requires DSA8300 Option ADVTRIG. The acquisition of precise electrical waveforms requires the [82A04B](#) Phase Reference Module and an [80E09B](#) 60 GHz Electrical Sampling Module for electrical signals. For optical signals, use the appropriate sampling oscilloscope module: [80C14](#) for SM/MM fibers up to 16 GBd, [80C15](#) for SM/MM up to 32 GBd, or [80C10C](#) for SM from 25 GBd to 60+ GBd.

There are advantages to both oscilloscope platforms; the real-time DPO70000SX, provides high bandwidth and low noise, with built-in clock recovery along with advanced troubleshooting capabilities, and the equivalent-time DSA8300 is ideal for diverse needs with its modular mainframe suitable for optical or electrical inputs.

Application Note



Figure 21. The Tektronix PAM4 BERT system.

- The Tektronix PAM4 BERT system consists of separate transmitters and receivers. The [PPG3202](#) with [PSPL5380](#) PAM4 Kit generates Gray coded PAM4 stressed test patterns. The [PED3202](#) BERT Error Detector with PAM4DEC reference receiver with clock recovery and Gray decoder and PAM4 BERT Control and Analysis provides a complete suite of BER contour analysis tools for analyzing transmitter quality and calibrating stressed receiver tolerance tests.

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