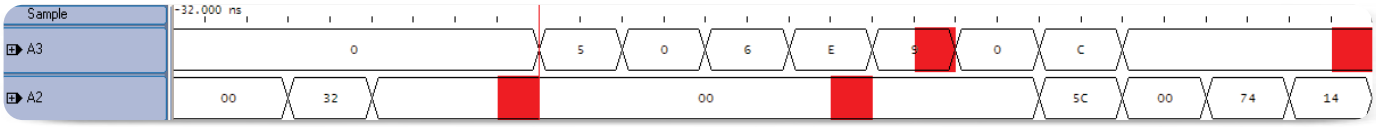
Quick Signal Integrity Troubleshooting with Integrated Logic Analyzers & Oscilloscopes

Meeting Fast Edge Signal Integrity Challenges

Fast product development requires fast and efficient troubleshooting of signal integrity problems. One class of signal integrity problems is caused by fast clock rates and fast digital edge rates. For example, computer, communications and digital video equipment are using fast clock and data rates to move data quickly. These fast clock and data rates are requiring high-speed digital edge rates. Also, designs using logic families such as ECL (Emitter Coupled Logic), PECL (Positive Emitter Coupled Logic), LVPECL (Low Voltage Positive Emitter Coupled Logic), HSTL (High Speed Transistor Logic) and other fast transitioning logic families are resulting in fast digital edge rates that are independent of the circuit's clocking rate. These fast digital edge rates are creating new signal integrity problems that did not occur in past digital designs using slower logic families.

Tektronix
Enabling Innovation



▶ **Figure 1.** *A3 bus and A2 bus waveforms with red glitch flags.*

Fast digital edges contain high frequencies that make proper termination of circuit board traces even more important. Fast edges can also cause increased crosstalk in a digital system. Circuit board traces that were treated as lumped circuit traces in the past are now transmission lines that require proper termination. Also, faster edges are causing larger transient currents that result in increased dynamic currents that may cause problems such as ground bounce and glitches in the power distribution.

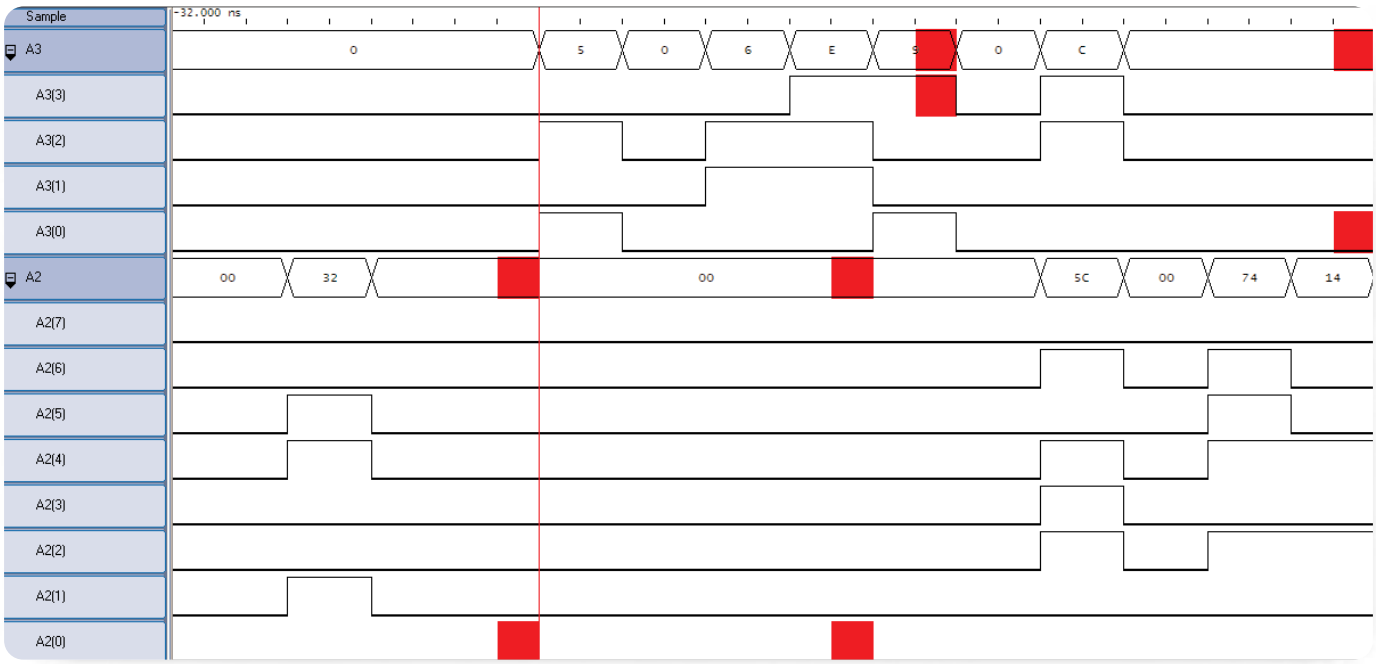
Fast digital edges can cause signal integrity glitch problems. These glitches are typically very short in duration, are unexpected, and may occur infrequently causing errors in state machine logic such as counter circuits, trigger circuits, etc. Signal integrity glitch problems are caused by many types of errors and can be difficult to debug. Tektronix' iLink™ Tool Set can quickly identify and analyze these problems.

The iLink Tool Set is a powerful integration of Tektronix TLA7000 Series logic analyzers and most Tektronix TDS/CSA Series oscilloscopes that quickly troubleshoots signal integrity glitch problems. The iLink Tool Set seamlessly integrates a logic analyzer and an oscilloscope for instant digital and analog insight; speeding debugging of many digital signals and helping you verify the integrity of your designs. The iLink Tool Set includes:

– iCapture™ simultaneous logic analyzer and oscilloscope measurements through a single logic analyzer probe

– iView™ time-correlated, integrated logic analyzer and oscilloscope measurements on one display

– iVerify™ multi channel bus analysis and validation testing using powerful oscilloscope-generated eye diagrams



▶ **Figure 2.** *A3 bus expanded into its four individual signal lines and the A2 bus into its eight individual signal lines.*

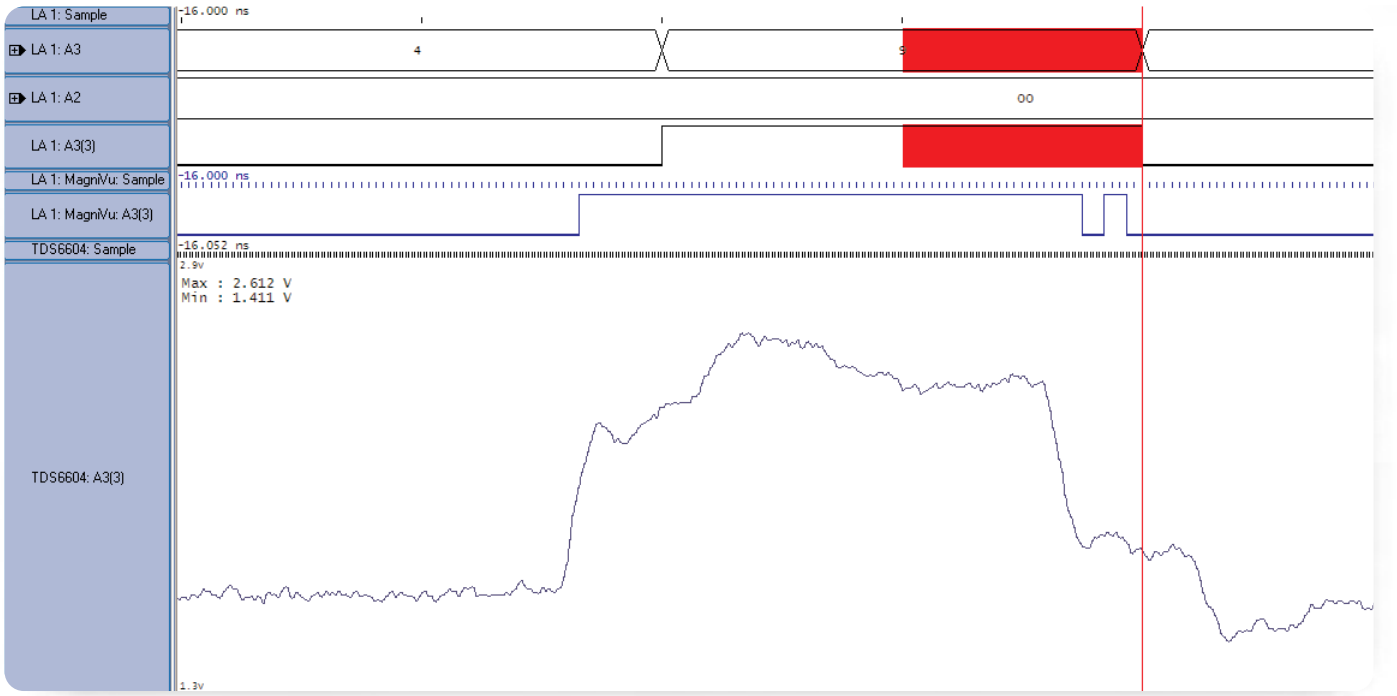
Debugging Buses with Signal Integrity Glitches

The following examples use a 4-bit and 8-bit bus to demonstrate debugging of signal integrity problems. You can use the debugging techniques in these examples to debug signal integrity problems in asynchronous circuits, synchronous circuits, processor address buses, data buses, control buses and just about any digital circuit. Applications include computer circuits, avionics, communications and most other applications that contain digital electronics.

The logic analyzer is an excellent instrument to capture digital bus signals and to flag glitches occurring on these buses. For example, debugging a 4-bit A3 bus and an 8-bit A2 bus is quickly accomplished using the iLink Tool Set. Figure 1 is an example of the A3 bus and the A2 bus waveforms with red glitch flags. The four red glitch flags indicate that there was more than one transition between the sample points at these locations on the bus waveforms. Each bus has two red glitch flags. The next step is to determine which signal on each bus has the glitches.

As shown in Figure 2, by expanding the A3 bus into its four individual signal lines and expanding the A2 bus into its eight individual signal lines it is easy to see that the A3 (3) and A3 (0) signals have one glitch each and the A2 (0) signal line has two glitches.

The next two sections show how these signals are quickly debugged using the iLink Tool Set which provides quick digital and analog visibility of these signals with glitches. The next section debugs the A3 (3) glitch.



▶ **Figure 3.** *A3 (3) Waveform Display. The logic analyzer screen displays both the digital and analog view of the A3 (3) signal with the glitch.*

Termination Glitches

The iLink Tool Set provides quick digital and analog insight by capturing and analyzing the circuit's digital and analog characteristics. The expanded bus waveforms identified that the A3 (3) signal has a glitch. The logic analyzer's triggering is changed from triggering on any glitch to trigger only on glitches on the A3 (3) signal. The expanded bus waveforms are collapsed back into two waveforms to save display space, and debugging focus is on the A3 (3) signal.

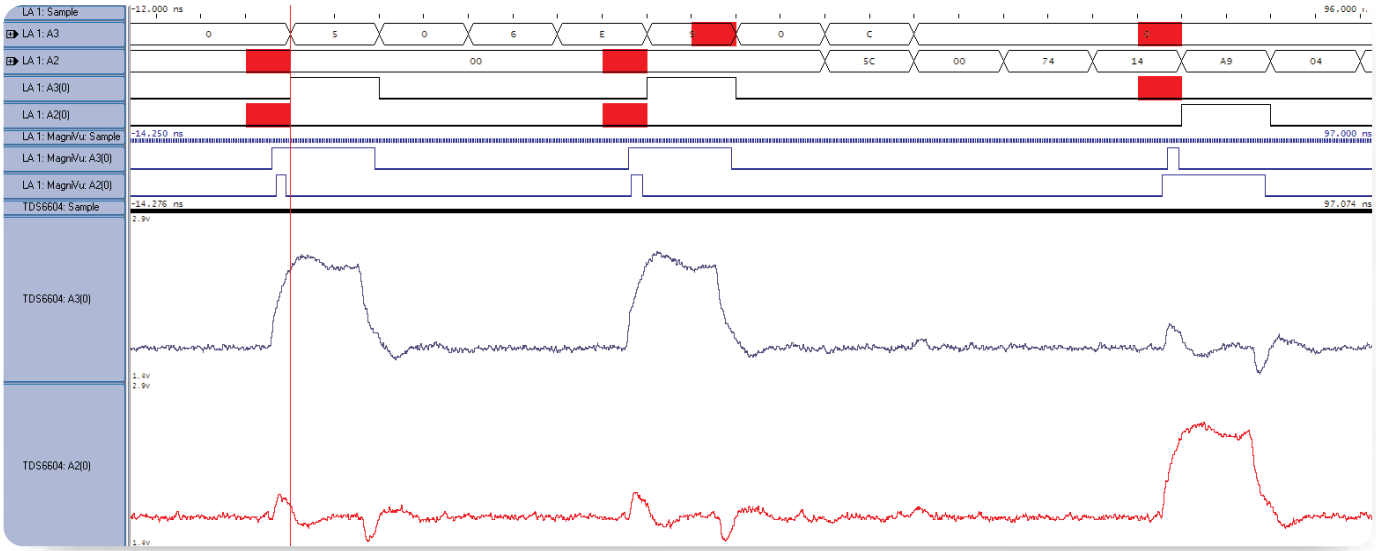
Figure 3 shows a logic analyzer screen with both the digital and analog visibility of the A3 bus and the A3 (3) signal with the glitch. To provide complete bus and signal visibility the iLink Tool Set provides four different views to analyze the A3 bus and its A3 (3) signal.

1. The logic analyzer's deep timing bus waveform (up to 32 M deep) shows all the signal lines of the bus by values and transition areas. The red glitch flag on the bus waveform indicates that there was more than one transition between the 4 ns deep timing sample points on one or more of its signal lines.
2. The logic analyzer's deep timing signal waveform (up to 32 M deep) of the signal line with a glitch. The A3 (3) waveform has a red glitch flag indicating the location on the waveform where there was more than one transition between the 4 ns deep timing sample points.

3. The logic analyzer's MagniVu™ 125 ps high-resolution timing waveform of the A3 (3) signal line with the glitch. High-resolution details of the glitch are measured and analyzed with 125 ps resolution. It is quickly seen that the glitch is at the end of a digital pulse. The glitch is not at the beginning of the pulse or isolated by itself. MagniVu 125 ps high-resolution timing is like having a second logic analyzer running all the time at 125 ps resolution on all channels at 16 Kb memory depth – through the same probe.
4. The oscilloscope's analog waveform (2 GHz analog bandwidth with 20 GS/s sample rate) of the A3 (3) signal line with the glitch. With iView the logic analyzer triggers the oscilloscope at just the right time to capture the glitch. iView transfers the oscilloscope analog waveforms to the logic analyzer display. iView displays both the oscilloscope's analog waveforms and logic analyzer's digital waveforms on the logic analyzer display. These automatically time-correlated analog and digital waveforms provide powerful insight that quickly identifies that there are multiple logic transitions on the falling edge of A3 (3) that is creating the glitch.

Debugging A3 (3) is accomplished quicker by using the logic analyzer's iCapture probing. The logic analyzer's iCapture probing provides the probing for both the logic analyzer and the oscilloscope. Any four of the A3 and A2 bus signals being probed by the logic analyzer can be routed to the oscilloscope. iCapture probing eliminates double physical probing and double probe loading that is typically required by using a logic analyzer and oscilloscope to measure the same signal.

Inspection of the prototype circuit board revealed that one of the A3 (3) circuit traces was improperly terminated. The LVPECL fast edge rates and the circuit board trace termination error caused poor rising edges and falling edges on the A3 (3) signal line. The poor rising edge is above the logic threshold and does not cause a problem on the rising edge. But, the poor falling edge is bouncing around the logic threshold and results in glitches occurring on some of the falling edges.



▶ **Figure 4.** *A3 (0) and A2 (0) Waveform Display. Complete digital and analog visibility with deep memory timing bus and individual signal waveforms with red glitch flags, MagniVu high-resolution timing waveforms and analog waveforms.*

Crosstalk Glitches

The next step is debugging the A3(0) and A2(0) signal lines. In Figure 4, the iLink Tool Set provides digital and analog visibility of deep timing bus waveforms with red glitch flags, deep timing of individual signals with red glitch flags, MagniVu 125 ps high-resolution timing waveforms and analog waveforms.

You can quickly see that the A3 (0) and A2 (0) have crosstalk by analyzing the time-correlated views of the A3 (0) and A2 (0) digital and analog waveforms. On every A3 (0) leading edge there is a corresponding small positive voltage pulse on A2 (0). On every A3(0) falling edge there is a corresponding small negative voltage pulse on A2(0). The same is true for A2 (0) affecting the A3 (3) signal.

Bus Eye Diagrams

The iLink Tool Set includes iVerify that measures an eye diagram of all the bus signals using powerful oscilloscope-generated eye diagrams. An eye diagram is a way to measure the data valid window and the signal integrity on clocked buses. All the signal lines are analyzed together in relation to the clock edge. The eye opening is a time and voltage measurement of the setup and hold time (data valid window) in relation to the clock edge. Data transfer problems will start to occur if the eye opening closes to smaller than the setup and hold requirements of the logic devices being used. Typically up to 4 channels of eye diagrams can be measured using the only the oscilloscope. As data bus clock go faster it is important that the eye opening is equal to or larger than the required setup and hold times (data valid window). Using iVerify with the logic analyzer and oscilloscope, a complete multi channel bus eye diagram of all 12 signal lines of the digital bus signals A3 and A2 can be quickly captured and measured. The bus eye diagrams quickly identify and isolate signal integrity problems on digital buses.

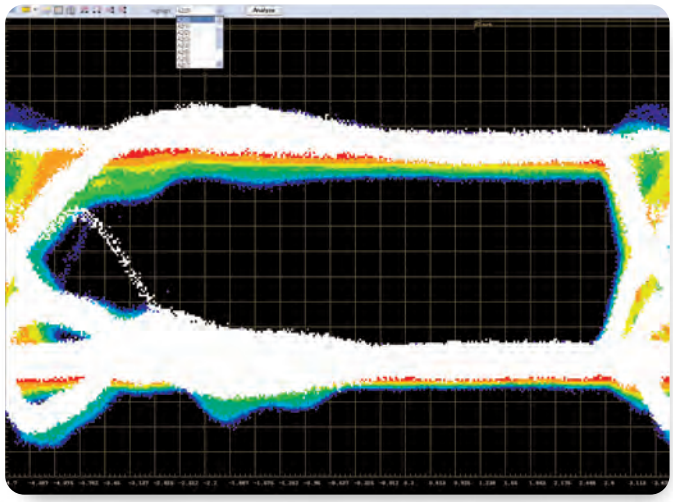
In Figure 5, the white highlighted eye diagram of the A2 (0) signal shows a cross talk problem, indicated by its transition into the right side of the eye opening.

Summary: Powerful iLink Tool Set Quickly Debugs Signal Integrity Problems

The iLink Tool Set with an integrated logic analyzer and an oscilloscope quickly debugs signal integrity glitch problems by using the following debugging technique:

1. Monitor the bus signals and trigger on glitches with the logic analyzer
2. Expand the bus signals into individual signals and display glitch locations
3. Trigger and display the individual signal line with the glitch
4. Measure glitch details with MagniVu 125ps high-resolution timing
5. Measure glitch analog characteristics using external oscilloscope with iCapture and iView
6. Analyze the time-correlated digital and analog waveforms and determine the cause of the glitches
7. Analyze entire bus eye diagrams with iVerify to identify trouble-some signal lines

In troubleshooting signal integrity glitch problems the logic analyzer triggers, captures and displays glitches on buses with deep timing acquisition while simultaneously capturing and displaying the glitch with MagniVu 125ps high-resolution timing on individual channels. Using iView triggering and iCapture probing, the oscilloscope measures the analog characteristics of the glitch with 20 GS/s resolution. Using iView, the logic analyzer display shows four time-correlated views of the signal: a deep timing digital bus waveform with red glitch markers, a deep timing individual channel waveform with red glitch markers, MagniVu 125ps high-resolution timing waveforms to measure glitch details, and the oscilloscope's 20 GS/s analog waveform measurements of the glitch. Use iVerify to quickly identify troublesome signals and speed up the debugging process.



▶ **Figure 5.** *On this oscilloscope-generated eye diagram, white highlights show a cross talk problem caused by the A2 (0) signal.*

The iLink Tool Set gives you time-correlated digital and analog insight to your circuit operation to debug signal integrity glitch problems. Integrated logic analyzers and oscilloscopes using the iLink Tool Set with iView, iCapture and iVerify features provide the most effective way to quickly debug the source of elusive signal integrity glitch problems that threaten product development schedules.

Contact Tektronix:

ASEAN / Australasia / Pakistan (65) 6356 3900
Austria +41 52 675 3777
Balkan, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium 07 81 60166
Brazil & South America 55 (11) 3741-8360
Canada 1 (800) 661-5625
Central East Europe, Ukraine and Baltics +41 52 675 3777
Central Europe & Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France & North Africa +33 (0) 1 69 86 81 81
Germany +49 (221) 94 77 400
Hong Kong (852) 2585-6688
India (91) 80-22275577
Italy +39 (02) 25086 1
Japan 81 (3) 6714-3010
Luxembourg +44 (0) 1344 392400
Mexico, Central America & Caribbean 52 (55) 56666-333
Middle East, Asia and North Africa +41 52 675 3777
The Netherlands 090 02 021797
Norway 800 16098
People"s Republic of China 86 (10) 6235 1230
Poland +41 52 675 3777
Portugal 80 08 12370
Republic of Korea 82 (2) 528-5299
Russia & CIS 7 095 775 1064
South Africa +27 11 254 8360
Spain (+34) 901 988 054
Sweden 020 08 80371
Switzerland +41 52 675 3777
Taiwan 886 (2) 2722-9622
United Kingdom & Eire +44 (0) 1344 392400
USA 1 (800) 426-2200

For other areas contact Tektronix, Inc. at: 1 (503) 627-7111

Last Updated June 15 2005

For Further Information

Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

08/05 FLG/WOW 58W-17254-1

Tektronix
Enabling Innovation