Understanding and Performing RapidIO Testing

COMPUTING COMMUNICATIONS VIDEO

Introduction

RapidIO® architecture delivers significantly increased transmission speeds to enable the design of next-generation networking and communications equipment, but with it comes compliance and interoperability issues. Tektronix' comprehensive tool set enables engineers to resolve these issues quickly and efficiently so that they can easily implement RapidIO into their designs.

Digital hardware and embedded software designers in the communications industry face a challenge introduced by the increase in processor speeds and the bandwidth available to feed data to the processor. The critical bottleneck lies in the speed at which various components "inside the box" communicate with each other.

RapidIO,an open communications standard designed for chip-to-chip and board-to-board connections using a backplane, eliminates this bottleneck. This high-performance, packet-switched bus technology addresses the demand for next-generation networking and communications equipment by delivering higher bandwidth, increased throughput, software transparency, greater reliability, fault tolerance, low latency, low power and low cost. Its architecture provides higher bus speeds that allow communications at performance levels scaling greater than 10 Gb/s. Designers can add multiple RapidIO ports to new I/O chips, reaping the performance benefits of a fabric interconnect without incurring the costs associated with adding a dedicated switching chip.

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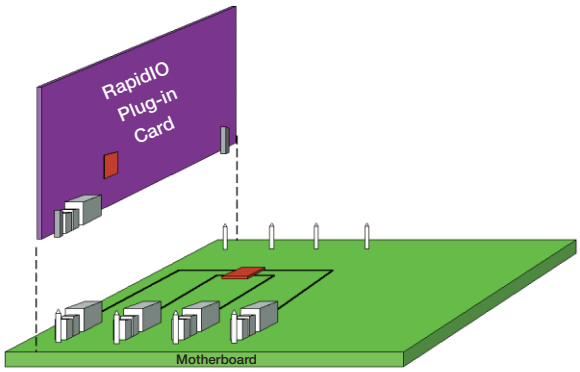


▶ ***Figure 1.*** *HIP Architecture.*

RapidIO Interoperability and Compliance Testing

With the emergence of RapidIO bus technology comes compliance and interoperability issues that design engineers must resolve before implementing RapidIO ports into their designs. RapidIO's hardware interoperability platform (HIP) architecture offers a common environment for silicon vendors to demonstrate seamless interoperability, opening doors to many tools and semiconductor vendors.

The HIP architecture employs a common form factor for switch fabrics and end points, and a common connector and pin assignments for power and RapidIO signal paths, the critical elements that impact interoperability testing. Its architecture consists of a motherboard and a RapidIO plug-in card, as illustrated in Figure 1. The HIP motherboard is intended to provide RapidIO connectivity for RapidIO plug-in cards.

In addition to providing a vehicle for silicon vendors to demonstrate interoperability, the HIP architecture offers a common environment for these vendors to evaluate why silicon does not interoperate. What happens when a 2 gigahertz data path between two point-to-point devices fails to communicate? When failures occur, designers must be able to accurately view, characterize, analyze and debug these errors.

Common questions may include:

- How do I verify that my design conforms to the RapidIO specification?
- How do I probe the RapidIO port?
- How do I trigger on real-time RapidIO port activity, which includes control symbols, packet types and transactions?
- How do I decode RapidIO symbols and packets?
- How do I automate the linking of transaction-level and operation-level bus activity between Tx and Rx buses?
- How can I get my whole design team up and running with minimal training?
- What are the tools required to fully debug RapidIO?

This platform, in conjunction with the appropriate test and measurement equipment, allows design engineers to accurately characterize and analyze such failures so they can ensure that their designs comply with RapidIO specifications.

Design engineers who implement RapidIO technology into their designs will need to examine both the physical layer—visibility of signal quality, and protocol layer—assurance that the RapidIO communication protocol is operating properly. The ideal diagnostic tools will enable these designers to capture, view and analyze specific signals of interest to ensure accurate, efficient verification, characterization and debug for RapidIO implementation. Their complete measurement system will include a logic analyzer, oscilloscope, probes and application-specific test software.

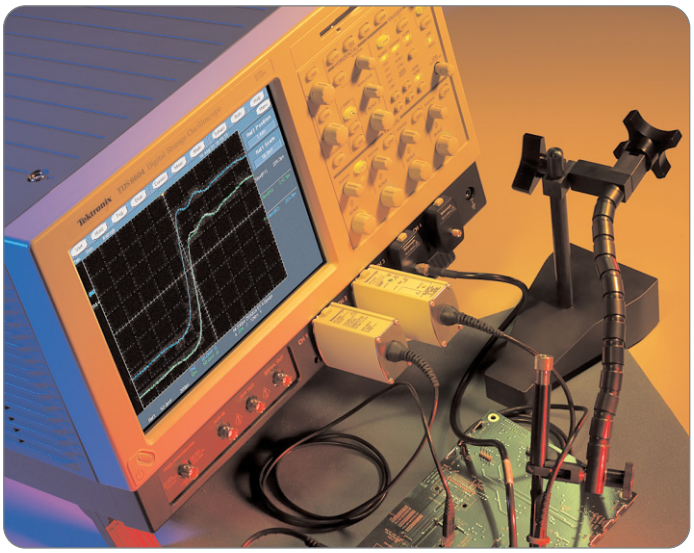
This application note will focus on understanding and performing compliance testing to ensure that your design conforms to the RapidIO specification and will include a discussion of the test instruments required.

Probing Solutions

RapidIO compliance testing begins at the probe tip. The ideal probing solutions used to implement RapidIO will allow non-intrusive acquisition of high-speed differential signals, characterization of the analog component of high-speed digital signals, and monitoring of RapidIO transmit and/or receive ports without the need for on-board connectors or external hardware.

High-bandwidth active and differential probes are required to properly characterize timing and signal quality. These probes ensure maximum signal fidelity, measurement accuracy and insight into signal behavior by preserving the signal, minimizing probe loading and providing easier access to today's densely packed circuitry.

	Probe Model	Analog Probe Bandwidth
Oscilloscope probe	P7260, TekConnect Interface	Single-ended DC to 6.0 GHz
	P7240, TekConnect Interface	Single-ended DC to 4.0 GHz
	P6249, TEKPROBE II™ Interface	Single-ended DC to 4.0 GHz
	P7330, TekConnect Interface	3.5 GHz Differential
	P6330, TEKPROBE II™ Interface	3.5 GHz Differential
Logic Analyzer probe	P6880 Connectorless High Density	2.0 GHz Differential
	P6810 General Purpose	2.0 GHz Differential
	P6860 Connectorless High Density	2.0 GHz Single-ended

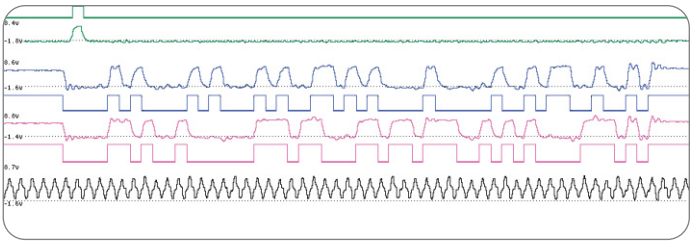


▶ ***Figure 2.*** *Oscilloscope probes.*

Oscilloscope Probes

The P7260 single-ended active probe delivers an unprecedented 6 GHz bandwidth and < 75 ps rise time capability to enable engineers to view the fastest signals for their next-generation digital designs. Its high performance, low circuit loading and low noise make it an excellent choice to examine high-speed communication buses. The P7260 allows engineers to make high-speed measurements quickly and efficiently, providing a greater level of insight into signal behavior with maximum signal fidelity. An unparalleled input capacitance < 0.5pF ensures minimum loading of the signal for the most accurate acquisition system available. Its small probe head allows placement within the tight physical constraints common in today's fine pitch circuitry.

In order to increase data transmission speeds, lower logic amplitudes are necessary. As amplitudes decrease, many of today's signals have gone differential to stay above the ground-induced noise where the signal would be lost. To measure these demanding differential signals, the P7330 high-performance differential probe provides a high-bandwidth, low circuit loading, low noise differential probing solution with 3.5 GHz bandwidth and <130 ps (typical) rise time measurements. Its small probe head geometry allows this probe to access points on densely packed circuits. The P7330 features the TekConnect™ interface, which preserves signal fidelity to 18 GHz to meet present and future bandwidth needs. The P7330 enables users to make time or frequency domain measurements on high bandwidth signals commonly found in communication applications, such as RapidIO.



▶ ***Figure 3.*** *Integrated digital/analog display.*

Two Worlds, One View

Ever-increasing signal speeds and the escalating complexity of high-speed buses, such as RapidIO, have driven the need for digital designers to view both digital and analog signal characteristics to effectively debug and verify their systems. The logic analyzer points to the problem while the oscilloscope looks at the problem with very high-resolution analog detail. In the case of RapidIO, designers must be able to view both the analog and digital content of their RapidIO ports simultaneously during the initial debug phase.

The TLA700 Series logic analyzer, equipped with Integrated View (iView) technology, integrates the multi-channel and powerful triggering capabilities of the logic analyzer with the sample speed and measurement accuracy of a Tektronix high-performance digital oscilloscope to make it possible for the digital designer to look at time-correlated waveforms of the digital and analog signals on an integrated display. Using iView technology, the designer can accurately relate the digital symptom to the analog cause of the error or failure, as illustrated in Figure 3.

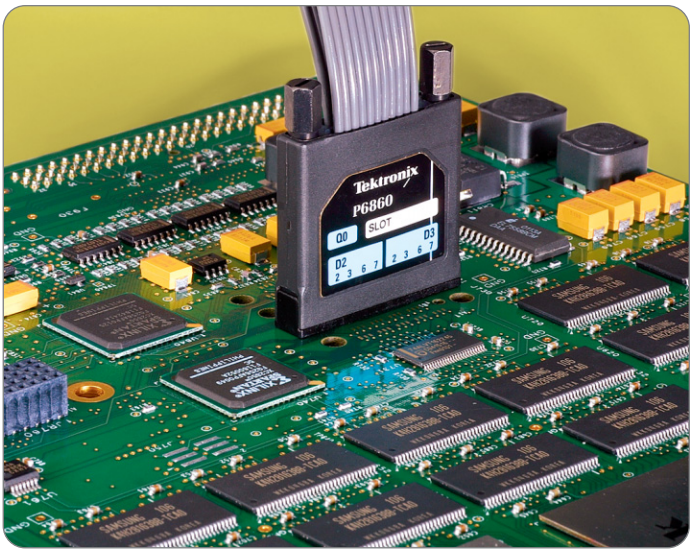
Logic Analyzer Probes

The pairing of iView technology with the TLA700 Series logic analyzer's TLA7Axx module, allows full integration and correlation of state, high-speed timing and analog analysis, enabling the engineer to view live RapidIO bus activity through a single logic analyzer connectorless, compression probing system. Due to the low capacitive load (0.7pF) provided by the P6880 logic analyzer differential probes, (see Figure 4), the signal under test is preserved and the engineer is provided with maximum signal fidelity and measurement accuracy.

In addition, the TLA700 Series logic analyzer, combined with the TMS805 RapidIO support package, provides a direct connection between the logic analyzer and the 8- or 16-bit RapidIO transmit and/or receive buses at data rates up to 1 Gb/s (500 MHz clock). This solution provides a powerful means to acquire packet and control symbol information without the need for external hardware.

A single TLA7Ax4 module can capture synchronous RapidIO transmit and receive buses (both buses are based on a single crystal at the same frequency without phase drift). For asynchronous transmit and receive buses (buses that are not based on the same crystal), a separate module is required to acquire each bus. The channel assignment of the RapidIO support package is intended to simplify routing to a probe footprint using the recommended pin escape of the RapidIO Interconnect Specification (part IV, section 6.6).

Please refer to www.tektronix.com/rapid_io for more information that describes how to integrate the P6880 connectorless, high-density probing technology to support both 8- and 16-bit RapidIO operation and includes both the Rx and Tx bus capture using a TLA7Axx logic analyzer module.



▶ ***Figure 4.*** *A Logic analyzer probe.*

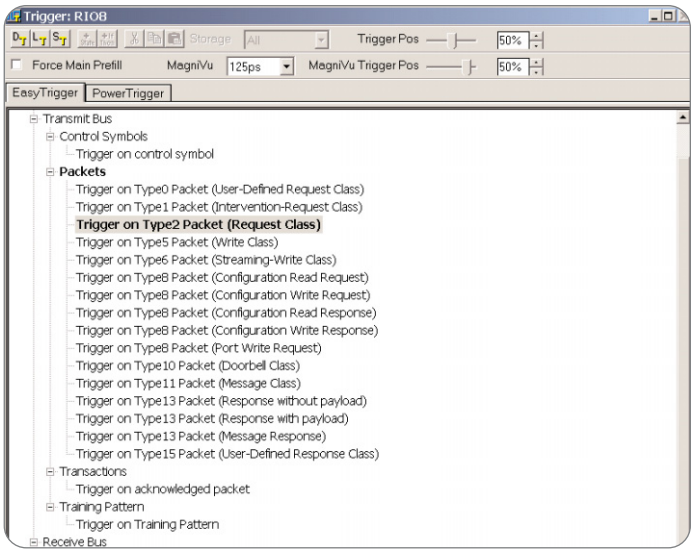
Protocol Layer Testing with a Logic Analyzer

Protocol layer testing begins with accurate signal acquisition. In addition to superior probing solutions, advanced triggering capabilities are critical. And once measurement data is properly acquired, it must be translated into meaningful results. The TLA700 Series logic analyzer, equipped with the TMS805 RapidIO support package, provides a powerful means to trigger, acquire, decode and display RapidIO port cycle activity.

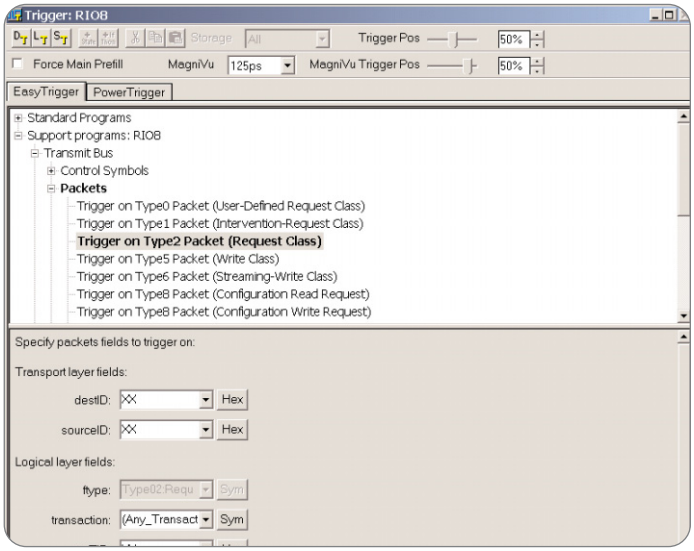
Triggering

When coupled with the TMS805 RapidIO support package, the TLA700 Series delivers advanced triggering capabilities to easily isolate and capture specified RapidIO transactions.

The TMS805 RapidIO support package includes a library of EasyTrigger templates (see Figure 5) to enable the user to quickly trigger and qualify common aspects of the RapidIO protocol, simplifying trigger setup for the complex serial nature of the RapidIO port architecture. Users can easily trigger on transactions (consists of a packet and its acknowledgement control symbol) if the transmit and receive buses are captured by the same module. By simply selecting the desired template and entering the information into the desired fields, users can transform the TLA700 Series logic analyzer into a tool that triggers on specific events of interest. At data rates up to 750 Mb/s, EasyTrigger templates allow the user to trigger on packets, control symbols and transactions (see Figure 6).



▶ ***Figure 5.*** *List of Easy Triggers provided with RapidIO support package.*



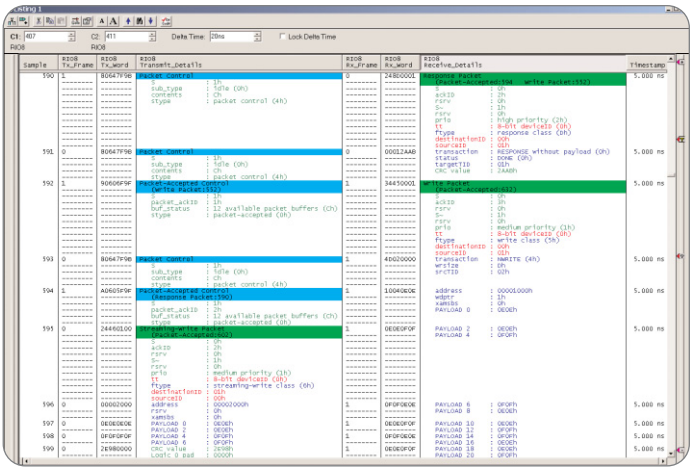
▶ ***Figure 6.*** *Example of Easy Trigger.*

Disassembly and Display

After measurement data is properly acquired, it must then be decoded into meaningful results and displayed in an appropriate manner. The TLA700 Series logic analyzer's disassembler decodes and displays the captured data from the RapidIO protocol in a packet-style view using its listing window, as illustrated in Figure 7.

The display includes three elements: a packet/control symbol summary, detailed decoding of the fields of a packet/control symbol and the raw data. Color-coding is used to differentiate the text in each of these three elements and to distinguish control symbols from packets in the packet/control symbol summary. Color is also used to differentiate transaction and operation levels of request and response packets in the details column.

Equipped with the TMS805 RapidIO support package, the logic analyzer delivers advanced disassembly features, such as deep capture of on-board processor activity correlated to RapidIO Tx and Rx ports and deep synchronous display of these ports. The disassembler provides control symbol decoding and display of individual fields in the physical layer; packet decoding and display of individual fields for physical, transport and logical protocol layers; and simultaneous decoding of both transmit and receive data ports.



▶ ***Figure 7.*** *Illustration of a packet-style view of captured data from a RapidIO protocol using a listing window.*

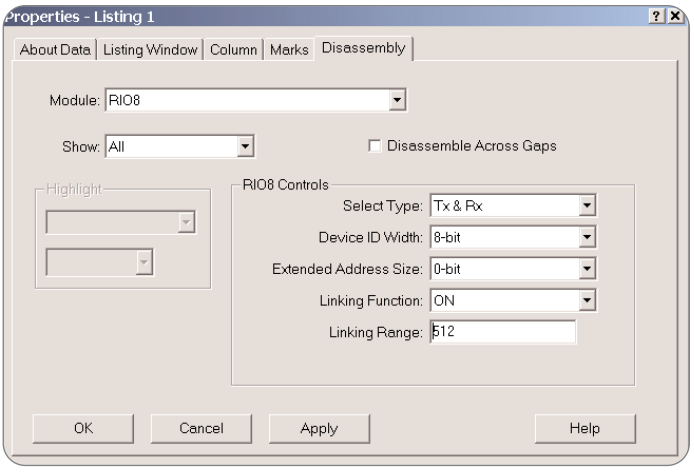
Linking Transmit and Receive Buses with the TMS805 RapidIO Support Package

The disassembler's powerful capabilities allow it to link transaction and operation levels of request and response packets between the acquired transmit and receive buses. If the transmit and receive buses are captured by one TLA7Axx module, the disassembler can link request and response packets together in addition to linking a packet with its acknowledgement control symbol. If the two buses are captured by separate modules, data from the buses is time-correlated. The disassembler allows the user to remove control symbols from the protocol decoder, which is useful when removing control symbols embedded in the middle of a packet. The disassembler can be configured to decode an 8- or 16-bit source and destination ID, or a 0-, 16- or 32-bit extension address.

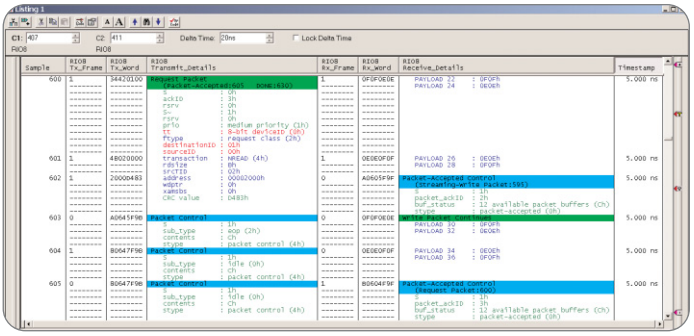
To link the transmit and receive buses using the TMS805 RapidIO support package, follow these steps, as illustrated in Figure 8:

1. With a listing window active, open the disassembly options window. The disassembly options window can be accessed by clicking View in the menu bar and selecting Properties. Then click the Disassembly tab.
2. In the drop-down list next to Select Type, select Tx and Rx. To ensure that linking works, the transmit and receive buses must be captured in the same module.
3. In the drop-down list next to Linking Function, select ON.
4. Enter a value next to Linking Range. The linking range specifies the number of samples from the request packet that the disassembler will search to find the corresponding response packet or control symbol.

After an acquisition is taken, the transmit and receive buses will be linked. In Figure 9, the request packet at sample 600 is linked to the packet-accepted control symbol at sample 605.



▶ ***Figure 8.*** *Disassembly options window.*



▶ ***Figure 9.*** *Illustration of linked transmit and receive buses.*

Module Requirements

One 136-channel TLA7Axx logic analyzer module is required per RapidIO port, which provides capture of both transmit and receive ports for the target port. Module acquisition speed depends on user requirements. The TMS805 RapidIO support package does not require additional hardware beyond TLA7Axx logic analyzer modules and compression differential probes.

The TMS805 RapidIO application support package supports 8- and 16-bit RapidIO port implementations with clock rates from DC to 500 MHz and data rates from DC to 1 Gb/s.

Support Package	Bus Width	Clock Rate	Data Rate
RIO8	8-bit	DC up to 375 MHz	DC up to 750 Mb/s
RIO16	16-bit	DC up to 375 MHz	DC up to 750 Mb/s
RIO8_T	8-bit	DC up to 500 MHz	DC up to 1 Gb/s
RIO16_T	16-bit	DC up to 500 MHz	DC up to 1 Gb/s

Physical Layer Testing with a Real-time Oscilloscope

While logic analyzers can provide the designer with insight into the protocol layer of RapidIO transactions to indicate whether or not a RapidIO protocol is operating properly, high-performance real-time oscilloscopes can offer the designer high-resolution analog detail of the physical layer of RapidIO transactions, providing maximum insight into signal behavior to resolve signal integrity challenges and to verify that designs comply with RapidIO AC specifications.

As high-speed buses such as RapidIO continue to increase in complexity, signal aberrations introduced by environmental, mechanical and electrical conditions become a significant challenge. High-performance, real-time oscilloscopes, such as the TDS6604, TDS7000 Series and CSA7000 Series, provide an ideal solution to measure and characterize these aberrations.

Depending on your RapidIO implementation, you will need to select an oscilloscope that will allow you to make your analog measurement, as specified in the chart below.

Data Rate	Clock Rate	Unit Interval	Time to Valid Data	Rise Time	Signal Bandwidth*
500 Mb/s	250 MHz	2000 ps	370 ps	200 ps	1.75 GHz
750 Mb/s	375 MHz	1333 ps	266 ps	133 ps	2.63 GHz
1000 Mb/s	500 MHz	1000 ps	212 ps	100 ps	3.50 GHz
1500 Mb/s	750 MHz	666 ps	158 ps	66.6 ps	5.26 GHz
2000 Mb/s	1000 MHz	500 ps	125 ps	50 ps	7.00 GHz

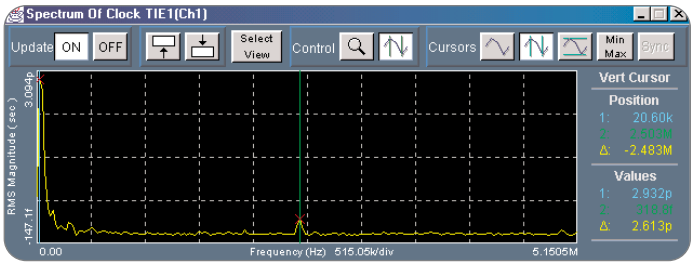
* Approximations based on 0.35/rise time rule.

Jitter Timing and Analysis

Jitter component identification and measurement is a necessary debug tool in the design of communications equipment, required for several serial data communication standards, such as RapidIO. The TDS6604 digital storage oscilloscope, equipped with TDSJIT3 jitter analysis software, delivers the highest accuracy real-time jitter measurements available in the industry, enabling designers to verify that RapidIO implementations meet the RapidIO AC specification defined by the RapidIO Trade Association. Its comprehensive jitter analysis algorithms simplify the discovery of jitter and its related sources so that engineers can accelerate the design process. This software package enables engineers to characterize random and deterministic jitter (Rj/Dj) and predict bit error ratio (BER) to quickly determine overall system quality and rapidly deliver more robust designs to market.

In RapidIO implementation, jitter compliance measurements are made using mask testing. While mask testing is valuable in considering the long-term effects of jitter components like wander, amplitude noise, gain stability, DC stability and DC drift, this technique does not help to identify any of the causes of the jitter. Using a real-time oscilloscope to measure jitter on a cycle-by-cycle basis gives engineers the ability to look beyond the basic signal to closely examine the jitter itself. An FFT plot of the jitter can quickly show power supply modulation effects, crosstalk from adjacent circuits, duty-cycle distortion and data-dependent effects due to transmission losses (see Figure 10).

Another advantage of using a real-time oscilloscope with an application package like TDSJIT3 to measure jitter is the ability to measure data signals and accurately predict eye closure that would otherwise take hours or even days to collect on an infinite persistence display. By using the BER capabilities in TDSJIT3, engineers can determine what the peak-to-peak jitter will be at 10^{-12} bits in just a few seconds. Any other technique used to estimate or measure BER can take several minutes to several hours: 30 minutes is a typical test time for mask analysis.

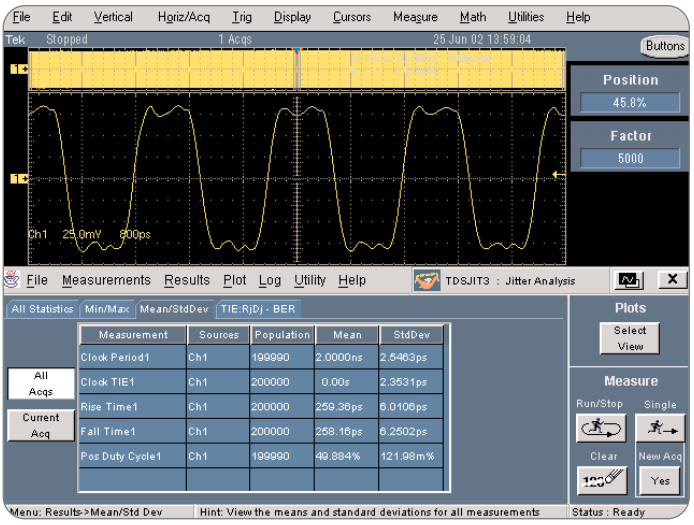


▶ ***Figure 10.*** *Jitter Spectrum.*

To measure other defined RapidIO requirements, like duty cycle (DC), static skew (t_{DPAIR}), and dynamic clock uncertainty (t_{DCU}), a real-time oscilloscope is required. Coupled with a real-time oscilloscope, application software like TDSJIT3 can be used to quickly and accurately measure these signals, either providing confidence that the signal is behaving as expected or offering additional insight into why the signal is behaving poorly. Even simple parameters like rise time and fall time (t_{RISE}, t_{FALL}) can exhibit changes occurring on a cycle-by-cycle basis that detrimentally effect circuit performance and are easily missed using non-real-time measurement techniques (see Figure 11).

Using equivalent-time instruments in infinite persistence mode to make timing measurements provides only a sample of the data stream, leaving large gaps in short-term information. Real-time instruments can be used to capture and display this short-term data, and can also be used in infinite persistence mode to capture long-term effects. TDSJIT3 jitter analysis software can plot any measurement variation versus time to provide engineers with insight into how or why the signal is being affected. This software can also plot the frequency spectrum of any measurement.

Again, mask tests can specify the absolute limits of a signal without individual parameters like rise and fall times, clock jitter or amplitude noise, but the mask test also requires that sufficient waveforms be recorded so that the resulting eye pattern is not materially changed by further increasing the recordings. Since no discrete bit tests are possible with a mask test, establishing a confidence level is difficult, so a very long test is indicated: 30 minutes or more for a reasonable population. Using advanced analysis techniques, TDSJIT3* running on a TDS6604, CSA7404 or TDS7404 real-time oscilloscope provides a faster and more efficient method to determine compliance.

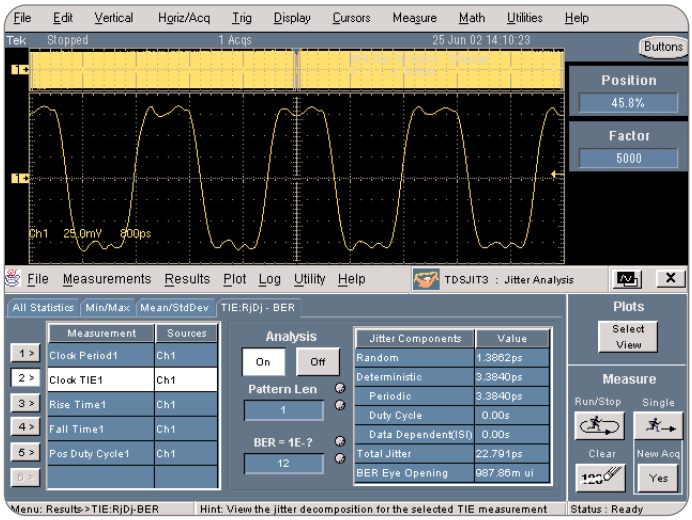


▶ ***Figure 11.*** *Real-time oscilloscopes permit analysis of cycle-cycle jitter effects.*

* TDSJIT3 correlates to standard BER testing with 2.1% at 10^{-12} BER.

Let's examine a RapidIO bus conveying data between two ports. The data rate is specified at 2 Gb/s with one UI being 500 ps. Using a real-time oscilloscope, you can easily measure the maximum data-to-data skew and maximum clock-to-data skew in addition to other static parameters. You can also directly measure clock jitter (t_{DCU}) using the Clock Period measurement standard deviation and peak results. Using TDSJIT3 also allows you to measure the eye opening of a signal at a specified BER level. Using the Clock TIE measurement, TDSJIT3 reports the estimated UI eye opening at the specified BER level and reports the total jitter broken down into its random and deterministic components (see Figure 12). If in measuring the t_{DCU} jitter the eye is closed beyond the specified limits, the discrete Rj/Dj results can be viewed to find what is causing the bulk of the jitter, and in the case of periodic jitter, the spectrum can be viewed to locate frequency relationships to a power supply or nearby oscillator frequency. Tests can easily be repeated and results can be correlated with confidence. And such tests are completed and results reported within seconds (using a single short oscilloscope acquisition of 10 µs duration or less).

Objectively looking into the symptoms and causes of signal integrity issues requires attention to correct probing techniques, acquisition system performance, measurement and analysis tools. No longer is simply viewing a waveform adequate; there is simply too much information in the typical signal for easy human comprehension. Using tools like the real-time oscilloscope with optional software components allow engineers a wide range of measurement and analysis capability to examine their design and improve its circuit performance.



▶ ***Figure 12.*** *TDSJIT3 reports the estimated eye opening at the specified BER level and breaks down its random deterministic components.*

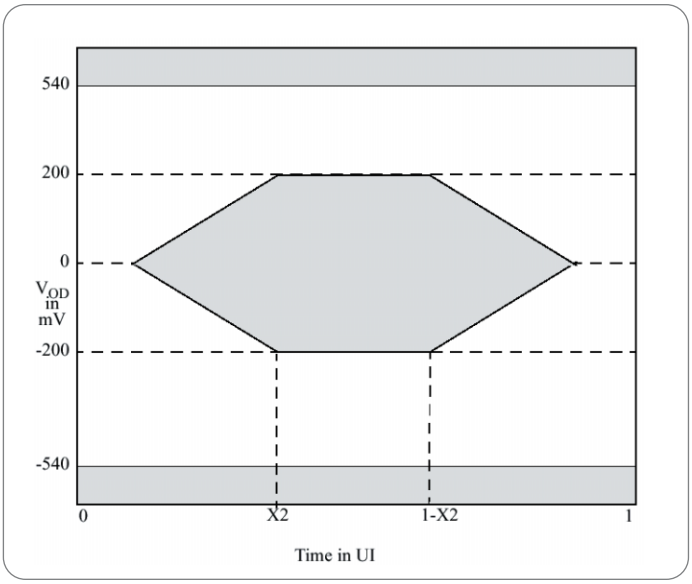
Compliance Testing with Communications Masks and RapidIO Eye Diagrams

Eye Diagrams

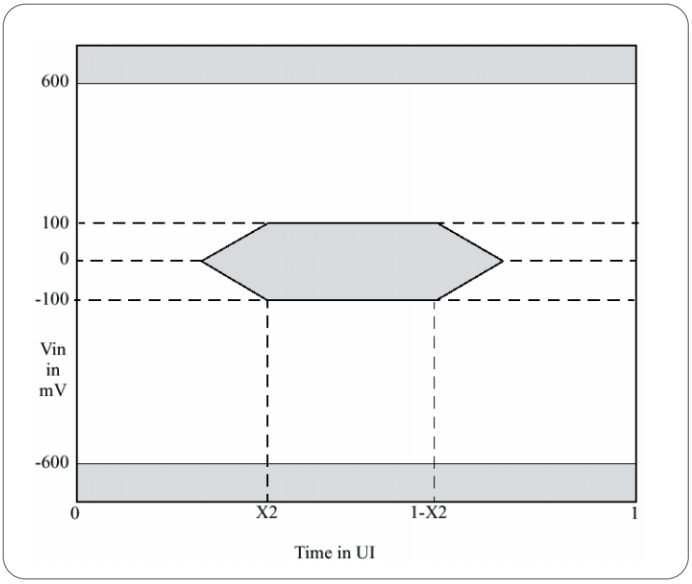
The "eye diagram"—the display that results from the overlap of a series of data waveforms—is the most common method of characterizing the quality of a signal. It is obtained when the oscilloscope is triggered synchronously to the data stream, while the input channel is connected to the data stream carrying random or pseudorandom bits. A synchronous clock signal, the data itself or the clock recovered from the data (if the oscilloscope has a clock recovery circuit) is used to trigger the oscilloscope. In one captured screen, all possible signal transitions of the signal are displayed, hence the eye opening, noise, jitter, rise and fall times and amplitude can be observed and measured from a single picture.

An eye diagram is a very convenient oscilloscope display that presents the most important time-domain signal characteristics all at once, saving time and showing the interaction of rise and fall time, overshoot, undershoot, ringing, jitter and noise. This display can be used for qualitative analysis, whereas the embedded statistical database of the oscilloscope can be used to make quantitative measurements.

Rather than extracting numeric information on the signal characteristics, the two-dimensional shape can easily be compared to a group of violation zones called a mask (see Figures 13, 14, 15 and 16). Masks are defined by and for each standard. Comparing the shape of an eye to a mask is a quick, efficient method of ensuring that the transmitter source signal will not cause excessive degradation of the receiver performance.



▶ ***Figure 13.*** *RapidIO Transmit Mask*



▶ ***Figure 14.*** *RapidIO Receive Mask*

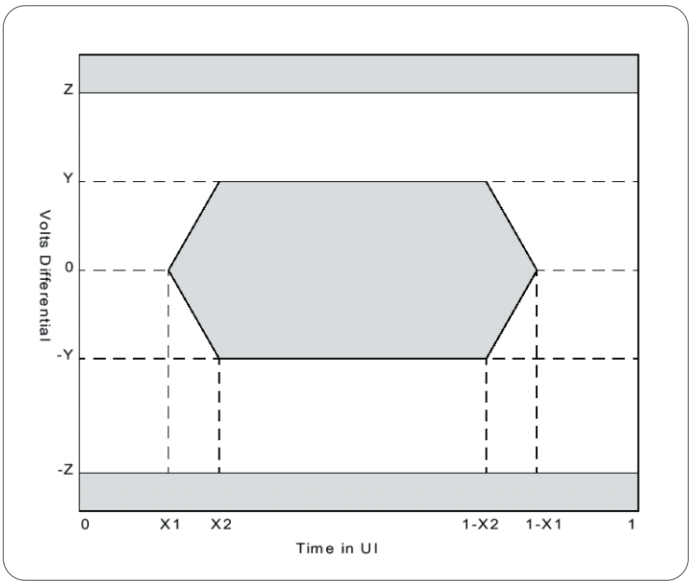
Eye Diagram Mask Testing

Eye diagram tests are a major component of the compliance and interoperability measurements listed in the RapidIO specifications. Specifically, the mask tests detailed in RapidIO AC specifications for both driver and receiver require eye diagram measurements (see Figures 13 and 14). The TDS6604, TDS7000 Series and CSA7000 Series real-time oscilloscopes are all excellent choices for these measurements. These oscilloscopes have a built-in clock recovery circuitry that can be used as a trigger source to expose pattern dependent anomalies or dropouts that data edge detection would miss.

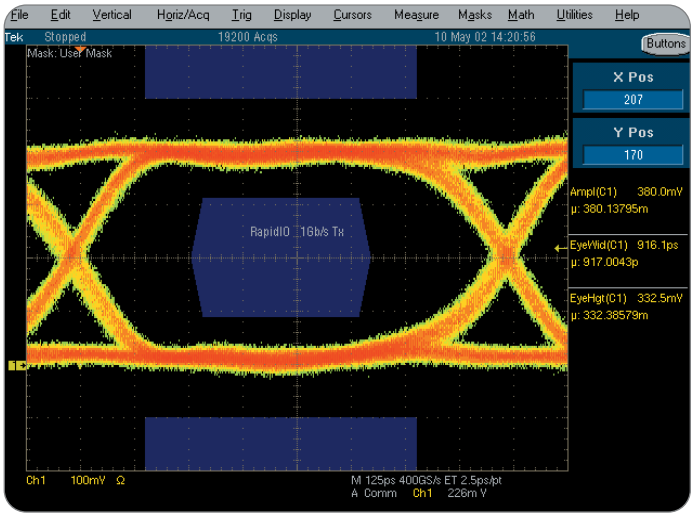
To perform an eye diagram test on an electrical signal, follow these general steps.

1. Connect the signal from the far end of the transmitter, exactly as it would enter the receiver, into the oscilloscope by using a breakout board. Start by looking at a single line of the differential pair, or use a differential probe such as the P7330. A RapidIO waveform will appear on that channel.
2. Select the RapidIO Mask corresponding to the data rate selected from the mask menu. (Note: This procedure assumes that there is an Option SM on the TDS6604 or on the TDS7000 Series. This feature is standard on the CSA7000 Series.)
3. Press Auto Set. (Note: If the mask is available as a user mask, then the signal will need to be adjusted manually.)
4. The eye diagram will appear on screen as shown in Figure 15.
5. It is also easy to use the native instrument mask testing capabilities of the oscilloscope to run a known number of waveforms or samples through the mask testing system. The system can then to stop and report a PASS or FAIL condition after it processes the prescribed waveform (or sample) population.

Please refer to www.tektronix.com for further information about how to setup and perform mask testing with real-time oscilloscopes.



▶ ***Figure 15.*** *Example of an eye diagram mask defined in differential voltage and Unit Interval.*



▶ ***Figure 16:*** *Actual RapidIO 1Gb/s Tx signal captured with a real-time oscilloscope. It passes the mask test.*

Conclusion

The emergence of RapidIO bus technology brings significantly increased transmission speeds to enable the design of next-generation networking and communications equipment, but with it comes compliance and interoperability issues for those design engineers who strive to implement RapidIO ports into their designs.

RapidIO compliance and interoperability testing will require these engineers to examine both the protocol and physical layers of RapidIO bus activity. In conjunction with RapidIO's HIP architecture, the ideal measurement system—logic analyzer, oscilloscope, probes and test software—will enable designers to capture, view and analyze specific signals of interest to ensure accurate, efficient verification, characterization and debug for RapidIO implementation.

Tektronix offers a comprehensive solution for RapidIO implementation that integrates the industry's superior logic analyzer, the TLA700 Series, with the world's highest performance digital oscilloscopes, the TDS6604, TDS7000 Series and CSA7000 Series. The TMS805 RapidIO support package, TDSJIT3 jitter analysis software package and communications-focused capabilities of the CSA7404 transform these instruments into highly specialized tools that enable the implementation of RapidIO technology for the design of next-generation networking and communications equipment.

The Integrated Tool Set for RapidIO Implementation

Together, Tektronix world-class logic analyzers, high-performance oscilloscopes and industry-leading probes deliver superior probing, triggering, display and analysis capabilities to enable design engineers to quickly and easily implement RapidIO into their designs.

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For Further Information

Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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