



Understanding and Performing MIPI[®] D-PHY Physical Layer, CSI and DSI Protocol Layer Testing

Application Note

Introduction

Currently many technologies are used in designing mobile or portable devices. These current interfaces are not well defined and are proprietary for each component or subsystem vendor. This fragmentation in the interfaces has made it difficult to quickly bring out mobile/portable products into the market with growing feature sets, higher performance, improved battery life, re-usability, and smaller form-factors, at lower costs.

MIPI Alliance was formed to define the hardware and software interfaces that would bring standardization, improve interoperability and help reduce many of the drawbacks faced by the mobile handset developers and manufacturers. With new MIPI technologies, all of the above problems are solved better. These MIPI standards are expected to revolutionize the entire mobile industry.

MIPI is a registered trade mark of MIPI Alliance www.mipi.org.

D-PHY/CSI/DSI Background

The MIPI Alliance defines D-PHY as a re-usable, scalable physical layer for interfacing various components such as cameras and displays to baseband processors in next generation smartphones, tablets, and other portable devices. Unlike many of the existing interfaces, D-PHY is unique because it can switch between differential (High Speed) and single-ended (Low Power) mode in real time depending on the need to transfer large amounts of data or to conserve power to prolong the battery life. The D-PHY interface is capable of operating in simplex or duplex configuration with single data lane or multiple data lanes, giving a flexibility to avail the links as needed. In addition, clock is always uni-directional (Master to Slave) and is in quadrature phase with data.

This design complexity introduces some unique challenges for testing and validating D-PHY based interfaces. Transmitter validation for D-PHY designs requires accurate jitter and timing analysis to the latest specifications coupled with minimal testing times.

With the inclusion of high resolution displays and cameras with the ability to capture or play high definition videos, the amount of data transfer needed to achieve this high definition functionality has increased tremendously. The Camera Serial Interface (CSI-2) and the Display Serial Interface (DSI) are the two packet-based high level protocols that carry image data between the peripheral and the application processor. Both these protocols use the D-PHY physical layer.

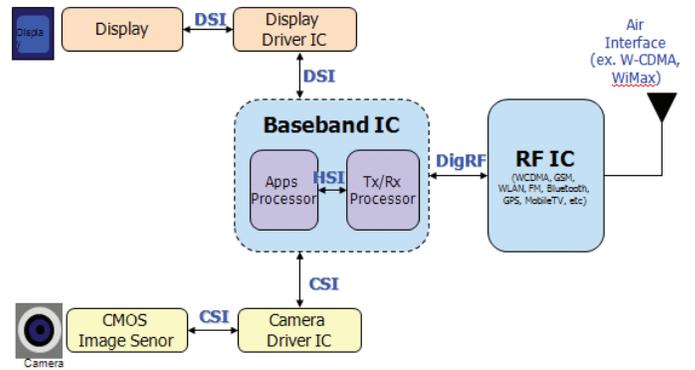


Figure 1. Block diagram of a typical mobile device.

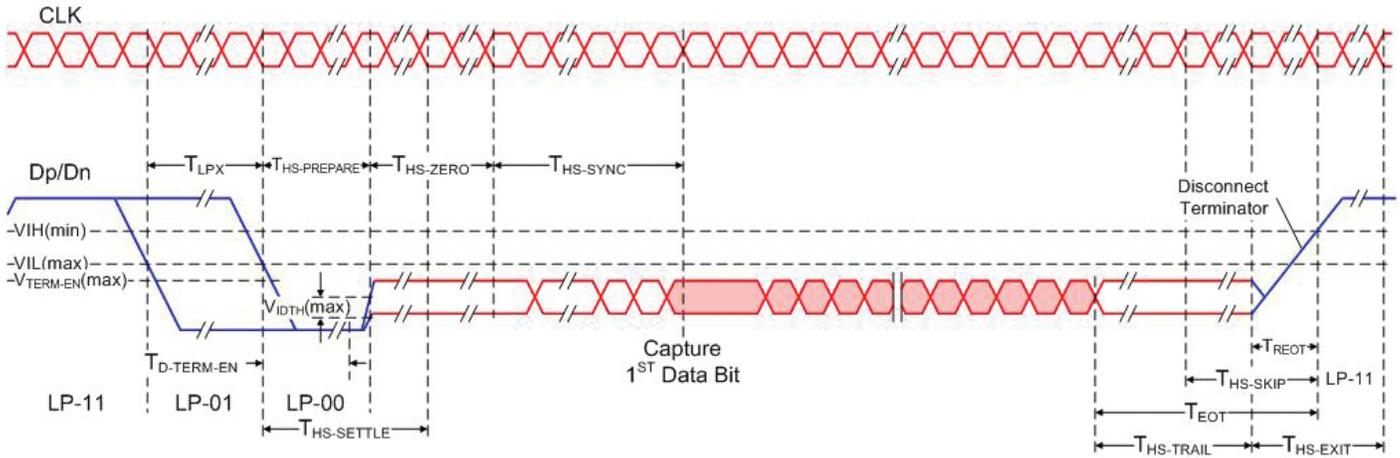


Figure 2. Modes and States in a D-PHY Data lane.

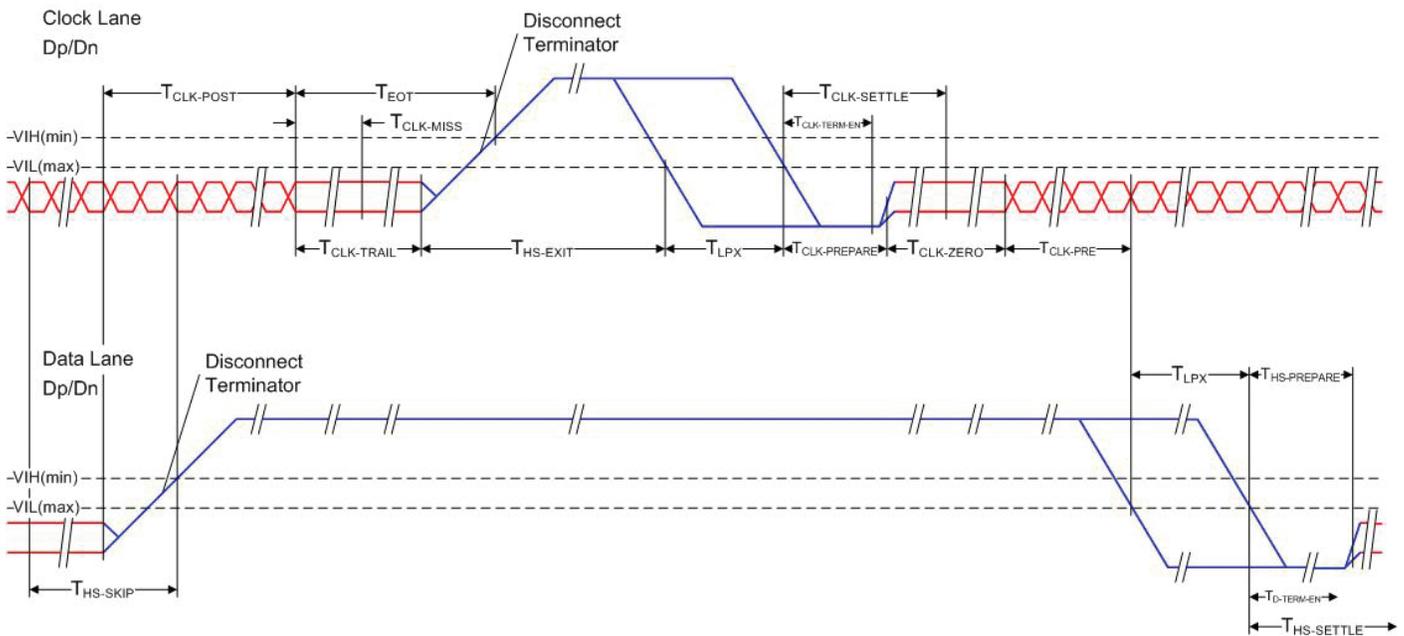


Figure 3. Modes and States in a D-PHY Clock lane.

Electrical Signal Challenges

A D-PHY interface can have a minimum configuration of one clock lane and one data lane, and a maximum configuration of one clock lane and four data lanes. As shown in Figure 2, each data lane operates in one of two modes: High Speed or Low Power. This means that the same two physical data paths alternate between high speed differential signaling and low power single-ended signaling.

In High Speed (HS) mode, the differential voltage is 140 mV min, 200 mV nominal, 270 mV max, with the data rate extending up to 1 Gb/s. The HS mode consists of two possible states: Differential-0 (HS-0) and Differential-1 (HS-1). In Low Power (LP) mode, the signaling is two single-ended with 1.2 V swing operating at a maximum data rate of 10 Mb/s. The LP mode consists of four possible states: LP-00, LP-01, LP-10, and LP-11. In addition, the rise times in the HS mode are different from that of the LP mode.



Figure 4. Pinpoint triggering.

Most of the HS and LP measurements can be performed while the signal transitions from HS mode to LP mode. The oscilloscope's trigger features enable you to acquire stable transitions from HS mode to LP mode. As shown in Figure 4 screen capture, pinpoint triggering is used to trigger and capture the DP and DN transition edges, and the HS burst.

Importance of Signal Integrity and Terminations

D-PHY operates at low speeds as well as at high speeds. At low speeds the signals are singled-ended, where the other end is not terminated. At high speeds, the signals are differential, but terminated during data transmission by the Receiver automatically.

Some of the MIPI interfaces might operate at broadcast mode where the signal will not be terminated at all, but the transmitter continues to transmit the signal in broadcast mode.

During the transition of signal from single-ended to differential, the impedance imbalance that occurs on the line which can cause the glitch may be due to non-synchronous termination transition between the TX and RX. In broadcast mode the source impedance changes, but the Receiver impedance remains open, so that you can see the glitch on the signal.

Most of the Global timing parameters must be measured during the HS entry mode. These need to be performed as Clock alone tests, data alone tests and Clock-to-data tests. You also need to acquire the C_p , C_n and D_p , D_n simultaneously, on separate channels of an oscilloscope

The probes that you use should be optimally chosen so that its impact should be minimal on the signal for both single-ended and differential operations. The probe should also be capable of capturing the activity on the bus during the transition.

We use a differential probe so that it has minimal impact during both non-terminated and terminated operations. Also, it has minimal input capacitance so that its effect in low frequency will not alter the signal rise time or fall time for both the speed of operations.

The measurement algorithm is capable of tolerating the Glitch as shown in Figure 4 when you operate in the broadcast mode and are still able to perform the measurement by selectively qualifying the HS entry mode.

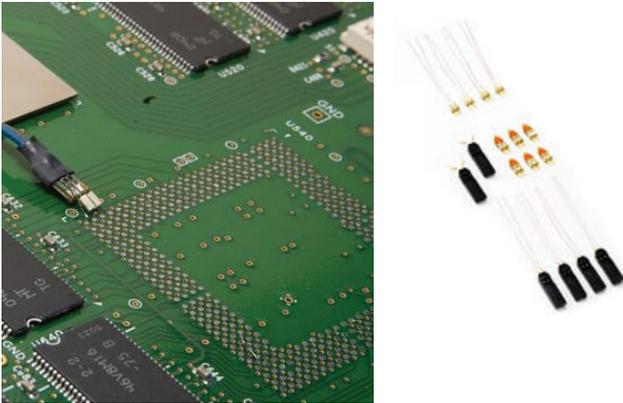


Figure 5. P7380 probe used with a probe-tip #020-3035-00 of P6780.

Signal Accessibility

The mobile designs are tiny in nature, with high packing density. Probing these signals using any regular probe is a challenging task. The signal traces cannot be extended at ease to meet a specific choice of probe. To probe signals from a miniature circuit, the probes with a wide range of accessories like miniature tips, micro clips, solder-tips, etc are needed. For example, a P7360 probe with square pin adapter, and a probe-tip of P6780 (Partnumber 020-3035-00, kit of 15 tips) provides miniature accessibility and best fidelity.

The probes should be capable of supporting both HS and LP modes, with variance of different voltage levels, multiple speeds of operations and different terminations. Other recommended probes like P7225 can also be used to acquire a D-PHY signal in broadcast mode.

The mobile/ portable devices also must be tested at extreme environmental conditions such as thermal chambers. In such cases, probes should provide sufficient long lead accessories such XL cables and probe tips that can sustain in a temperature chamber.



Figure 6. Risetime measurements at various bandwidths.

Choice of Oscilloscopes

The D-PHY bus data rates vary from 80 Mb/s to 1 Gb/s, with typical implementations at 500 Mb/s. According to base or conformance specifications, the rise times are no faster than 150 ps and no slower than 0.3 UI (Unit Intervals). For example, to measure a 150 ps rise time of a signal (20 to 80 percent) using a flat-response oscilloscope to an accuracy of +/- 5 percent would require a minimum of 3.2 GHz ($1.2 \times 0.4 / 150$ ps) bandwidth oscilloscope.

The screen capture in Figure 6 with a source of 148 ps indicates an oscilloscope with a bandwidth of 3.5 GHz onwards is sufficient for D-PHY signal measurements.

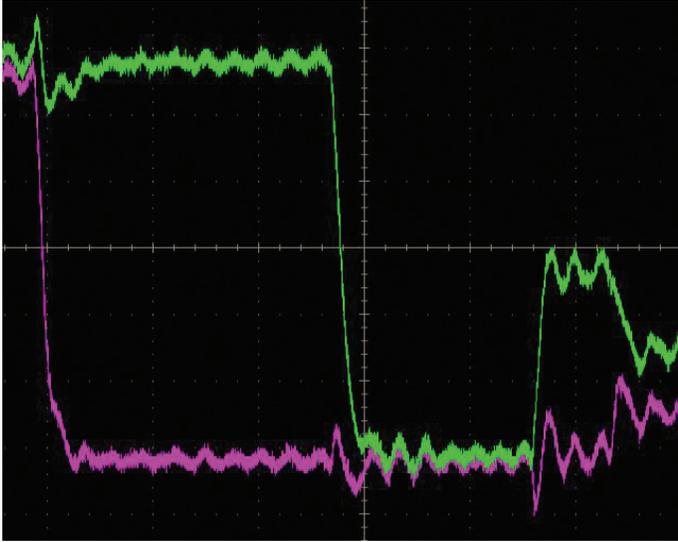


Figure 7.

Broadcast and Terminations

Before beginning of Data burst transmission, the High speed data transmission happens in burst and it start with LP-01 state and end at stop state (LP-11) The minimum payload can be as less as one of one byte where as the maximum payload is protocol dependent.

During the start of transmission drivers get into HS-Rqst state by driving the lane to LP01 state for the time TLPX, During this interval, It is expected at the RX to change its termination from High impedance to low impedance state. While testing, It is not always possible to have TX and RX together for example, device with MIPI interface may be forced to operate in broad cast mode (Data is sent continuously) where the Rx is not present. During the HS entry on these situation, the lanes are switched to operate at expected termination, then there is spike that occurs during the end of TLPX which might prevent us to do the measurement of Thevanin low voltage at LP 00 state and other timings.

Tektronix D-PHY solutions designed with algorithms to handling these scenarios as shown below, which are most common during the debugging and the integration. You can perform all the measurements related to HS timing during the HS entry under these practical circumstances.

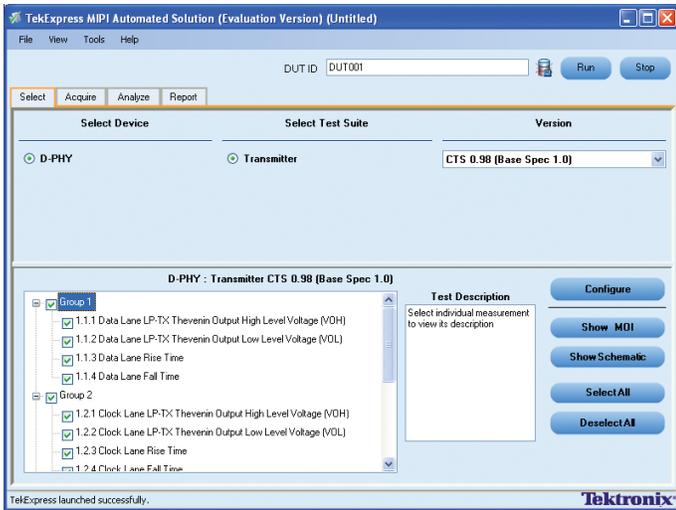


Figure 8. D-PHYTX fully-automated solution.

| Test Name | Measurement Details | Low Limit | Measured value | High Limit | Margin | Units | Test Result | Compliance Mode | Analysis Time | Comments |
|---|--|-----------|----------------|------------|-----------|-------|-------------|-----------------|---------------|----------|
| 1.1.1 Data Lane LP-TX Theverin Output High Level Voltage (VOH) | Data Lane LP-TX Theverin Output High Level Voltage (V) | >= 1.1 | 1.17E+00 | <= 1.3 | 0.089 | V | Pass | Yes | 1 Min | |
| | Data Lane LP-TX Theverin Output High Level Voltage (mV) | >= 1.1 | 1.18E+00 | <= 1.3 | 0.084 | mV | Pass | Yes | 1 Min | |
| 1.1.2 Data Lane LP-TX Theverin Output Low Level Voltage (VOL) | Data Lane LP-TX Theverin Output Low Level Voltage (V) | >= -60 | 8.00E+00 | <= -50 | 58.42 | mV | Pass | Yes | <1 Min | |
| | Data Lane LP-TX Theverin Output Low Level Voltage (mV) | >= -60 | -8.00E+00 | <= -50 | 42.58 | mV | Pass | Yes | <1 Min | |
| 1.1.3 Data Lane Rise Time | Data Lane Rise Time (RP) | - | 1.10E+11 | <= 25 | 14.47 | ns | Pass | Yes | 1 Min | |
| | Data Lane Rise Time (RN) | - | 1.00E+11 | <= 25 | 14.5 | ns | Pass | Yes | 1 Min | |
| 1.1.4 Data Lane Fall Time | Data Lane Fall Time (RP) | - | 1.00E+11 | <= 25 | 14.66 | ns | Pass | Yes | <1 Min | |
| | Data Lane Fall Time (RN) | - | 9.70E+10 | <= 25 | 15.24 | ns | Pass | Yes | <1 Min | |
| 1.2.1 Clock Lane LP-TX Theverin Output High Level Voltage (VOH) | Clock Lane LP-TX Theverin Output High Level Voltage (V) | >= 1.1 | 1.20E+00 | <= 1.3 | 0.1 V 0.1 | mV | Pass | Yes | 1 Min | |
| | Clock Lane LP-TX Theverin Output High Level Voltage (mV) | >= 1.1 | 1.18E+00 | <= 1.3 | 0.092 | mV | Pass | Yes | 1 Min | |
| 1.2.2 Clock Lane LP-TX Theverin Output Low Level Voltage (VOL) | Clock Lane LP-TX Theverin Output Low Level Voltage (V) | >= -60 | 8.00E+00 | <= -50 | 58.42 | mV | Pass | Yes | <1 Min | |
| | Clock Lane LP-TX Theverin Output Low Level Voltage (mV) | >= -60 | -8.00E+00 | <= -50 | 2.98 | mV | Pass | Yes | <1 Min | |
| 1.2.3 Clock Lane Rise Time (SP) | Clock Lane Rise Time (SP) | - | 8.50E+00 | <= 25 | 20.36 | ns | Pass | Yes | <1 Min | |

Figure 9. D-PHYTX test report.

Solution for D-PHY Testing

TekExpress™ software with D-PHYTX option and chosen oscilloscopes and probes provides a completely automated, simple, and efficient way to test D-PHY signals, specifically for Conformance and Verification.

The TekExpress software provides a graphical user interface (GUI) and an intuitive workflow through setting up and testing,

irrespective of lane terminations. D-PHYTX allows you to perform the measurements under in-circuit operations, along with setup configurability, limits-editing, and customization for a DUT-specific data rate.

The D-PHYTX reports not only provides Pass/Fail summary table, but also margin details on each test in a “single-exportable” report.

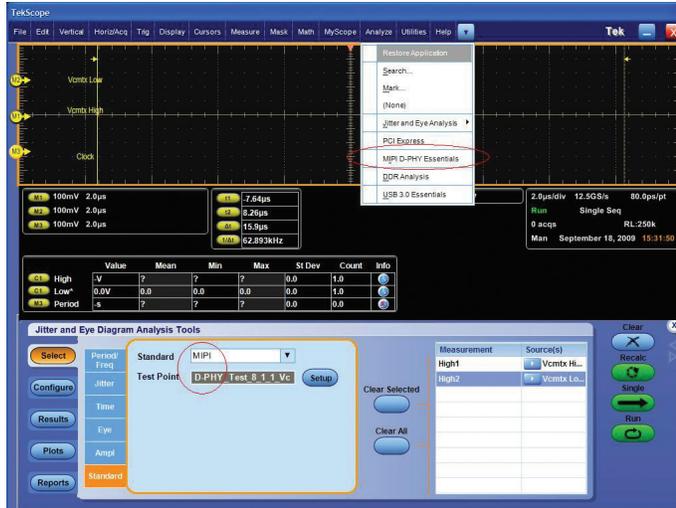


Figure 10. DPOJET D-PHY Essentials.

Specifically for D-PHY Debug and Analysis, DPOJET software with Option D-PHY provides an essential set of D-PHY Transmitter measurements with greater flexibility in the test setup.

D-PHY Essentials DPOJET Measurements and Setup Library (Opt. D-PHY) for the DSO/DSA70000B Series oscilloscopes provides a semi-automated D-PHY Transmitter solution. D-PHY provides precise verification, characterization, and debug environment built upon the general-purpose analysis capabilities of DPOJET.



Figure 11. DPOJET D-PHY Essential for Debug and Analysis.

In Opt. D-PHY, a comprehensive analysis environment is provided allowing you to quickly create a customized setup, and use the oscilloscope built-in/ DPOJET measurements and oscilloscope cursors. It enables you to perform timing intensive analysis on clock signals, data signals, and clock-data timing.

For example, single or multiple eye diagrams can be displayed at one time allowing you to analyze the effects of different clock recovery techniques. With DPOJET you can easily compare the results of both eye diagrams at the same time.

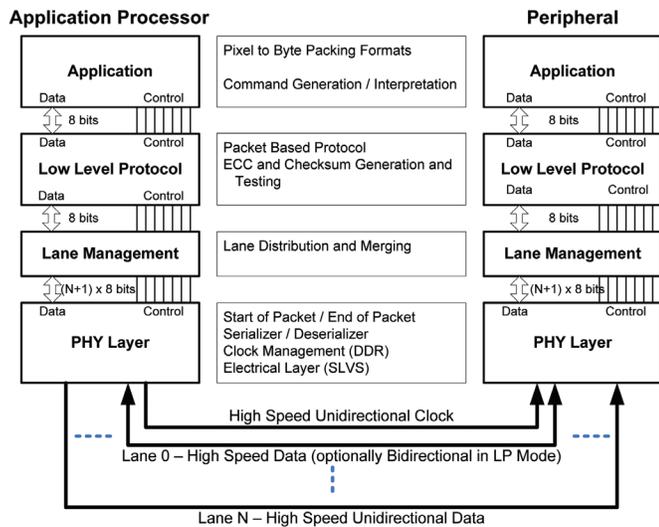


Figure 12. MIPI DSI Layered Architecture.

DSI or CSI-2 Protocol Testing Complexity

DSI can be organized into several functional layers. The Physical layer is responsible for carrying the information between the Application processor and the peripheral (in this case the Display). The Physical layer conforms to the D-PHY specification.

Lane Management Layer: The transmitter distributes the data that is transferred to several lanes (1 to 4) based on the bandwidth requirement.

The protocol layer defines how the bits and bytes are organized into packets and which bits constitute the header and payload as well as taking care of the error checking.

The application layer is responsible for interpreting the data from the below layer into pixel information or commands.

Planning for future capability & M-PHY

Planned for later implementation is a higher speed variant of D-PHY called M-PHY. With data rates exceeding 5 Gb/s, the M-PHY provides designers with the ability to speed up memory transfer and CSI/DSI interface speeds.

The MIPI Alliance intends to have M-PHY be an extension to existing D-PHY so that ongoing support for both PHY types are expected in the future.

For testing considerations; M-PHY is an 8b/10b signal with an embedded clock. It will require a faster oscilloscope for the higher speed characterization efforts. In addition, M-PHY signal integrity testing will need to include accurate clock recovery methods like those found in the Tektronix DPOJET platform. Look for more information as the M-PHY Testing Specifications are completed in late 2010. In the interim, contact Tektronix directly for more information and planning support.



Figure 13. Original Image.



Figure 14. Image Displayed on the Screen.

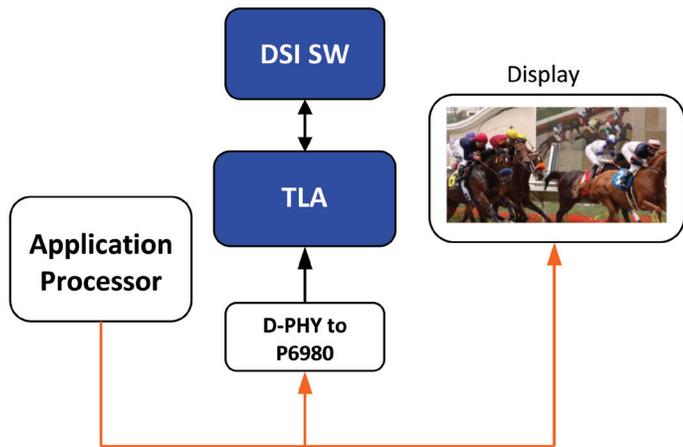


Figure 15. Typical Setup for DSI Digital Debug.

A mobile handset will consist of several subsystems. In most cases each subsystem is developed separately and then all the subsystems are integrated to make a complete system.

Consider a scenario when during system level integration and testing the image in Figure 13 is sent by the applications processor to the display.

In such scenario, the resulting image on the display unit would be as shown in Figure 14.

Figure 15 shows a typical setup that is used to debug this problem. The D-PHY to P6980 adapter from The Moving Pixel Company is a solder-in adapter that provides a single set of loads to the system. It separates the LP and the HS signals before they are sent to the Logic Analyzer.

The data that is acquired in the Logic Analyzer can be viewed at different levels of abstraction. The listing window shows the state transitions that occur in the D-PHY Physical layer,

| Sample | MIPI_DSI Lane0 State | MIPI_DSI LP_Data | MIPI_DSI LP_Data0 | MIPI_DSI LP_Data1 | MIPI_DSI LP_Data2 |
|--------|----------------------|------------------|-------------------|-------------------|-------------------|
| 524 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 525 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 526 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 527 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 528 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 529 | HS-Request | 01000000 | 01 | 00 | 00 |
| 530 | HS-Request | 01000000 | 01 | 00 | 00 |
| 531 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 532 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 533 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 534 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 535 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 536 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 537 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 538 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 539 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 540 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 541 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 542 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 543 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 544 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 545 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 546 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 547 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 548 | HS-Prepare | 00000000 | 00 | 00 | 00 |
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| 550 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 551 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 552 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 553 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 554 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 555 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 556 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 557 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 558 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 559 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 560 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 561 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 562 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 563 | HS-Prepare | 00000000 | 00 | 00 | 00 |
| 564 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 565 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 566 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 567 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 568 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 569 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 570 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 571 | HS-Sync | 00000000 | 00 | 00 | 00 |
| 572 | Lane0 HS-Data: 0x15 | 00000000 | 00 | 00 | 00 |
| 573 | -- | 00000000 | 00 | 00 | 00 |

Figure 16. Listing Display.

when the links moves from LP mode to HS mode (and all the states in between) before it begins to transmit highspeed DSI packets with image data. This provides link level information and helps in debugging the physical layer.

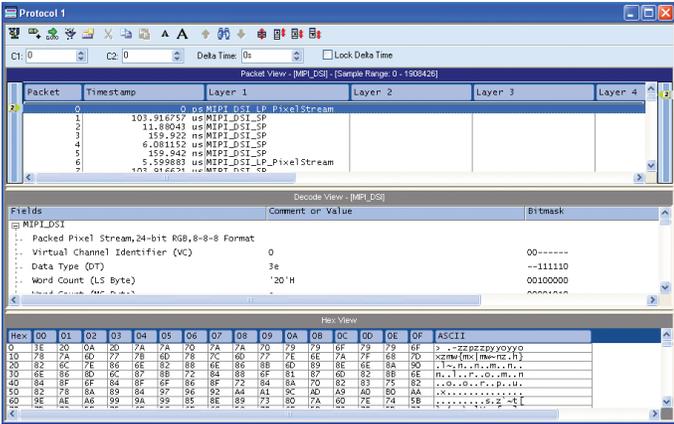


Figure 17. Protocol Decode Display.

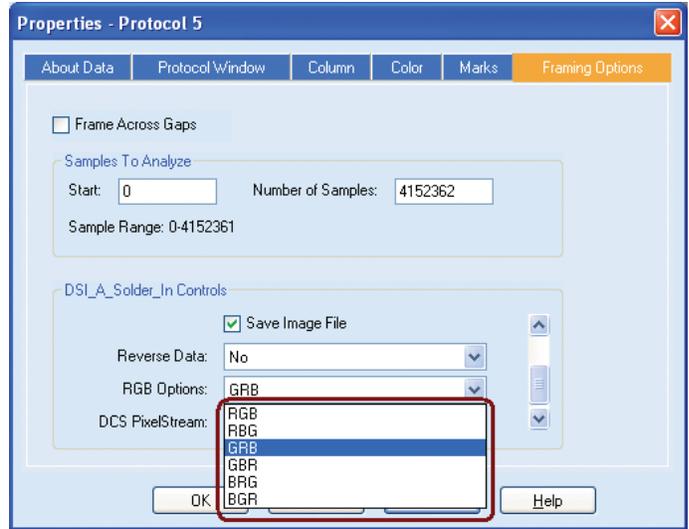


Figure 18. Export Options.



Figure 19. Saved Image with Modified RGB values.

The data can also be viewed at higher level of abstraction in the protocol view. In this view the acquired data is decoded into DSI packets and each field in the packet is decoded and displayed and errors in the packet field or the ECC/Checksum are highlighted in red thus making it easy to identify any transmission errors.

Apart from this, the acquired data can also be exported and saved as an image file; the image file can then be compared with the display to verify the correctness. In the scenario that we are considering, the image appears with a bluish tinge as shown in Figure 19.

During the image export, options are provided to interchange the RGB values as shown in the picture in Figure 18. These options could be used to see if after interchanging the RGB values the exported image matches the actual image that is sent. Using these options we can figure out if the data is being sent incorrectly by the transmitter. Figure 19 shows the exported image after the RGB values were interchanged.

If it turns out that the exported image matched the image that was sent then it could be problem with the display. More rigorous testing on the display can be done in a standalone mode. The DSI decode SW also has the following features:

- Decode and display of all types of Short and Long packets of MIPI DSI
- Supports all the following RGB Schemes:
 - RGB-888
 - RGB-565
 - RGB-666 Packed
 - RGB-666 Loosely Packed
- Supports upto 4 lanes
- Image rendering capability. Stores the pixel information in bmp format. Images are stored in C:\My Documents folder
- Image rendering capability for DCS Command Support
- Supports ECC and Checksum verification. If there is a mismatch, the Protocol Window displays the Error Packet in red
- Provides an RGB Option to support different R, G and B combinations
- MIPI DSI Packet Summary feature is added. The Packet Summary is written to a text file PktSummary.txt which is placed under "C:\My Documents"
- Renders partial images
- Supports LPDT mode decoding

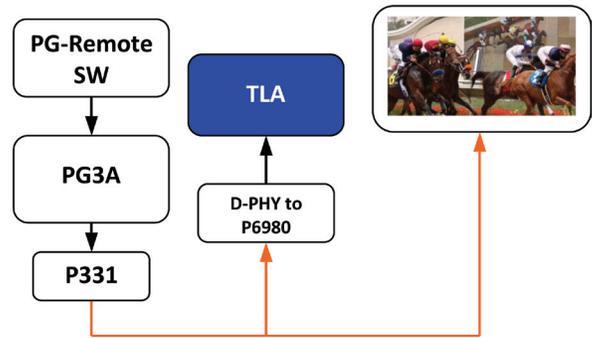


Figure 20. Typical Setup for Display Testing.

To test the display subsystem separately the following setup can be used. This setup can also be used during the development of the display subsystem or to evaluate the performance of different displays without the need to integrate them into a full system. This involves using The Moving Pixel PG3A with P331 D-PHY probe as a stimulus to generate the DSI data over D-PHY. The P331 probe features four data lanes and one clock lane. Data rate operation up to 1 Gb/s per lane is supported. LP Voh, HS Voh and Vol are adjustable.

The P331 also features an optional clock-in; the user can supply a clock signal which will be then used as output clock signal as well as clock the data out in the HS mode. They can also use this input to add jitter to the clock signal.

Because of the flexibility of the P331, it allows the user to test corner cases and recreate infrequent events to see the system's response to such events.

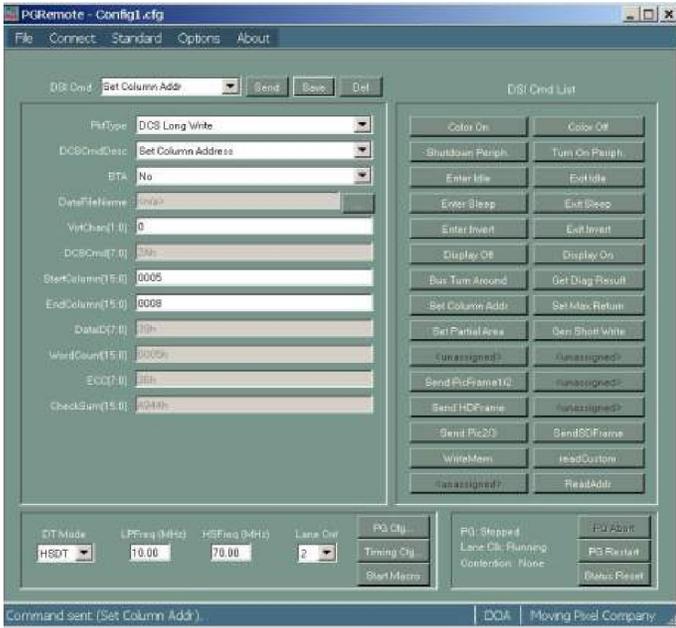


Figure 21. PGRremote Software.

The P331 probe is designed to be used with the PG-Remote software. The PG-Remote software is a separate software package that was expressly developed to provide an easy-to-use push button interface for user to generate the DSI or the CSI2 data. The software allows the user to operate at a protocol level than at bit level. All the packet types and the fields are predefined in the software the user must pick the packet type that needs to be generated and fill in the packet fields and click the Send button. The PG takes care of formatting the data and generating the output that confirms to the D-PHY standard. It also provides the option of creating macros with a predefined set of commands and assigning it to the button like other commands.

Once the setup shown in Figure 20 is done, an Image can be sent to the display in a specific format preceded by all the required commands to setup the display. This information can also be acquired by the Logic Analyzer (optional). The displayed image can then be compared to the image sent to verify the correctness.

In this way image or video information with several types of commands can be sent to the display to verify the correctness of the operation as well as compatibility with the other subsystems. The variable voltage, timing and skew parameters also allow us to do margin testing or evaluate display from different vendors.

Apart from this the PG along with the P331 can also support

- One lane to Four Lanes of D-PHY data
- Support Data rates of upto 1 Gb/s
- Supports both CSI2 and DSI protocols
- Several parameters like the voltage, skew and the timing can be varied on a per channel basis on both the High Speed and the Low Power Modes.
- The PG can play looping video and can insert commands during active video.
- The PG can be operated in several modes
 - Pushbutton Mode using the PGRremote software
 - Macro Mode using the PGRremote software
 - Scripting
 - Full remote control mode

The PG can also be used as a general purpose instrument to generate the required stimulus with different PG probes. The investment on a PG is preserved as it can be modified to suit different applications by changing the probe to generate different kinds of data.

Summary

The emergence of MIPI technologies solves a number of problems for the mobile industry around the need to expand feature sets and improve battery life while increasing bandwidth and lowering costs through component reuse. The MIPI testing requirements involve a daunting set of PHY layer checkpoints. The automated functionality provided by TekExpress with Option D-PHYTX together with Tektronix oscilloscopes and probes shortens the time to market and simplifies testing setup for D-PHY characterization and conformance tests to the latest specifications.

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