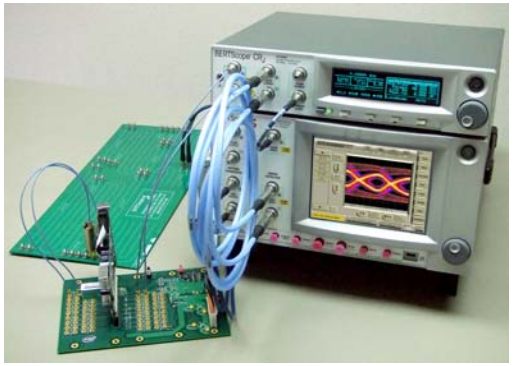
BSA Series BERTScope™ Bit Error Rate Analyzers Fact Sheet

The Confidence of a BERT with the Insight of a Scope

Features	Benefits
Pattern Generation and Error Analysis, high-speed BER Measurements up to 26 Gb/s	The combination of generation and analysis in one instrument enables receiver BER compliance testing for today's 2nd and 3rd Generation Serial Standards
Integrated Stress Generator for stressed eye sensitivity (SRS) and jitter tolerance compliance testing	A test signal's data rate, applied stress, and data pattern can be changed on the fly, independent of each other; enabling a diverse set of signal variations for testing chipset/system sensitivity.
Integrated, BER correlated eye diagram analysis with pass/fail masks for PCI Express, USB, SATA and other serial standards	Enhances the debug experience unlike other BERT's by providing a familiar eye diagram of the test results to compare against a standards specific mask.
Error Location and BER contour analysis on PRBS signals up to 26 GB/sec	Provides a quick understanding of signal integrity in terms of BER. Error location provides detailed BER pattern sensitivities to speed up identification of deterministic vs. random BER errors
Optional Jitter Map provides fast jitter decomposition, accurate stress calibration at the DUT input.	Fast, effective method for determining long pattern PRBS31 jitter composition with triangulation. Graphical representation makes jitter analysis more thorough, yet simpler to follow.
Optional Digital Pre-emphasis Processor provides user controlled pre-emphasis on pattern generator supplied data.	Enables testing with compliant signals for standards like PCI Express, 10GBASE-KR, SATA, 40GBASE-KR4, 100GBASE-CAUI
Optional Clock Recovery Units provide clock recovery up to 28.6 Gb/s	Enables compliant testing and accurate Eye Pattern Analysis for high-speed serial and communication system standards.

"Critical for resolving analog issues in digital systems"



Stressed Receiver Tolerance Testing with a BERTScope

Taking the stress out of receiver testing

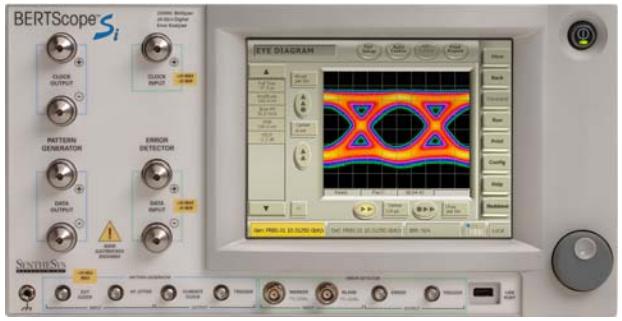
- Flexible PRBS Pattern Generation up to 26 Gb/sec
- BER Measurements and analysis to BER 10^{-12}
- High quality stress impairments including built in RJ, SJ, BUU, and ISI for worst case RX Test Characterization
- Flexible Clock Generation including SSC modulation for many serial standards
- BER-contoured masks support analysis of specified 1×10–12 eye opening.
- Accurate jitter analysis/display of jitter spectral components from 200 Hz to 90 MHz
- Jitter map enables decomposition of DJ into components like BUJ, DDJ, DCD, SRJ, F2
- Pattern capture for easy, customized signal generation

BSA Series BERTScope™ Bit Error Rate Analyzers Fact Sheet

Key Specs and Ordering Information

Models	Data Rate	Description
BSA85C	8.5 Gb/s	Bit Error Rate Analyzer
BSA125C	12.5 Gb/s	Bit Error Rate Analyzer
BSA175C	17.5 Gb/s	Bit Error Rate Analyzer
BSA260C	26 Gb/s	Bit Error Rate Analyzer
BSA85CPG	8.5 Gb/s	Pattern Generator
BSA125CPG	12.5 Gb/s	Pattern Generator
BSA175CPG	17.5 Gb/s	Pattern Generator
BSA260CPG	26 Gb/s	Pattern Generator

Service Options	Description
CA1	Provides a single calibration event or coverage
C3	Calibration service 3 years
R3	Repair service 3 years (including warranty)
R1PW	Repair service coverage 1-years post warranty
R2PW	Repair service coverage 2-years post warranty
R3PW	Repair service coverage 3-years post warranty



Recommended Software Options

F2	F/2 Jitter Generation at 8G/10.3125G (requires STR)
STR	Stressed Signal Generation (includes option ECC, MAP,PL,XSSC,JTOL,SF)
XSSC	Extended Spread Spectrum Clocking (SSC)
J-MAP	Jitter Decomposition SW (C Models only)
ECC	Error Correction Coding (C Models only)
LDA	Live Data Analysis SW (C Models only)
MAP	Error Mapping SW (C Models only)
PL	Physical Layer Test Suite (C Models only)
PVU	PatternVu EQ Processing (C Models only)
SF	Symbol Filtering SW (C Models only)
SLD	Stressed Live Data SW (C Models only)

Serial Standard Test Packages

SATATESTSW	Serial ATA Interop Test Suite Automation Software
PCIETB5G	PCI Express Test Bench for 5 and 2.5 GT/s
PCIETB125	PCI Express Test Bench for PCIe 3.0
PCIETK	PCI Express Compliance Interface Kit

Digital Pre-Emphasis Processor

DPP125	12.5 Gb/s 3-Tap Digital Pre-emphasis
4-TAP	Add 4-Tap capability to above processor

Clock Recovery Instruments

CR125A	1Mb/s to 12.5 Gb/s Clock Recovery
CR175A	1Gb/s to 17.5 Gb/s Clock Recovery
CR286A	1 Gb/s to 28.6 Gb/s Clock Recovery

Fixture, Cable & Kit Options

100PSRTFILTER	100 ps Rise Time Filter
BSA12500ISI	Differential ISI Board
PMCABLE1M	Phase Matched Cable Pr,1 m
SMAPOWERDIV	SMA Power Dividers
BSASATATEE	BSA-SATA-Tee for OOB Signaling
SATATESTPLUG	Serial ATA Plug to SMA Test Cable, 80 mm
SATATESTRECPT	Serial ATA Receptacle to SMA Test Cable 80 mm
BSARACK	BSA-Rackmount Kits

Key Applications	Benefits
▪ Silicon Verification & Debug	▪ Enables quick movement from BER Testing to Debugging on very fast silicon above 8.5 GB/sec.
▪ High Speed Serial RX Characterization	▪ Complete evaluation of BER performance while stressing the receiver for 2nd / 3rd Gen Serial Standards like PCI Express, USB.
▪ Signal Integrity of High Speed Communications Systems	▪ Support for Mask Testing, Jitter Peak, BER Contour, and Q-Factor Analysis enables a deep level of Signal Integrity insight.
▪ Design and Verification of Optical Transceivers	▪ Verifies performance using optical inputs and stressed eye analysis for Fibre Channel and IEEE803 Ethernet Standards

06/10 CL/WOW 65W-25456-0

Tektronix