BERTScope[™] CR125A, 175A, & 286A Clock Recovery Fact Sheet

Versatile Precision Clock Recovery and Analysis



Features	Benefits
Data Rate Range up to 28.6 Gb/s	Continuous data rate coverage for next generation I/Os including PCIe 3.0, 10GBASE-KR, 16xFC, 25 & 28G CEI and 100GBASE-LR-4 & ER-4.
Independent control, measurement, and display of phase lock loop (PLL) BW, JTF (jitter transfer function) and peaking.	Provides accurate "Golden PLL" response for transmitter jitter compliance testing and stressed receiver sensitivity test calibration. Provides full flexibility for device characterization.
Clock Recovery Input Equalization	Enables clock recovery on high ISI signals without impacting the data stream under test. Recovered clock enables other analysis including "clean eye", application of FIR filtering to signal, and BER testing.
Edge Density Measurement	Allows instant determination of the mark density of the signal under test.
Jitter Spectral Analysis and Frequency Gated Integrated Jitter Measurements	Provides 200 Hz to 90 MHz display of jitter vs frequency with cursor based measurements of jitter peaks' amplitude and frequency. Frequency gated integrated jitter measurements PCIe 2.0 compliance testing.
Optional 24 MHz PLL BW	Meets the JTF bandwidth requirements of USB 3.0, 6 G SATA, and PCIe-Gen 3.
Extensive set of subrate (recovered) clock outputs.	Frequently needed for device reference clocks.

"The choice for resolving analog issues in digital systems"



Instrumentation Quality Clock Recovery with BERTScope CR

Taking the stress out of receiver testing

- BER Measurements and analysis to BER 10⁻¹²
- BER-contoured masks support analysis of specified 1×10–12 eye opening.
- Independent control, measurement, and display of phase lock loop (PLL) BW, JTF (jitter transfer function) and peaking
- Accurate jitter analysis/display of jitter spectral components from 200 Hz to 90 MHz
- Jitter Spectral Analysis and Frequency Gated Integrated Jitter Measurements

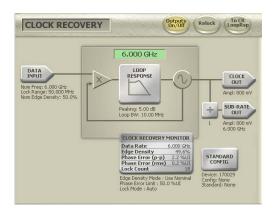


BERTScope[™] CR125A, 175A, & 286A Clock Recovery Fact Sheet Key Specs and Ordering Information

Models	Data Rate	Description
CR125A	12.5 Gb/s	Clock Recovery Instrument
CR175A	17.5 Gb/s	Clock Recovery Instrument
CR286A	28.6 Gb/s	Clock Recovery Instrument

Recommended Software Options		
GJ	Spectral Jitter Analysis	
PCIE	PCIe 2.5 and 5.0 G PLL Loop Analysis (Requires Option GJ)	
Recommended Hardware Options		
XLBW	Extends PLL BW to 24 MHz	
Fixture, Cable and Kit Options		
CR125ACBL	High Performance Delay Matched Cable Set (required for BERTScope & CR in SSC applications).	

Service Options	Description
CA1	Provides a single calibration event or coverage
C3	Calibration service 3 years
R3	Repair service 3 years (including warranty)
R1PW	Repair service coverage 1-years post warranty
R2PW	Repair service coverage 2-years post warranty
R3PW	Repair service coverage 3-years post warranty



Key Applications	Benefits
 Device & Module Transmitter Compliance Test 	 Provides clock recovery with the required "Golden PLL" BW and peaking for compliance testing
 Device & Module Stressed Receiver Sensitivity and/or jitter tolerance testing. 	 The stressed data signal needs to be measured and calibrated using clock recovery with a compliant "Golden PLL" BW and peaking.
 Signal Integrity of High Speed Communications Systems 	 Support for Mask Testing, Jitter Peak, BER Contour, and Q-Factor Analysis enables a deep level of Signal Integrity insight.
 Design and Verification of Optical Transceivers 	 Verifies performance using optical inputs and stressed eye analysis for Fibre Channel and IEEE803 Ethernet Standards

