Signal Integrity of Reference Clock Bleed-Through in an IC

Application Note

Introduction

This application note examines some signal integrity examples related to AMB testing, but also with wider applicability. Clock bleed-through is examined, as well as the effect of a lowered supply voltage on error performance.

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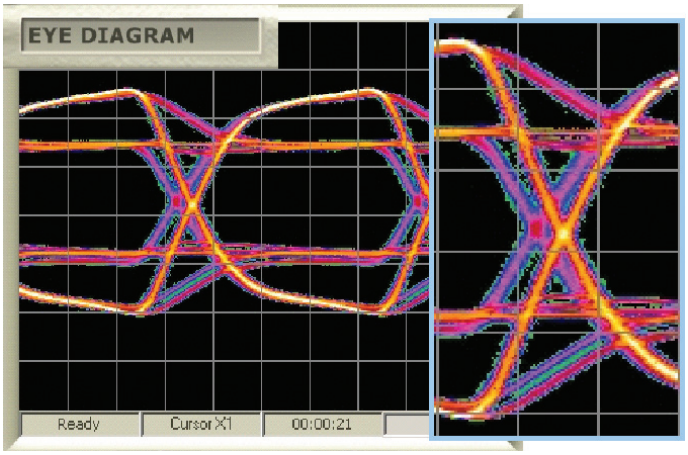


Figure 1a. Clean Eye Diagram.

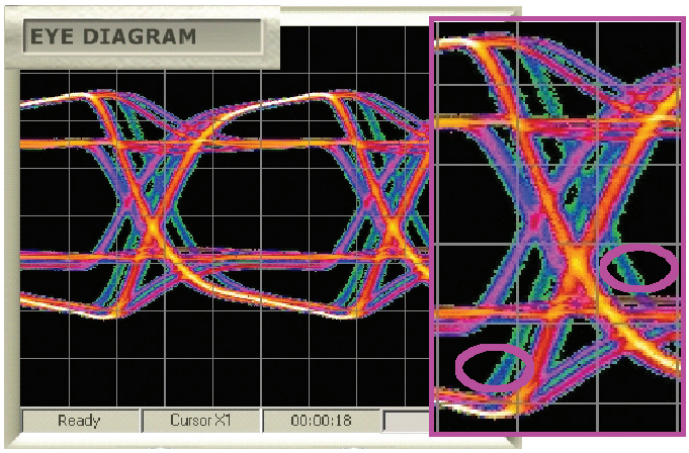


Figure 1b. Reference Clock Bleed-through Eye Diagram.

Clock Bleed-Through Example

The following discussion is based on measurements given in Figures 1a and 1b. Note that the measurements were taken directly from the output of an IC using a BERTScope BSA Series with de-emphasis switched on, giving the characteristic eye shape seen in these measurements. After the appropriate amount of travel through a dispersive medium, such as a circuit board, the signal would look like a normal NRZ eye.

The measurements on the right column of Figure 1c were taken from an early design prototype chip. For comparison purposes, measurements from a later version of the chip are given on the left.

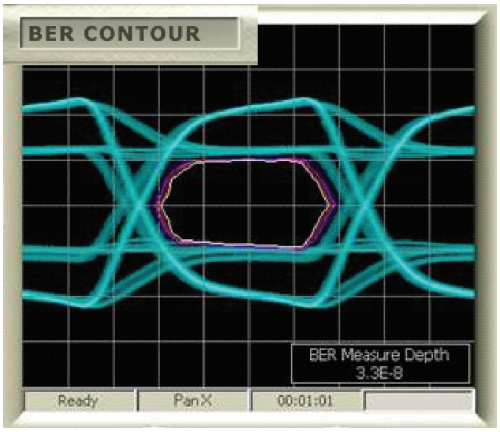
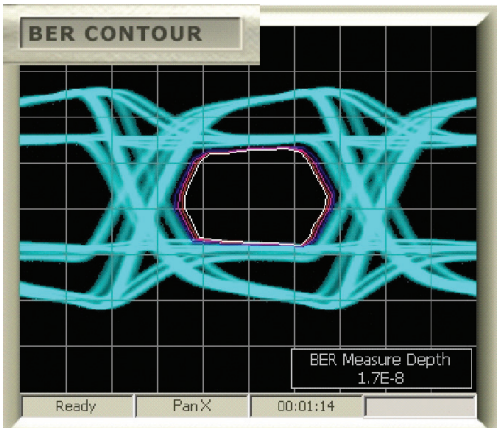
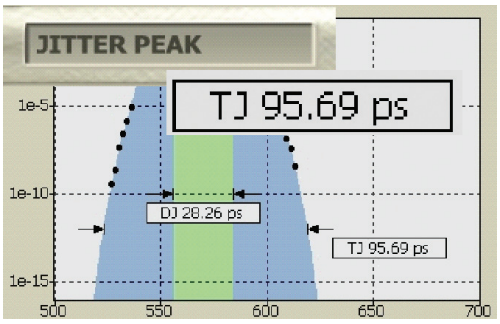
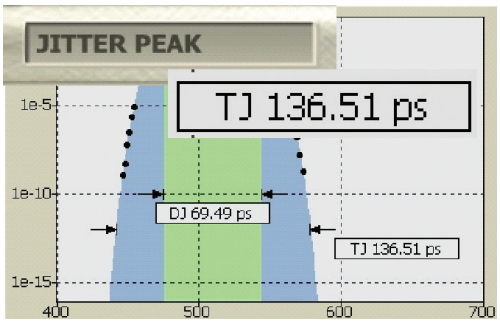
	Clean	Reference Clock Bleed-Through
BER Contour		
Jitter Peak		

Figure 1c. Operation at different supply voltages, the left column showing signal integrity measure-ments in the correct operating region. The right column showing measurements following the IBIST pattern generator failing. Note that the eye diagram looks identical in either case, but the BER and related measurements show otherwise.

The first clue that the situation was not as intended are given by the jitter measurements shown at the bottom of Figure 1a. The earlier part exhibits considerably more jitter than the design target. It can be seen from this that the problem seems to be mainly a DJ (Deterministic Jitter) problem. The BER Contour shows that in both cases, this is not a noise-related problem, and there are no rare events lurking – the contour lines are closely grouped and the center of the eye is quite open, again aligning with the conclusion that this is a deterministic effect. The major clue derives from the eye diagram, where there are mysterious extra traces apparent in the eye compared to its companion on the left (as indicated by the purple circles on the magnified portion of the eye). These traces are happening frequently (they must be to appear in an eye diagram) but obviously less frequently than the main data edges. The mystery edges also seem to be synchronous with the data edges, and timed with the data transitions.

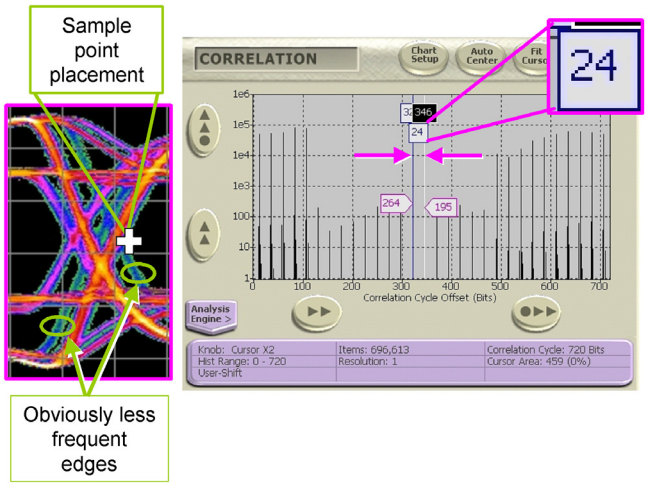


Figure 2. Placing the BERTScope sampling point where it starts to intersect with one of the mystery edges allows the designer to use error analysis. This shows a connection to errors occurring every 24 data bits.

Moving the BERTScope sampling point, it is possible to explore the less frequently occurring edges (see Figure 2). Using error analysis on the BERTScope, it becomes obvious that there is a relationship between errors, and the data rate divided by 24. For this system, this happens to corresponds to the reference clock rate (÷24) and turned out to be the cause.

The design was changed to increase isolation between clock and data paths, with the obviously improved performance seen in the measurements in the left column of Figure 1.

Summary

The BERTScope BSA Series was used to look at a semiconductor chip suffering from reference clock bleed-through, and was able to detect symptoms visible in signal integrity measurements that helped a successful redesign.

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