

# Stress Calibration for Jitter >1UI – A Practical Method

## Application Note

### Abstract

While measuring the amount of jitter present on a signal is relatively straight forward conceptually; when the levels of jitter are small, amounts above a bit period (1 unit interval or UI) can be more difficult. This has practical consequences

for standards such as USB 3.0 where calibration at the test device of 2 UI at 500 kHz of sinusoidal jitter is required. This note describes use of patterns and triggering on a BERTScope to allow such calibration.

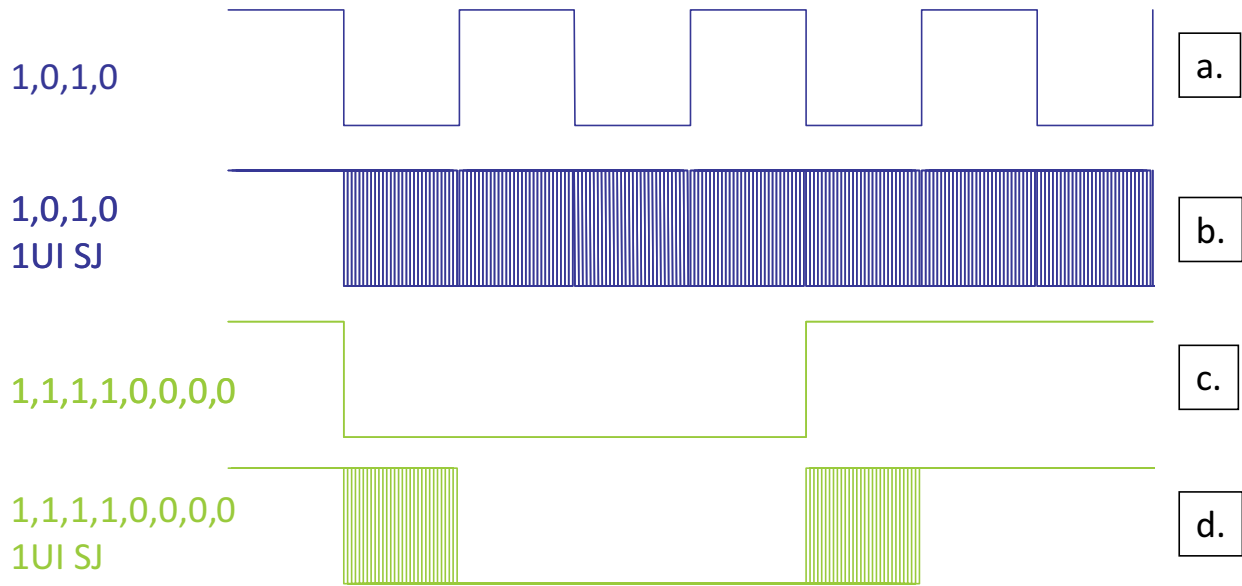


Figure 1. Applying 1 unit interval of sinusoidal jitter to two different patterns at the same data rate.

## Introduction

Stressed eye receiver testing for standards such as USB mandate that applied stress be calibrated at the device under test (DUT) rather than at the instrument front panel. For example, it is required that sinusoidal jitter of 2 UI be applied at 500 kHz modulation frequency. This can be a challenge for traditional BERT's to manage.

To illustrate the issue, Figure 1(a) shows a continuous one/zero pattern. When 1 UI of sinusoidal jitter is applied, it might look something like Figure 1(b). For jitter measurement

methodologies that require at least some eye opening to function, it is clear why they would struggle. However, for situations such as stressed eye calibration where we have control of the pattern, Figure 1(c) and (d) suggest a way forward. If the pattern is changed to 4 ones, 4 zeroes, that same amount of jitter is not causing complete eye closure, and therefore can be measured. The trick is to cause the jitter measuring instrument to believe that the unit interval is now four times longer; this can be accomplished by triggering the analyzer with a divided clock.

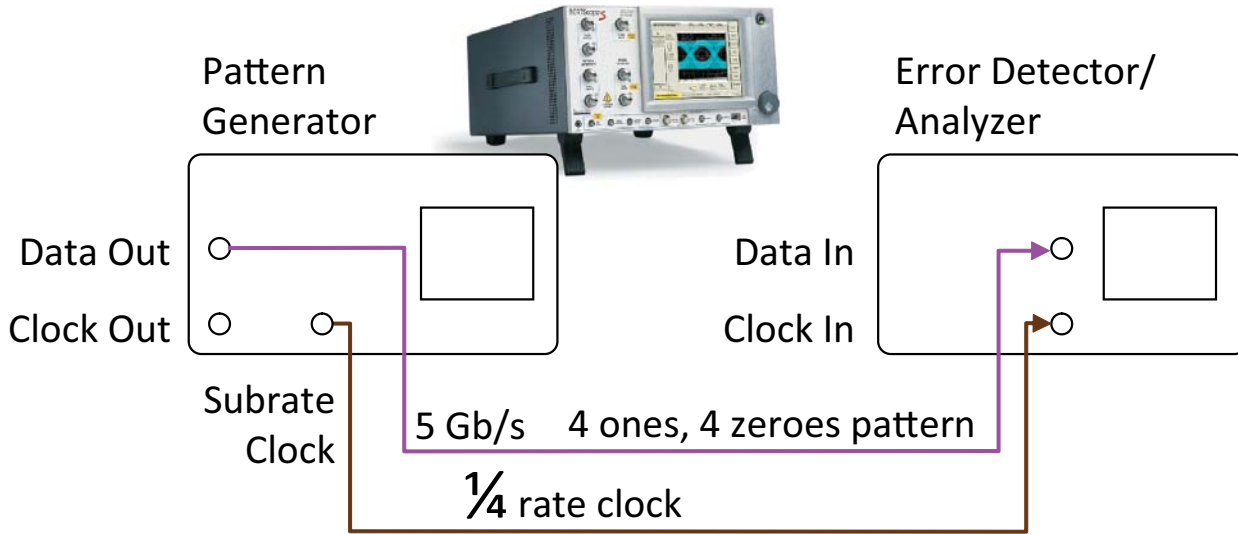


Figure 2. Test setup for measuring 2UI of sinusoidal jitter.

## Measurement Example

A generic setup is shown in Figure 2; this methodology is not specific to the BERTScope. For our measured example, the 4 ones/4 zeroes pattern is being sent by the pattern generator to the analyzer, along with a divided clock. The generator was set to 5 Gb/s, and around 2 UI of sinusoidal jitter applied.

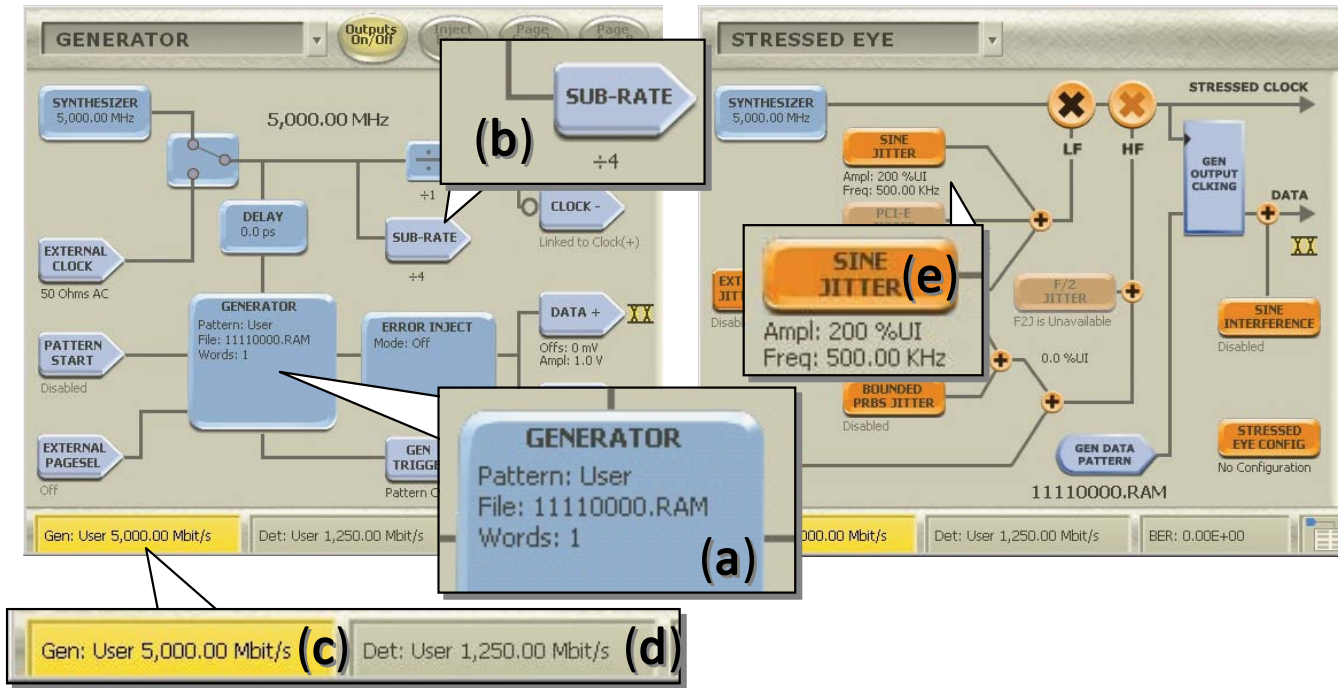


Figure 3. The Pattern Generator (PG) setup showing the 4 ones/4 zeroes pattern loaded (a), the divided clock output (b), the data rate of 5 Gb/s (c) and the received clock rate of 1.25GHz (d). Some of the subsequent screenshots have 2UI of SJ applied as shown on the stress setup screen (e).

The analyzer received the clock at 1.25 GHz and the measurements were executed using the 1.25 GHz bit period of 800 ps as the unit interval, as shown in Figure 3 and 4. (The measurement setup had a filter and short length of ISI in the measurement path, which are not shown in Figure 2.)

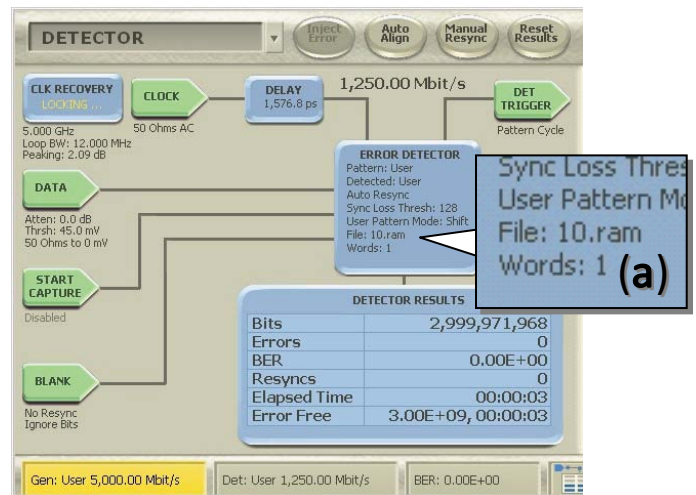


Figure 4. The Error Detector (ED) showing the one/zero pattern loaded (a).

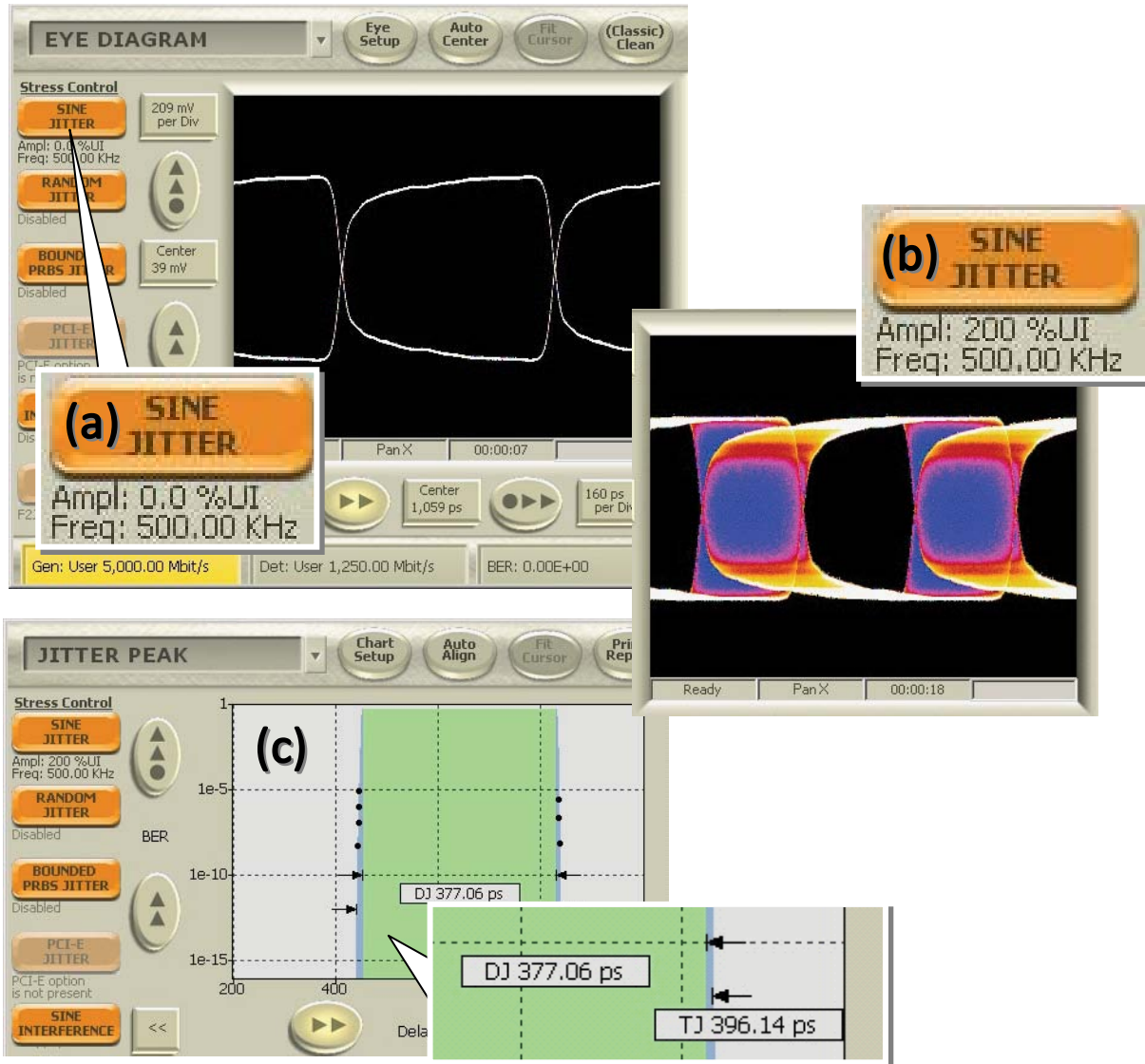


Figure 5. Measured results showing an eye diagram with no jitter applied (a), 2UI of jitter applied (b) and a successful measurement of TJ (c).

## Measured Results with a BERTScope

The unstressed eye diagram is shown in Figure 5(a). The effects of the filter and ISI are visible in the rounded edges, but are not relevant to understanding this example. 5(b) shows the same eye diagram with sinusoidal jitter added. Remember that the applied level is 2 UI, significantly beyond the measurement range of dual-Dirac-based measurement in normal use. Figure 5(c) shows a Jitter Peak measurement of Total Jitter (TJ). As expected, the measurement is dominated by Deterministic Jitter (DJ).

## Limitations

This methodology lends itself to a situation such as stressed eye calibration where the user has control over the pattern. Obviously it is also only useful for sources of applied jitter that are pattern-length independent. The approach can be extended to patterns containing longer runs of ones and zeros, but this necessitates a higher divide ratio; for high speed instruments such as sampling scopes and BERTs, care must be taken to make sure the incoming clock rate doesn't go below the lowest operating rate of the analyzer, or that measurement times don't become inconveniently slow.

## Reference

For jitter tolerance testing requirements of USB 3.0, refer to “USB 3.0 Receiver Compliance Testing” by Cynthia Nakatani, January 2010, [www.tektronix.com](http://www.tektronix.com).



**Contact Tektronix:**

- ASEAN / Australasia** (65) 6356 3900
- Austria\*** 00800 2255 4835
- Balkans, Israel, South Africa and other ISE Countries** +41 52 675 3777
- Belgium\*** 00800 2255 4835
- Brazil** +55 (11) 3759 7600
- Canada** 1 (800) 833-9200
- Central East Europe, Ukraine and the Baltics** +41 52 675 3777
- Central Europe & Greece** +41 52 675 3777
- Denmark** +45 80 88 1401
- Finland** +41 52 675 3777
- France\*** 00800 2255 4835
- Germany\*** 00800 2255 4835
- Hong Kong** 400-820-5835
- India** 000-800-650-1835
- Italy\*** 00800 2255 4835
- Japan** 81 (3) 6714-3010
- Luxembourg** +41 52 675 3777
- Mexico, Central/South America & Caribbean** 52 (55) 56 04 50 90
- Middle East, Asia and North Africa** +41 52 675 3777
- The Netherlands\*** 00800 2255 4835
- Norway** 800 16098
- People's Republic of China** 400-820-5835
- Poland** +41 52 675 3777
- Portugal** 80 08 12370
- Republic of Korea** 001-800-8255-2835
- Russia & CIS** +7 (495) 7484900
- South Africa** +27 11 206 8360
- Spain\*** 00800 2255 4835
- Sweden\*** 00800 2255 4835
- Switzerland\*** 00800 2255 4835
- Taiwan** 886 (2) 2722-9622
- United Kingdom & Ireland\*** 00800 2255 4835
- USA** 1 (800) 833-9200

**\* If the European phone number above is not accessible, please call +41 52 675 3777**

Contact List Updated 25 May 2010

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