The Challenge of Mixed Signal Development

I. Introduction

Designers creating next-generation designs need to intermix complex digital with RF elements for wireless consumer devices. As clock frequencies increase and circuit sizes shrink, engineers are finding a need to address the increasing analog behavior from digital components while dealing with a mixture of analog, digital and form factor requirements in these complicated designs. In the move to combined digital and RF technologies, these new design challenges grow in significance as designers endeavor to rapidly and correctly characterize their design.

II. Market Drivers

The highly competitive commercial market is driving the need for lower development costs and faster time to market – the fact is it's expensive to be late. This need to speed development and reduce costs is driving the migration to Digital RF, where the device is defined more in software and digital baseband, allowing it to be less dependent on analog components. This development has had a profound impact on the RF world, from the pace of innovation to the increasing availability of high performance, lower power consuming circuits which perform traditional analog radio functions. The availability of these advanced digital RF technologies suggests ever more ways to expand wireless communications.

Whether commercial or military, customers want more information, faster, anywhere, anytime. Digital RF technologies make wireless access available in more places, to more people, and for less money. Increasingly, this demand is being met by devices which are software defined, allowing for changes to be made via a simple update in firmware and a plug-in analog front end (RFIC). This, in turn, is driving the need for more development and testing to be done in the digital baseband realm. Consequently, interfaces are in transition from analog to digital.

The signals being created by these innovative devices are increasingly complex and dynamic; there is a growing need to create signals which use complex modulation and multiplexing schemes which rapidly change frequency, amplitude, and phase.

The government and military sectors are also increasing their utilization of these technologies. Modern radar systems are increasingly making use of digital baseband signals, FPGA's, and digital beam-forming antenna systems known as phased array. Some examples from the United States include communications systems such as Joint Tactical Radio (JTRS) and Project 25 (P25) which are software defined radios. These systems can also benefit from a mixed signal source such as the Tektronix AWG5000 Series arbitrary function generator.

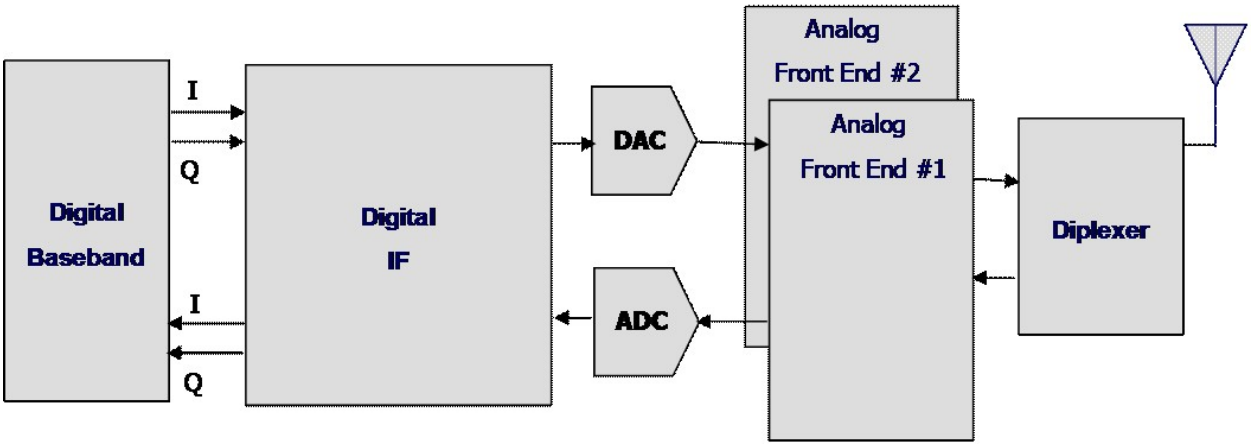

Figure 1. Block diagram of a software-defined approach where the analog front end is inter-changeable

III. Design Verification in a Mixed Signal Environment

The explosion of digital RF has created a highly complex technology environment. More often devices are utilizing a zero-IF (direct conversion) or a low intermediate frequency (IF) approach. With both of these, the traditional use of analog filters is no longer as easy or even feasible. The emphasis is now growing toward correction in baseband, utilizing active nulling of gain and DC offset mismatches as well as IQ quadrature imbalances.

First, we will explore the zero-IF approach. In this approach, the Digital IF shown in Figure 1 is removed and the signal goes directly between digital baseband and the data converters.

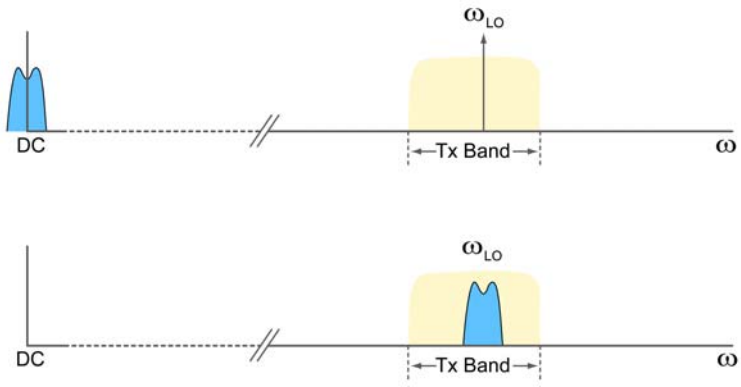

Figure 2. Zero-IF Spectrum

Figure 2 describes the frequency transformation that occurs in a zero-IF architecture. In this architecture, the modulating signal is centered on DC. When this signal is mixed with an LO, the result is a single spectrum centered around the LO frequency. Any imperfections in the transmitter such as I/Q level imbalance, LO leakage, I/Q offsets and imperfect quadrature in the I/Q modulator will manifest themselves as imperfections in the desired RF spectrum and not as unwanted out-of-channel components (such as sidebands).

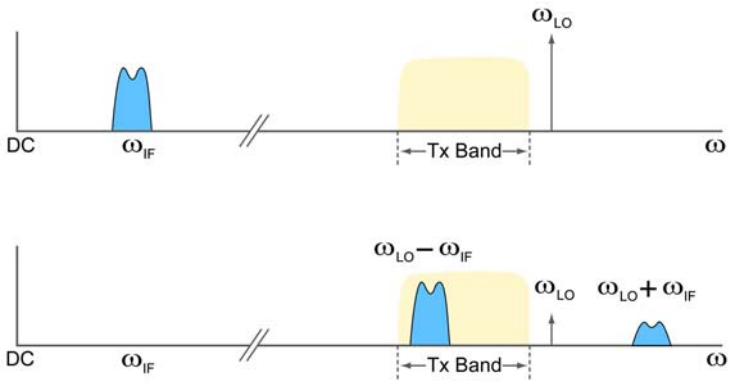

Figure 3. Low-IF Spectrum

Figure 3 highlights the low-IF architecture. Similar components are used in this architecture. However there is a key difference. The modulating signal from the DAC is no longer centered on dc but has been synthesized as an image-free low IF. When this signal is mixed with the LO in the I/Q modulator, a more complex spectrum results. The spectrum of the desired signal appears at an offset from the LO that is equal to the low IF frequency (i.e. (ωLO-ωIF).

Each of these approaches offer trade-offs in terms of advantages and disadvantages. In the 'low-IF" approach, imperfections in the I/Q modulator result in an unwanted LO leakage component along with an unwanted upper sideband. However, by increasing the low IF frequency, these unwanted components can be moved far away enough from the desired spectrum to make filtering practical.

It should also be noted that modern DACs allow for active nulling of gain and offset mismatches. Calibrating the gain and offset mismatches reduces the unwanted out-of-band components (LO leakage and sideband image), making the filtering process that much easier. Assuming that these unwanted components can be adequately filtered, the net result of this scheme (compared to a baseband to RF conversion) is a perfectly modulated carrier.

In zero-if schemes, there is no possibility to use filtering to improve signal quality. So, to improve signal quality, we must rely on improved baseline component performance and/or active nulling of LO leakage and I/Q quadrature imbalances. The DAC may also contain a complex modulator, allowing for the generation of an image-free low IF. The AWG5000 arbitrary waveform generator provides these digital baseband signals which can be varied both in amplitude and phase to allow for testing of active nulling/correction algorithms in the baseband.

IV. Data Converter Testing

Data converters, both DACs and ADCs, are becoming even more of a key component in modern transceiver design with the drive being ever higher bandwidth utilization and linearity.

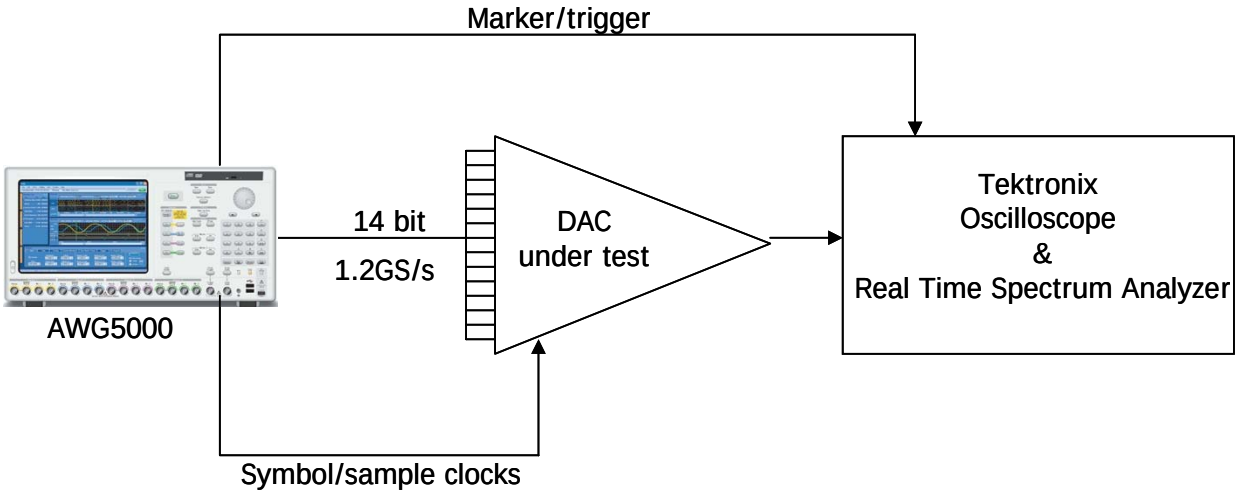

Figure 4. DAC test setup

Figure 4 shows a typical test setup for DAC testing of parameters such as non-linearity (both integral and differential), gain error, offset error, settling/slew time, cross-talk, glitch energy and spectra. The AWG5000 provides a 14 bit digital ramp signal at a sample rate as high as 1.2 GS/s and 2 marker outputs per analog channel (up to 8) to allow for timing the generated bits to sample bits. There are also multiple analog channel outputs (up to 4) to allow for mixed analog and digital test signals. This can be especially useful in instances where the symbol and sample clock are separated as well as when the inputs are differential rather than single-ended.

V. Partitioning Presents Major Challenges for Engineers

Often ASIC designs are tested using a FPGA prototype which allows the design to be verified while running “real-speed”. This approach increases the need for a “real stimulus in – real response out” technique. Then the decision needs to be made on how to partition the functionality so it can be implemented in an ASIC. The appropriate partitioning of analog and digital functionality results in faster time to market and longer time-in-market. Another consideration is cost; there is the ongoing struggle to minimize the number of pins for each ASIC, thereby reducing package cost. Some designs partition so that the chip interface is digital, others utilize an analog, some use both. Deciding which design approach to take requires mixed-signal testing using digital IQ, analog IQ, and IF signals.

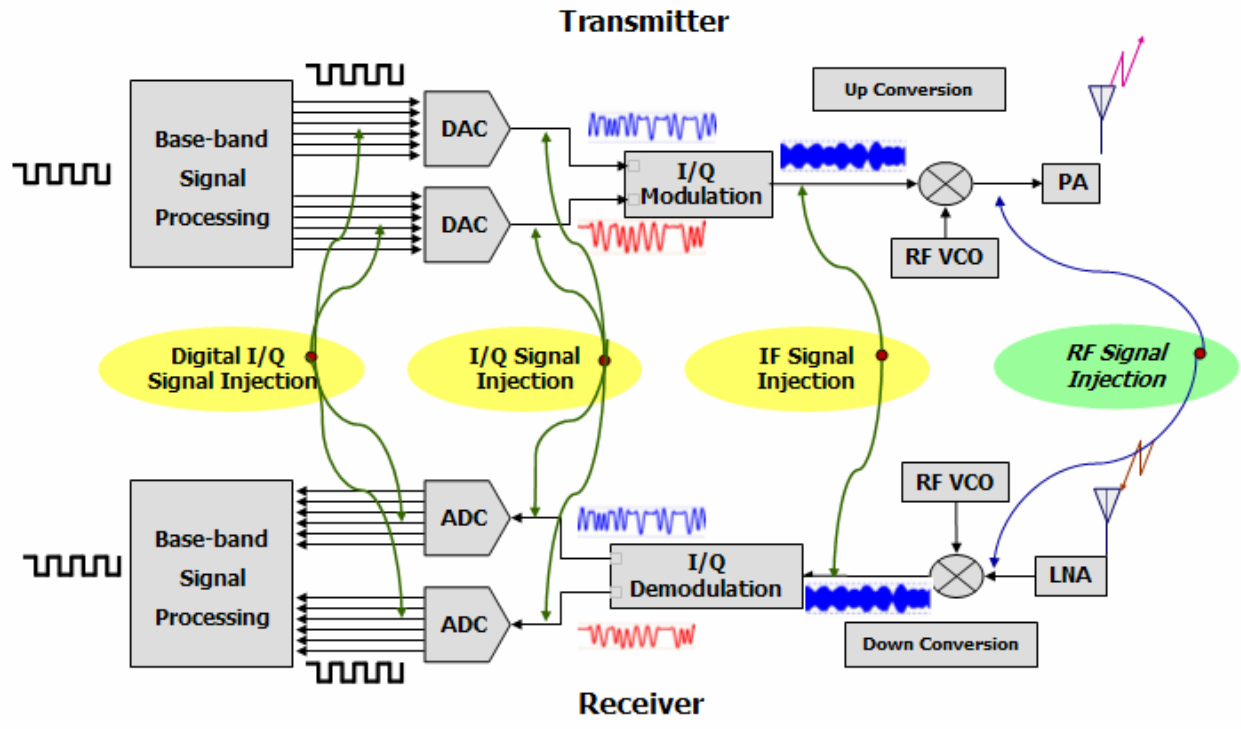

Figure 5. Analog approach to IQ modulation

In some instances the device is partitioned such that IQ modulation is performed in analog as shown in Figure 5. Note the signals on the far left labeled as “Digital IQ”; the AWG5000 allows for up to 28 digital outputs (14 bit output for up to 2 channels). When used in conjunction with marker outputs, there are a total of 36 digital channels available to the user.

However, as mentioned previously, there is a growing move toward simplifying the transceiver by implementing IQ modulation at baseband; this also allows for modulation format to be modified via software control of the baseband signal. A block diagram of this approach is shown in Figure 6.

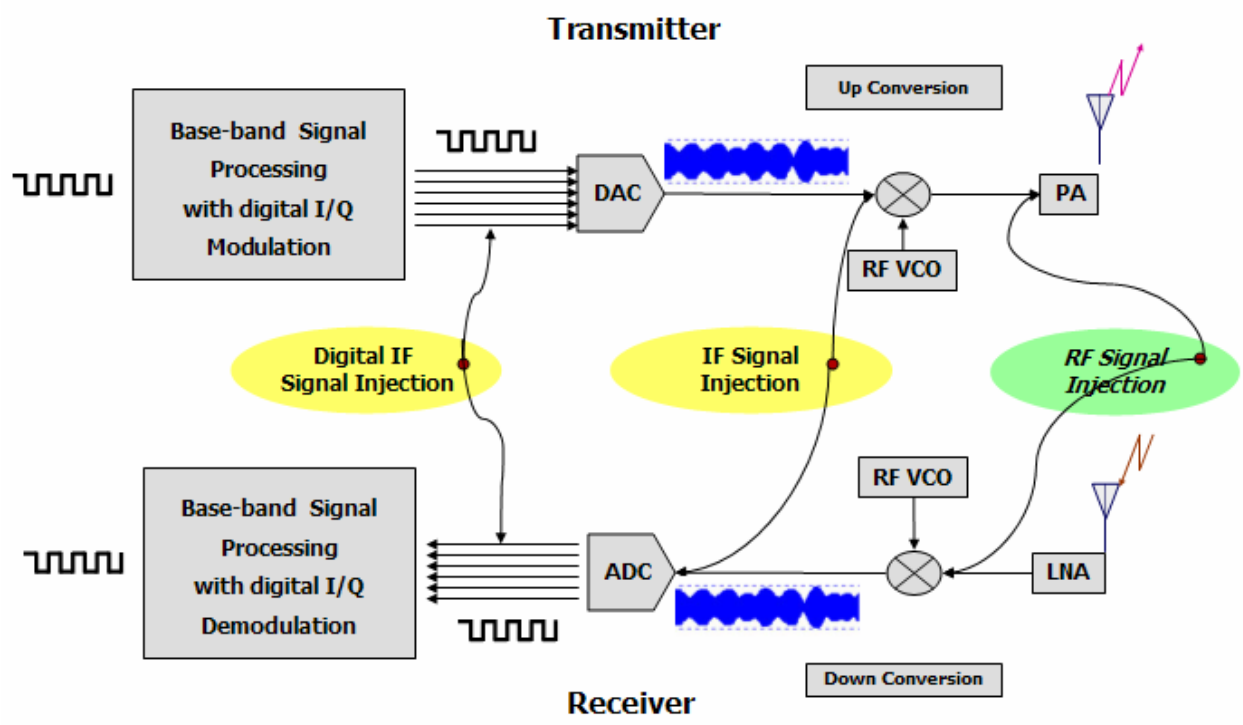

Figure 6. IQ modulation being performed in baseband (digital)

VI. The Multiple Input, Multiple Output (MIMO) Approach

There is a growing movement toward the use of Multiple Input, Multiple Output (MIMO) technologies which requires numerous multi-beam or adaptive-array antennas; an example of this is 802.11n. Currently, most wireless systems which use this technology are implementing a 2X2 matrix, whereby 2 antennas are used in the transmit and receive path but work is in progress on 4x4 matrix devices which are just on the horizon. Rather than use two or more expensive Vector Signal Generators (VSGs), it is much more cost-effective to utilize an AWG approach; this offers multiple independent channels with the ability to simulate the amplitude and phase variations found in a real-world MIMO environment without the use of electronic switching. The design engineer faces the challenges found in the analog vs. digital approach: should an RFIC be implemented to combine the signals from the antenna, or should the digital approach be implemented with a data converter for each down-converted antenna signal? Using the AWG5000 provides real-world signal simulation for testing both approaches.

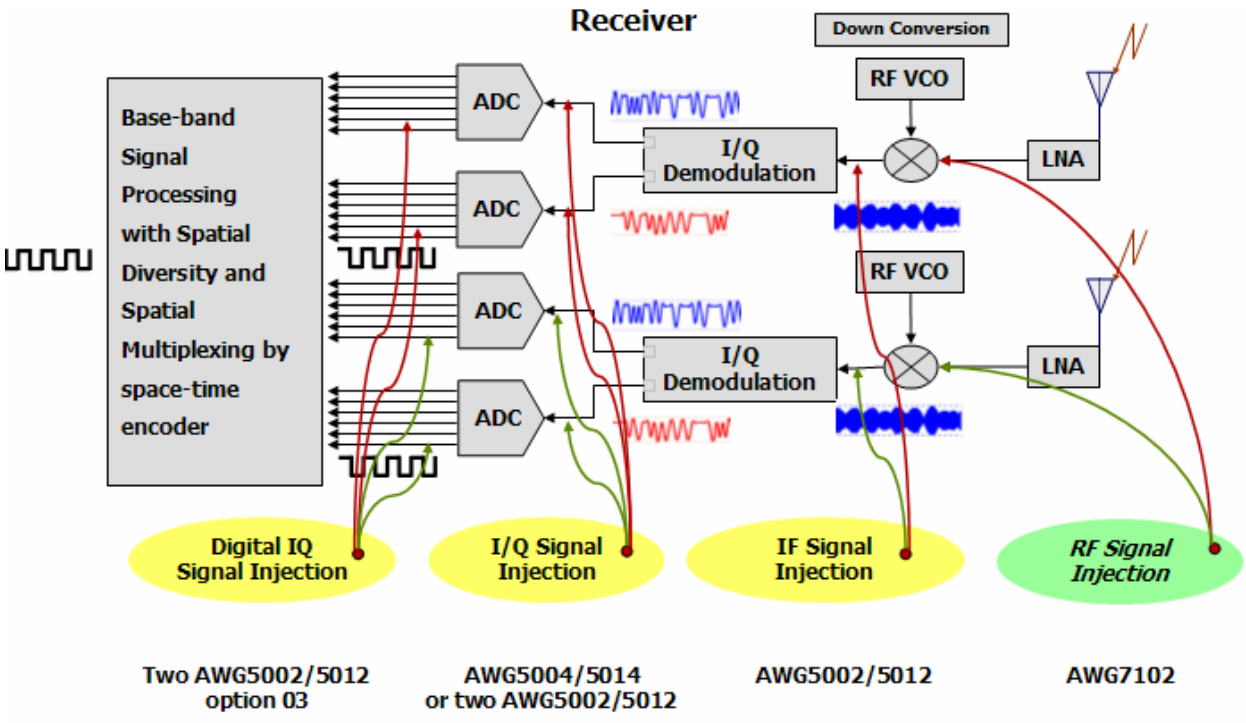

Figure 7. MIMO Receiver Test Setup

Figure 7 shows an example of test injection points on a MIMO receiver. Regardless of the injection point utilized, the signal from the AWG5000 (typically modulated) needs to have very good modulation quality so that any signal degradation is known to be a result of the device under test, rather than the test signal.

Modulation quality is measured using Error Vector Magnitude (EVM) and there is a direct correlation between signal to noise and spurious free dynamic range. With 80dB of SFDR, the AWG5000 can provide extremely 'clean' digital modulation signals as shown in Figure 8.

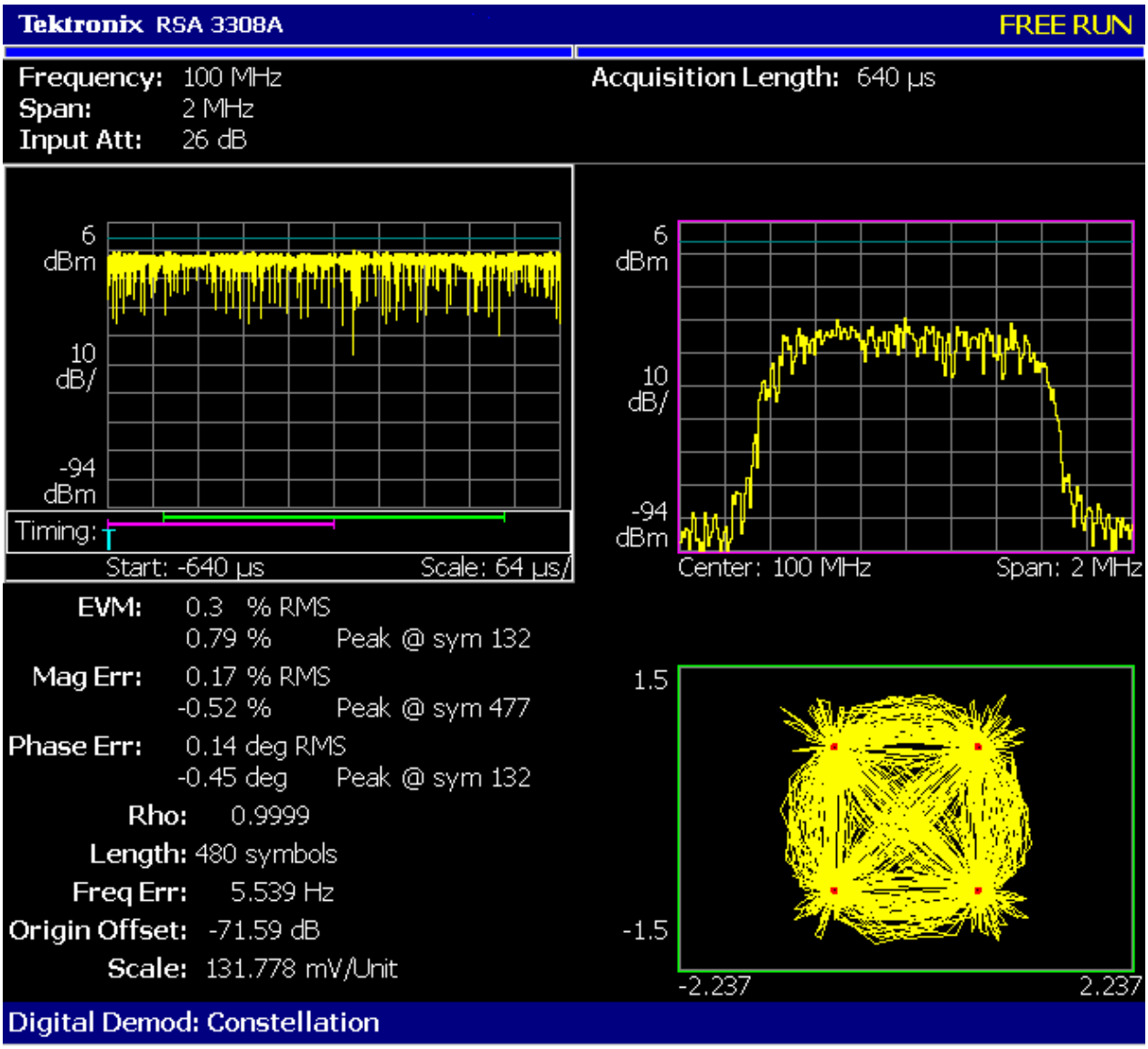

Figure 8. Screen capture from a Tektronix Real Time Spectrum Analyzer showing the extremely good modulation quality of a QPSK signal being generated by an AWG5000

Key AWG5000 Arbitrary Waveform Generator Benefits for Mixed Signal Testing

- ► Unique combination of analog and digital output performance permits one-box solution for analog and digital IQ as well as IF signal generation
- ► Highly linear 14 bit DAC providing leading edge combination of sample rate and SFDR
- ► The combination of analog output and marker output provides synchronized sine wave and clock signal to data converter devices with extremely low relative jitter.
- ► Four channel version is ideal for MIMO testing
- ► Internally - variable sample rate clock (up to 1.2 GS/s) allows for signal optimization without the use of an external clock source
- ► Integrated user interface allows for easy setup

VII. Conclusion

Digital signal processing continues to become a larger part of RF design, with new methods that are needed to provide RF signal analysis. For years, baseband signals have been digitally processed, but increasingly IF and even some RF signals are developed as digital. New developments in arbitrary waveform generation technology have made possible the effective combination of mixed digital and RF signal generation.