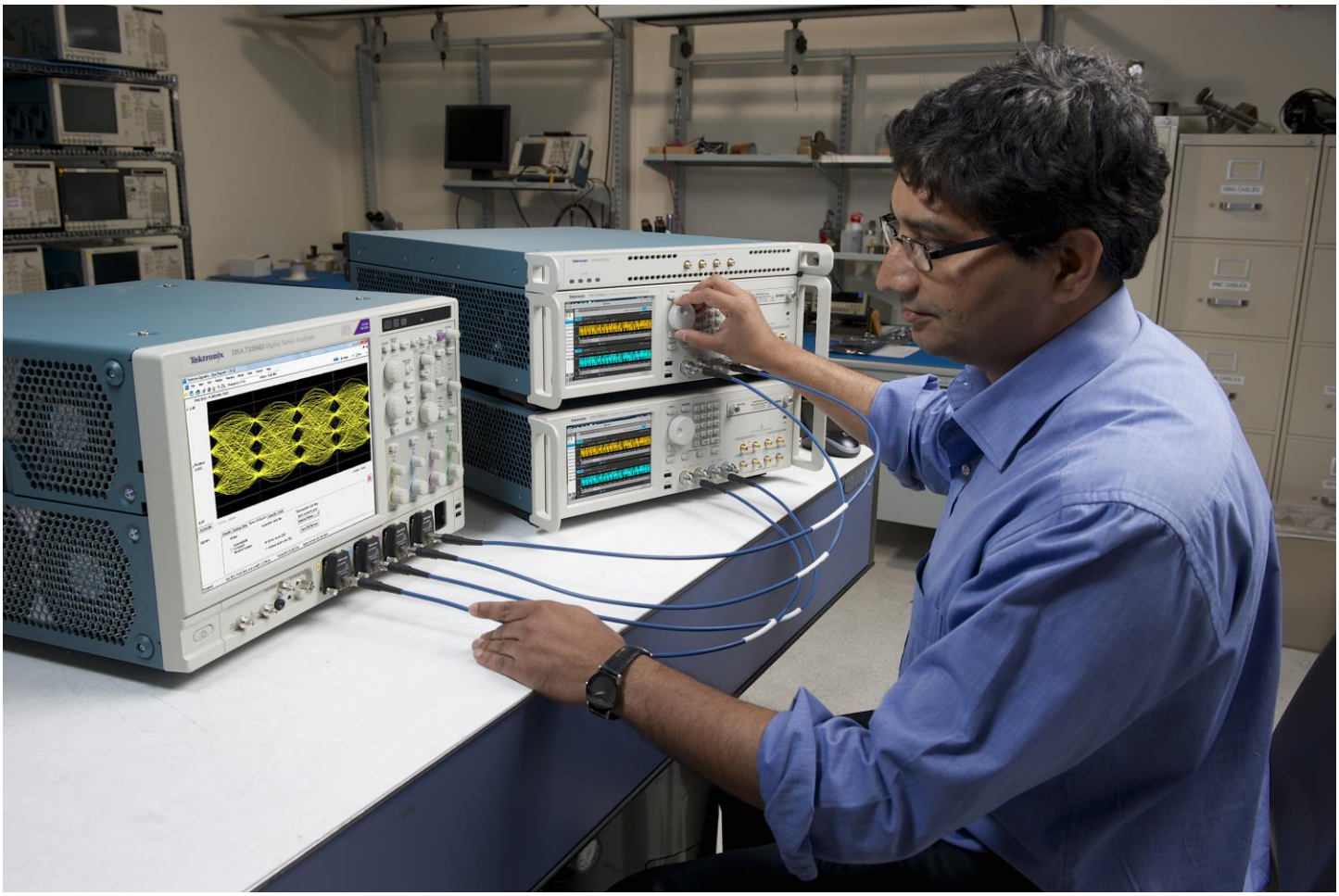
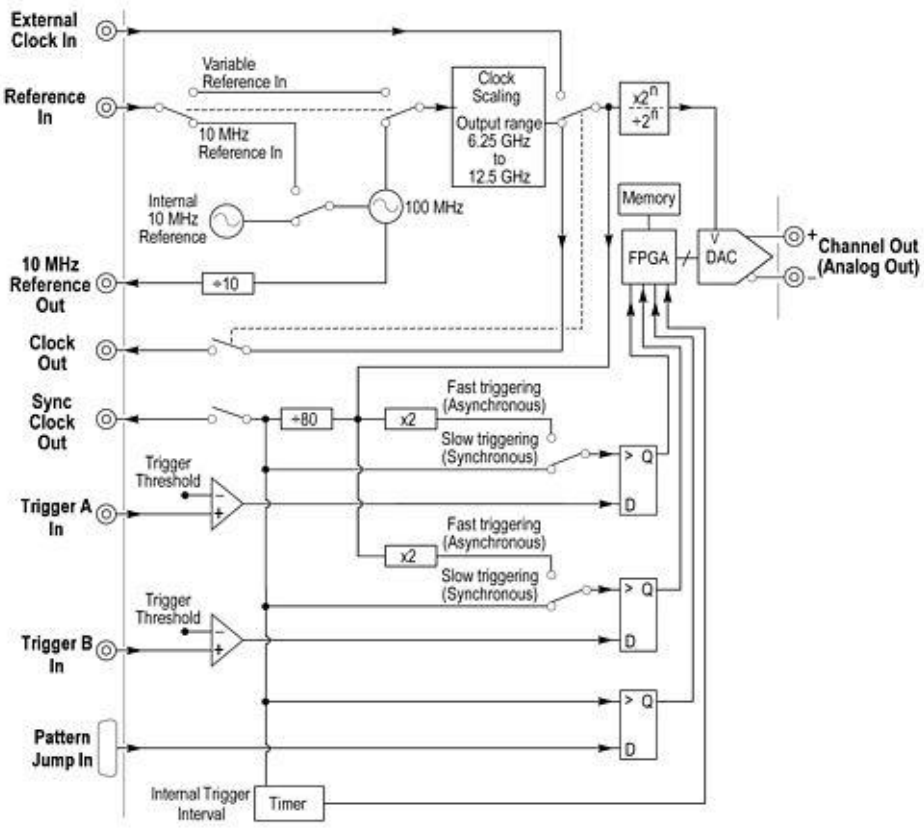


Using Tektronix AWG70000 series in synchronous and multiple unit applications

Arbitrary Waveform Generators (AWGs) can be used in many types of applications as stand-alone generators, but there are many applications that require the ability to generate waveforms relative to an external system trigger and or clock. In these scenarios the user would like to have confidence that the AWG can output a signal or signals consistently in relation to their system timing requirements. Also because there are limited output channels on a single AWG especially when high sample rates are required, there is the need to synchronize multiple AWGs. To meet these requirements the user needs to understand the AWG regarding the trigger and clocking specifications and also understand the external configuration regarding how to set up the AWG in order to achieve maximum performance.

External triggering is one of the most important requirements when trying to synchronize to any system. Understanding the characteristics of the AWG trigger and clocking system can be challenging so hopefully after reading this document you will have a better grasp of the characteristics and how to use the instrument to solve your complex application requirements. Let us first look at the block diagram of the clock and trigger system. Specifically the trigger portion. Where the triggers control when a waveform starts to output, after the Play button has been pressed. A trigger event is necessary when the instrument's Run Mode is set to wait for a trigger event or in a sequence where triggers or events are used.



Clock and Trigger block diagram

Basically there are 5 methods of triggering:

1) Internal Triggering (repetitive from 1us – 10sec)
2) External A and B Trigger (external SMA input on rear panel)
3) Pattern Jump (external DIN connector on the rear panel)
4) Manual Trigger (through the front panel)
5) Using program control (using program interface)

Notice the trigger system is synchronized to the specific clock used.

Also notice that in the Slow triggering mode (Synchronous) there is a divide by 80 from the clock source. (this will be discussed later)

Let us now look at some of the specification that will be of interest.

Trigger delay to analog output	Asynchronous trigger mode: 32,480 / (2 * fclk) ±20 ns Synchronous trigger mode: 30,880 / (2 * fclk) ±20 ns fclk is the frequency of the DAC sampling clock The DAC sampling clock frequency is displayed on the clock settings tab when the external clock output is enabled.
Trigger hold off	>1.4 µs Trigger hold off is the amount of delay required at the end of a waveform before another trigger pulse can be processed.
Trigger asynchronous jitter	The asynchronous jitter performance is directly proportional the frequency of the DAC sampling clock. The DAC sampling clock frequency is displayed on the clock settings tab when the external clock output is enabled.
1 kΩ selected	130 ps_{p-p}, 26 ps_{rms} for 6.25 GHz DAC sampling clock 90 ps_{p-p}, 17 ps_{rms} for 12.5 GHz DAC sampling clock
50 Ω selected	105 ps_{p-p}, 24 ps_{rms}s for 6.25 GHz DAC sampling clock 70 ps_{p-p}, 14 ps_{rms} for 12.5 GHz DAC sampling clock
Trigger synchronous jitter	Clock In = 12.5 GHz: 300 fs_{rms}, 4.2 ps RJ_{p-p} BER@10-12 Variable Reference In = 156.25 MHz: 400 fs_{rms}s, 5.6 ps RJ_{p-p} BER@10-12 Fixed Reference In = 10 MHz: 1.7 ps rms, 23.8 ps RJ_{p-p} BER@10-12 Sample rate = 25 GS/s Trigger input impedance = 50 Ω

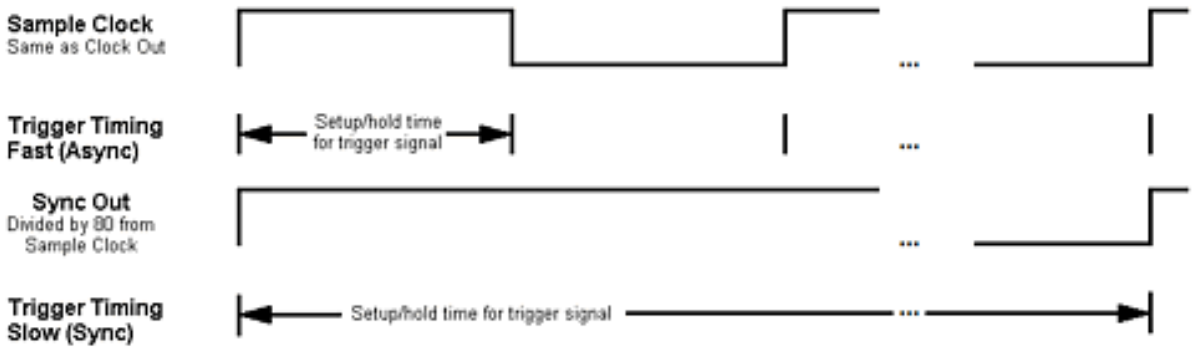
All of the internal AWG's timing characteristics are derived from a precision Yttrium Iron and Garnet (YIG) 6.25 – 12.5 GHz tuned oscillator or an external clock or reference. In order to get the best synchronization and the lowest Trigger Jitter, the external trigger has to align with the internal clock edges of the AWG. Also the trigger has to come within a specific duration in order to meet the clocking requirements when outputting the data out of Random Access Memory (RAM) and into the Digital to Analog Converter (DAC). This duration is based on the AWG architecture where the waveform memory is clocked out of memory in 80 sample blocks with each clock edge. To enable easier trigger to clock synchronization or the best trigger uncertainty a switch is available to divide down the clock such that this synchronous trig to clock edge can be accomplished much more repeatedly (this is the slow synchronous triggering mode) By turning on this divide feature the external trigger timing duration requirement is much more flexible. Here is a description of these modes.

The Timing control in the Trigger setup window allows you to select the method most suited to your application.
Fast (Async) is appropriate for situations like these:

- You do not need trigger timing uncertainty better than ± (sample clock period) / 2.
- You are using a single trigger event to start AWG output.
- You want to minimize trigger uncertainty without synchronizing the AWG to your external system or device under test (DUT).

Slow (Sync) is useful if your application is like one of these examples:

- You need to minimize trigger uncertainty and have the ability to synchronize your trigger signal to the AWG clocks using one or more of these signal inputs/outputs: Reference In, Reference Out, Clock Out, or Sync Clock Out.
- You are using a trigger signal from your system to the AWG to achieve tight alignment between the AWG and your external system.
- You are synchronizing multiple AWGs.



Async and Sync timing diagram

To understand the difference between these choices, you need some background on the AWGs internal clock signals.

- The internal sample clock signal is what causes the DAC to output waveform samples.
- The DAC's output sample rate is generally a multiple of the sample clock or divided down from the sample clock
- The sample clock is always a value between 6.25 GHz and 12.5 GHz, while the sample rate can be anywhere from 1.49 kSamples/s to 50 GSamples/s. (The maximum rate varies by instrument model and options).

The Clock Out signal is the same as the internal sample clock. The Sample Clock is divided by 80 to produce another timing signal; the Sync Clock Out. The Clock Out and Sync Clock Out signals are available on rear-panel of the AWG for use in synchronizing the AWG to your external device or system.

The AWG determines when a trigger event has occurred by comparing the trigger input signal's voltage level against the trigger level you have set in the Trigger setup window. This comparison occurs at the rising and falling edges of the

Sample Clock signal for Fast trigger timing, and at the rising edge of the Sync Clock Out signal if Slow trigger timing is selected.

The Sample Clock period for Fast (Async) trigger timing can be as short as 40 ps (for 50 GS/s sample rate). If the trigger signal applied to the AWG misses its setup/hold window by being either too early or too late, it will be recognized in the previous or next cycle, leading to an 80 ps uncertainty for Fast (Async) mode if you do not use one or more of the clock signals to synchronize your trigger events to the AWG sample clock.

Minimum trigger uncertainty is achieved by using shared clock and/or reference signals to insure that your trigger event arrives at a consistent location within the selected Trigger Timing clock cycle. The Sample Clock period for Slow (Sync) trigger timing is 160 times longer than for the Fast (Async) trigger timing. This extra time makes it easier for your system to assert the trigger event within the setup/hold window.

Using the AWGSYNC01 (Sync Hub) to synchronize up to 4 AWGs

Many applications such as Coherent Optical, Serial Data and many others require more than 1 or 2 channel output capability. In order to accomplish this multiple AWGs need to be synchronized so they can output numerous signals simultaneously. As we saw earlier; trigger to clock synchronization can be challenging and this is even more so when multiple AWGs are required to be synchronized.

The AWGSYNC01(Sync Hub) enables the multi-instrument synchronization of up to four AWG70001A or AWG70002A units allowing up to eight channels to be aligned to the same clock, pattern jump and trigger inputs. The AWGSYNC01 requires no additional software and allows for the rapid and consistent synchronization of multiple devices. The AWGSYNC01 provides calibration ports to deskew up to four AWG70000 instruments to within ±10ps. After the deskew process the AWGSYNC01 can repeatedly return to within ≤5 ps of the same deskew point even if the units need to be powered down or sample rate changes. Here are the specifications for the AWGSYNC01:

Specifications

General

Jitter

Random Jitter (typical)	315 fs RMS
Total jitter (typical)	13 ps_{p-p} at 12.5 Gb/s

Skew

Instrument to instrument skew	±10 ps
Skew repeatability/accuracy	≤5 ps
	After changes of sample rate or power cycle and within ±5 °C from deskew calibration.

Inputs, outputs

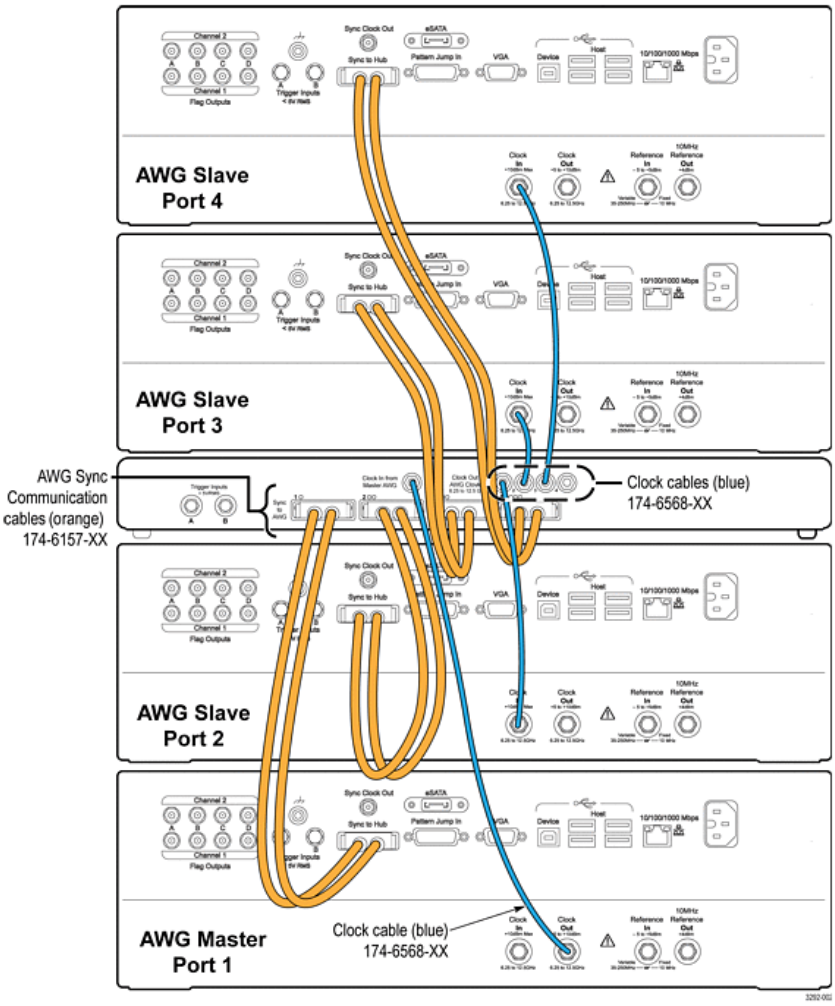
Calibration Ports	Four SMA type connectors used to deskew the instrument signal delays. Only use the supplied matched silver calibration cables with these connectors when deskewing the AWG70000 instrument signal outputs.

Trigger Inputs (A, B)	External trigger inputs
Connector	SMA
Number of trigger inputs	2
Impedance	50 Ω or 1 kΩ selectable
Polarity	Positive or negative selectable
Input voltage range	50 Ω: <5 VRMS
	1 kΩ: ±10 VRMS
Threshold range	-5.0 V to 5.0 V
Threshold resolution	0.1 V
Minimum trigger pulse width	20 ns
Trigger holdoff	>1.4 µs
Trigger delay to analog output	Asynchronous trigger mode: 32,480 / (2 * fclk) ±20 ns
	Synchronous trigger mode: 30,880 / (2 * fclk) ±20 ns
	fclk is the frequency of the DAC sampling clock
	The DAC sampling clock frequency is displayed on the clock settings tab when the external clock output is enabled.
Trigger asynchronous jitter	80/sampling clock frequency
	The asynchronous jitter performance is directly proportional the sync clock out frequency. The sync clock out is derived from the DAC sampling clock. The DAC sampling clock frequency is displayed on the clock settings tab when the external clock output is enabled.
Trigger synchronous jitter	Clock In = 12.5 GHz: 300 fs_{RMS}, 4.2 ps RJ_{p-p} BER@10^{-12}
	Variable Reference In = 156.25 MHz: 400 fs_{RMS}, 5.6 ps RJ_{p-p} BER@10^{-12}
	Fixed Reference In = 10 MHz: 1.7 ps_{RMS}, 23.8 ps RJ_{p-p} BER@10^{-12}
	Sample rate = 25 GS/s

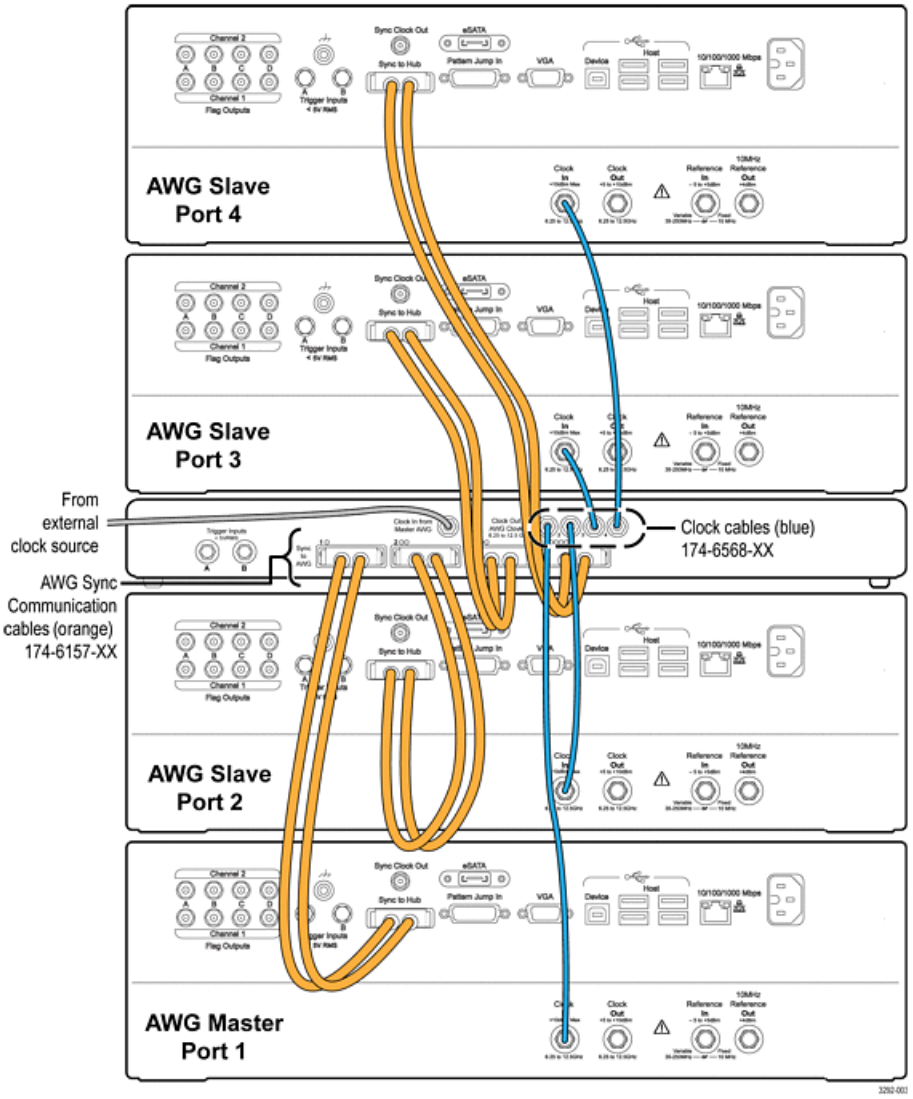
As you can see most of these specification are derived from the AWG main specifications. The main difference with this multi instrument configuration is that the user only has to provide one trigger to the sync hub to enable all attached AWGs to playout the waveforms synchronously. It is also possible to send commands to the Master AWG to force a trigger programmically that will also trigger all the Slave units since the sync hub does not have any direct communication capability. The sync hub requires deskew calibration once you have all the hardware configured and cables attached. This Deskew calibration is done from the master AWG's GUI and once done should not need to be repeated unless the HW configuration is changed in any way. This calibration is all done through the sync hub and does not require any external instruments.

Sync hub connections

The following are typical cable connection examples connecting the AWG70000A series instruments to a AWGSYNC01 Sync Hub.

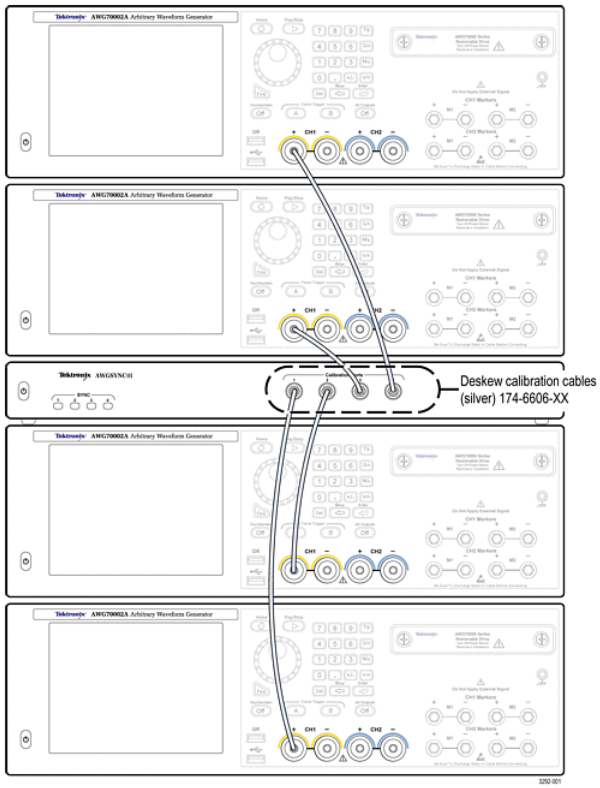


Clock Out signal from the Master used for synchronization



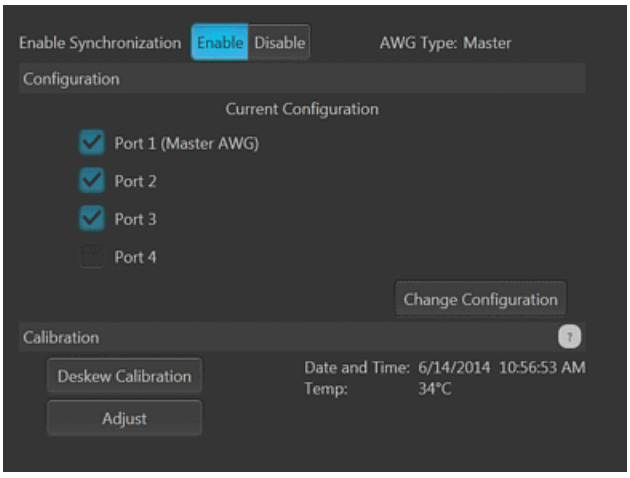
External clock signal is used for synchronization

Connection diagram to connect the Sync Hub calibration ports to the analog output connectors on the AWG70000A series instruments. Once the connections are made, run the Deskew Calibration process.



Calibration (deskew)

For best performance, always run the Deskew Calibration process after making the initial connections or changing connections between the AWGs and the Sync Hub.



When the calibration process is complete, the deskew cables can be disconnected.

Conclusion

Hopefully this document will enable you to understand and use the AWG in synchronous applications much easier.