Using Tektronix AWG7000 Series in Synchronous Applications

Technical Brief

Introduction

Arbitrary Waveform Generators (AWGs) can be used in many types of applications as stand-alone generators, but there are many applications that require the ability to generate waveforms relative to an external system trigger and or clock. In these scenarios the user would like to have confidence that the AWG can output a signal or signals consistently in relation to their system timing requirements. And in some applications more than two channels or multiple high speed outputs are required, so there is a need to synchronize multiple AWGs. To meet these requirements the user needs to understand the AWG regarding the trigger and clocking specifications and also understand the external configuration regarding how to set up the AWG in order to achieve maximum performance.

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Trigger specifications

External triggering is one of the most important requirements when trying to synchronize to any external system, and the "Trigger to Output Uncertainty" or “Trigger Jitter” specification is one users need to understand the most. This specification informs the user how much variation there is between when an external trigger arrives and the signal is output. This specification is dependent on how the AWG is clocked and how the trigger is synchronized to the clock. If we look at the Data Sheet you will find these specifications and conditions.

1. **Asynchronous Between Internal/External Clock and Trigger Timing**
   Between internal/external clock and trigger timing: 0.5 ns at 12 GS/s, 0.7 ns at 10 GS/s, 0.8 ns at 9 GS/s, 0.9 ns at 8 GS/s, 1.0 ns at 6 GS/s

   This specification is when the Clock and Trigger circuits are not synchronized. This is the most general use case when either using the internal AWG clock or an external clock but the trigger event is not synchronized to either of these clocks. The specification is dependent on the sample rate or clock rate used and several use cases are listed.

2. **Synchronous Between External Clock and Trigger Timing**
   Between external clock and trigger timing: 12 GS/s, X1 divider, synchronous trigger mode with specific timing (120ps p-p, 30ps RMS)

   This specification is when the External Clock and External Trigger circuits are synchronized. This method gives good results but does require precise synchronization between a quality external clock and the trigger event circuitry. The specification is also dependent on the sample rate or clock rate used and the best use case is listed.

3. **Synchronous Between External 10 MHz Reference and Trigger Timing**
   Between an external 10 MHz reference and trigger timing: 12 GS/s, synchronous trigger mode with specific timing (120ps p-p, 30ps RMS)

   This specification is when the External 10 MHz Reference and External Trigger circuits are synchronized. This method gives good results but does also require precise synchronization between a 10 MHz reference and the trigger event circuitry. The specification is also dependent on the sample rate or clock rate used and the best use case is listed.

4. **Synchronous Between External Variable Reference and Trigger Timing**
   Between external variable reference and trigger timing: 2n (n:integer) clock reference, synchronous trigger mode with specific timing (50ps p-p, 10ps RMS)

   This specification is when the External Variable Reference and External Trigger circuits are synchronized. This method gives the best results but does also require precise synchronization between a reference clock and the trigger event circuitry. The specification is also dependent on the sample rate or clock rate used and the best use case is listed.

As you can see from these specifications using the 4th configuration (Synchronous Between External Variable Reference and Trigger Timing) gives the best performance, so this method will be used in these discussions. This configuration also gives the user the capability of providing a lower frequency precision reference clock and the ability to multiply it up to <= 12 GHz or 12 Gs/s.

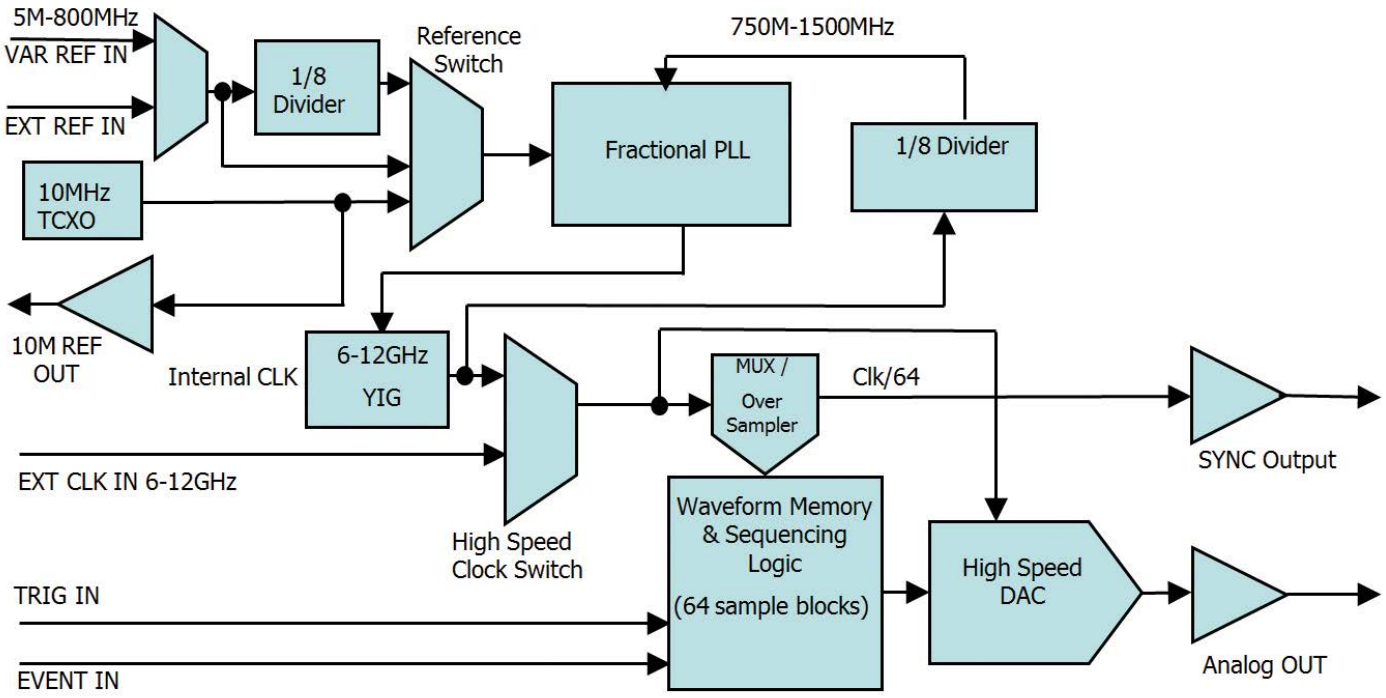

Figure 1. Simplified AWG clocking diagram.

AWG timing architecture

All of the internal AWG's timing characteristics are derived from a precision Yttrium Iron and Garnet (YIG) 6 – 12GHz tuned oscillator. In order to get the best synchronization and the lowest Trigger Uncertainty, the external reference and external trigger have to align with the internal clock edges of this YIG oscillator. To achieve low jitter on triggered waveforms out of the AWG, the trigger needs to be synchronized with the internal clock. If the trigger does not have a stable phase relationship with the internal clock, the output will jitter relative to the trigger as the instrument waits for the next available clock edge. Further restrictions are imposed by the fact that the waveform is pulled from memory in large blocks (64 samples for the AWG7122C). In a simple system this would mean that the waveforms could only start on boundaries of 64 sample clocks. The 7122C includes functionality to shift the waveform internally and start on boundaries of 4 sample clock cycles (333ps for a 12 GHz clock). This is called the trigger over-sampler and is the default configuration. This is where careful trigger timing comes in. In order to make the waveform start after a consistent delay from the trigger, the trigger needs to be time aligned to the center of the 4 sample wide trigger bins. So the trigger system needs to be designed to be synchronous and include a precision phase/delay adjustment mechanism.

There are two methods available to handle this trigger clock relationship.

Option 1

Use the Sync-Out signal with the trigger oversampler turned on (default) and use the Sync Out to know what the phase of the internal clocks are so that the trigger can be adjusted into one of the trigger sampling bins. The trigger sampling window size is small with this approach and a very accurate and stable system trigger is required.

Option 2

Turn off the Internal AWG trigger over-sampler. "TRIGger:SEQuence:MODE SYNChronous" This can only be done with a Program Interface (PI) command and must be re-sent if the instrument is turned off. The instrument will only start on boundaries of 64 samples (non-Interleaved), 128 samples (Interleaved). This makes the trigger time alignment relatively easy and robust. You only need to get it centered in the 64 sample interval. (64/12 GHz = 5.33 ns) . The restriction here is making sure the trigger is generated on multiples of 64. You still have to adjust the phase relationship of the trigger window so you would use the delay line to adjust the delay on the trigger and monitor on the scope to adjust for minimum trigger uncertainty.

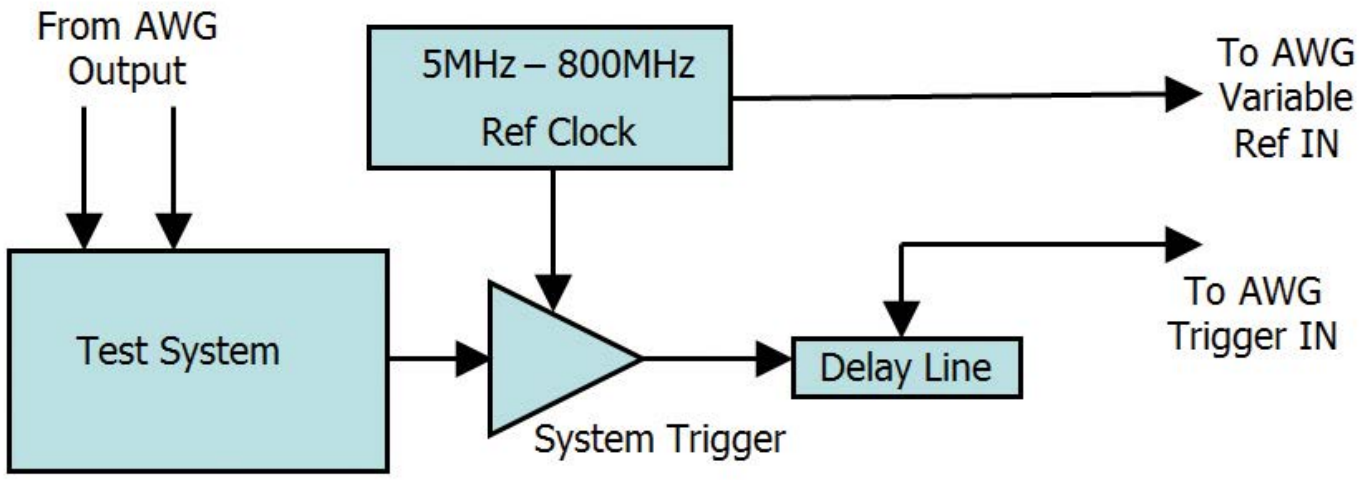

Figure 2. Simplified System clocking and trigger diagram.

External system requirements

Next we need to understand the requirements for the external clocking and trigger system. Since we are using the external variable reference as our reference source, it is important that the system trigger is synchronous to the ref clock being used.

In order to align the system trigger so that it matches the AWG clocking, the system needs some method to change the phase or delay of the trigger. In most cases the best method to do this is with a programmable variable delay line. See Figure 2 for more detail.

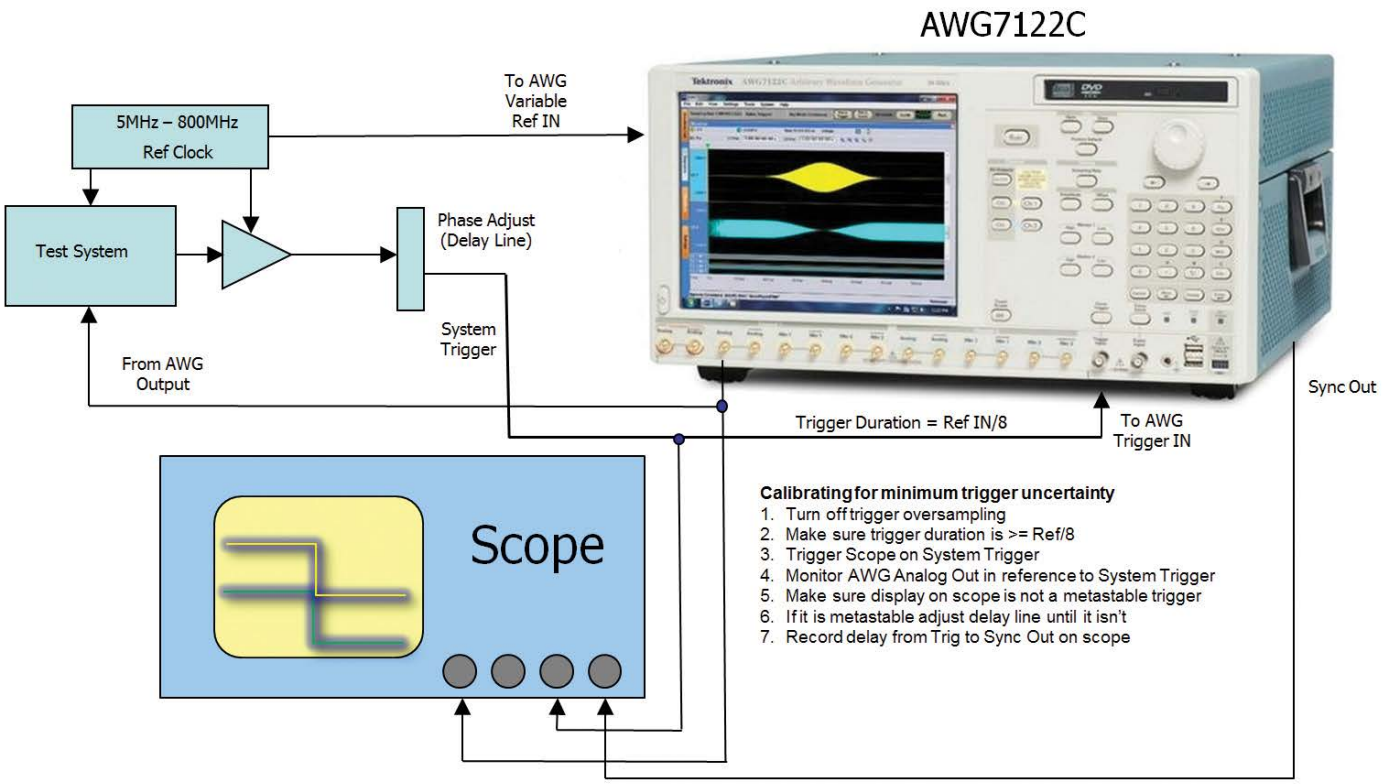

Figure 3. Calibration of Minimum Trigger Uncertainty.

Minimum Trigger Uncertainty Calibration

Looking at Figure 3 gives us an example of the configuration required to calibrate the minimum trigger uncertainty. To achieve this, the trigger needs to be synchronized with the sample clock. If the trigger does not have a stable phase relationship with the clock, the output will jitter relative to the trigger as the AWG waits for the next available clock edge. Once the calibration has been done and the measured delay values from Sync Out to the System trigger are recorded. These recorded values can be used when a new waveform or sequence is loaded instead of having to go through this whole procedure again.

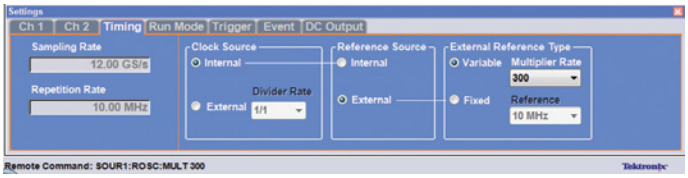

Figure 4. AWG Timing setup.

To guarantee minimum Trigger Uncertainty using option 2, these steps are required.

1. Turn off the Internal AWG trigger over sampler. Using the program interface command “TRIGger:SEQuence:MODE SYNChronous”
    a. This can only be done with a PI command, and has to be resent if the AWG is powered down.
2. Under the AWG Timing tab set the Clock Source to Internal. The Reference Source to External and the External Reference Type to Variable.
    a. For this setup let’s assume the Reference Clock being used is a precision 40 MHz clock and let’s also assume we would like to run the AWG at 12 Gs/s.
    b. In order to get 12 Gs/s we need to set the multiplier to 300. (40 MHz * 300 =12 GHz)

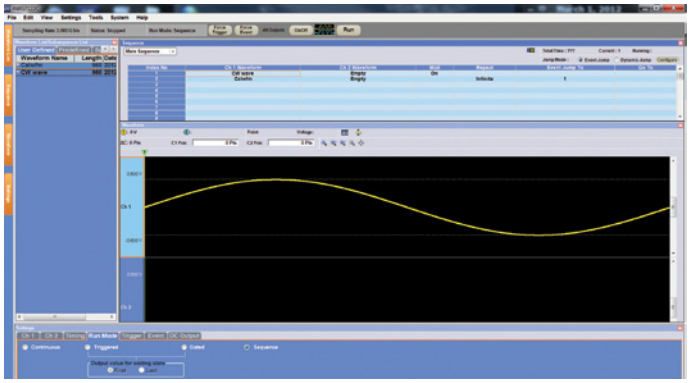

Figure 5. AWG Sequence Run mode setup.

3. Set AWG in Triggered or Sequencer Run mode. If using the sequencer the first waveform should have Wait turned on.

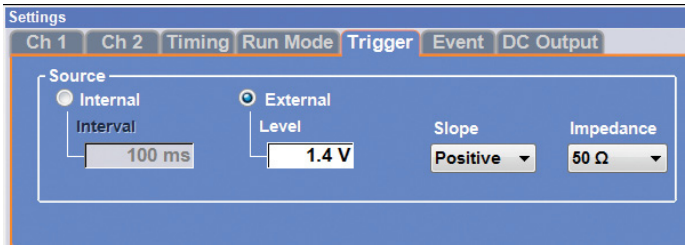

Figure 6. AWG Trigger setup.

4. Make sure external trigger is set correctly for the external system
5. Calculate Trigger duration. The simple calculation used to guarantee the trigger falls within the 64 sample boundary is to take the Ref CLK frequency and divide it by 8 (40 MHz / 8 = 5 MHz). So the minimum trigger period would be 5 MHz.
6. Set the trigger duration of the external system trigger to this calculated value (5 MHz)
7. Run the AWG
8. View the output of the AWG on the scope in an infinite persistence mode and adjust the trigger delay line until the minimum trigger is observed. In most cases using a phase detector can be used for this step instead of a scope.
9. Once the displayed trigger jitter is at its minimum, measure the delay between the Sync Out trigger and the system trigger. This will be our calibrated value and would be used if another waveform is loaded into the AWG without the need to look at the output again.

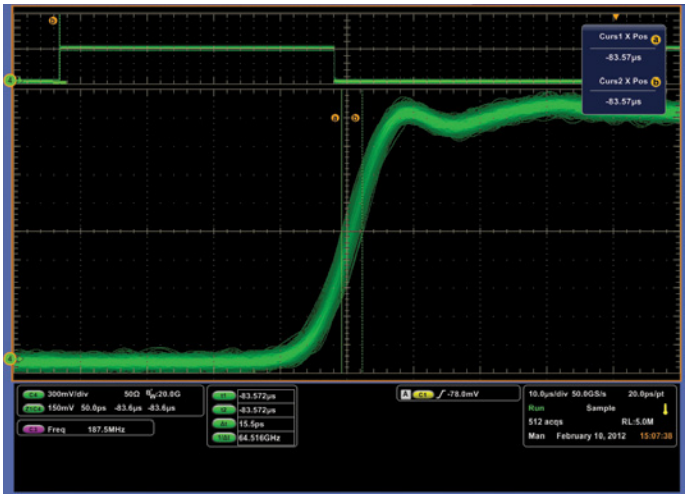

Figure 7. Minimum trigger jitter displayed (15.5ps).

10. If a new waveform or Sequence is loaded, in order to reset the alignment to the calibrated values, follow these steps.
    a. Turn off the Internal AWG trigger over sampler. Using the program interface command “TRIGger:SEQuence:MODE SYNChronous”
    b. Monitor Master Sync out and System Trigger with scope or phase detector.
    c. Adjust Trigger Delay (delay Line) until the delay value recorded in step 9 is set.

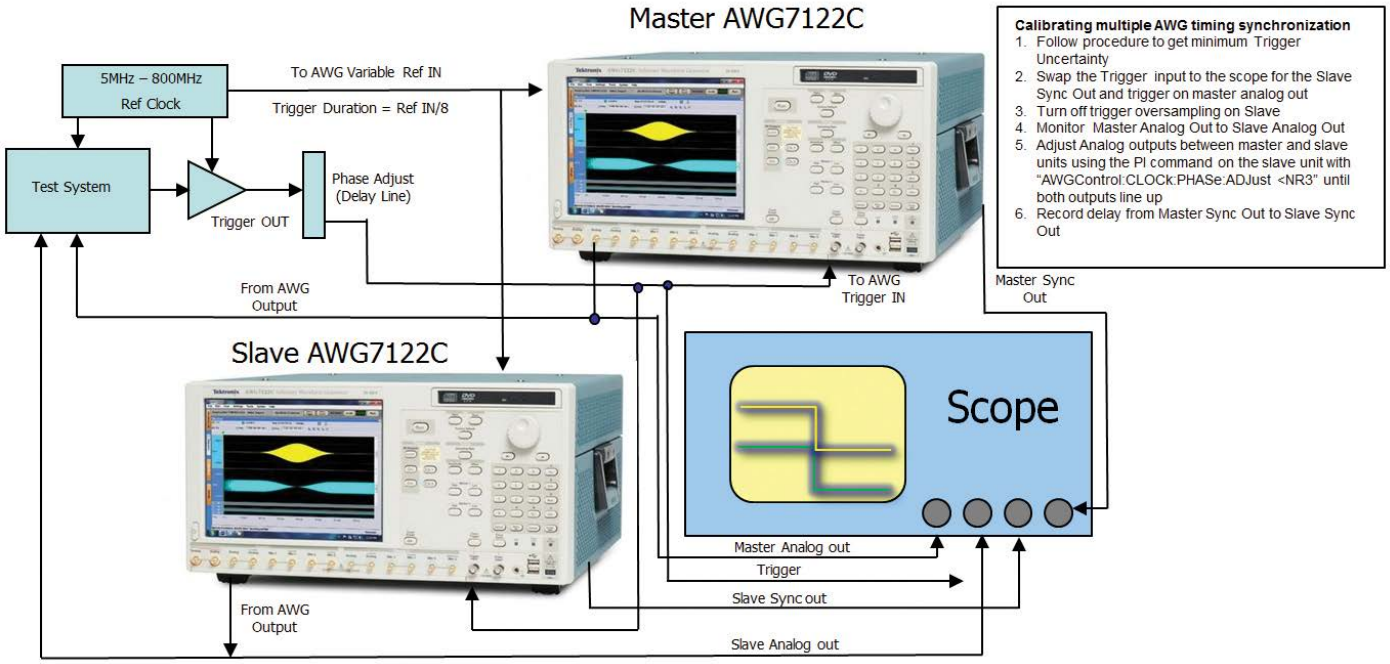

Figure 8. Multi AWG synchronization setup.

Synchronizing multiple AWGs using Sync Out

Once the minimum trigger jitter has been achieved this AWG would be used as the Master AWG in a multi-unit configuration. In order to guarantee multiple AWGs start at the same time more calibration is required.

1. Setup Master instrument using previous configuration to get minimum trigger uncertainty.
2. Turn off the AWG trigger over sampler on both AWGs. "TRIGger:SEQuence:MODE SYNChronous"
3. Adjust Analog outputs between master and slave units using the PI command on the slave unit with "AWGControl:CLOCk:PHASe:ADJust <NR3>" (NR3 = ± 72000) **7000B and C units only*
4. Measure Master Sync Out and the Slave Sync Out timing relationship. *(This is used to reset timing if a new waveform is loaded)*

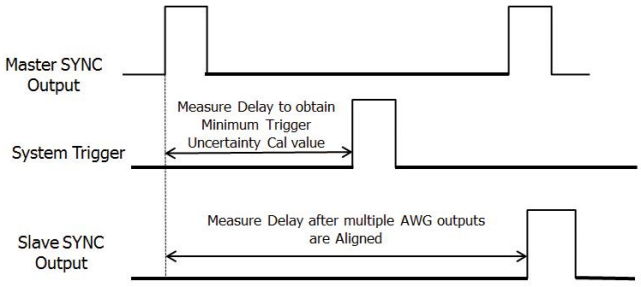

Figure 9. Multi AWG cal timing diag.

5. If a new Waveform or Sequence is loaded, in order to reset the alignment to the calibrated values, follow these steps.
   a. Turn off the Internal AWG trigger over sampler. Using the program interface command "TRIGger:SEQuence:MODE SYNChronous".
   b. Make sure previous setup for re-establishing minimum trigger uncertainty is performed.
   c. Monitor the Slave Sync Out in reference to the Master Sync Out signals.
   d. Adjust the Slave unit clock phase with "AWGControl:CLOCk:PHASe:ADJust" command until the calibrated value that was recorded is set.

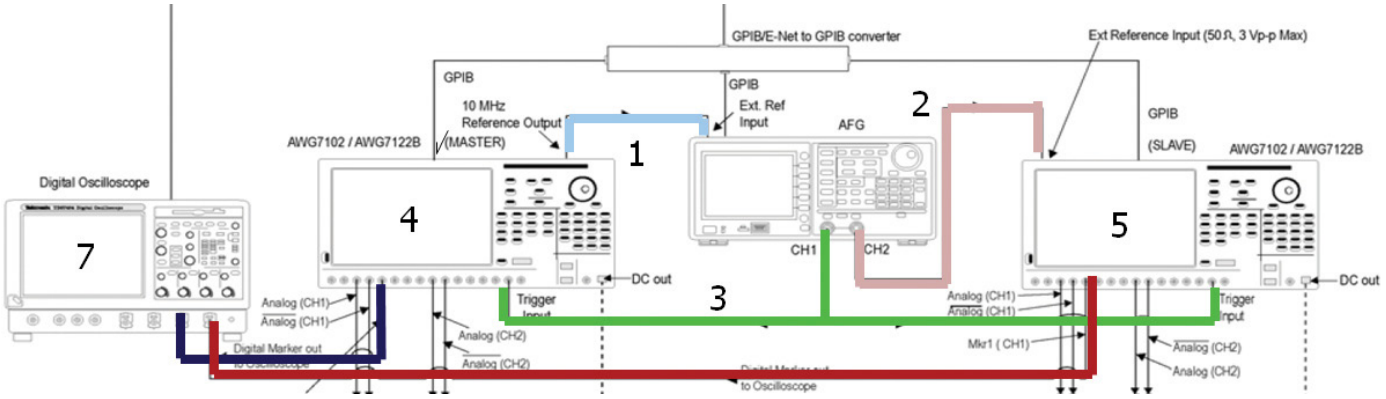

Figure 10. Multi AWG synchronization setup using AFG.

Synchronizing multiple AWGs without Sync Out

AWG7000 series with serial numbers below B040xxx will not have the sync output connectors so another method can be used. This method is used in Tektronix HDMI HT3 application where two AWGs are required. This example uses an AFG3000 series as the Trigger and Ref Clock instead of using an external system trigger and clock.

The procedure is as follows.

1. Connect Master AWG 10 MHz Ref Out to AFG Ref In
2. Set AFG Ch2 for 10 Mhz sine, continuous (used for ref clock phase adjust)
   Connect to AWG slave ref clock input
3. Set AFG Ch1 for Pulse 10 MHz 5% duty (used for trig)
   Burst mode 1 cycle, clock = external ref from master AWG, external trig
   Connect Ch1 output on AFG to Ext Trigger inputs on both AWGs
4. Set AWG Master CH1 square wave 960pts, 1 cycle, internal clock, 10 MHz ref out goes to AFG ref in

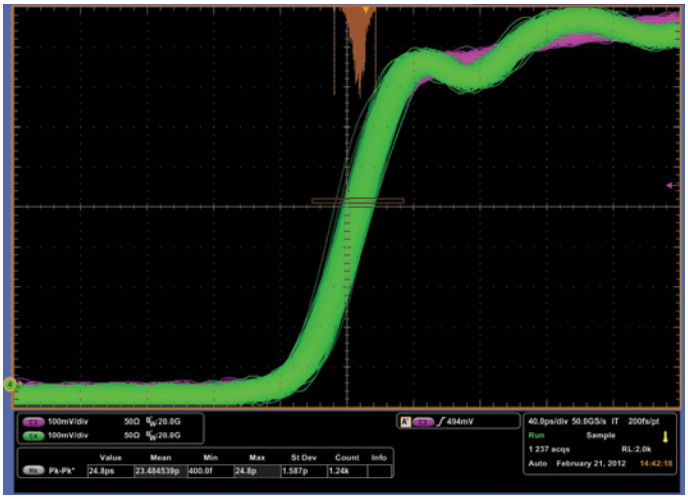

Figure 11. Multi AWG channel alignment using AFG.

5. Set AWG Slave ch1 square wave 960pts, 1 cycle, Set External variable Ref multiplier to 1200
6. Set both AWGs using Wait in Sequence and external trigger from AFG CH1.
   Run both AWG, notice they are waiting for trigger
7. Adjust the Phase on AFG Ch2 until Markers on AWGs align on scope as in Figure 11.

Conclusion

Synchronous test systems are becoming more important in many applications and being able reduce any uncertainty of when a trigger is sent to when the signals are outputted is challenging for any system. Being able to add multiple boxes to enable more channels and still maintain timing relationships is also very important to many users, especially when higher sample rates and more than one channel are required. With the discussed configurations users can support these applications that require these very precise timing characteristics. It is also possible to synchronize with other configurations but this discussion is to provide the best methods to achieve maximum performance.

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