



AWG70000 Series Multiple Unit Synchronization

How-To Guide

What you will learn:

This guide will explain the AWG clocking and triggering and then provide a step-by-step recommended method of synchronization.

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Introduction

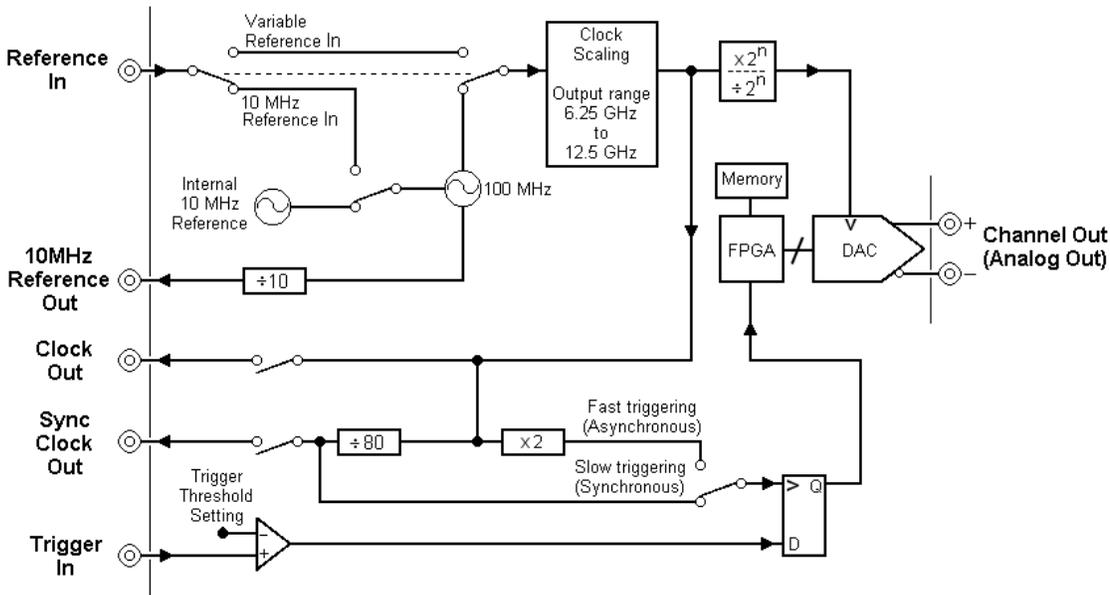
With data and transmission speeds increasing, faster test generator requirements are also increasing. With AWG (Arbitrary Waveform Generator) sample rates and max freq. response now available up to 50GS/s and 20GHz respectively, engineers can now finally test many designs that were only simulations before. The newest test challenges are pushing the limits on these test equipment capabilities. Applications such as Coherent Optical Transmission with up to 30GB/s rates and long haul optical data transmission, with rates up to 1.5Tb/s, require the fastest sample rates available. Not only that, but these capabilities require multiple channels to support IQ modulation techniques.

With the introduction of the Tektronix AWG70001A and its 50 GS/s single channel capability, engineers are looking to combine two or more of these units to fulfill these challenging requirements. Not only do they need multiple channels at these rates, but the units must also be synchronized to each other and be able to output coherent signals totally synchronized.

This guide will walk you through the recommended method of synchronization.

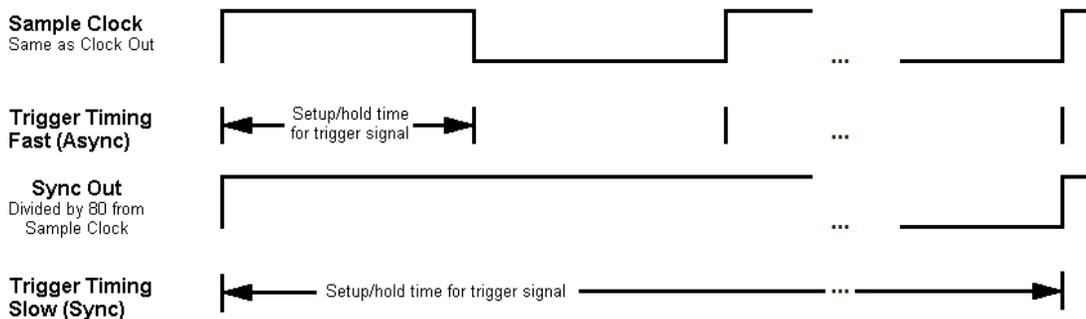
AWG Clocking and Triggering

In order to understand the best methods of synchronization first we need to familiarize ourselves with the AWG clocking and triggering. Notice in this diagram that when we use the slow triggering (Synchronous mode) the ref clock is still divided by 80 (the same as the Sync Out).



Clock and Trigger Block Diagram

Async and Sync Timing



Async and Sync Timing Diagram

As you can see in this diagram, using the **Slow Sync** mode allows for a much wider trigger sample and hold area to allow for easier trigger synchronization.

Alignment Between Instruments is a Three Step Process

1. First we need to set the instruments up with a common clock reference and the same sample rate.

- It is best to use a higher frequency reference rather than 10 MHz to minimize jitter between channels. The Variable reference input accepts signals between 35 and 250 MHz.
- The sample rate must be an integer multiple of the divided reference in the clock circuit. The easiest way to insure this is to select the "Jitter Reduction" mode in the clock menu. (The reference circuit divides the variable reference by 1,2 or 4 to insure an internal frequency between 35 MHz and 70MHz)

2. To start waveforms at the same time the multiple AWGs can be triggered with a common external trigger.

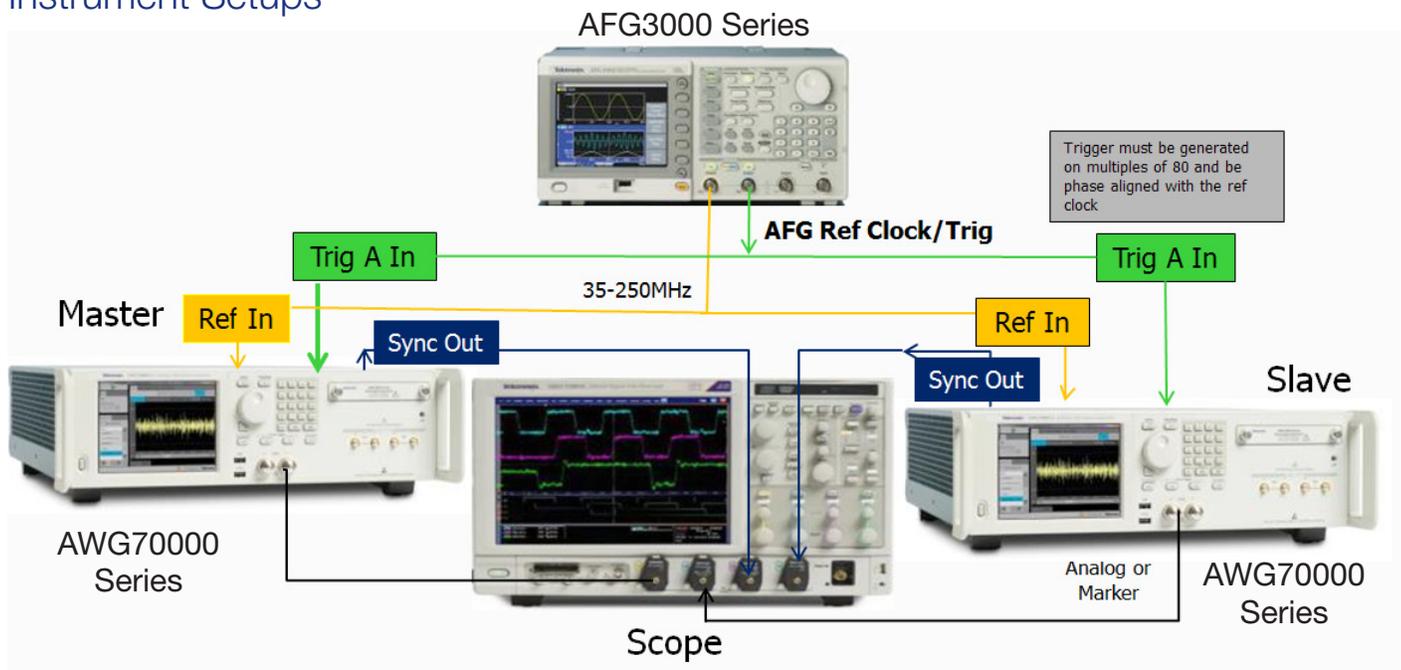
- The AWGs are set to synchronous trigger mode, which starts waveform output on a divided clock edge rather than a sample clock edge. This provides a wider setup and hold window trigger timing.
- The trigger should be synchronous with the internal divided clock for the most reliable triggering.
- The divided clock frequency is the clock frequency/80. So for an interleave sample rate of 50 GS/s, each DAC operates at 25 GS/s, the clock is at 12.5 GHz and the divided clock is 156.25 MHz. The Sync out clock on the back panel is a replica of the divided clock. It can be enabled in the clock menu.
- We need to generate a trigger from the 100MHz reference that is also synchronous with the divided clock. $156.25\text{MHz}/250\text{KHz} = 625$ (an Integer) and $100\text{MHz}/250\text{KHz} = 400$ (also an integer). So 250 KHz will work. It might be better to use a lower rate like 50 KHz with a short pulse so there is a smaller chance of pushing output on button during the high part of the trigger pulse. Note:
 - In order to guarantee synchronization the trigger rate needs to be a multiple of the /80 clock. So trigger rate needs to be a divide rate that works for both the reference clock and /80 clock.
 - It is also recommended to reduce the duty cycle of the trigger pulse to around a 30 ns high time along with the 50KHz rate which is really what will reduce the probability of turning on the AFG during a high pulse on the trigger.

- We can set up an AFG to provide the 100MHz reference from one channel and a synchronous 50 KHz output from the second channel. Then we manually switch the 50 KHz on and off to enable the trigger.
- It is useful to observe the Sync Out clocks of the AWG's, but because of the skew from the divided clock to the analog output, the Sync Out clocks of the AWGs might not line up when the outputs are aligned. For a given sample rate, however, the timing relationship is stable. Triggering occurs on the positive half cycle of the Sync Out clock, so it might be necessary to use different length cables in the trigger paths to trigger on the same cycle.
- The delay of the trigger relative to the reference might need an experimental adjustment to get reliable setup and hold timing.

3. When the AWGs start up, the internal divided clocks start with a random phase relative to one another. As a result, the outputs need to be aligned each time the sample rate is changed or the clock is stopped. In addition, there is timing skew from this divided clock to the output that is unique to each instrument.

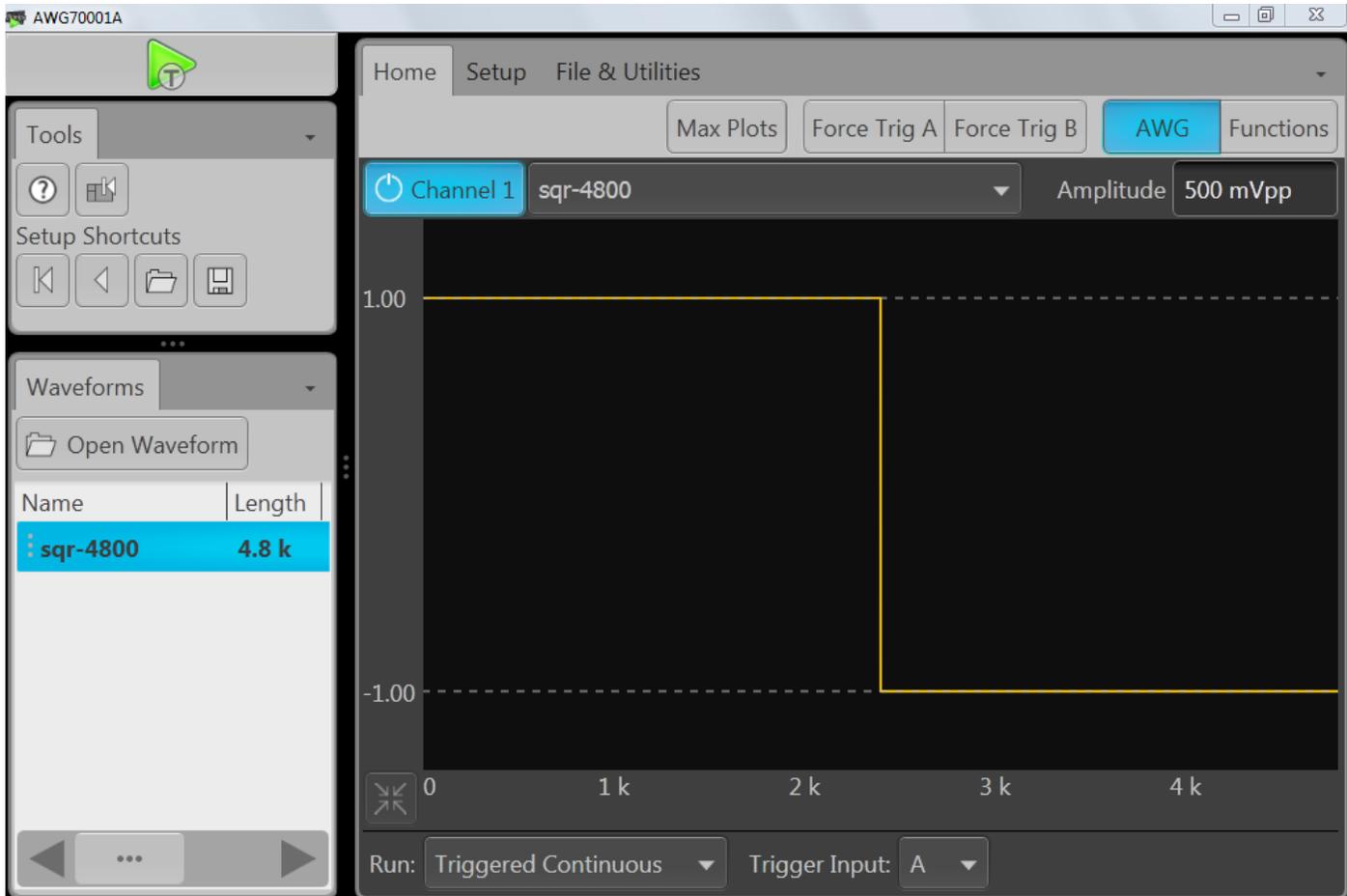
- Alignment is accomplished by observing the output signal or marker from each AWG and adjusting the clock phase until they line up.
- This is where there is an element of random chance in the setup. If the initial startup is too far out of alignment ($> 2\text{ns}$) then there will not be enough range to adjust the phase of one AWG to line up with the other. In this case you need to force the clocks to start again until a reasonable starting condition is achieved. This can be done by switching to Internal Reference and back to External in the Setup/Clock menu. Restart both AWGs if necessary. Experiment with this while observing the AWG outputs and the Sync Out clocks. The outputs need to start out less than 2ns apart to be within range of alignment.

Instrument Setups



Recommended Equipment:

- 2) AWG70Ks
This method will also work with more than 2 AWGs, although care will have to be taken to match cable delays.
- 1) AFG3252
- 1) High BW scope \geq DPO70804C
- 2) 103-0030-00 - BNC "T" connectors
- 4) 015-1018-00 - SMA Male to BNC Female adapter
- 4) 012-0076-00 - 18 in., male-to-male BNC cables
- 4) 174-5771-00 - 38 in. male-to-male precision SMA cables



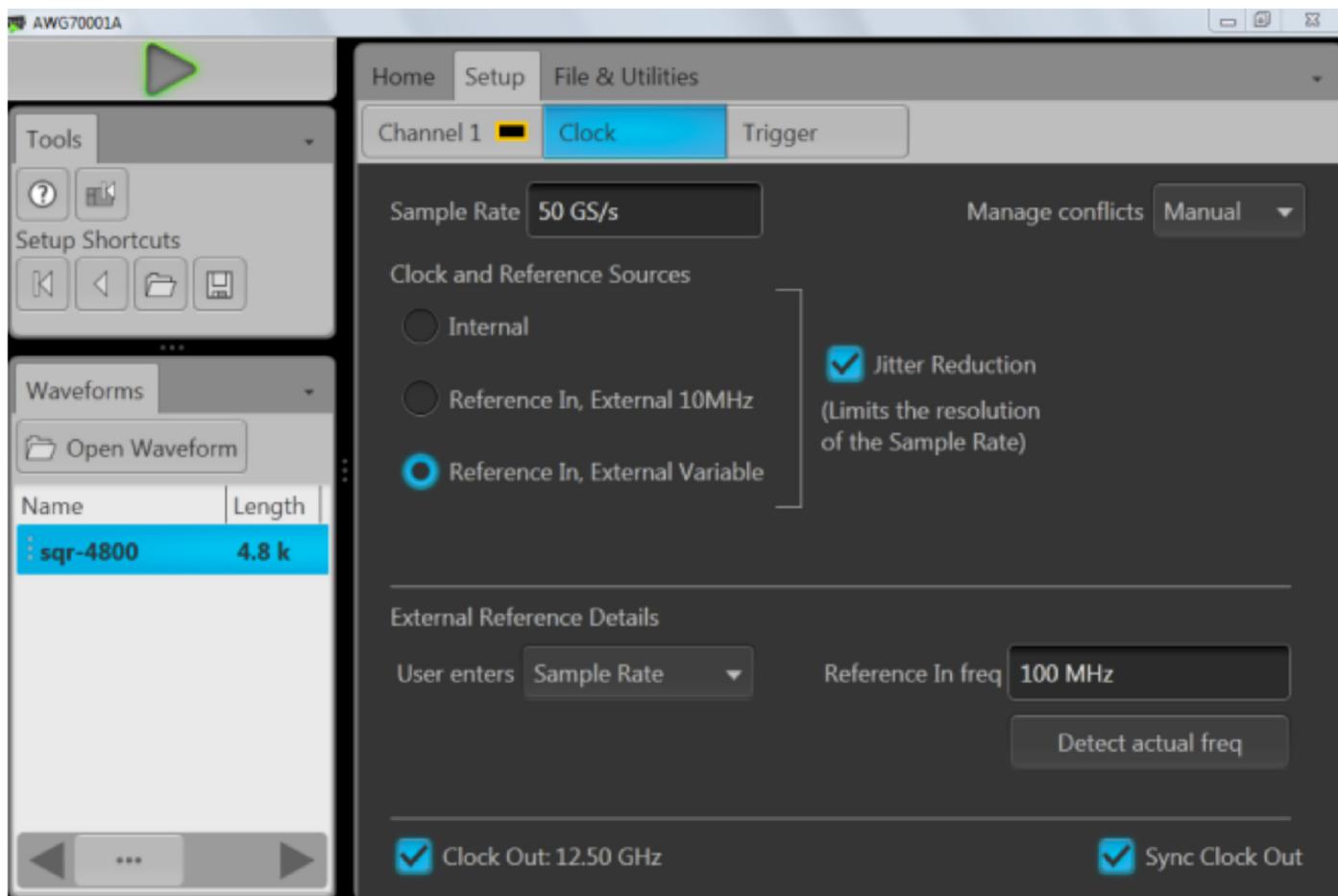
AWG Home menu and A trigger and Triggered Continuous selected.

AFG3000 Series Setup

1. Set AFG Ch1 to 100MHz sine wave, 5vp-p, Continuous
2. Set AFG Ch2 to pulse 50KHz, width 100ns, 5v High 0 low, Continuous
3. Ch1 on
4. Ch2 off (this will be used as a manual trig later)

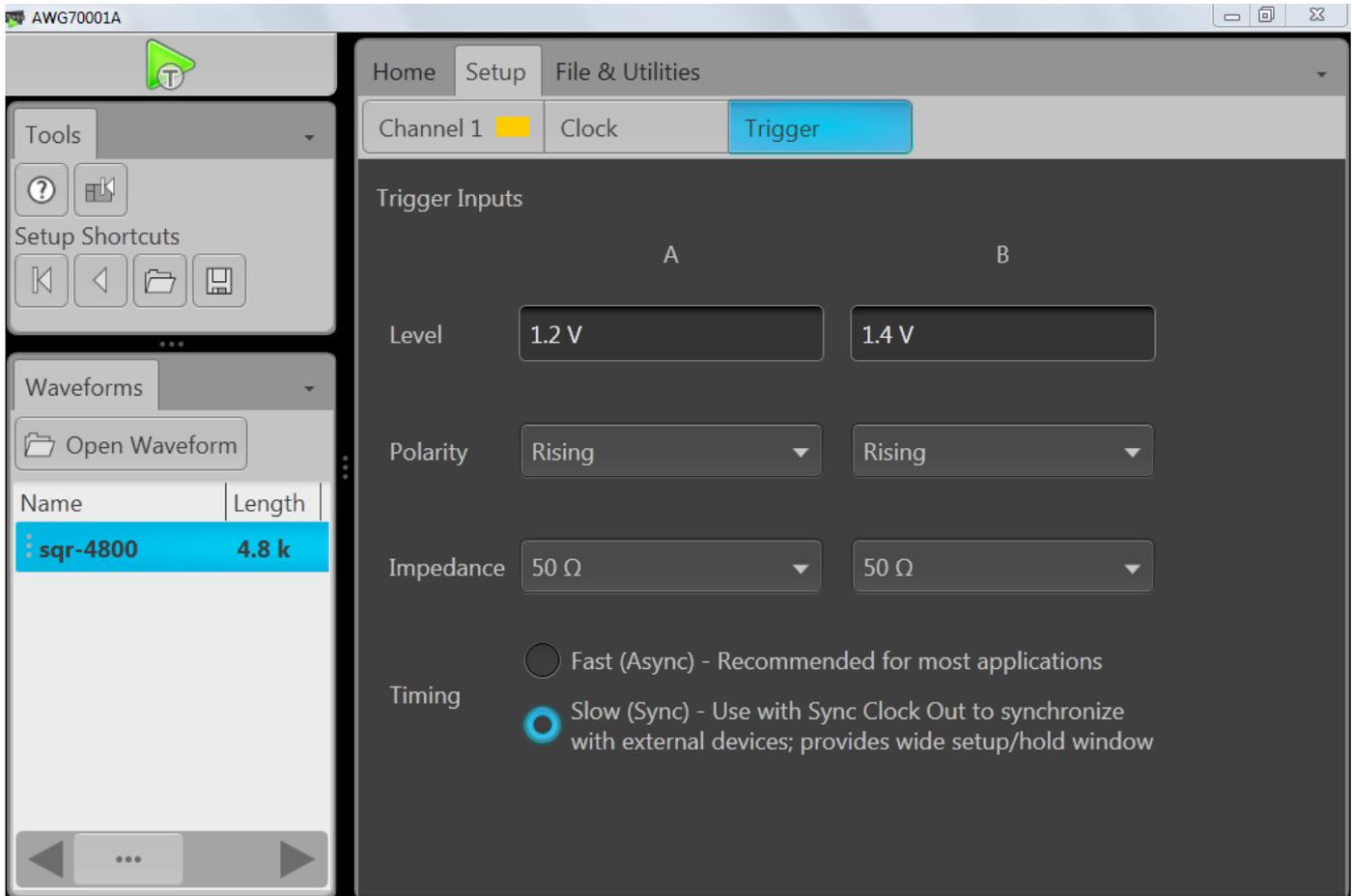
AWG70001A Setup

1. If using AWG70001As, load a 4800 point square wave into CH1 of both instruments. If using AWG70002As, load a 2400 point square wave into Ch1 of both instruments.
2. From the Home menu select Trigger input to Trig A , Run Mode Triggered Continuous
 - a. It may be useful to set the Run mode to Triggered, this will allow real time output phase adjustment while watching signals on the scope.
 - b. Using the Trigger Continuous Run mode once everything is setup would give best performance since the AWGs only wait for one trigger and then run the waveforms continuous.



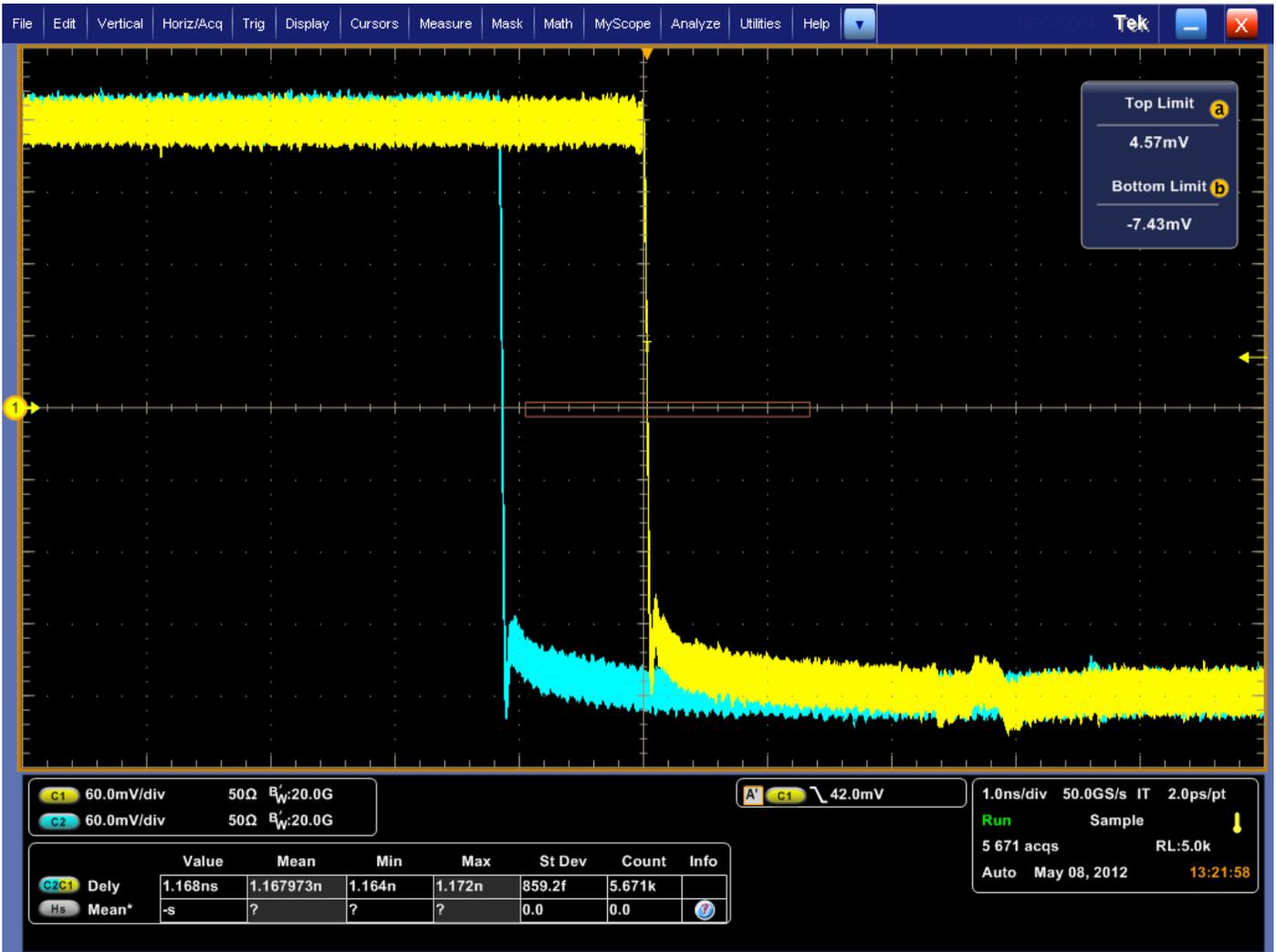
Clock setup menu using External Variable Reference of 100MHz and sample rate of 50GS/s.

3. From the setup clock menu set both AWGs to use **Variable Ref Clock**
4. Set **Manage conflicts** set to **Manual**.
5. Make sure to set AWGs to **Jitter Reduction Mode**
6. Make sure the Reference in Freq locks to the **100MHz Ref** when selecting **Detect actual freq**.
7. Set **Sample Rate** to **50GS/s**
8. Select **Sync Out** (*this turns on the sync output*)
9. In the Trigger menu, Set **Trigger A** to **1.2V, Rising, 50ohms**.
10. Select **Timing Slow (Sync)**



Trigger setup menu.

11. Make sure AWGs are waiting for a Trigger by toggling the Play button making sure it is yellow.

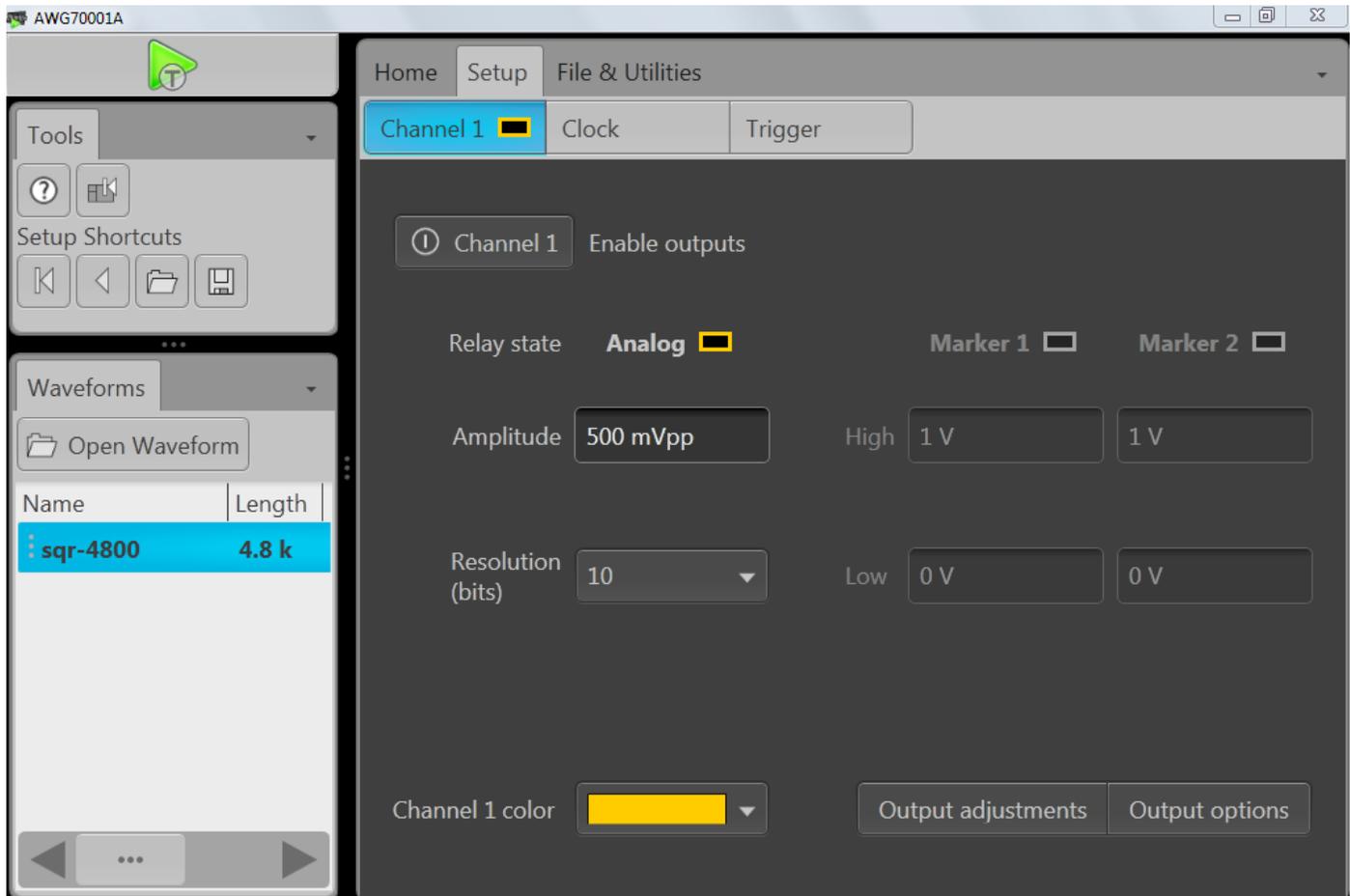


Timing skew between AWGs analog output. (Notice skew is less the 2ns).

Aligning Output

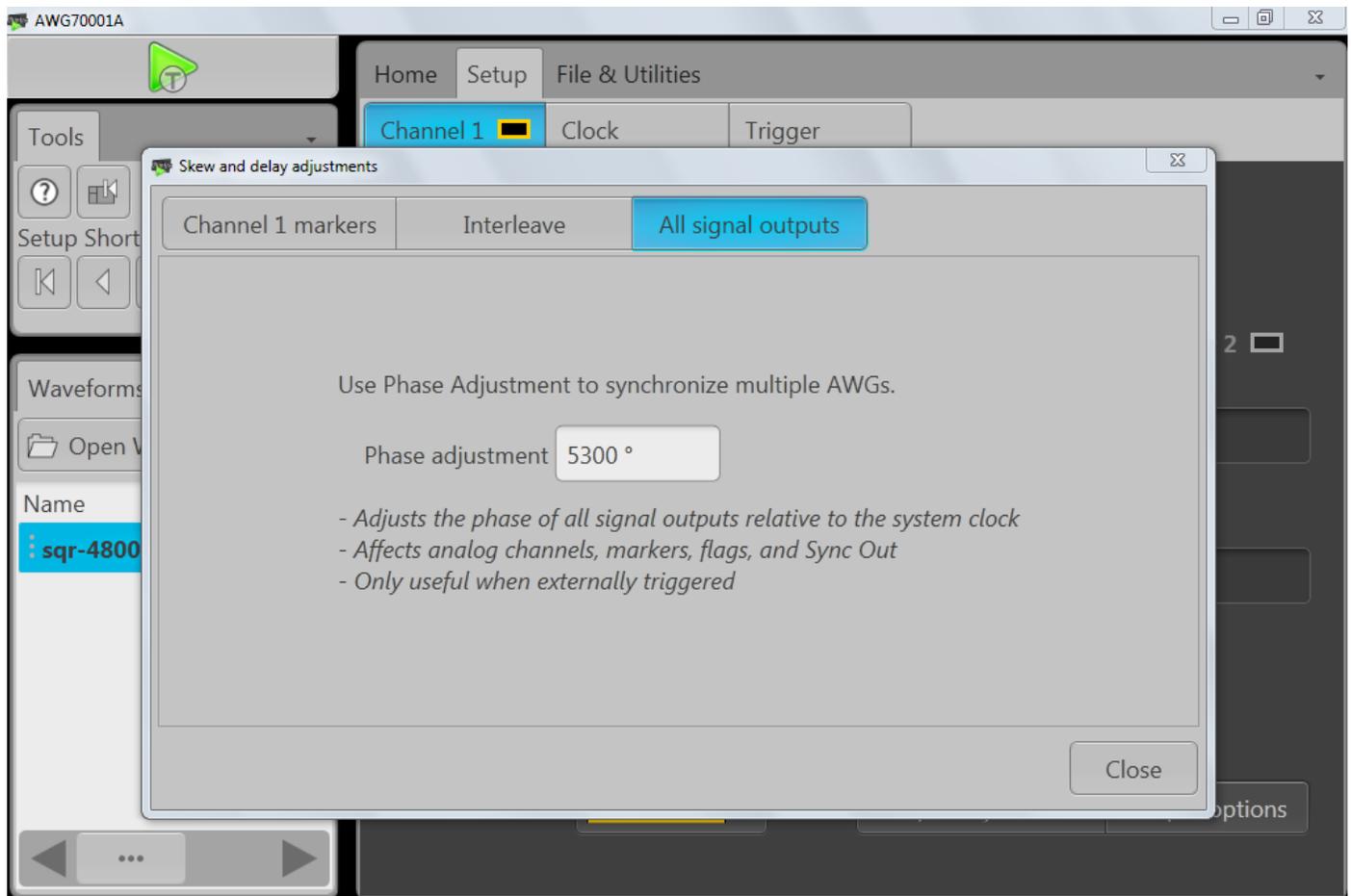
1. Turn on Ch2 of AFG
2. Both AWGs **Play** icon should turn green
3. If the analog and sync signals being observed on the scope are > 2ns apart this step will have to be repeated.
 - a. Turn off Ch2 of AFG.
 - b. Set AWG clock to Internal and back to External Reference.
 - c. Turn on AFG ch2 again.
4. Once the outputs are within adjustment range.

- In **Setup Channel** menu select Output Adjustments

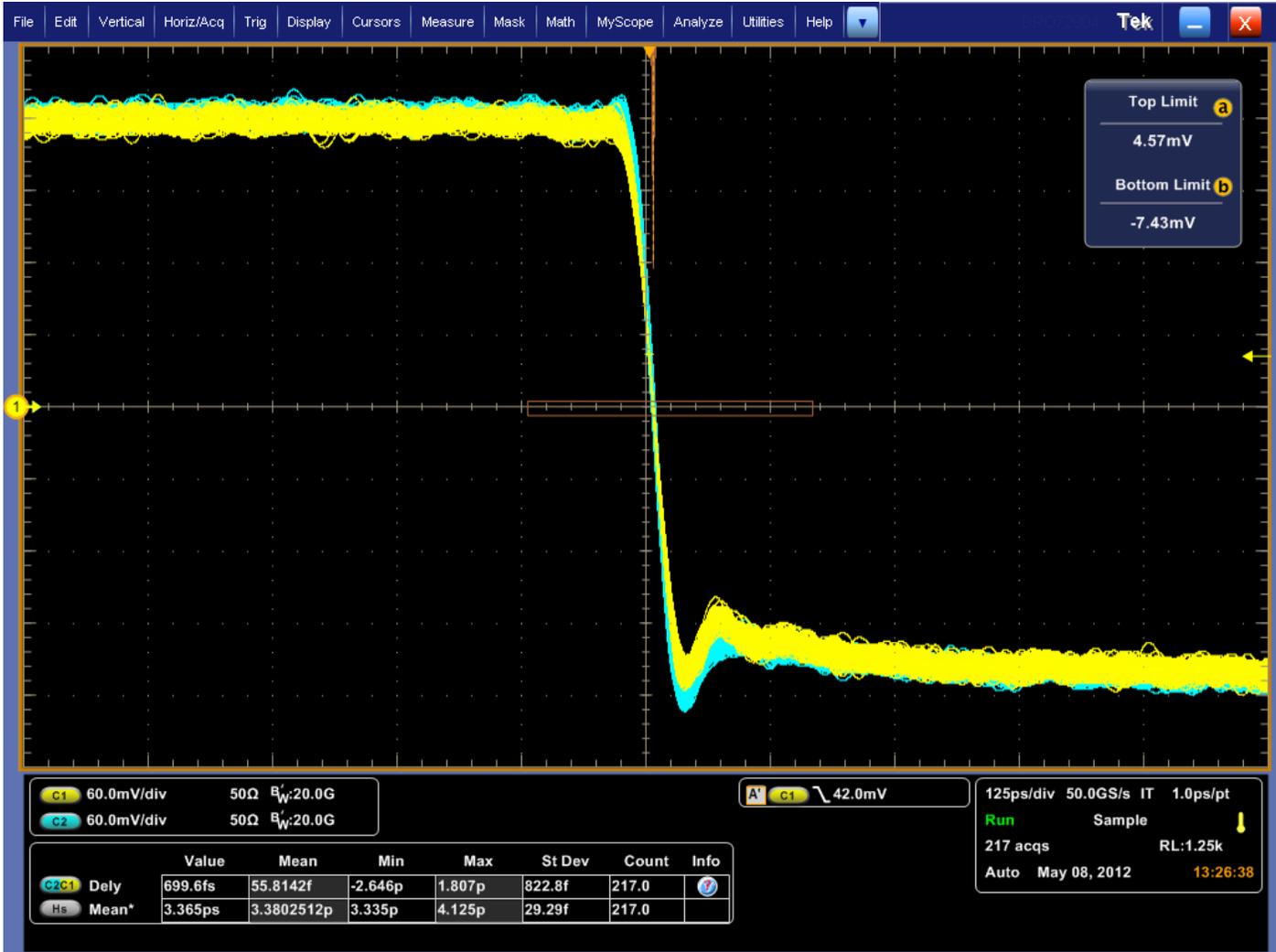


AWG Channel setup with Output adjustments selection.

- Then select the **All Signal Outputs** tab

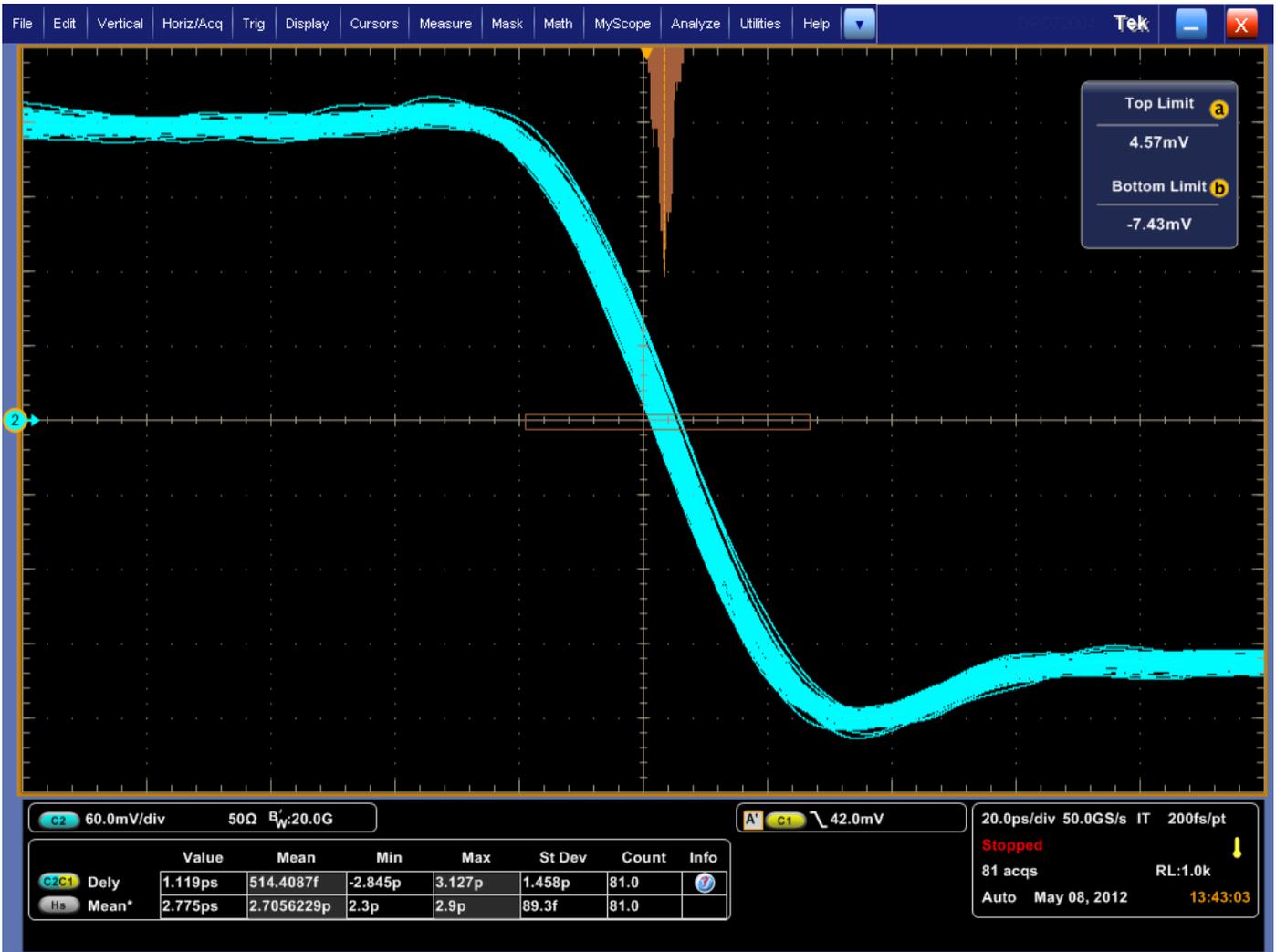


7. Adjust **phase** on slave unit until both AWGs ch1 line up on scope.



Minimum Skew adjusted between the two AWG outputs.

- Timing between AWGs: The **All signal outputs** phase can be adjusted and any time for fine timing alignment.



Minimum Skew adjusted between the two AWG outputs. Notice the 2.775ps measurement. With this configuration trigger jitter as low as 700fs has been achieved.

- Interleave timing: In the AWG70001A at sample rates above 25 GS/s, timing between the two interleaved DACs can be adjusted as well as the amplitude balance. The control is in the **Setup/Channel** tab. Click the **Output adjustments** button.

Changing Waveforms in AWGs

1. In order to change the waveform without losing the sync timing you need to first turn off ch2 of the AFG to remove the trigger.
2. Change to new waveform making sure that the Sample Rate is not changed.
3. Check that the AWGs run button is yellow making sure the AWG's triggers are armed. If not Re-arm the triggers on both AWGs by pushing the Run button.
4. Turn the AFG Ch2 on to send a new trigger to start the waveforms.

Conclusion

- With the AWG70001A sample rates as high as 50GS/s and output frequency responses as high as 20GHz. Engineers can now test circuits that were not easily tested before.
- Many of these applications require more than a single output capability.
- The AWG70000 series can be synchronized with minimum trigger uncertainty and phase delays to allow multiple high data rate outputs.

Contact Tektronix:

- ASEAN / Australia** (65) 6356 3900
- Austria*** 00800 2255 4835
- Balkans, Israel, South Africa and other ISE Countries** +41 52 675 3777
- Belgium*** 00800 2255 4835
- Brazil** +55 (11) 3759 7627
- Canada** 1 (800) 833-9200
- Central East Europe and the Baltics** +41 52 675 3777
- Central Europe & Greece** +41 52 675 3777
- Denmark** +45 80 88 1401
- Finland** +41 52 675 3777
- France*** 00800 2255 4835
- Germany*** 00800 2255 4835
- Hong Kong** 400-820-5835
- Ireland*** 00800 2255 4835
- India** +91-80-30792600
- Italy*** 00800 2255 4835
- Japan** 0120-441-046
- Luxembourg** +41 52 675 3777
- Macau** 400-820-5835
- Mongolia** 400-820-5835
- Mexico, Central/South America & Caribbean** 52 (55) 56 04 50 90
- Middle East, Asia and North Africa** +41 52 675 3777
- The Netherlands*** 00800 2255 4835
- Norway** 800 16098
- People's Republic of China** 400-820-5835
- Poland** +41 52 675 3777
- Portugal** 80 08 12370
- Puerto Rico** 1 (800) 833-9200
- Republic of Korea** +822-6917-5000
- Russia** +7 (495) 7484900
- Singapore** +65 6356-3900
- South Africa** +27 11 206 8360
- Spain*** 00800 2255 4835
- Sweden*** 00800 2255 4835
- Switzerland*** 00800 2255 4835
- Taiwan** 886-2-2656-6688
- United Kingdom*** 00800 2255 4835
- USA** 1 (800) 833-9200

* If the European phone number above is not accessible,
please call +41 52 675 3777

Contact List Updated March 2013

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