Simplifying Validation and Debug of USB 3.0 Designs
- Tektronix USB Testing Solutions

USB Industry Leadership

- Tektronix 1st to market for USB 2.0
- Millions of certified products shipped, enabled by Tektronix USB solutions
- Only approved Method of Implementation (MOI) for WiMedia PHY Leadership in USB
- Tektronix is only T&M Technical Contributor in the USB 3.0 specification!
- Members of the Compliance Workgroup and Contributors to the Physical Layer Compliance Test Specification
USB 3.0 Technology Timeline & Tektronix Involvement

<table>
<thead>
<tr>
<th>Year</th>
<th>Events</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>Spec Development, Silicon Phase</td>
</tr>
<tr>
<td>2009</td>
<td>Test Vendor Compliance Group Participation, USB-IF Tool Development, Test Vendor Compliance Group Participation, PIL (Peripheral Interop Lab)</td>
</tr>
<tr>
<td>2010</td>
<td>USB-IF Plugfests, continuous time linear equalizer (CTLE) at Rx, link layer</td>
</tr>
<tr>
<td>2011</td>
<td>USB-IF Plugfests, continuous time linear equalizer (CTLE) at Rx, link layer</td>
</tr>
</tbody>
</table>

Tektronix Test Solution Updates
- Transmitter, Receiver, Channel

USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12’ Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Link Layer
  - Equalization
  - Link Training
  - Scrambling/Polarity Inversion
  - Low power states

Source: USB 3.0 Rev 1.0 Specification
Differences from High-Speed Electricals

- **High-Speed**
  - 480MT/s
  - No-SSC
  - 2 wires for signaling
    - Tx and Rx use the same wire
    - 1 bi-directional link
  - DC coupled bus
  - NRZ encoding

- **SuperSpeed**
  - 5.0GT/s (10X speed increase)
  - SSC is required
  - 4 wires for signaling
    - 2 for Tx and 2 for Rx
    - Each Uni-directional
  - AC Coupled bus
  - 8b/10b Encoded (Scrambling)
  - Link Layer (Similar to PCIe)
  - Power Management

Tektronix Solutions for USB 3.0 Transmitter Testing

- **Comprehensive Solution Goes Beyond Compliance**
  - All measurements accessible in DPOJET for debug
  - Support for multiple test points (i.e. at the silicon pins or compliance test point)

- **Complete Toolset for Characterizing USB 3.0 Designs**
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)

- **Automated**
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG

- **SigTest Integration**
  - SigTest is completely integrated into TekExpress
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results

- **Comprehensive Reporting**
  - Complete Test Report in .mht format with pass / fail and margin results
  - Plots include for quick visual inspection
USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
  - Reference channel is embedded and CTLE is applied
- USB 3.0 Reference Channels
  - Host Reference Channel
    - 11" back panel is applied for device testing
  - Device Reference Channel
    - 5" device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels
- USB 3.0 Reference Equalizer
  - Attenuates the low frequency content of the signal to open the eye

USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing
    - Available from the USB-IF
Fixture and Channel De-Embedding

- Why de-embed - Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins
- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software

Channel Embedding

- Compliance Testing is done by embedding the compliance channel, but many designers want to validate other channel models
  - Understand transmitter margin given worst case channels
  - Model channel and cable combinations beyond compliance requirements
  - Create interconnect models with SDLA software to analyze channel effects

Before After

USB-IF Host & Device HW Channels
Receiver Equalization

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix’ USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)

USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation
Voltage and Timing Measurements

- Measured on 1M UI after JTF has been applied
- Voltage
  - Measured on CP0 Pattern
- Jitter
  - Measured on CP0 and CP1 Pattern
    - DJ is measured on CP0 and RJ on CP1
    - TJ is computed by combining DJ on CP0 and RJ on CP1

SSC Measurements

- Verify that the DUT SSC profile meets the requirements of the specification
- Done on CP1 Pattern

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Units</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>M_{\text{modulation}}</td>
<td>Modulation Rate</td>
<td>30</td>
<td>33</td>
</tr>
<tr>
<td>\sigma_{\text{SSC}}</td>
<td>SSC deviation</td>
<td>&lt;0-4000</td>
<td>&lt;0-3000</td>
</tr>
</tbody>
</table>

- NOTE: If a host does not generate its own SSC profile it will be tested with the SSC profile of the motherboard. Motherboard SSC profile should be verified before testing
LFPS Measurements

- Low Frequency Period Signaling
  - Used to establish link communication during link bring-up, exit from power states, and link re-set
- TX Test
  - Verifies that the DUT transmitted LFPS signal is in specification
- RX Test
  - Verifies that the DUT will respond to LFPS signal by sending out Transmitter Equalization (TSEQ) sequence
  - Tested over different amplitude and duty cycle

Transmitter Compliance Test Setup

- USB-IF or Tektronix fixtures can be used
  - Test configuration is the same
- Compliance channel and 3 meter cable are emulated in software
  - Compliance sparameters were used to create channel filters

CTLE is applied to open the eye, then compliance measurements are taken.
Compliance channel and Cable are applied in software, resulting in a closed eye.
USB 3.0 Compliance and Automation

- Complete Automation of USB 3.0 Measurements with TekExpress
- No need to learn technology specific software applications- TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
- TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug

TekExpress USB 3.0 Automated Solution

- Supports testing for USB 3.0 Hosts and Devices
- Automatically selects the correct channel emulation filter when software is selected
- Easily select measurements of interest for test execution
- Supports all compliance and LFPS TX measurements
- User choice of algorithm execution- SigTest or DPOJET
- Automates DUT toggling to acquire CP0, CP1, and LFPS Patterns
Automated SigTest or DPOJET Measurement Selection

• What is SigTest
  – SigTest is Compliance Certification Software provided by the USB-IF that provides pass/fail results
  – Is the Gold Standard for Certifying Devices
• Flexibility to chose between SigTest or DPOJET to make USB 3.0 Measurements
• SSC and LFPS Measurements will always be made with DPOJET as they are not supported in SigTest
• SigTest will automatically be invoked by TekExpress with no need for manual intervention
• The acquired waveform with the compliance channel embedded will be set to SigTest for processing
• SigTest will apply the CTLE and then report the measurement results in the SigTest report

Test Execution Results

• Real Time Update of Test Results
• Easily distinguish between pass or fail tests
• Limits are displayed along with margins to quickly identify how much margin exists in the design
Comprehensive Test Report

- Includes overall test status in tabular format and plots
- Details of test configuration are listed on the report, including Test Equipment Firmware and Software versions and test parameters
- Direct link in the test report to the SigTest report
- Test report can be saved and distributed for further analysis

USB 3.0 Characterization and Debug

Tektronix Toolset for Testing Beyond Compliance

- Silicon validation and System Characterization need tools that go beyond compliance testing
  - Base Specification Measurements for Silicon Validation
    - USB 3.0 specification has informative measurements
      - Measurements at silicon pads
      - AC/DC parametric, common-mode measurements
    - De-embed fixture for accurate results
  - Compliance Measurements and Advanced Analysis Tools
    - Complete link analysis with custom equalization functions
    - Perform USB 3.0 measurements with silicon specific RX equalization models
    - Model channel and cable beyond required compliance reference channels
    - Worst case channel analysis
Characterization and Debug Tools

• What happens if a measurement fails SigTest?
  – Could it be the channel?
    – Measurements can be taken before the channel to evaluate results
    – Different channel models can be applied using TekExpress
      • Channel filters can be created with SDLA with known Sparameters
  – Could it be the RX equalization?
    – Measurements can be taken with custom CTLE models (created with SDLA) that model the RX
  – Does deeper analysis of the waveform need to be done?
    – Measurements can be re-taken in DPOJET with USB3 module
      • Move to failures in the waveform with DPOJET
    – Analysis can be done of the waveform prior to the channel
    – Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance

USB 3.0 Comparison - USB3 / USB-TX / SIGTEST

<table>
<thead>
<tr>
<th>Feature</th>
<th>USB3</th>
<th>USB-TX</th>
<th>SigTest</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated support for SigTest and Tektronix measurements</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Fully Automate waveform acquisition and processing of SigTest</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Integrate custom channel filters</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Support for embedding compliance channel</td>
<td>YES</td>
<td>YES (USB-TX embeds channel for SIGTEST)</td>
<td>NO</td>
</tr>
<tr>
<td>User defined limits</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Support for compliance measurements (except SSC and LFPS)</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Support for SSC and LFPS compliance measurements</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Support for non-compliance measurements</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Debug Analysis (DPOJET)</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Automated DUT state control for CP0 / CP1 Acquisition</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Validation of Data Pattern before Analysis</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Used for Compliance Certification</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>
Complete USB 3.0 Transmitter Solution
DPO/DSA70000 Series Oscilloscopes

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures

- Automation software for characterization and compliance
  - TekExpress with option USB-TX
    (includes option USB3)

- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

BERTScope USB 3.0 Receiver Testing
USB 3.0 Receiver Testing Overview

- Faster data rates can lead to a receiver incorrectly interpreting incoming data
- Long channels result in a closed eye at the receiver, thus RX equalization techniques (CTLE) are required to ensure that the receiver correctly interprets incoming data
- SSC, Asynchronous Ref Clocks can lead to interoperability issues
- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions

USB 3.0 Compliance Receiver Tolerance Test Overview

- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- De-Emphasis Level is set to -3dB
- Amplitude at the end of the compliance channel: 180mV Hosts and 145mV Devices
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SJ</th>
<th>RJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500kHz</td>
<td>400ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>1MHz</td>
<td>200ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>2MHz</td>
<td>100ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>4.9MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>10MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>20MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>33MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>50MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
</tbody>
</table>
BERTScope Solution for USB 3.0

1. Stressed Pattern Generation
   - Random Jitter (RJ)
   - Sinusoidal Jitter (SJ)
   - Spread Spectrum Clocking (SSC)
   - Pre-emphasis
   - Programmable for easy debug/characterization

2. Loopback initiation capability
   - Automation software performs single click loopback initiation

3. Jitter Tolerance Testing
   - Seamlessly handles clock compensation characters (SKPs for USB and PCIe and ALIGNs for SATA and SAS) for accurate BER measurement
   - Compliance test and Search modes to find device’s pass/fail point

4. Automation software
   - Further automation of receiver testing
   - Report generation
   - Easy recall and management of past tests
1. Stressed Pattern Generation, SSC, SJ, and RJ

SSC, SJ, and RJ are adjustable with a turn of the knob, and changes happen instantly for fast debug and characterization.
1. Stressed Pattern Generation Compliant Pre-Emphasis

BERTScope DPP125B provides 3 and 4 tap pre-emphasis, compliant to USB 3.0 and other standards.

2. Loopback Initiation

- Loopback initiation prepares devices for receiver testing.
- Automation software controls the loopback sequence, eliminating guesswork so users focus on testing and debugging.
3. Jitter Tolerance

- Choose to run a compliance test or search for device margins
  - Choice of several algorithms in search mode allows users to customize the algorithm that best suits their DUT
- Asynchronous BER testing allows testing with various SSC frequency and ranges including 5000 ppm required for USB 3.0

4. Automation Software Makes Testing Even Easier

- Results stored to database for easy recall and management
- HTML style test reports
- Cabling diagrams for straightforward setups
- Automated Stressed Eye Calibration
Cable Testing

**DSA8200 Sampling Oscilloscope with IConnect®**

- **Test Fixtures**
  - A Receptacle
  - B Receptacle
  - USB2/USB3 Connectors Available for Crosstalk measurements

- **Using Sampling Oscilloscope & S-Parameter SW**

- **Measurements:**
  - Impedance
  - Intra-Pair Skew
  - Differential Insertion Loss
  - Differential Return Loss
  - Differential Near-End Crosstalk
  - Differential Crosstalk between USB3.0 and USB2.0 Pairs
  - Differential to CM Conversion

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**Tektronix USB 3.0 Summary**

- **Complete**
  - Solutions available today for USB3.0 Transmitter, Cable, Channel, and Receiver Testing
  - Scaleable solutions to meet debugging, characterization, and compliance needs

- **More than a Compliance Solution**
  - Isolate measurement failures with DPOJET
  - Correlate system debug ports with the MSO70K
  - Receiver stresses that go beyond compliance with the BERTScope

- **Increased Productivity**
  - Automated Measurements, DUT Control, and SIGTET integration for Transmitter Testing
  - Analysis tools integrated on the BERTScope enable the isolation and root cause determination of receiver errors

- **Performance**
  - 26Gb/s BERTScope provides coverage for next generation testing needs
  - Low noise floor enables measurements of small data eyes for compliance testing and receiver calibration
  - Only 6.25Gb/s hardware serial trigger to capture protocol events that are causing failures or interoperability problems

- **Engaged**
  - Actively engaged in the USB Working Groups
Simplifying Validation and Debug of USB 3.0 Designs
- Total Phase, Inc. USB Protocol Testing Solutions

Total Phase

- Incorporated in 2001 in Sunnyvale, CA
- First USB Analyzer introduced in 2005
- Fastest growing analyzer company today
- Our Mission:
  “Be the #1 test solution supplier in our segments”
- How do we do that?
  - State of the art architecture
  - Customer-driven feature set
  - Willing to look at things differently…
Product Line

Aardvark I2C/SPI Host Adapter
Cheetah SPI Host Adapter
Beagle I2C/SPI Protocol Analyzer
Beagle USB 12 Protocol Analyzer
Beagle USB 480 Protocol Analyzer
Beagle USB 5000 Protocol Analyzer

What is a Protocol Analyzer?

- Captures and analyzes traffic between host and device
- Inspects traffic and identifies errors
- Provides view of device enumeration
- Allows users to pinpoint events of interest
- Captures low-level bus states
What is new in USB 3.0?

- **Link Layer**
  - Equalization
  - Link Training
  - Scrambling/Polarity Inversion
  - Low power states

- **Increased Protocol Complexity**
  - Independent Bidirectional Traffic (Rx, Tx)

Link Layer Debug Challenges - Increased Traffic

- Need to see it as it happens on the wire (LiveDisplay™)
- Need to see only what you want (Live Filter™)
- Need to find problem quicker (Live Search™)
- Automatic decode of link settings (Scramble, Polarity Inversion)
Link Layer Debug Challenges - LiveDisplay™

Link Layer Debug Challenges - LiveFilter™
Link Layer Debug Challenges -
LiveSearch™

Scramble, Polarity Inversion
Link Layer Debug Challenges - Complex State Machine

- Comprehensive View of LTSSM
- Track the transitions between states
- Understand state transition violations
Link Layer Debug Challenges - Low Power States

- Faster bit lock and symbol lock (Real Discrete PHY)
- Frequent Transition in and out of Low Power States

<table>
<thead>
<tr>
<th>Time</th>
<th>Event Description</th>
<th>State Transition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.05</td>
<td>Link Layer / Phy Error</td>
<td>US → US</td>
</tr>
<tr>
<td>0.05</td>
<td>Link Layer / Phy Error</td>
<td>US → US</td>
</tr>
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</tr>
</tbody>
</table>

Increased Protocol Complexity

- Find problems faster with flexible state based Advanced Triggering
  - 8 independent states with 6 data matches per state
Increased Protocol Complexity
User Customizable Views

Adjustable
Columns

Block
Increased Protocol Complexity
User Customizable Views

Adjustable Columns

Block

Details

Increased Protocol Complexity
User Customizable Views

Class Transaction Packet

Data Payload Packet

Link Good 0

Link Credit A

Link Credit B

Link Credit C

Data Packet Header

Data Transaction

[Table with data]

IN Tlm: 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F

[Table with data]

ACK Transaction: [SeqNum=11] [Num=1] [PP] [HdrSeq=1]

[Table with data]

ACK Transaction Packet: [SeqNum=11] [Num=1] [PP] [HdrSeq=1]

[Table with data]
Complex Topography

- Simultaneous capture of USB 2.0 and 3.0 Traffic
- Instant Class Level
**Complex Topography**

- Simultaneous capture of USB 2.0 and 3.0 Traffic
- Instant Class Level

**Total Phase USB 3.0 Summary**

Beagle USB 5000 SuperSpeed Protocol Analyzer addresses the challenges of USB 3.0:

- **Link Layer Debug:**
  - Increased Traffic
  - Complex LTSSM State Machine:
  - Low Power States:

- **Increased Protocol Complexity:**
  - Finds problems faster with advanced triggering
  - Provides user-customizable views

- **Complex Topography:**
  - Captures USB 3.0 and USB 2.0 data simultaneously
  - Instantly decodes class-level data
Resources

- Access to Specifications
  - Rev 1.0, http://www.usb.org/developers/docs/

- Tektronix USB Electrical PHY Tools and MOI's
  - www.tektronix.com/usb
  - www.tektronix.com/software