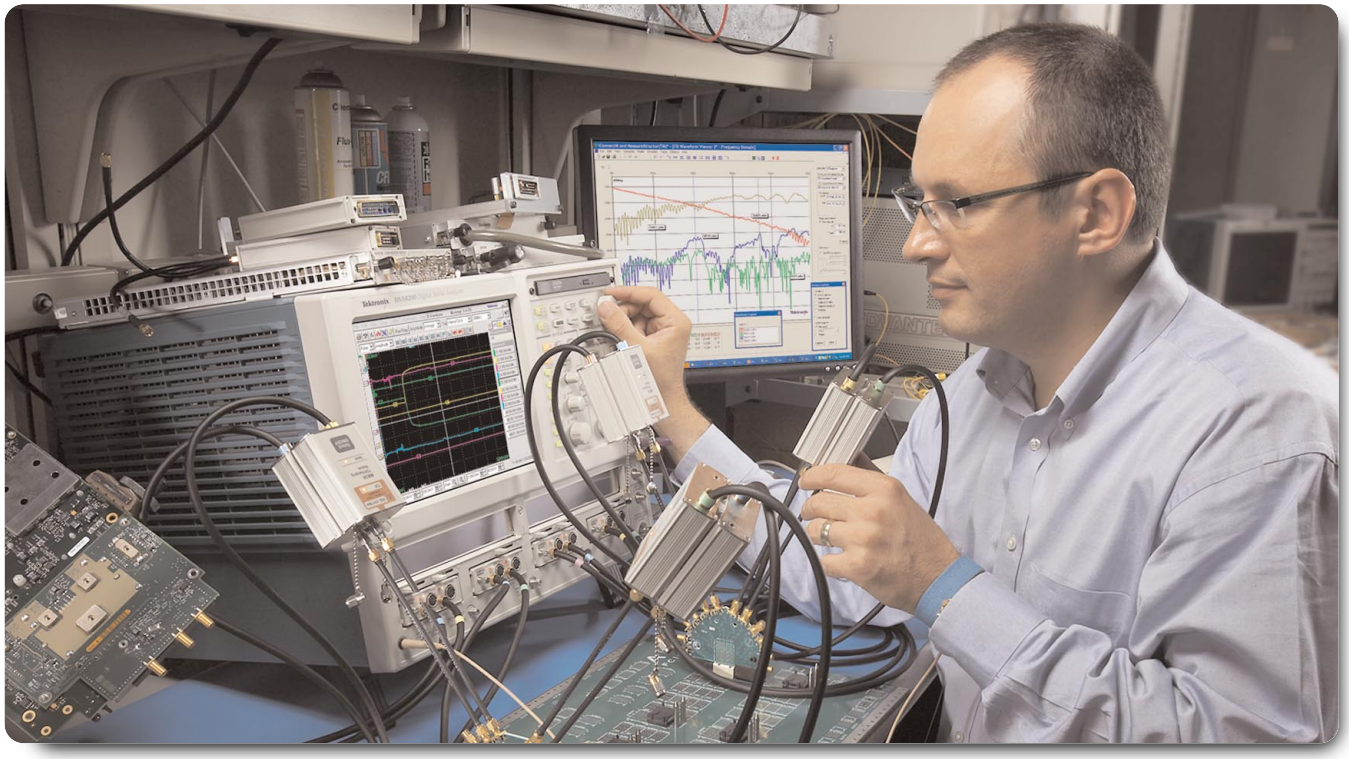
TDR and S-parameters Measurements – How Much Performance Do You Need?



Serial Data Network Analysis (SDNA) Application

The transition in computer, communications, and consumer electronics industries from parallel to high-speed serial data is creating new design challenges. As more data bits must pass through the same interconnect link, the data rates are pushed higher into multi gigabit regime, creating substantially tighter timing budgets. Higher data rates also create more inter-symbol interference (ISI) due to high-frequency losses in the interconnects. Additionally, to allow designers to achieve even higher data transfer rates, several of these serial links are commonly used at the same time, creating what is referred to as multilane configuration, where crosstalk again plays an important role.

As a result, characterization of interconnect reflections, losses and cross-talk must be managed more closely. This characterization must be done differentially, and is done more and more often in frequency rather than in time domain, using so-called S-parameters (see Appendix A – *S-parameter Backgrounder*). S-parameters give you quantitative insight into causes of bit errors and bit error rate (BER) degradation, jitter, ground bounce, and EMI. Crosstalk can also be done as an S-parameter measurement, looking at signal transfer from one line pair to the adjacent one. Many electrical standards – such as SATA, PCI Express, FibreChannel and Gigabit Ethernet to name just a few – now require S-parameters in their compliance test procedures. The differential serial data compliance testing and differential characterization of serial data components can be jointly described as Serial Data Network Analysis (SDNA).

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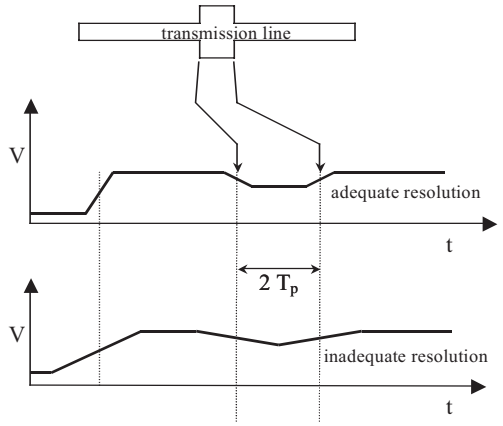
Traditional tools for S-parameter measurements commonly referred to as Vector Network Analyzers (VNA). These tools tend to be very powerful – but that power may very well be their own undoing, as their accuracy is achieved through extensive calibration procedures. For SDNA applications, these differential calibration procedures are excruciatingly lengthy and difficult to follow, resulting in lengthy test times and being prone to human error. Electronic calibration modules for VNAs are available, but operate only at relatively low frequencies for most SDNA applications. Additionally, the cost of the VNA instruments tend to be high compared to an average instrument that a digital designer would have on their workbench.

TDR-based S-parameter measurement tools (see Appendix B – *TDR-based S-parameter Measurements*) are proven to be cost effective, easy to use, easy to calibrate, highly accurate, and provide higher throughput. For example, one can obtain a differential insertion loss measurement with TDR and post-processing software within a minute instead of the 15 minutes or so typically required by a VNA. VNAs also can not measure directly to DC, they can take a long time to accurately measure low frequencies for long DUTs such as cables, and they compute the differential response of the system from single ended measurement rather than measure it directly. A TDR-based system can measure DC and low frequencies directly, and Tektronix' DSA8200 and IConnect® S-parameter measurement system can obtain true differential TDR and S-parameters directly by firing more than one source simultaneously – a unique capability of this kind in the industry. IConnect also allows acquisition of extremely long records (up to 1,000,000 points), which is required for making S-parameter measurements for very long devices such as cables. Finally, the typical cost of a TDR-based system can easily be $^1/_2$ the cost of a comparable VNA system – and the VNA system will provide lower time domain resolution than the TDR with comparable bandwidth. There are several misconceptions about TDR-based S-parameters, which are clarified in Appendix C – *Misconceptions about TDR-based S-parameters*. Overall, a TDR-based S-parameter measurement system provides a high throughput and easy-to-use approach to performing S-parameter compliance tests required by many digital standards, as well as for characterization of digital devices operating at gigabit speeds.

TDR Spatial Resolution Requirements



▶ **Figure 1.** *TDR resolution limit per IPC TM-650.*

TDR system risetime	Resolution
10 ps	5 ps / 1 mm (0.04 in)
20 ps	10 ps / 2 mm (0.08 in)
30 ps	15 ps / 3 mm (0.12 in)
100 ps	50 ps / 10 mm (0.39 in)
200 ps	100 ps / 20 mm (0.79 in)
500 ps	250 ps / 50 mm (1.97 in)

▶ **Table 1.** *Resolution of TDR systems per IPC TM-650 (microstrip, $v_p \approx 2x10^8$ m/s).*

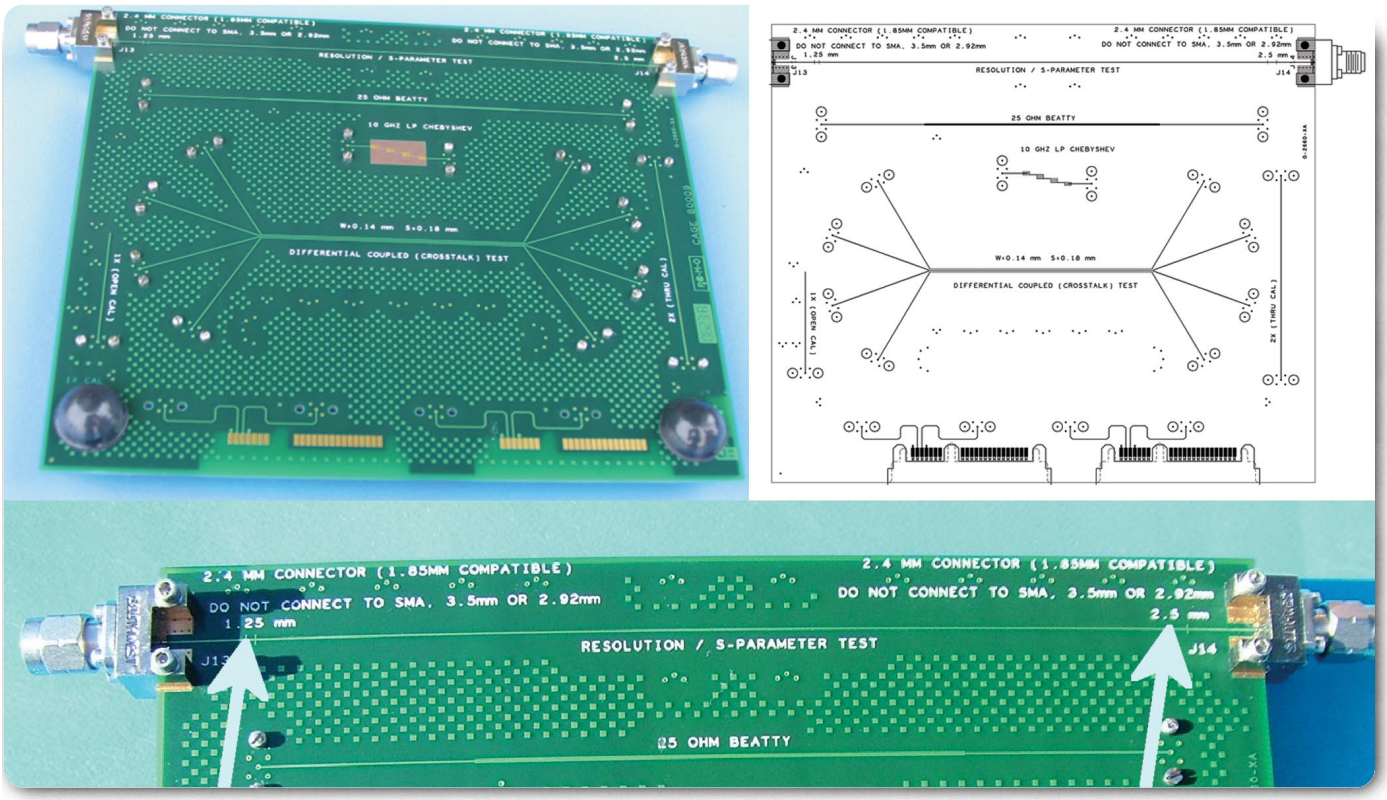
Rise time, ps	Resolution in air, mm	Resolution in FR4, buried run ($v_p=0.446*C_{light}$), mm	Tektronix Products
10	1.50	0.67	
15	2.25	1.00	80E10
20	3.00	1.34	80E08
28	4.20	1.87	80E04
40	6.00	2.68	80E04
150	22.50	10.04	80E04

▶ **Table 2.**

Let's start with the most basic requirement for TDR, which is to provide sufficient resolution for locating faults in a package or a circuit board. The Institute for Printed Circuits (IPC) TM-650 2.5.5.7 document defines TDR resolution as "the resolution limit … wherein two discontinuities or changes on the transmission line … begin to merge together … Per this definition, the resolution limit is: half the … 10% to 90% risetime or 90% to 10% fall time (depending on whether the TDR response is calibrated with a short or open circuit)."

For typical surface microstrips in the air, and on FR4 circuit boards ($V_p \approx 2x10^8$ m/s), the resolution and TDR rise time requirements are summarized in IPC TM-650 using the preceeding table.

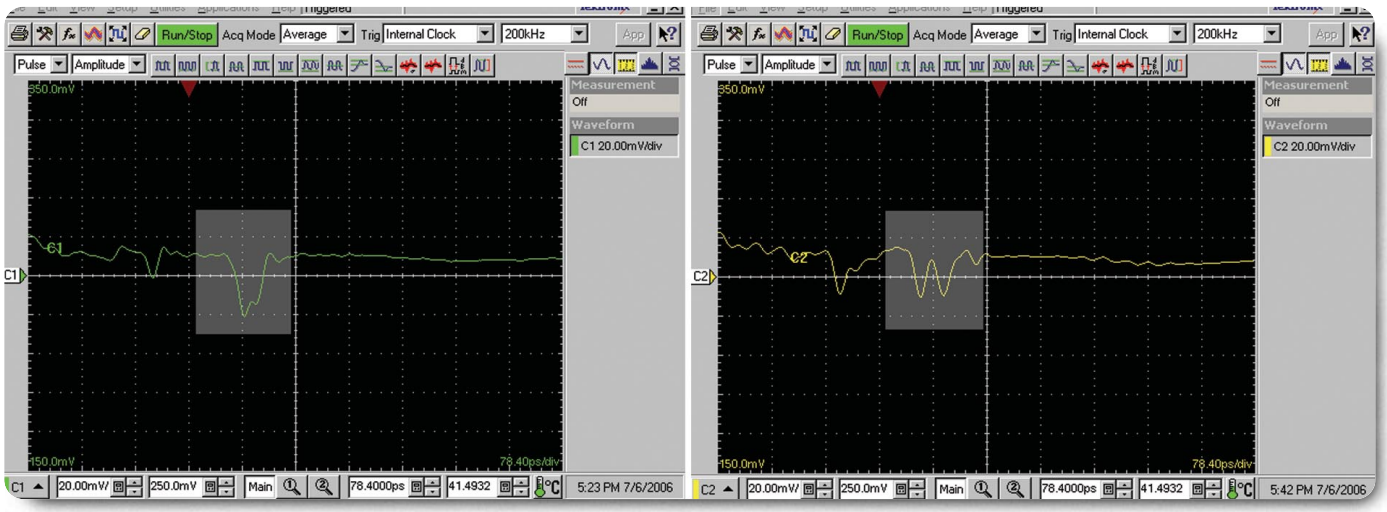
An inner board layer (a stripline) is much more representative of the typical board run. Additionally, it is useful to provide the resolution data for propagation in free air. For stripline, we assume $V_p = 0.446xc_{light}=1.34x10^8$, and the resulting resolution data, based on the rule of $t_{TDR}/2$, is summarized in Table 2 above.



▶ **Figure 2.** *Resolution structure on Tektronix TDR demo board – see two vertical bars separated by 1.25 mm on the left and 2.5 mm on the right, both marked with arrows.*

Let's look at a practical situation. On the Tektronix TDR demonstration board, there are resolution structures that are reasonably close to the 2.4 mm (S) connector on the board (Figure 2).

Figure 3 presents the results of TDR testing using the Tektronix 80E10 15 ps reflected rise time TDR module, with the signal launched from the left to access 1.25 mm structure, and the signal launched from the right to access 2.5 mm structure.



▶ **Figure 3.** *Resolution of 15 ps (reflected) 80E10 module on a structure with 1.25 mm spacing between discontinuities (left) and on a structure with 2.5 mm spacing (right).*

Clearly, on the structure with 2.5 mm separation, the two discontinuities are resolved perfectly, whereas on the structure with 1.25 mm separation, you start to lose resolution (the trace on the demo board is a microstrip, and according to Table 1 there is a different limit on the resolution for microstrips). The interesting question is, however, what happens for spacing under 1.25 mm between discontinuities. The discontinuities do not disappear; they simply become one single discontinuity. Clearly then, when a failure analyst attempts to locate a single discontinuity, even a sub-mm discontinuity will be observed by 80E10. This is an important conclusion; sub-mm resolution can be achieved with 15 ps reflected rise time in 80E10 module.

Rise Time Requirements for Serial Standards

Standards	Datarates, Gb/s*	$t_{standard\ rise}$ as a ratio of bit width
1st generation standards	1.125 - 3.125	15%
2nd generation standards	4.25 - 6.5	20%
3rd generation standards	8 - 12	25%

▶ **Table 3.** *Rise time as percentage of the bit width for three generation of standards.*

When using a TDR-based S-parameter measurement system for characterization or for a compliance test defined by a specific standard, it is important to know what rise time is required to accurately perform measurement or test. When specifying the rise time, standards focus primarily on the maximum (slowest) rise time, looking at the minimum rise time as an informative parameter. SATA test procedures, for example, state the required minimum rise time but then a footnote clarifies that “Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for interoperability testing.” So, for most standards the question for a designer remains – what is the TDR rise time do you need for a given specification, given data rate, and given S-parameter bandwidth specified by a standard?

Standards		Standards Characteristics				TDR Rise Time Needs	
		Data Rate (Gb/s)	Bit width (ps)	Rise time spec'ed ps*	Rise time est., ps*	Reflected t_{TDR} needs, ps**	Tektronix module
1st generation standards, t_{rise}* = 15% of bit width	Infiniband	2.50	400	100	60	40(30)	80E04
	PCI Express	2.50	400	50	60	40(30)	80E04
	SATA II	3.00	333	67	50	34(25)	80E04
	XAUI	3.125	320	60	48	32(24)	80E04
2nd generation standards, t_{rise}* = 20% of bit width	4 Gb/s FC	4.25	235	60	47	32(24)	80E04
	SATA II	6.00	167	N/A	33	22(17)	80E08
	Double XAUI	6.25	160	N/A	32	21(16)	80E08
3rd generation standards, t_{rise}* = 25% of bit width	8 Gb/s FC	8.50	118	N/A	29	32(24)	80E08
	10 G Base-R	10.31	97	24	24	20(15)	80E10
	10 G Base-R FEC	11.10	90	24	23	15(11)	80E10

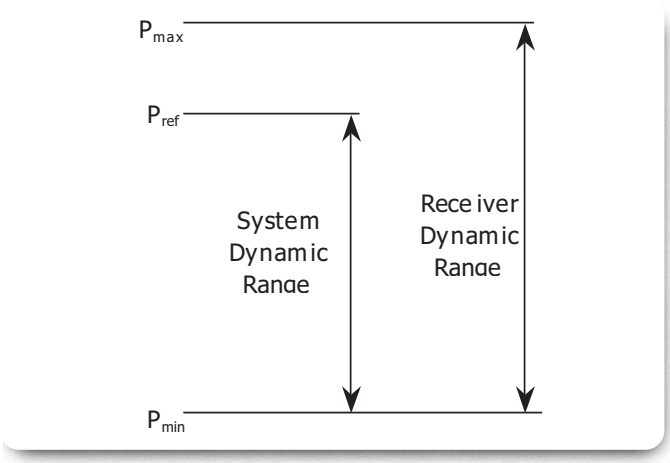
* 20-80% rise times, when available from a standard
** 10-90% TDR rise time specifications (20-80% equivalent provided in parenthesis)

► **Table 4.** *Reflected TDR rise time requirement for standards.*

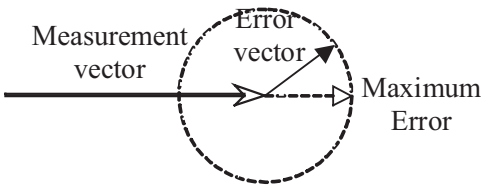
During a recent study of standards at Tektronix, a clear trend has been observed, where rise times for 1st generation standards (e.g., Infiniband SDR, PCI Express etc.) constituted a substantially smaller portion of the bit width (or unit interval) than the 2nd (e.g, Infiniband DDR, PCI Express 2.0, 4 Gb/s FibreChannel) and 3rd (8 Gb/s FibreChannel, 10 Gb/s Ethernet) generation standards. The approximate dividing line between the generations of standards can be drawn at 3.125 for 1st to 2nd generation transition and 6.5 Gb/s for 2nd to 3rd generation transition. We found that the rise time constituted approximately 15% of the bit width for the 1st generation standards, 20% for 2nd generation, and 25% for 3rd generation (all rise times are measured as 20-80%). This information is summarized in the table above.

If a designer used TDR rise time that is 50% faster than the rise time used by the devices in various standards, complete characterization of the channel with more than adequate guardband could be achieved (note that TDR rise time is defined in terms of 10-90%, which provides additional guardband over the 20-80% rise time specified by the standards). This assumption ensures that the rise time provided is sufficiently fast for characterization. If the rise time needs to be slowed down, this can be achieved with either mathematical filtering in the oscilloscope, or using sufficiently lossy cables or filters. Using this 50% guardband assumption, the following summary table specifies how much TDR rise time is required by various standards, and what Tektronix modules can address that.

Frequency Domain Dynamic Range and Bandwidth Requirements for Serial Standards



▶ **Figure 4.** *Dynamic range definitions.*

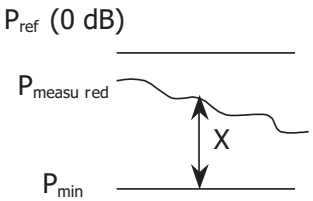


▶ **Figure 5.** *Interaction between the measurement vector and error vector in frequency domain.*

Dynamic Range Requirements for Serial Data

Now let's define dynamic range. Typically, receiver dynamic range is defined in terms of difference between maximum and minimum power that can be measured – P_{max} and P_{min} (Figure 4). System dynamic range is defined in terms of the difference between the nominal power of the source (P_{ref}) and the minimum power that can be measured (P_{min}).

In TDR-based S-parameter measurements, P_{max} is related to maximum operating spec of a sampling module, and is less relevant when one focuses on the passive component (interconnect) measurements. As a consequence, system dynamic range is what matters for serial data interconnect characterization.



How does this relate to the serial data dynamic range requirements? In essence, per the discussion above, dynamic range is the difference between 0 dB and the noise floor. The actual accuracy of the measurement at a given frequency depends on what is the difference between an actual measurement level ($P_{measured}$) vs. the noise floor (P_{min}). If our actual device under test is measured with the noise floor at X dB below reference measurement level, it can be demonstrated that the accuracy in %, can be related to the X dB below reference value as follows

$$Accuracy(\%) = 10^{\left(\frac{-X(dB)}{20}\right)}$$

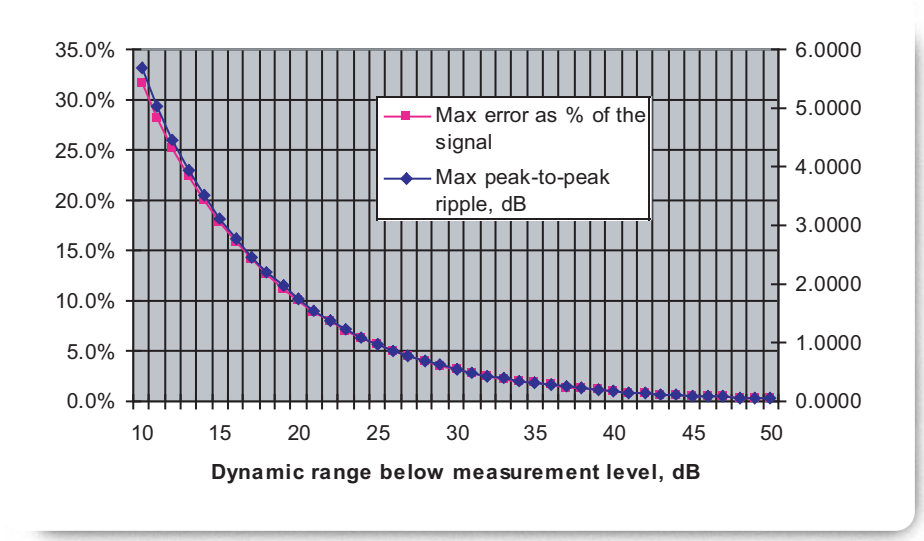
Note that since the signal and noise in frequency domain add vectorially (equation above shows worst case accuracy) when the noise vector is completely in phase (or 180 degree out of phase) with the signal vector.

Additionally, it can be demonstrated that total peak-to-peak ripple (error circle diameter in Figure 5) on that signal will be Y dB using the following equation:

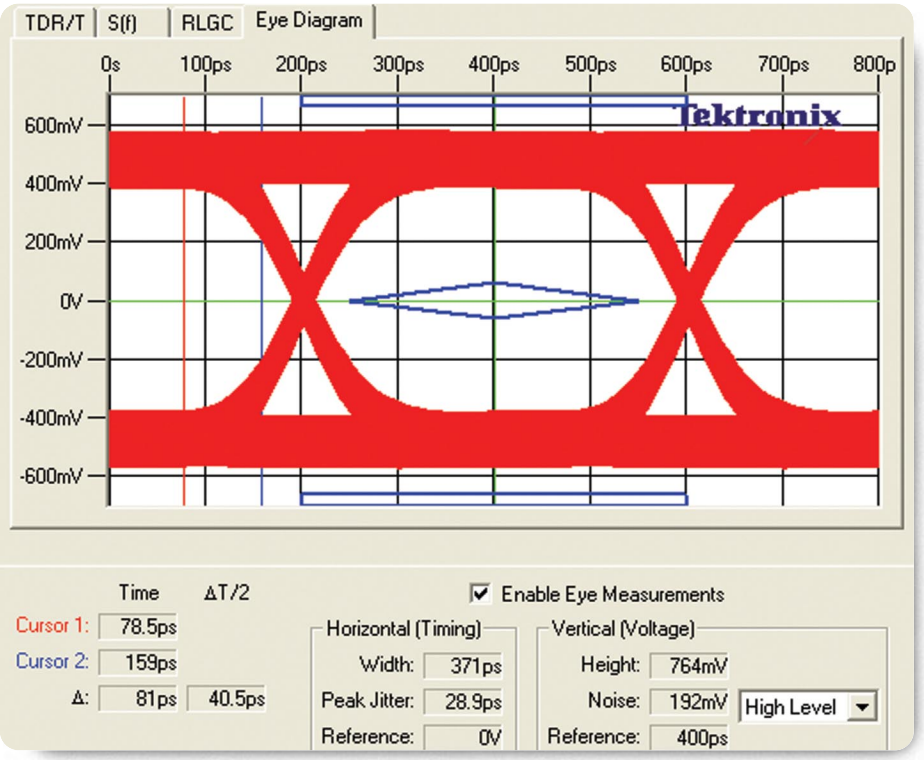
$$Y(dB) = 20\left[\log\left(100\% + Accuracy(\%)\right) - \log\left(100\% - Accuracy(\%)\right)\right]$$

This equation includes both the positive and the negative ripple observed on the waveform.

You can now produce the following charts, which demonstrate what accuracy can be achieved depending on how far the dynamic range is below the measurement level. Detailed tables are given in Appendix E – *Accuracy vs. Dynamic Range Below Measurement Level*.



▶ **Figure 6.** *S-parameter measurement system error vs. the difference between the measured signal level and the dynamic range of the system at that frequency.*



▶ **Figure 7.** *80% open eye at 2.5 Gb/s. Eye closure is caused by crosstalk that is 10% of the signal amplitude.*

For a typical characterization work in any of the serial data standards, you would want to measure a voltage no smaller than approximately 10% of the full signal amplitude. This voltage glitch can be caused by reflections, or by crosstalk from an adjacent differential line pair. This type of voltage glitch still will provide an 80% eye opening, approximately, as illustrated by Figure 7.

Minimum measured voltage size and accuracy, as % of signal amplitude (% accuracy)			
% values	At 0.5 V signal	At 1 V signal	At 2 V signal
10%±1% (10%)	50 m V±5 m V	100 m V±10 m V	200 m V±20 m V

▶ **Table 5.** *Minimum measured voltage size and accuracy requirements for various voltage levels.*

Characterization of Standards		Data Rate (Gb/s)	Required bandwidth, GHz
1st generation standards	Infiniband, PCI Express	2.50	6.25
	SATA II	3.00	7.50
	XAUI	3.125	7.813
2nd generation standards	4 Gb/s FC	4.25	10.63
	SATA II	6.00	15.00
	Double XAUI	6.25	15.63
3rd generation standards	8 Gb/s FC	8.50	21.25
	10 G Base-R	10.31	25.78
	10 G Base-R FEC	11.10	27.75

▶ **Table 6.** *Summary of bandwidth requirements for characterization of serial data standards.*

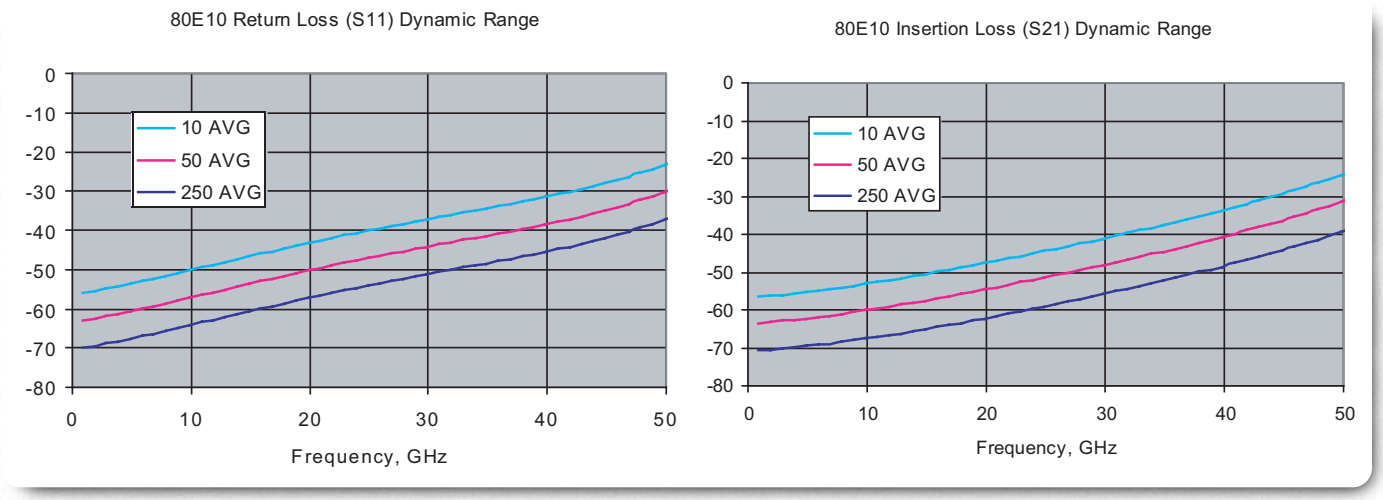
It is adequate to measure this voltage glitch with 10% accuracy (which translates into accuracy that is 1% of the full signal amplitude). This set of typical measurement requirements is summarized in Table 4, and examples are given for translating the percentage into voltage at 500 m V, 1 V, and 2 V peak to peak amplitude signals.

Using the accuracy chart (Figure 6) and the table in Appendix E, it can be determined that a signal that is 10% of total amplitude is -20 dB, and to measure it with 10% accuracy, the noise floor needs to be another -20 dB below the measurement level, making the *total dynamic range requirement -40 dB.*

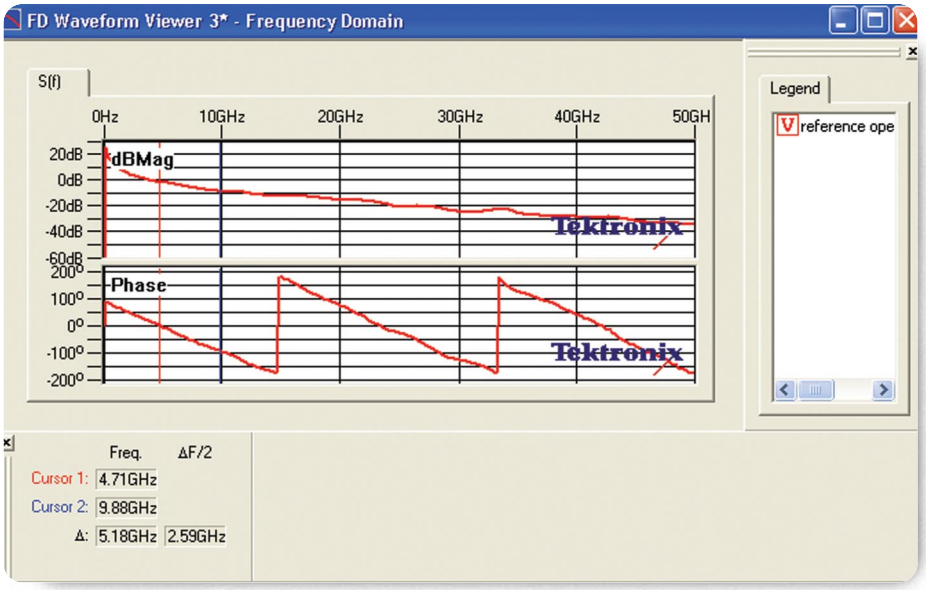
Frequency Requirements for Serial Data

Tracking the 1st-2nd-3rd generation division for serial standards discussed above, it was discovered that the later generation of standards place less stringent requirements on characterization of digital components. For the 1st and 2nd generation standards, designers talked about characterization to the 5th harmonic of the clock (even though much lower compliance testing requirements were stated in the standards), and for 3rd generation standards designers talked about the 3rd harmonic.

Overall, performing characterization to the 5th harmonic ensures adequate characterization bandwidth, and provides sufficient confidence to the designer. Using the 5th harmonic as a guideline, Table 5 provides the frequency requirements.



▶ **Figure 8.** *Estimate of a dynamic range for Tektronix 80 E10 module.*



▶ **Figure 9.** *Tektronix 80E10 incident power at 500 ps/division, 256 averages.*

Tektronix TDR Modules Meet the Challenge

Figure 8 is the typical dynamic range for the 80E10 module. Notably, dynamic range degrades with frequency. This is due primarily to step-like nature of the TDR incident waveforms, which causes the incident power to roll off as 1/f.

Where does it place us in relationship to the dynamic range and bandwidth requirements? Table 7 provides the answer.

Characterization of Standards		Data Rate (Gb/s)	Required Bandwidath, GHz	Typical Dynamic Range at Req. BW, dB	Tektronix module
1st generation standards	Infiniband, PCI Express	2.50	6.25	-64	80E04
	SATA II	3.00	7.50	-62	80E04
	XAUI	3.125	7.813	-61	80E04
2nd generation standards	4 Gb/s FC	4.25	10.63	-60	80E04
	SATA II	6.00	15.00	-63	80E08
	Double XAUI	6.25	15.63	-63	80E08
3rd generation standards	8 Gb/s FC	8.50	21.25	-58	80E08
	10 G Base-R	10.31	25.78	-54	80E10
	10 G Base-R FEC	11.10	27.75	-53	80E10

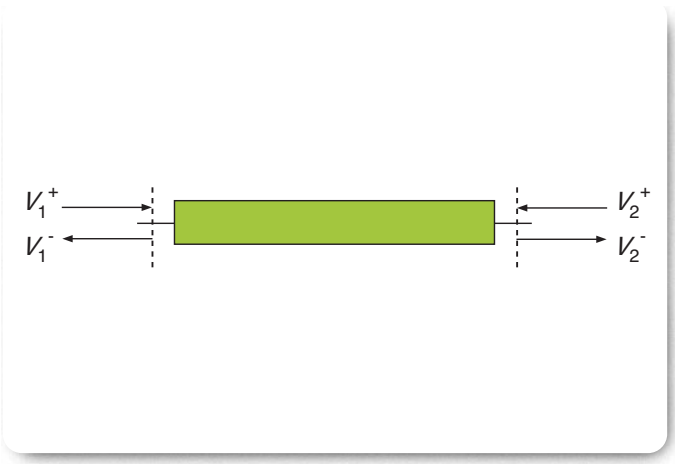
▶ **Table 7.** *Tektronix position in relationship to bandwidth and dynamic range requirements for serial data.*

Summary

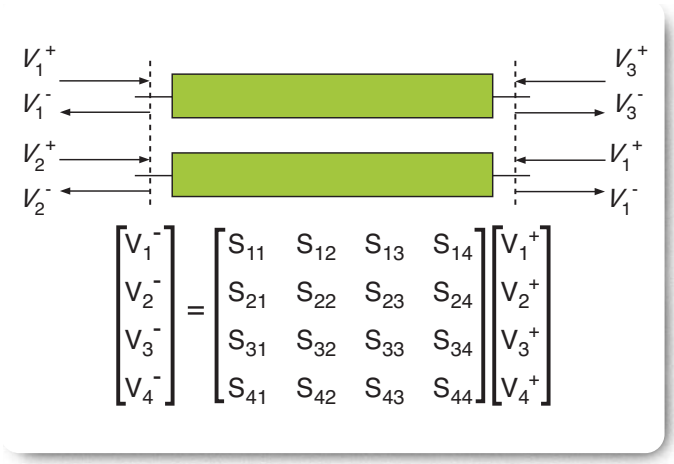
In this paper we identified, based on expert user knowledge, accuracy requirements for SDNA debug, compliance, validation, and characterization applications. We defined the following requirements for SDNA applications:

- TDR rise time to resolve smallest relevant discontinuity
- TDR rise time for standard characterization
- Dynamic range and bandwidth requirements for standards characterization

Appendix A – S-parameter Backgrounder



▶ **Figure 10.** *S_{ij} parameter is the ratio of the reflected (or transmitted) wave at port j to the incident wave at port i.*



▶ **Figure 11.** *For a four port, more voltage and current values are involved in computing the S-parameter matrix, and the matrix itself is 4x4 in dimension.*

S-parameters are defined in terms of incident and reflected waves at each port. Each S_{ij} parameter is the ratio of the reflected (or transmitted) wave at port j to the incident wave at port i.

The generalized term for reflection or transmission is "scattering." If we make an assumption that the power transmitted is given by $^1/_2 |V_i^+|^2$, then the voltages at each port can be defined as $V=V^+ + V^-$ and currents as $I=I^+ + I^-$. For a reciprocal junction (such as an interconnect) the scattering matrix is symmetrical, i.e. $S_{21}=S_{12}$.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

For a four port, the picture is more complicated, even though a 4-port is direct extension of a 2-port definition.

What really is of interest, however, are the differential and common mode measurements. Differential measurements are performed between the lines, whereas common mode measurements are performed from the lines, tied together, to ground. In practical terms, the type of stimulus and response define the type of S-parameters you are looking at. Differential stimulus and differential response define the differential S-parameter quadrant, common mode stimulus and response define the common mode quadrant; differential stimulus and common mode response define the differential-to-common mode conversion mixed-mode quadrant, and common mode stimulus and differential response define common-to-differential mode conversion mixed-mode quadrant.

		Differential	Common
Response	Differential	S_{dd}	S_{dc}
	Common	S_{cd}	S_{cc}

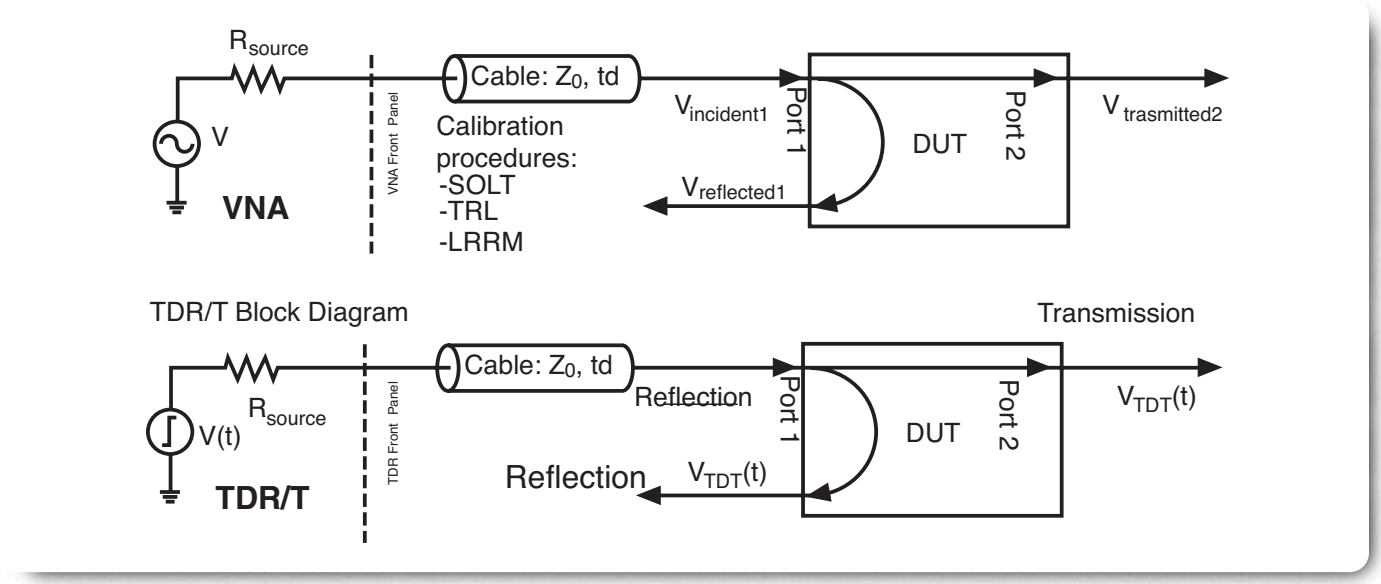
▶ **Figure 12.** *Differential stimulus and differential response define the differential S-parameter quadrant, common mode stimulus and response define the common mode quadrant, differential stimulus and common mode response define the differential-to-common mode conversion mixed-mode quadrant, and common mode stimulus and differential response define common-to-differential mode conversion mixed-mode quadrant.*

The resulting S-parameters matrix looks as follows:

$$\begin{bmatrix} V_{d1}^{-} \\ V_{d2}^{-} \\ V_{c1}^{-} \\ V_{c2}^{-} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{c11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} V_{d1}^{+} \\ V_{d2}^{+} \\ V_{c1}^{+} \\ V_{c2}^{+} \end{bmatrix}$$

S-parameters are relevant in different degrees to digital design. Differential S-parameter quadrant relates to direct degradation of bandwidth and BER/jitter. Common mode explains skew and ground bounce problems. Mixed mode illustrates EM interference (EMI, differential-to-common mode) and EM susceptibility (EMS, common-to-differential); however, a time domain view of the same data produces much more intuitive results when looking for sources of EMI and EMS. Crosstalk, on the other hand is a form of insertion loss (S_{21}), except that it is insertion loss between lines which do not have direct connection from input to output.

Appendix B – TDR-based S-parameter Measurements

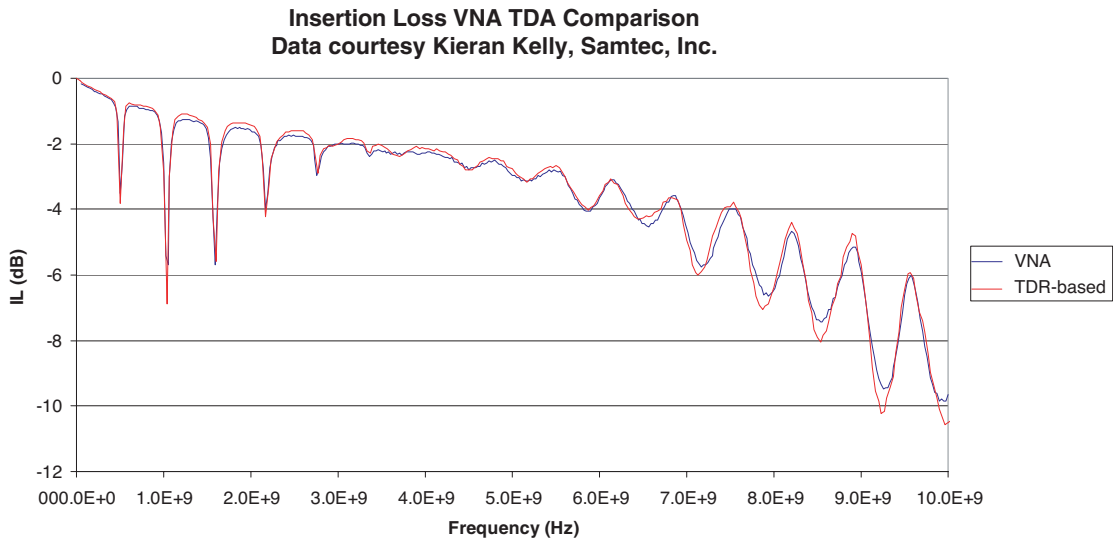


▶ **Figure 13.** *Conceptual block diagram of TDR-based TDNA system vs. a VNA. The main conceptual difference is in the use of a wide-band step-like source for TDNA vs. a narrow band sine-wave generator for VNA.*

TDR-based S-parameter measurement techniques has been studied extensively by US National Institute of Standards and various research institutions in the USA and abroad (for example [1] and [2], and has been commercialized by a number of products. Conceptually, the similarity between VNA-based and TDR-based S-parameters is obvious (Figure 13).

The main conceptual difference is in the use of a wide-band step-like source for TDR vs. a narrow band sine-wave generator for VNA. Additionally, TDR is a transient measurement (all transitions are observable) whereas VNA is a steady-state measurement - all transitions are lumped together, and the measurement is performed at a single frequency, with narrowband filtering employed to minimize the effects of noise.

VNAs were designed with microwave design in mind, and targeted such applications as microwave filter and mixer design. The need for extremely high dynamic range resulted in some very advanced calibration procedures (such as Short-Open-Load-Thru (SOLT) or Thru-Reflect-Line (TRL)) having been developed, and the overall design of the instrument targeted not towards ease of use, but towards this very high dynamic range. The frequency domain has become the domain of choice for microwave design, and thus the FDNA is more easily understood by microwave designers. However, these same calibration procedures that make FDNA so accurate also make it an instrument much more difficult to use, and make it much more time-consuming to perform the required tests – very undesirable qualities particularly when manufacturing testing is involved.



▶ **Figure 14.** *S-parameter measurement system error vs. the difference between the measured signal level and the dynamic range of the system at that frequency.*

TDR-based S-parameters were developed as an extension of TDR technology. TDR is more intuitive to the digital designers than to the microwave designers, and as the result the conversion of TDR into S-parameter data is an intuitive and straightforward process for them. Even though it is possible to apply advanced calibration such as SOLT and TRL to TDR to improve its accuracy, these procedures would make TDR-measurements much less easy and intuitive. Even without these calibration procedures, the dynamic range of TDR-based S-parameters is well into -50 to -60 dB range [3], which is more than adequate for a typical measurement in digital design or signal integrity, as analysis in the section Dynamic Range Requirements for Serial Data above illustrates. The dynamic range of TDR-based S-parameters is improved by increasing the number of points and number of averages in the time domain acquisition window; more averaging and a larger number of points play the same role as narrow band filtering of the signal in VNA. Overall, the correlation between VNA and TDR-based S-parameters has been studied extensively (see, for example Figure 14 or [4]) and accepted as more than adequate by many standard groups. Combined with substantially lower cost of the typical TDR S-parameter measurement system, the TDR solution provides an excellent easy to use solution for SDNA application.

Another important point is that the compliance test point for many standards is defined in such a way that the fully mated connector must be part of the compliance test. The compliance test point is defined so as the fully mated connector must be included in the passive physical layer measurement. The receptacle must be de-embedded, excluding the connector mated on the board. Even though it is not an impossible task to perform with a VNA, it adds yet another layer of complexity to VNA measurements. At the same time, with TDNA, the ease of calibration (only a short, open or thru reference is required) allows to de-embed the receptacle very easily, providing additional advantage to the TDNA approach. Overall, as demonstrated in [5], the fixture de-embedding strips away the accuracy advantage of VNA altogether, while the ease of use and high-throughput advantages of TDNA remain intact, making TDNA a much more attractive approach for most standards compliance testing.

Appendix C – Misconceptions about TDR-based S-parameters

Misconception 1. TDR-based S-parameter bandwidth is limited by the sampling rate of the TDR.

This misconception is the easiest to refute. The bandwidth of the TDR-based S-parameters is totally unrelated to the sampling rate, but is completely dependent on the TDR rise time. With Tektronix DSA8200 mainframe, 80E10 TDR module, and IConnect software, 50 GHz bandwidth can be achieved due to extremely fast (12 ps incident) TDR rise time. Figure 9 illustrates this point nicely.

Misconception 2. TDR-based S-parameters do not provide insertion loss.

This one is pretty easy too – TDT will give insertion loss, and differential TDT will give differential insertion loss.

Misconception 3. The noise floor of TDR is inherently higher because of lack of IF filtering.

Digital averaging in time domain achieves the same effect as IF filtering in frequency domain. There is nothing that "inherently: limits the TDR noise floor. Adding advanced (SOLT or TRL) calibration to TDR would bring its noise floor in line with that of a VNA - however, while loosing the TDR's ease of use at the same time. Because of SDNA measurement accuracy requirements, we believe that truncated calibration procedures (such as those supported in Tektronix IConnect TDR and VNA software) are preferred for SDNA applications. These procedures include a reference (open or short or thru) and, optionally, a 50 Ohm load calibration measurements.

Misconception 4. The TDR power roll-off at higher frequencies results in substantially lower dynamic range at those frequencies – effect that does not exist in VNAs.

This partially true - the power in a TDR system does roll off with frequency. However, it is not true that the VNA power is completely flat - in fact, it substantially varies with frequency as well. It is the calibration procedures, which are both powerful and at the same time lengthy and not user friendly that make the calibrated power in a VNA to be flat. The same can be achieved in TDRs with similar calibration procedures – then again, we would not trade off TDR ease of use for additional dynamic range for SDNA applications.

Misconception 5. TDR-based S-parameter dynamic range is limited to 40 dB.

We found that we can easily achieve 70 dB when using DSA8200, 80E10, and IConnect with 256 averages on the mainframe - Figure 8. Additional averaging helps improve this performance even further.

Misconception 6. TDR calibration is a complex, multi step process.

We are not sure where this misconception is coming from. Certainly, it is desirable to perform vertical (DC) compensation on TDR modules. However, these compensation procedures are extremely simple compared the complicated VNA calibration procedures. Overall, TDR calibration and compensation is substantially simpler than that of a VNA.

Misconception 7. Limited bandwidth can be achieved when testing longer devices with TDR because of long record time window requirements and limited record lengths (number of points) in a typical TDR oscilloscope.

This used to be true. However, when using Tektronix DSA8200 TDR oscilloscope with Tektronix IConnect® software, the user can acquire records of up to 1,000,000 points, making this a moot point. S-parameters for cable assemblies as long as 100 of meters can now be measured. Now, the Tektronix TDR-based system is actually more accurate than a VNA, since it can measure the long cables to DC, rather than to a 300 KHz or 40 MHz like most VNAs.

Appendix D – Precision Microwave Connector Care and Connector Compatibility

Module	Connector type	Max connector bandwidth	Mates with
80E10	1.85 mm (V)[1]	67 GHz	2.4 mm
	2.4 mm (S)	50 GHz	1.8 mm
80E08	2.92 mm (K)	40 GHz	3.5 mm, SMA[2]
80E04	3.5 mm	26.5 GHz (some rated to 34 GHz)	2.92 mm, SMA
	SMA	18 GHz (some rated to 26.5 GHz)	3.5 mm, 2.92 mm

Tektronix TDR module come with precision microwave connectors. The following table summarize the connector type of the front of the module, and the other connectors that you can mate your module to. Note that when mating two connectors, the bandwidth of the connection is limited to the lower bandwidth of the two.

Mating incompatible connector types will cause damage to the connector. All Tektronix TDR modules come with a female version of the connector, and using an appropriate size male-to-female adapter as a connector saver is an easy way to avoid expensive damage to the module, in particular in environments where many designers are using the same TDR instrument.

When mating two microwave connectors, make sure that they mate without any force. Rotate only the connector nut – not the device to which the connector is attached or connector body. Use a torque wrench to make final connection.

Connectors should be cleaned with Isopropyl Alcohol (IPA) regularly. Use lint-free swabs only for cleaning. Always wear a static strap when cleaning or handling the connectors.

Connector quality can be checked by visual observation. However, connector gauges are precision instruments to determine connector quality or possible deterioration of the precision connector.

SMA connectors have a fundamentally different design from precision connectors. SMA has a dielectric-based design, whereas other connectors are air-interface design. Air-interface design provides a more repeatable connection and better electrical performance. As we noted above, even though SMA connectors are common and less expensive, their dimensions and performance are not as precisely maintained as those of the other precision microwave connectors. Continuous mating of SMAs with precision microwave connectors can increase wear and degrade performance of the precision connectors.

[1] 80E10 comes with S-to-K connector adapter to enable compensation only (not that V connector mates directly with S-connector, and K-connector mates directly with 3.5 mm or SMA). Use of this adapter to perform measurements will result in degradation of the module performance.

[2] SMA connectors are common and less expensive. However, their dimensions and performance are not as precisely maintained as those of the other precision microwave connectors. Continuous mating of SMAs with precision microwave connectors can increase wear and degrade performance of the precision connectors.

Appendix E – Accuracy vs. Dynamic Range Below Measurement Level

Dynamic range below measurement level, dB	Max error as % of the signal	Max peak-to-peak ripple, dB
10	31.6%	5.6884
11	28.2%	5.0322
12	25.1%	4.4590
13	22.4%	3.9561
14	20.0%	3.5133
15	17.8%	3.1224
16	15.8%	2.7766
17	14.1%	2.4703
18	12.6%	2.1986
19	11.2%	1.9574
20	10.0%	1.7430
21	8.9%	1.5524
22	7.9%	1.3828
23	7.1%	1.2319
24	6.3%	1.0975
25	5.6%	0.9779
26	5.0%	0.8714
27	4.5%	0.7765
28	4.0%	0.6919
29	3.5%	0.6166
30	3.2%	0.5495
31	2.8%	0.4897
32	2.5%	0.4365
33	2.2%	0.3890
34	2.0%	0.3467
35	1.8%	0.3090
36	1.6%	0.2753
37	1.4%	0.2454
38	1.3%	0.2187
39	1.1%	0.1949
40	1.0%	0.1737
41	0.9%	0.1548
42	0.8%	0.1380
43	0.7%	0.1230
44	0.6%	0.1096
45	0.6%	0.0977
46	0.5%	0.0871
47	0.4%	0.0776
48	0.4%	0.0692
49	0.4%	0.0616
50	0.3%	0.0549

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