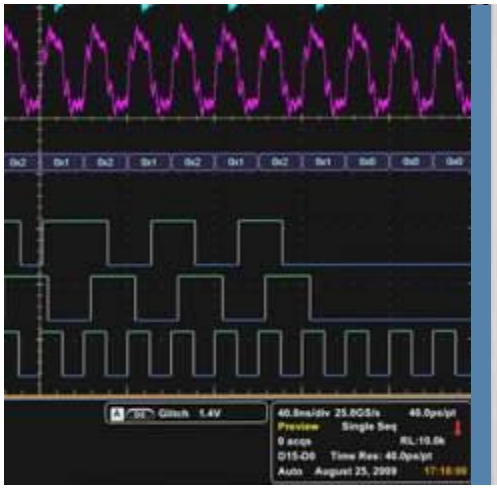
THUNDERBOLT™

DisplayPort

PHY Validation of Thunderbolt & DisplayPort



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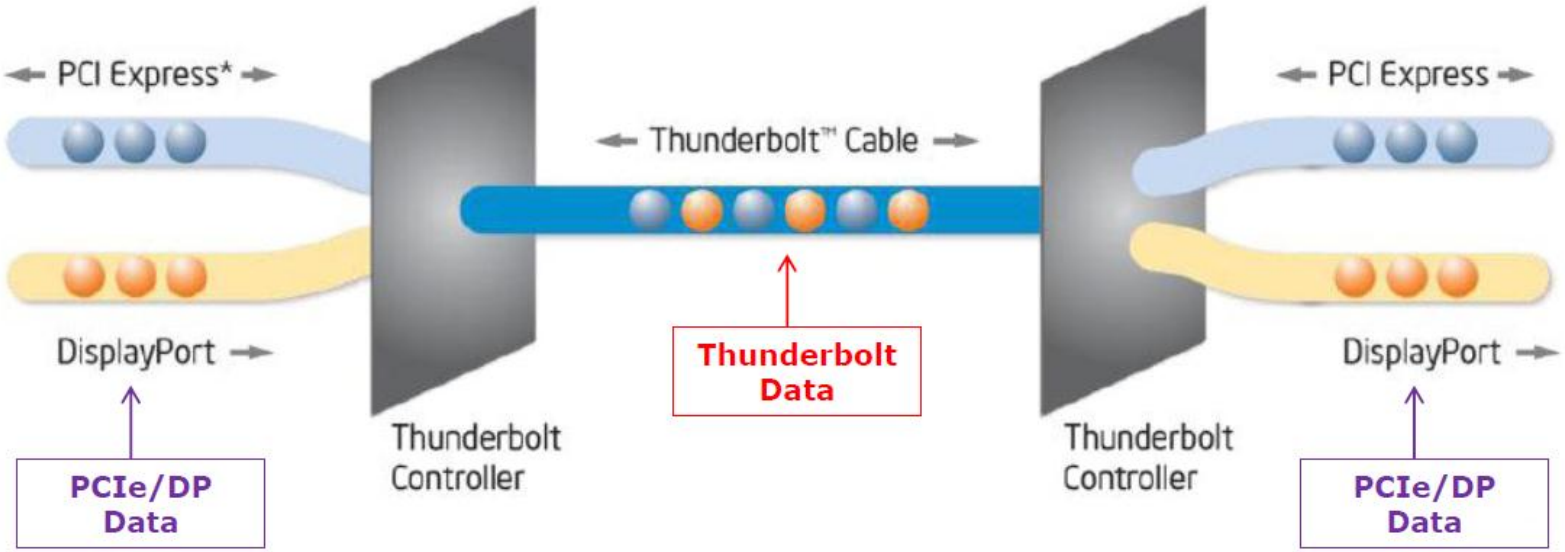
Thunderbolt Overview

- High Speed Data Bus for PC's
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.



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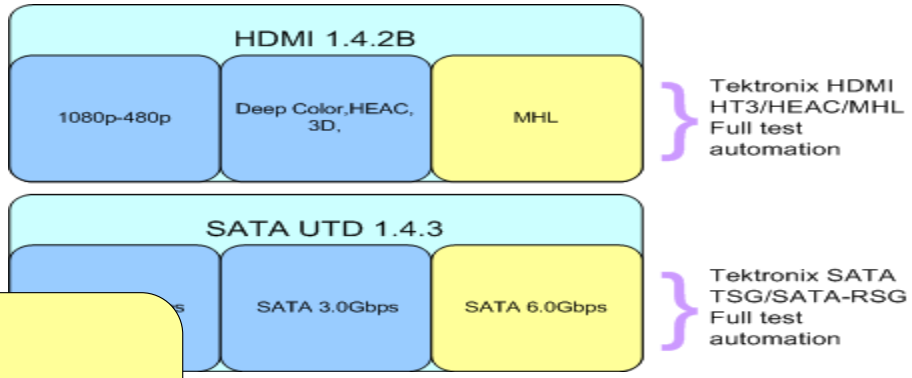
Thunderbolt Electrical Validation

Tektronix DPOJET
Thunderbolt .7 MOI
Manual Test



Thunderbolt (.7 Spec Revision)
10.3125Gbps

Thunderbolt (future Interop)

Display Port DP1.2

RBR (1.6Gbps),

HBR (2.7Gbps)

HBR2 (5.4Gbps)

DP++

Tektronix DP12
Full test automation

Dual Port Device Compliance Test Summary

- Physical Layer Testing
  - (Rev 0.7 Spec)
1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. DP Source MOI
5. DP++ (HDMI) Source MOI
6. Power Delivery MOI

- Functional Testing
  - Thunderbolt Functional CTS Rev 3.0.1
1. ROM Validation
2. Basic Device Functionality
3. EFI
4. Downstream Device Functionality
5. Downstream Display Functionality
6. Extended Test Functionality
7. Complex Topology
8. DUT Specific Verification
9. Negative Testing
10. Firmware Update Validation

CTS – Compliance Test Specification
MOI – Method of Implementation (Test Procedure)

Single Port Device Compliance Test Summary

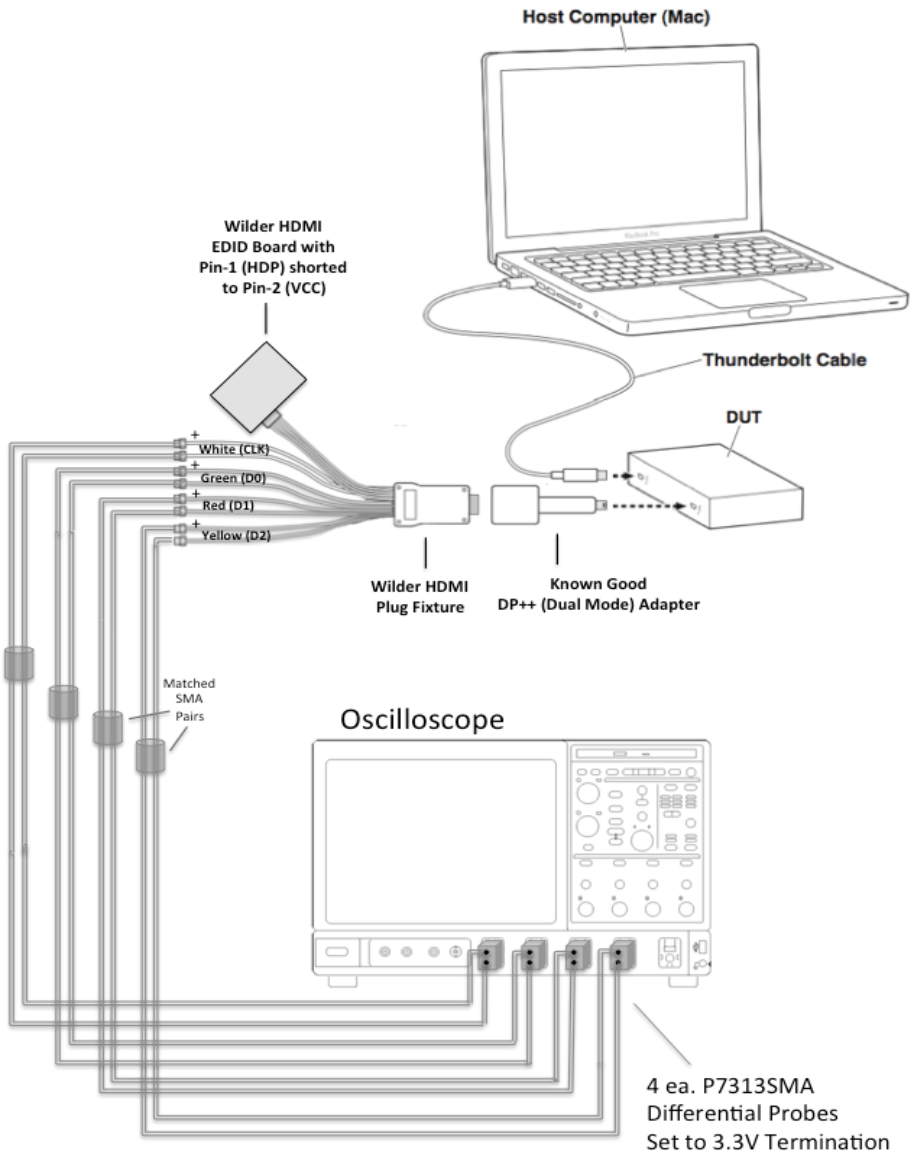
- Physical Layer Testing
  - (Rev 0.7 Spec)
1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. Power Consumption

- Functional Testing
  - Thunderbolt Functional CTS Rev 2.4 (IBL 488434)
1. ROM Validation
2. Basic Device Functionality
3. EFI
4. DUT Specific Verification
5. Negative Testing
6. Firmware Update Validation

CTS – Compliance Test Specification
MOI – Method of Implementation (Test Procedure)

HDMI Test Setup

- DSA70804C or higher
- SMA Differential Probes
  - Provides 3.3V bias
- HT3 HDMI Compliance SW
- Mac or equivalent tool used to control downstream port on a 2 port device
- Both ports tested

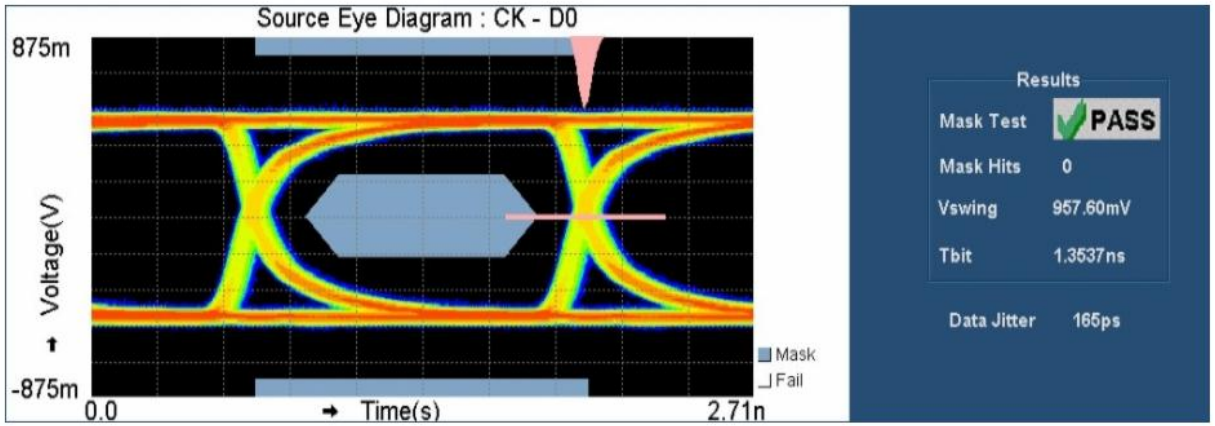


Example of HDMI Passing Results

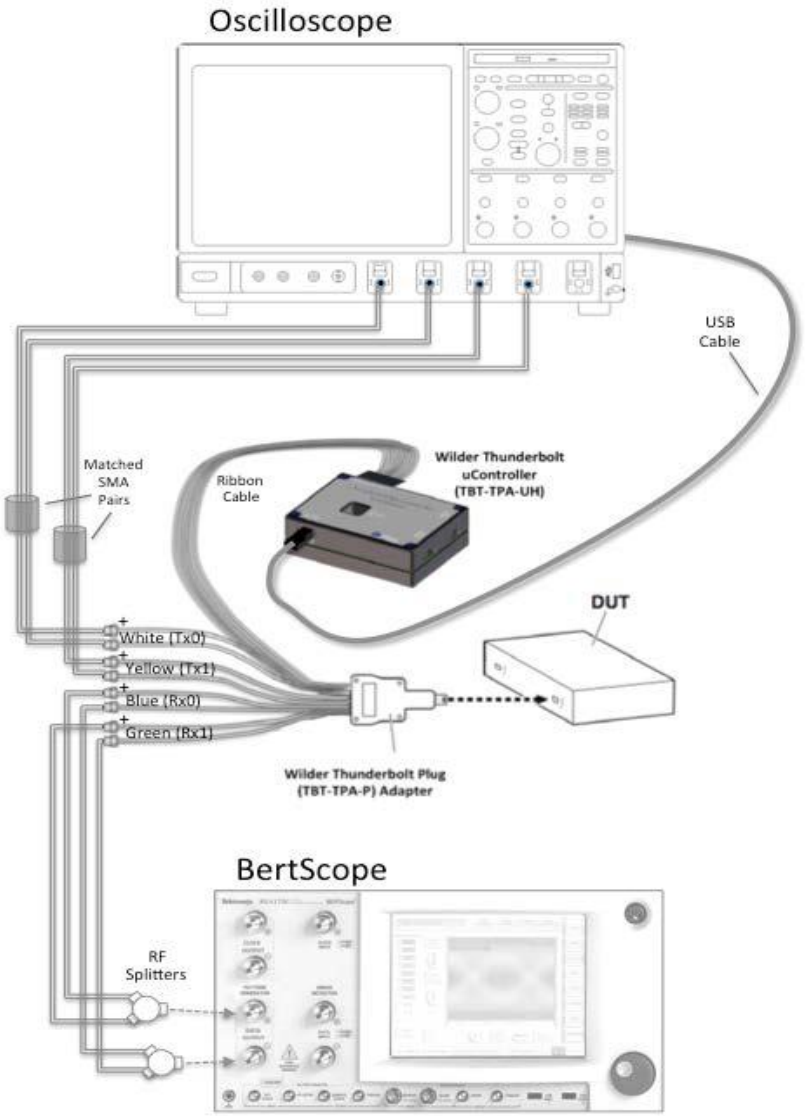
- **Test Summary**

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.08*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.1*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.007*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.012*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.005*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	220.23ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	208.34ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	210.28ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	223.47ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	212.71ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	219.38ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	208.07ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	254.07ps	Pass
16	7-8 : Max Duty Cycle	CK	--	--	Error
17	7-8 : Min Duty Cycle	CK	--	--	Error

- **Waveform/Plot**



Automated Thunderbolt Tx Testing



Recommended Equipment

- DPO/DSA/MSO71604 (≥ 16 GHz BW)
- BSA125C (crosstalk source)
- Option DJA (DPOJET)
- Option TBT-TX (TekExpress)
- TF-TB-TPA-P (Plug fixture) & TBT-TPA-UH (port microcontroller)

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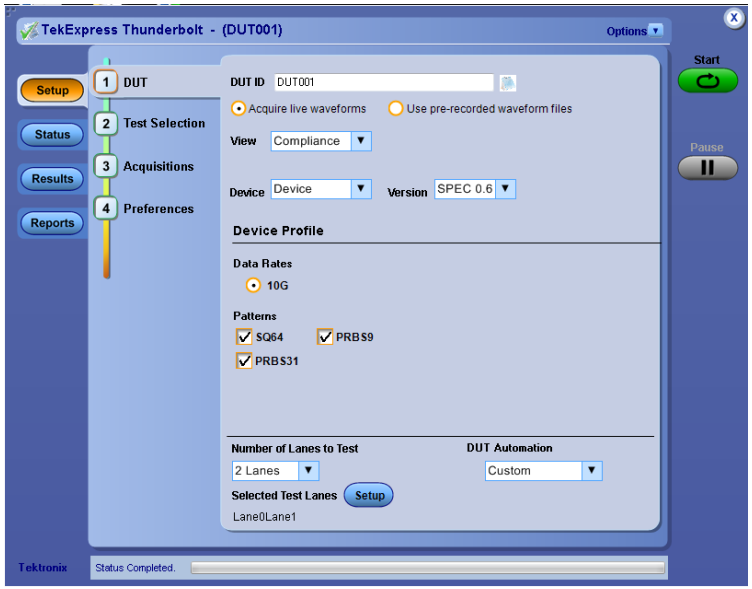
Option TBT-TX
Compliance Automation Software

- Automates scope setup & compliance measurements per the Tek Thunderbolt MOI
- Fast test execution
  - Simultaneous two lane testing
  - Automated DUT state control for devices
- User-selectable tests
- Creates complete test report



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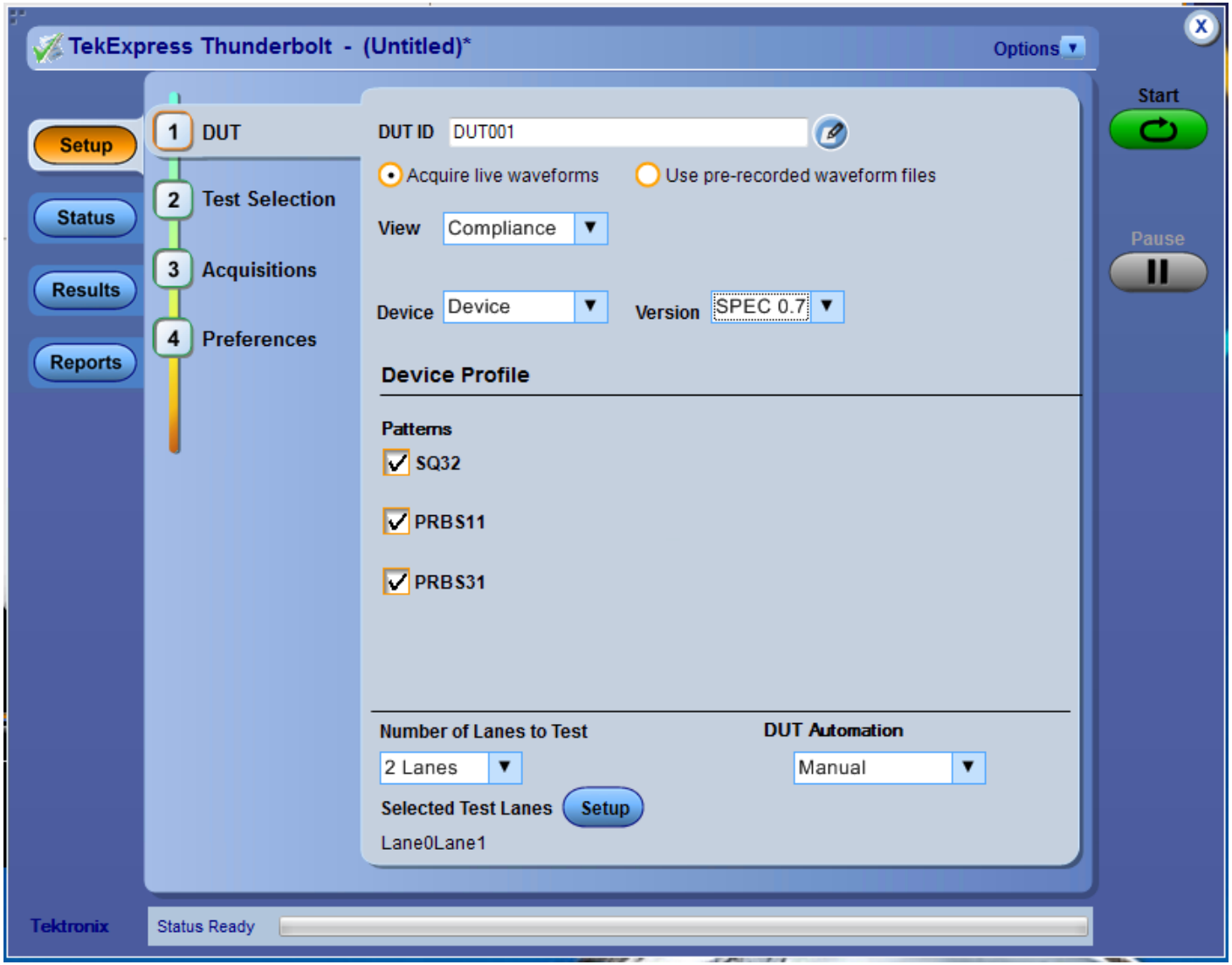
Thunderbolt Transmitter Testing

- **Step 1:** Select Measurement Setup



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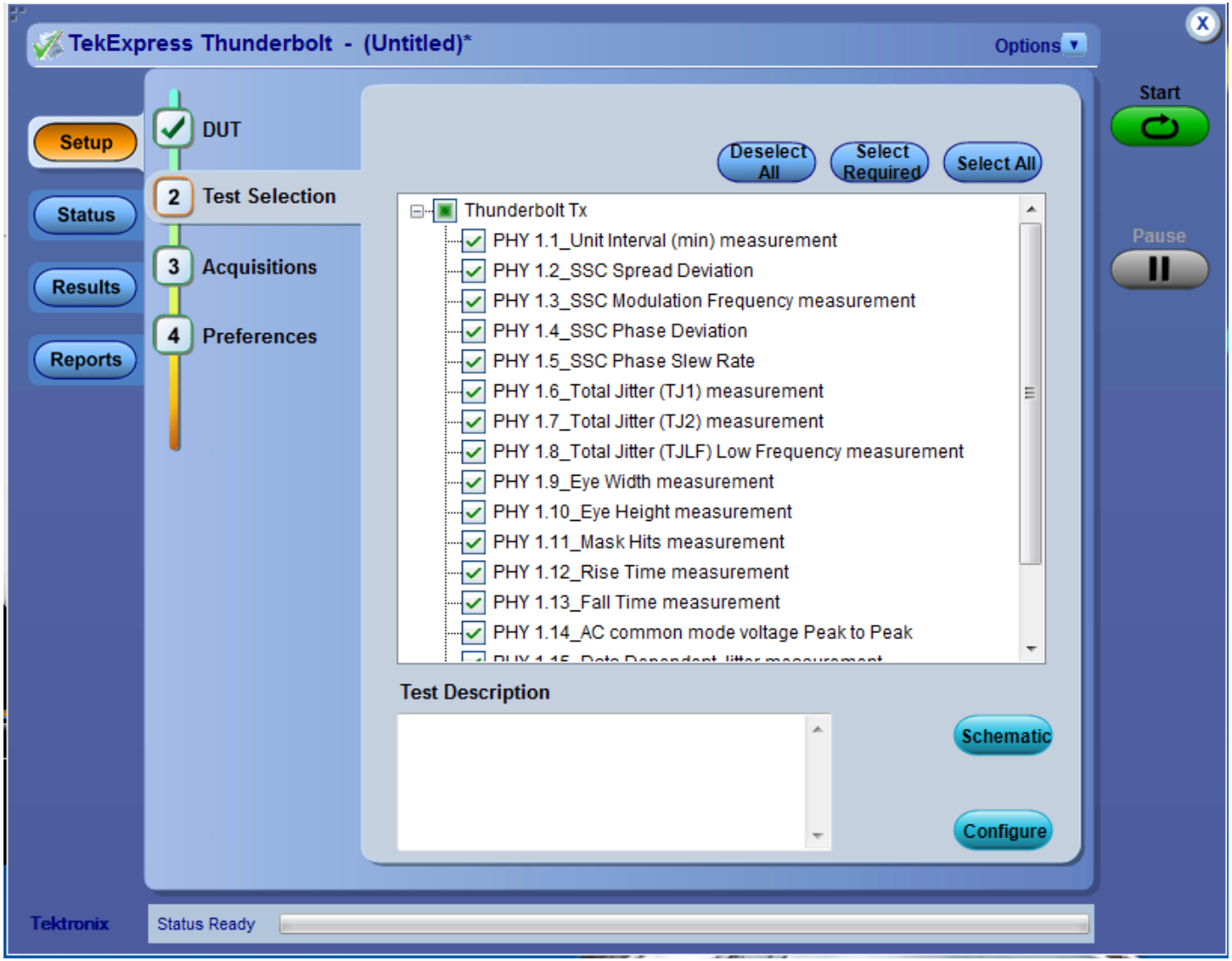
Thunderbolt Transmitter Testing

- **Step 2:** Select Measurements (total 18 measurements)



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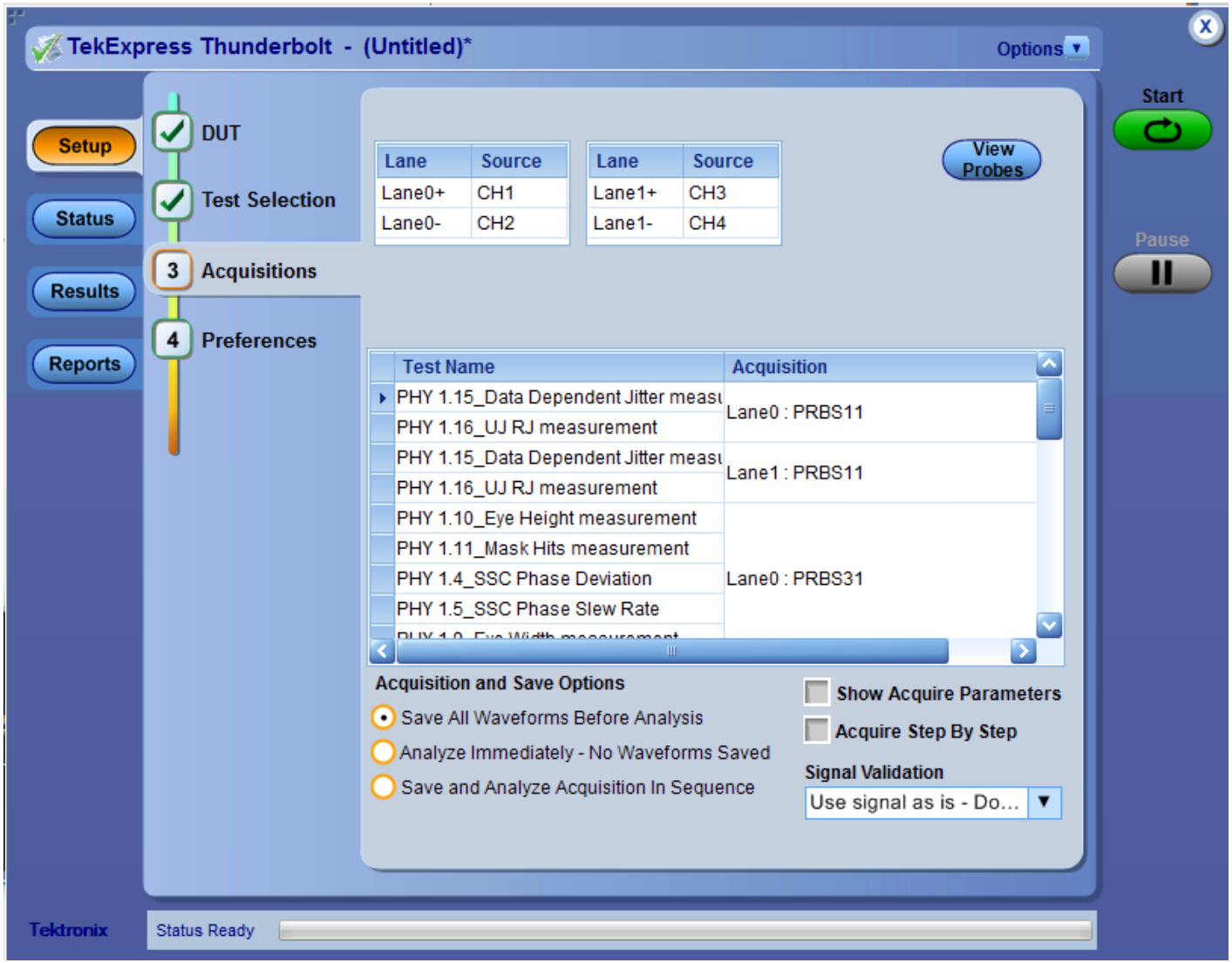
Thunderbolt Transmitter Testing

- **Step 3:** Configure Acquisitions



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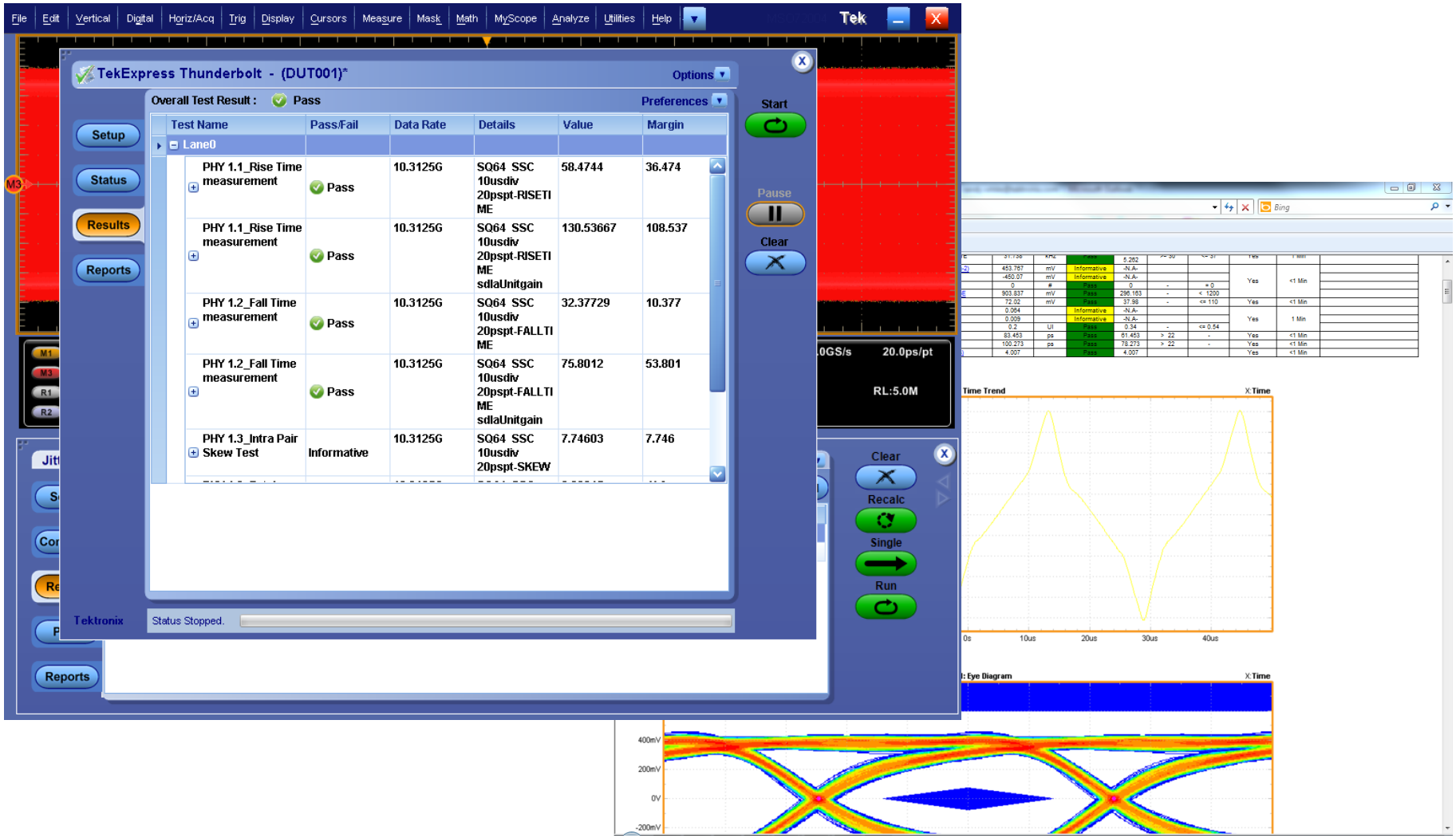
Thunderbolt Transmitter Testing

- **Step 4:** Start Tests and Generate Report



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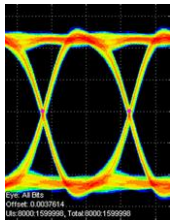
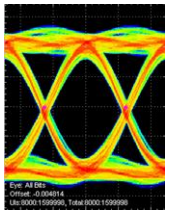
Test Challenge: De-Embedding
Transmitter Compliance Testing

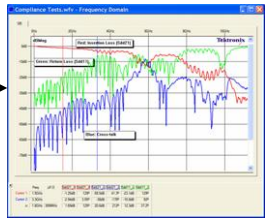
- Host/device compliance point at TP1 (mated plug/receptacle)
- De-embedding required to remove fixture effects
- S-Parameters are acquired from calibration fixture



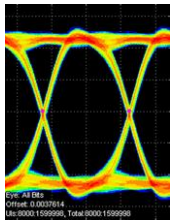
Signal at TP1



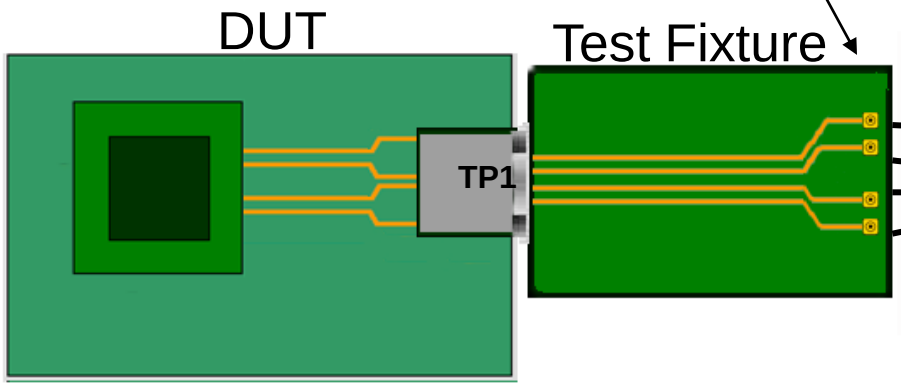
Measured Signal

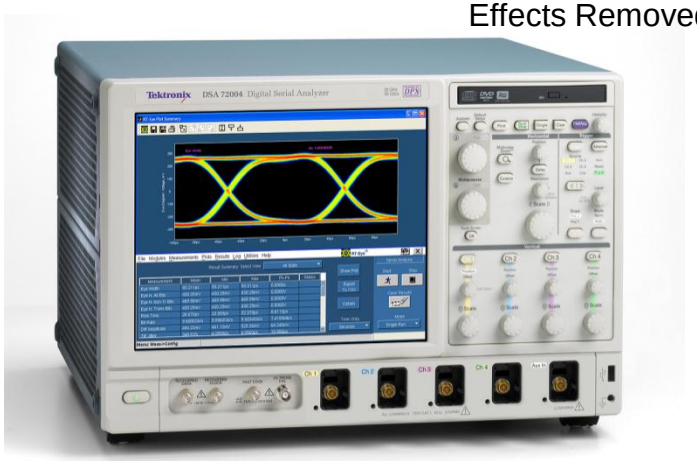


Apply Sparameters



Signal with Fixture Effects Removed



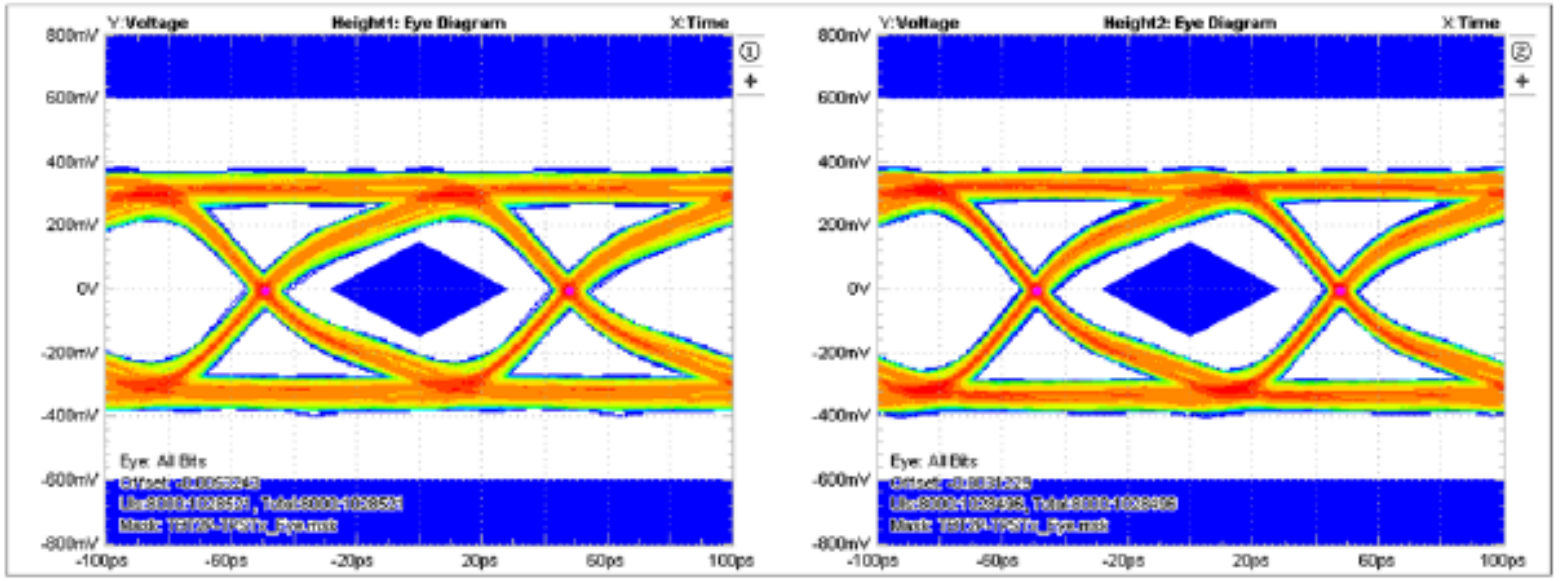


Thunderbolt Fixture De-Embed results

- **Measurement Results**

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Height1, Math1	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Height2, Math3	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
TJ@BER2, Math3	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s

- **Pass/Fail Summary** No pass/fail limits are currently selected.
- **Plot Images**
  - **Measurement Plot(s)**



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Test Challenge: Crosstalk
Measuring Bounded Uncorrelated Jitter (BUJ) is Critical

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio.
- The implications of complex channel interaction can be observed and identified by examining the type and amount of BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

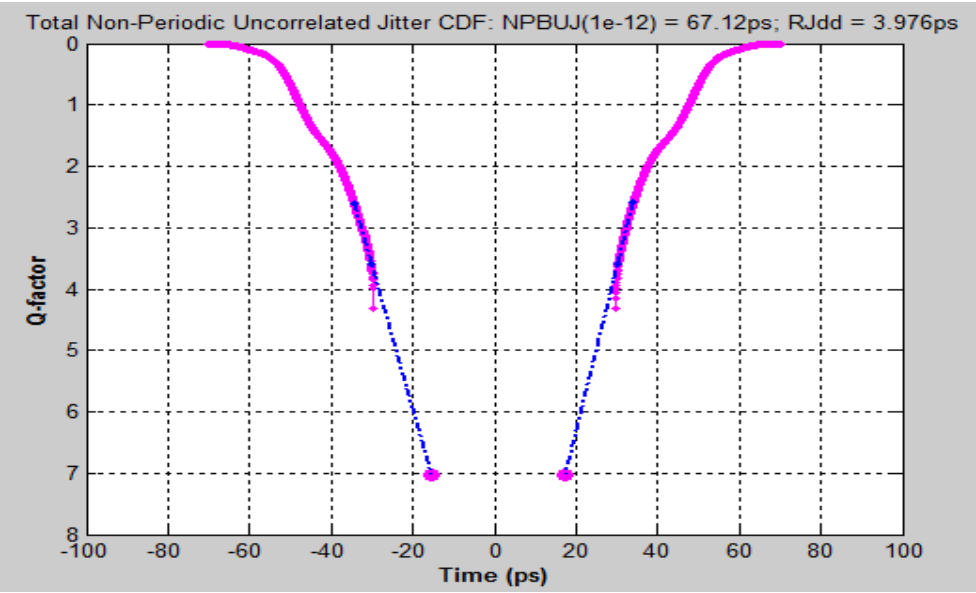

Table 4-6. Stressed Receiver Conditions

Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter

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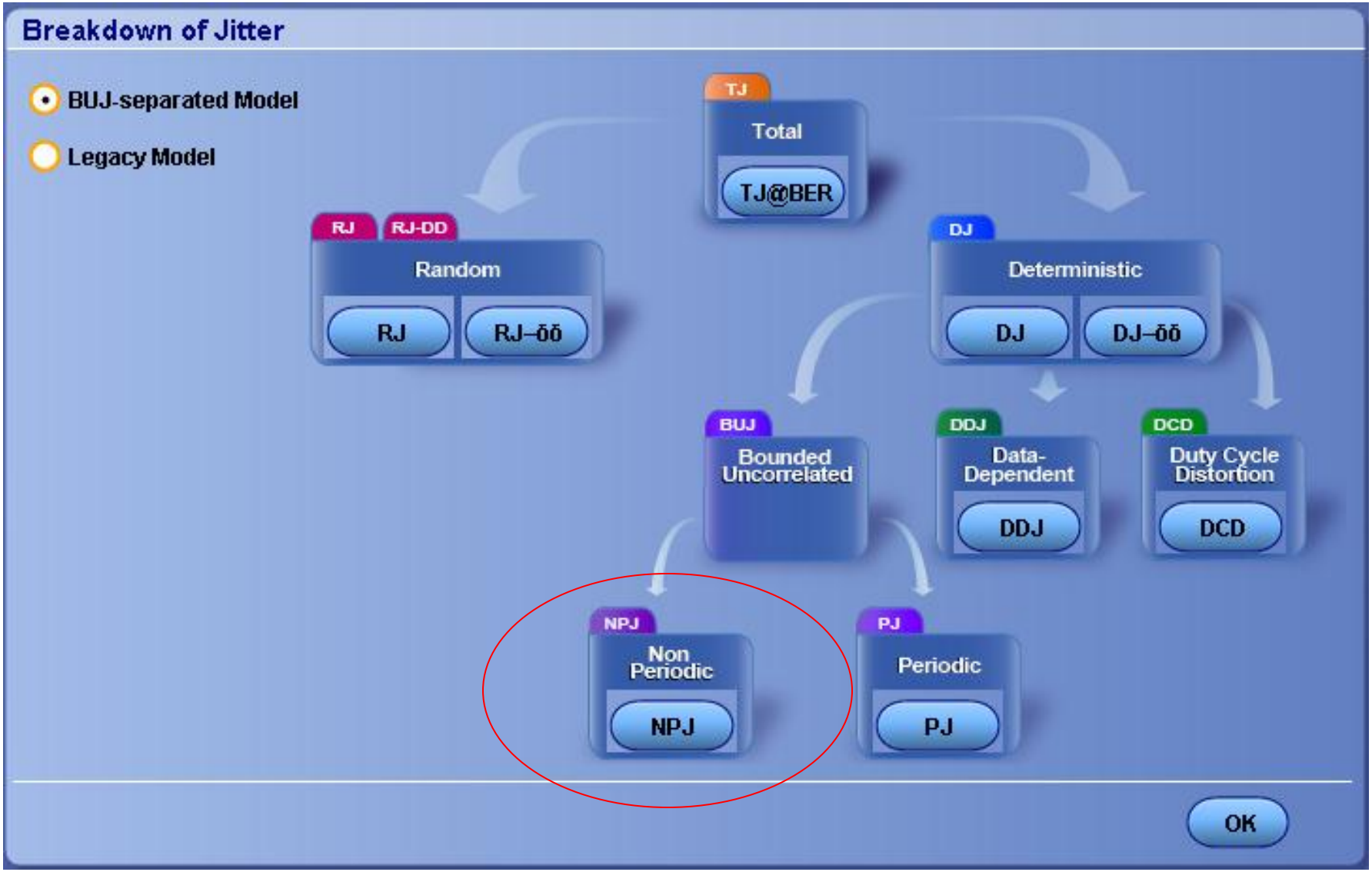
BUJ in real time jitter analysis



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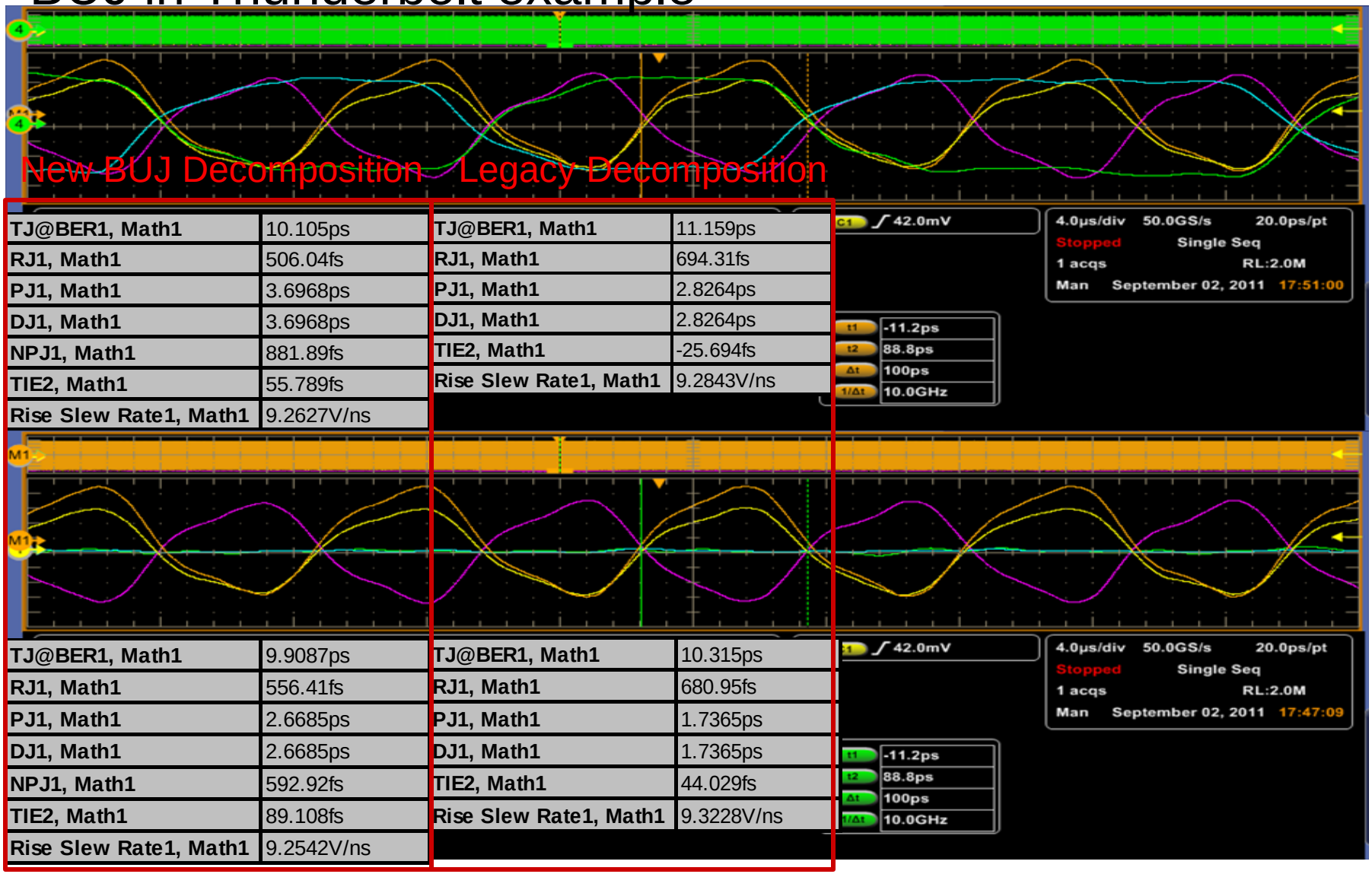
BUJ in Thunderbolt example



TJ@BER1, Math1	10.105ps
RJ1, Math1	506.04fs
PJ1, Math1	3.6968ps
DJ1, Math1	3.6968ps
NPJ1, Math1	881.89fs
TIE2, Math1	55.789fs
Rise Slew Rate1, Math1	9.2627V/ns

TJ@BER1, Math1	11.159ps
RJ1, Math1	694.31fs
PJ1, Math1	2.8264ps
DJ1, Math1	2.8264ps
TIE2, Math1	-25.694fs
Rise Slew Rate1, Math1	9.2843V/ns

TJ@BER1, Math1	9.9087ps
RJ1, Math1	556.41fs
PJ1, Math1	2.6685ps
DJ1, Math1	2.6685ps
NPJ1, Math1	592.92fs
TIE2, Math1	89.108fs
Rise Slew Rate1, Math1	9.2542V/ns

TJ@BER1, Math1	10.315ps
RJ1, Math1	680.95fs
PJ1, Math1	1.7365ps
DJ1, Math1	1.7365ps
TIE2, Math1	44.029fs
Rise Slew Rate1, Math1	9.3228V/ns

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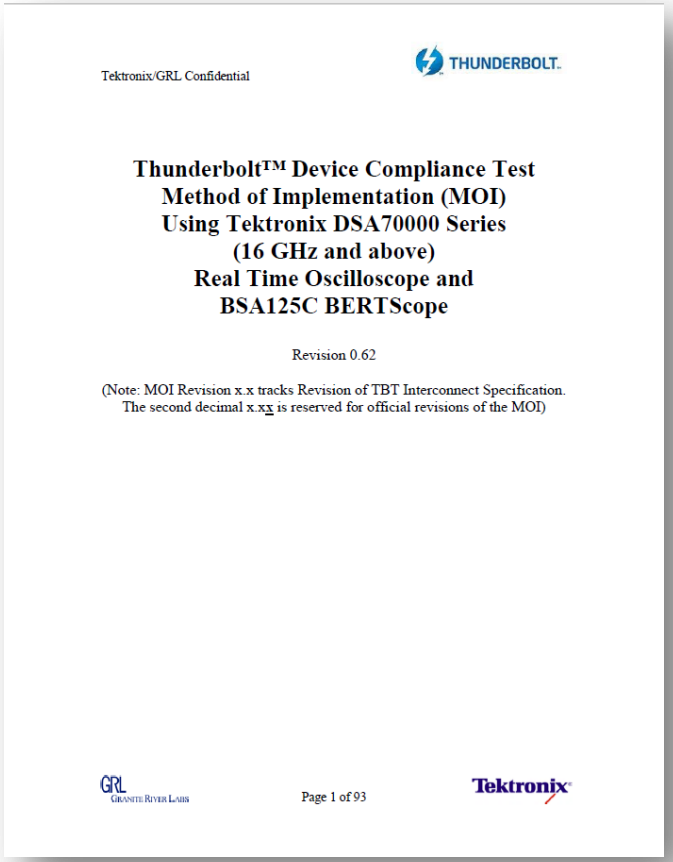
Receiver Testing Overview

- MOI critical to Rx Test
- Includes step-by-step procedure along with setup files for calibration



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THUNDERBOLT

Thunderbolt™ Device Compliance Test
Method of Implementation (MOI)
Using Tektronix DSA70000 Series
(16 GHz and above)
Real Time Oscilloscope and
BSA125C BERTScope

Revision 0.62

(Note: MOI Revision x.x tracks Revision of TBT Interconnect Specification.
The second decimal x.xx is reserved for official revisions of the MOI)

GRL Granite River Labs

Page 1 of 93

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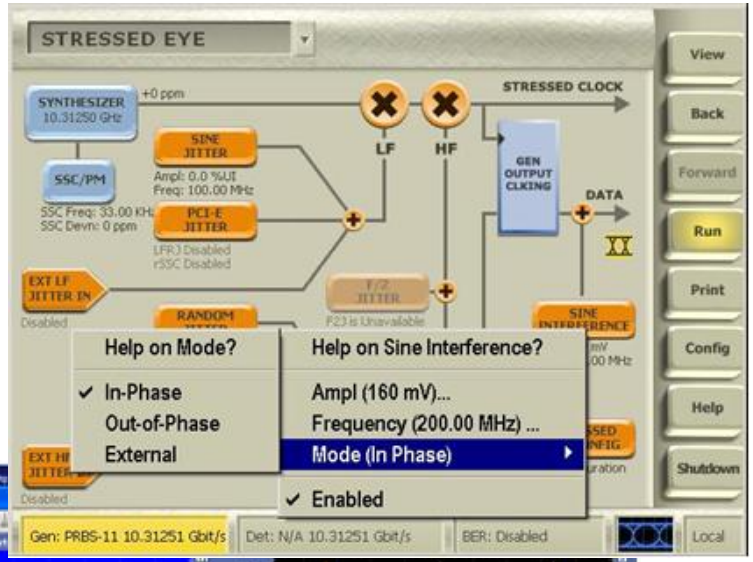

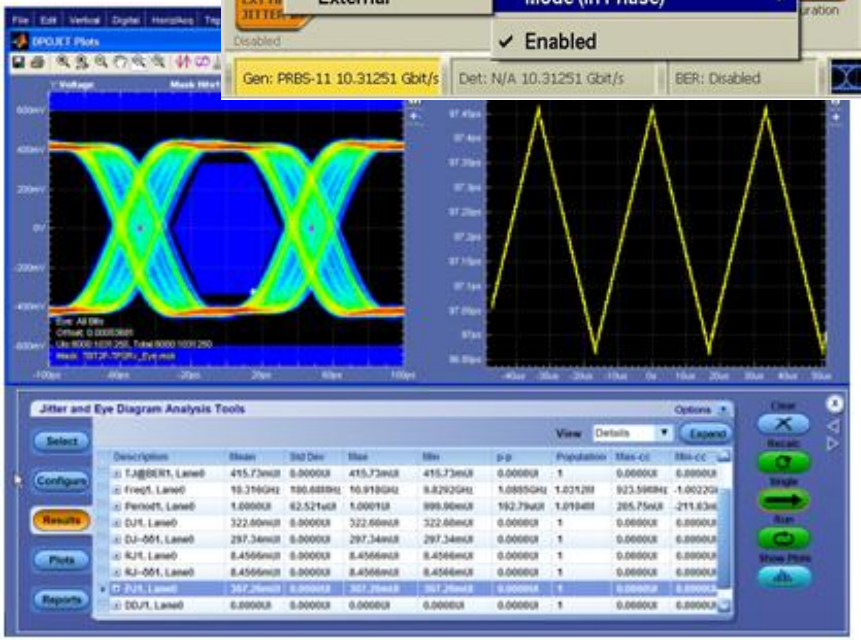

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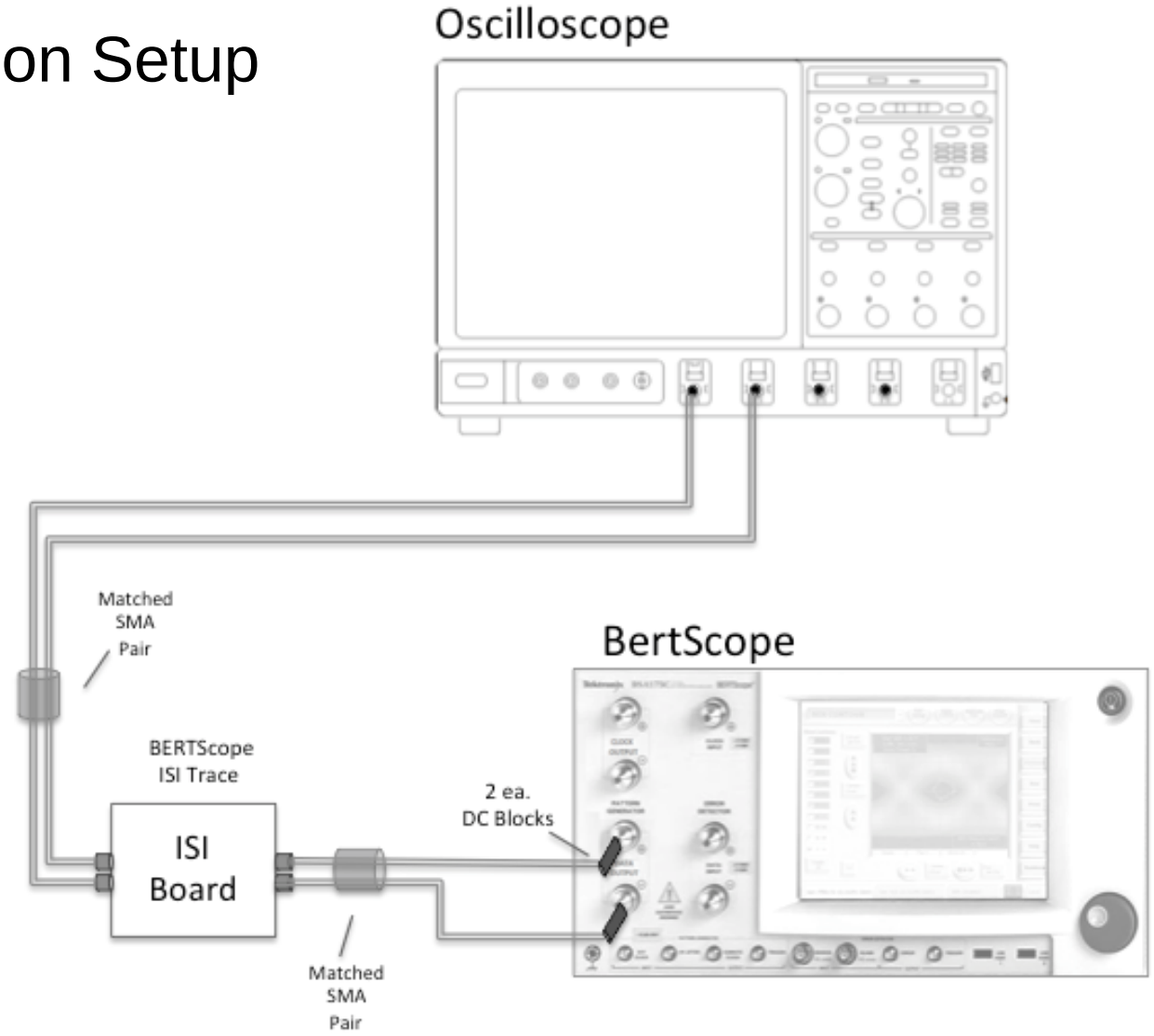
Calibration Setup



Physical Setup → ISI Calibration → RJ calibration → SJ calibration → AC Common Mode calibration → Eye Height Calibration and TJ → RX Testing

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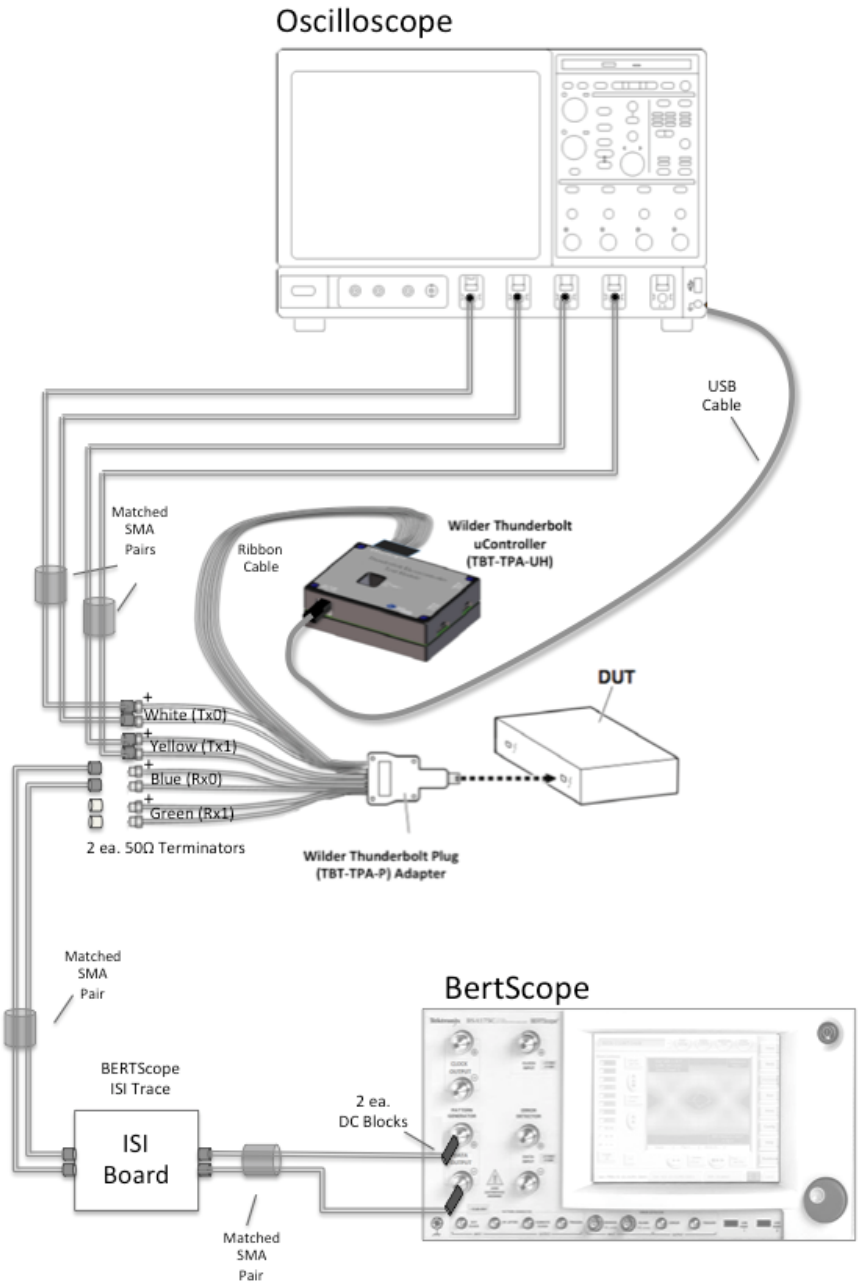
Rx Testing

Steps to Run BER test:

- Attach DUT & microcontroller
- Turn on required stresses
- Run RX BER script for 6 mins

```
C:\Program Files\Intel Corpora
Rev 1.1
DUT found is LR
Please wait for Lane check
Lane under test is Lane 0
Wait for BER testing
BER is 0.000000e+000
Symbol_count is 2110019967936
Error_count is 0
Please hit Enter to close the window
```



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Complete Thunderbolt Instrument Portfolio

Receiver Tests/Active Cable Tests Receiver silicon and system margin testing. Tj, Rj, DDJ, BUJ, AC-CM	**BSA125C** 12.5 Gb/s BERTScope **DPP125B** Digital Pre-Emphasis Preprocessor **CR125A** Clock Recovery Unit **TF-TB-TPA-P/R** Plug & Receptacle Test Fixtures	
Channel Tests Return Loss (HF,LF) (SDD11,SDD22) Common Mode Return Loss (SCC22) Channel Insertion Loss (SDD21) Near End Crosstalk (NEXT)	**DSA8300** Sampling Oscilloscope **80E04** 20 GHz TDR Sampling Module **80SICON** S-Parameter Analysis Software for DSA8300 **TF-TB-TPA-P** Test Fixture	
Transmitter Tests AC Parametric measurements Jitter Eye Opening	**DSA71604C** with option **TBT-TX** **DPOJET** Jitter Analysis software **TF-TB-TPA-P** Test Fixture	

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Debug Example

- TBT design fails during certification
  - Report shows voltage/timing failures
- What's the next step?

Test Name	Lane	Pattern	Speed	SSC	Measurement Details	Measured value	Units	Test Result
PHY 1.5_Eye Height measurement	Lane0	PRBS31	10.3125G	SSC	HEIGHT	147.238	mV	Fail
PHY 1.6_Eye Width measurement	Lane0	PRBS31	10.3125G	SSC	WIDTH	0.404	UI	Fail
PHY 1.9_Unit Interval (min) Measurement	Lane0	PRBS31	10.3125G	SSC	PERIOD(Fig-1)	97.225	ps	Pass
PHY 1.10_SSC Modulation Frequency Measurement	Lane0	PRBS31	10.3125G	SSC	SSCMODRATE	31.76	kHz	Pass
PHY 1.7_Max Differential Voltage Measurement	Lane0	PRBS31	10.3125G	SSC	EYEHIGH(Fig-2)	484.697	mV	Informative
	Lane0	PRBS31	10.3125G	SSC	EYELOW	-480.843	mV	Informative
	Lane0	PRBS31	10.3125G	SSC	MASKHITS	154	#	Fail
	Lane0	PRBS31	10.3125G	SSC	MAXDIFFVGE	965.54	mV	Pass
PHY 1.4_AC common mode voltage Peak to Peak	Lane0	PRBS9	10.3125G	SSC	PK2PK	58.355	mV	Pass
PHY 1.8_Total Jitter measurement	Lane0	PRBS31	10.3125G	SSC	DJ	0.127		Informative
	Lane0	SQ64	10.3125G	SSC	RJ	0.006		Informative
	Lane0	SQ64	10.3125G	SSC	TJBER	0.56	UI	Fail
PHY 1.1_Rise Time measurement	Lane0	SQ64	10.3125G	SSC	RISETIME	83.023	ps	Pass
PHY 1.2_Fall Time measurement	Lane0	SQ64	10.3125G	SSC	FALLTIME	104.417	ps	Pass
PHY 1.3_Intra Pair Skew Test	Lane0	SQ64	10.3125G	SSC	SKEW(Fig-3)	4.231		Pass

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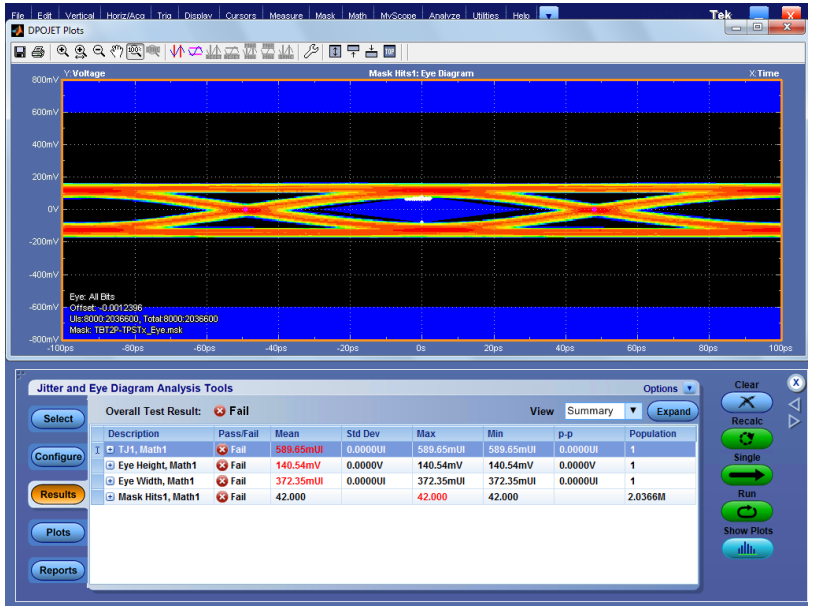
Drilling into Root Cause

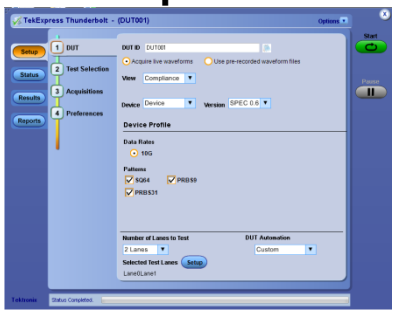
- Import saved waveforms into DPOJET
- Re-run measurements that fail
- Based on results can:
  - Compare against addition plots
  - Modify DPOJET or acquisition settings (filters, RL, etc.)
  - Investigate signal anomalies with DPOJET sync features



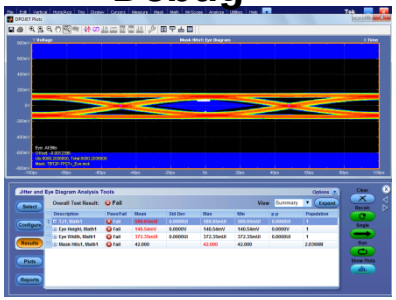
Final Resolution

- Voltage droop on D^- (Ch3) causes amplitude imbalance
- Customer suspects RC time constant not set correctly (DC block/pull down)

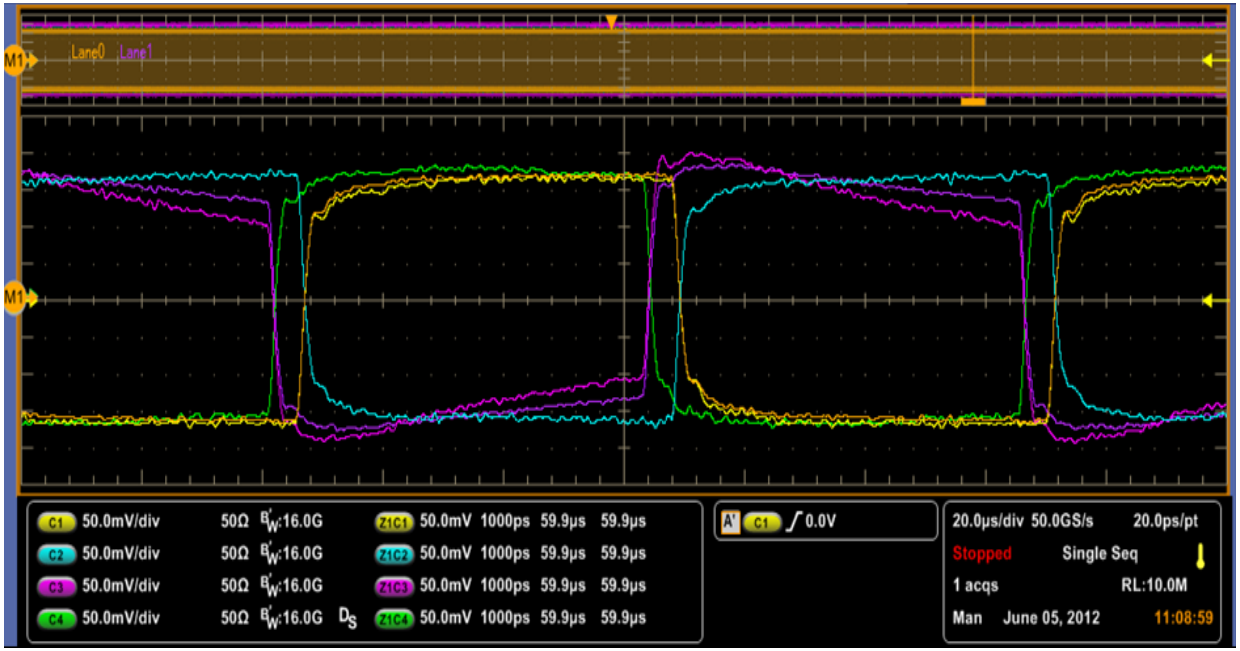
Compliance



Debug



Root Cause



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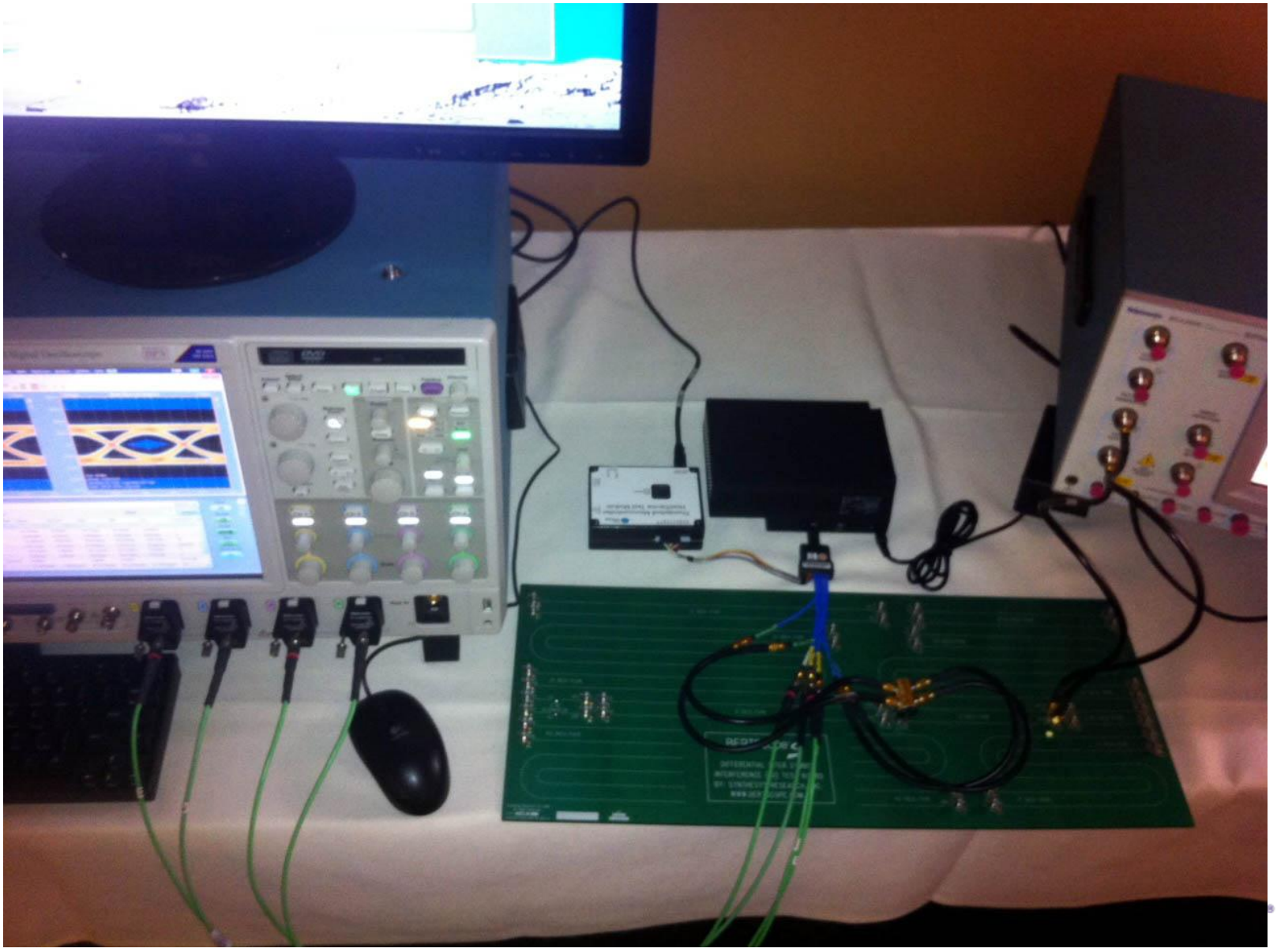
THUNDERBOLT™

DisplayPort

DEMO

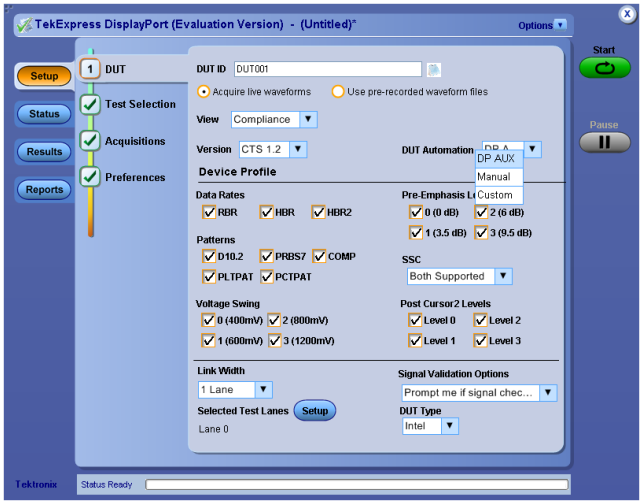


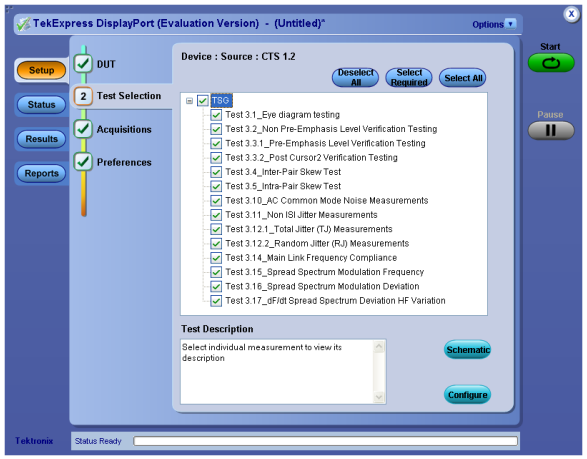
Display Port Source testing

1. Select

2. Acquire

3. Analyze





Can it be just that easy?

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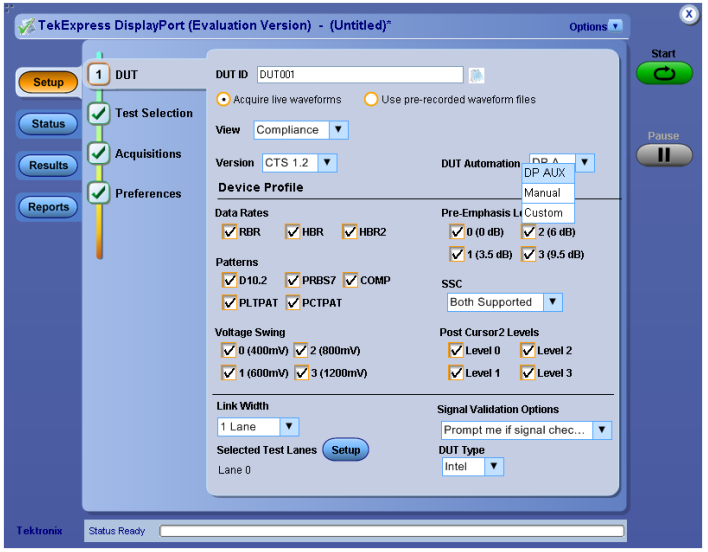
Customer needs in Display Port testing

- Challenges
  - Device State control
  - Measurements algorithms
  - Setups
- Requirements
  - Straight forward operations and setups
  - Complete testing for both single ended and differential measurements
  - Flexibility in testing
- Results
  - Pass or Fail
  - Margins and Limits
  - Complete and easy to read report



How does Tektronix help with Display Port testing

- Tektronix offers a complete and easy testing solution to support the testing needs for Display Port.

- Compliance and Characterization.
  - Minimum user intervention
  - Easy Pass fail status
  - Test result provide margins

- Debugging
  - Automatic saving of the failed data set.
  - Offline failure analysis of the save data
  - Flexible probing for debugging

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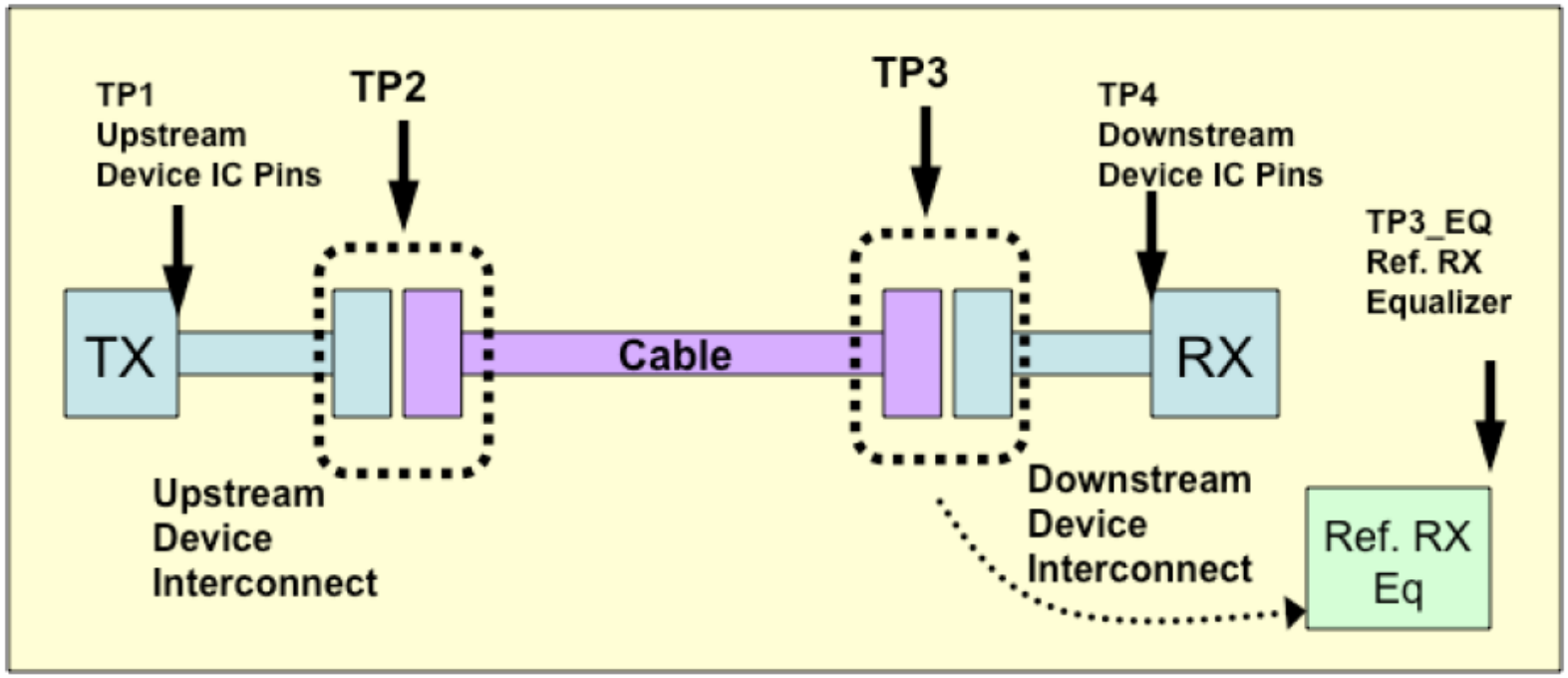
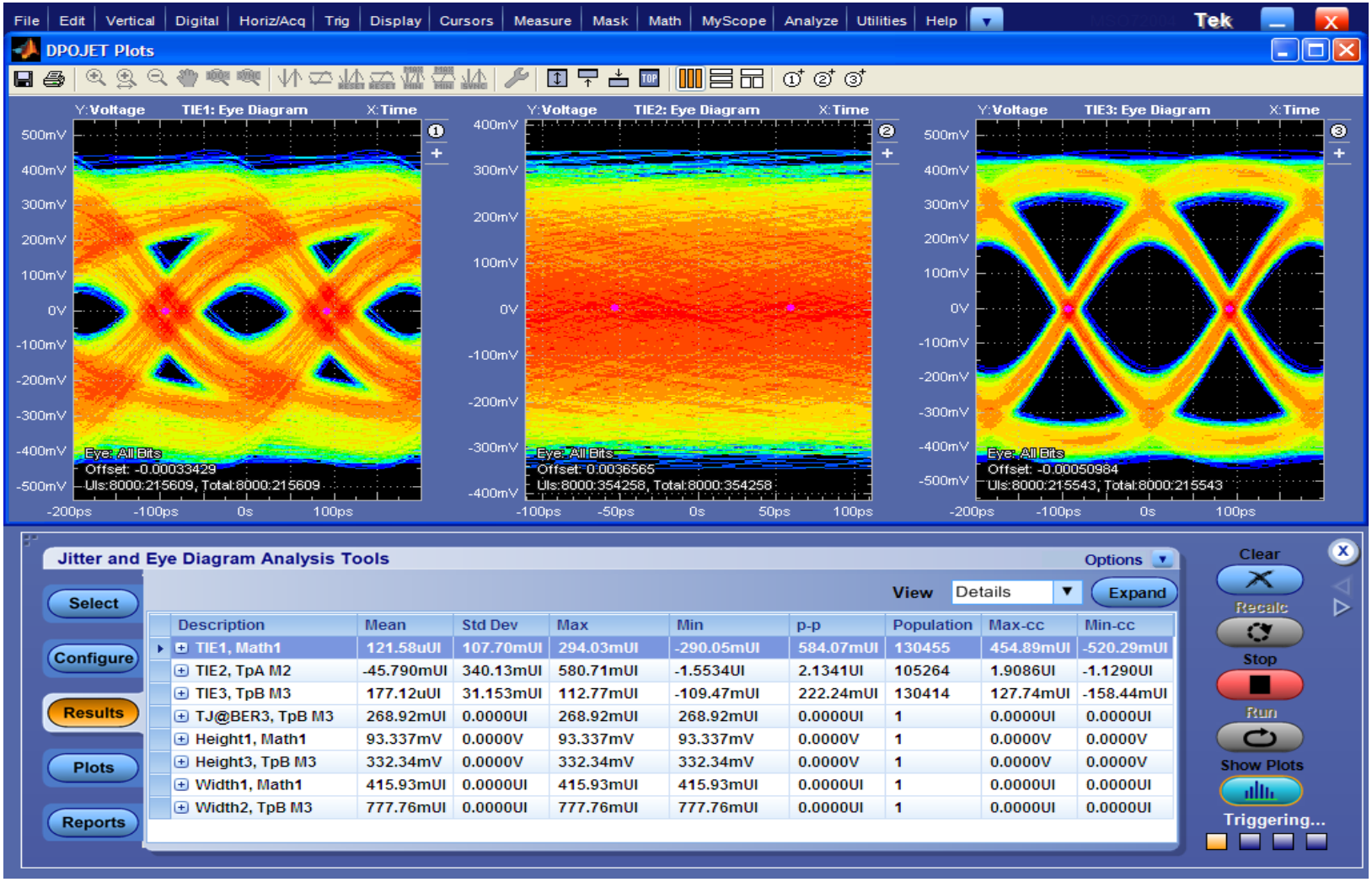
DisplayPort Test Point

- Test Point Definitions
  - TP1: at the pins of the transmitter device.
  - TP2: at the test interface on a test access fixture
  - TP3: at the test interface on a test access
  - TP3_EQ: TP3 with equalizer applied.
  - TP4: at the pins of a receiving device.



Eye Diagram Test using Eye Compliance Pattern

- An Eye diagram test for 800mV , 0dB pre-emphasis at TP2,TP3, TP3-EQ.



Automation: DP Testing is a large task!

Combination Parameters For DP1.2 testing

Data Rate	**- 3**
Lanes	**- 4**
Pre-Emphasis	**- 4 Levels**
Voltage Swing	**- 4 Levels**
Post Cursor2	**- 4 Levels**
SSC	**- 2 Levels(SSC On and Off)**
Patterns	**- 5 Supported Patterns**

Combination of tests

1. **Differential tests**
2. **Single Ended tests**

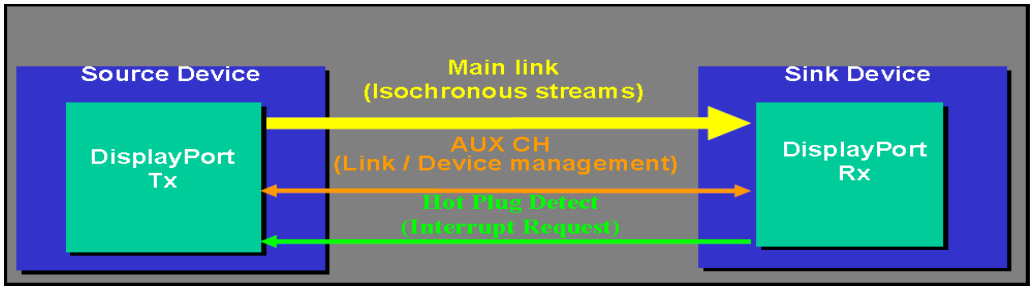
Test	Waveforms(SSC, 4 Lanes possible Combinations)
Eye Diagram test	80
Pre-Emphasis Test	240
Non-Pre-Emphasis	32
Total Jitter	80

~432 Acquired signals for DP1.2 Normative Measurements per lane.
X4 lanes results in 1728 Automated Acquisitions per DUT.

DisplayPort Auxiliary Channel Controller (DP-AUX)

Why use Aux channel controller in physical layer testing?

- Speeds up Test Time – No User Interaction is Required to Change Source Output Signal or Validate Sink Silicon State or Error Count
- No Need to Learn Vendor-specific Software - A Single GUI Supports All Vendors
- View & Log Decoded AUX Traffic and Hot Plug Detect (HPD) Events from the Device under Test to the DP-AUX DisplayPort AUX Controller
- Ability to Read and Write DPCD Registers Supports Debug Activities
- Tektronix DP-AUX can serves as a DP1.2 Sink, enabling the source to transmit the required patterns for testing.



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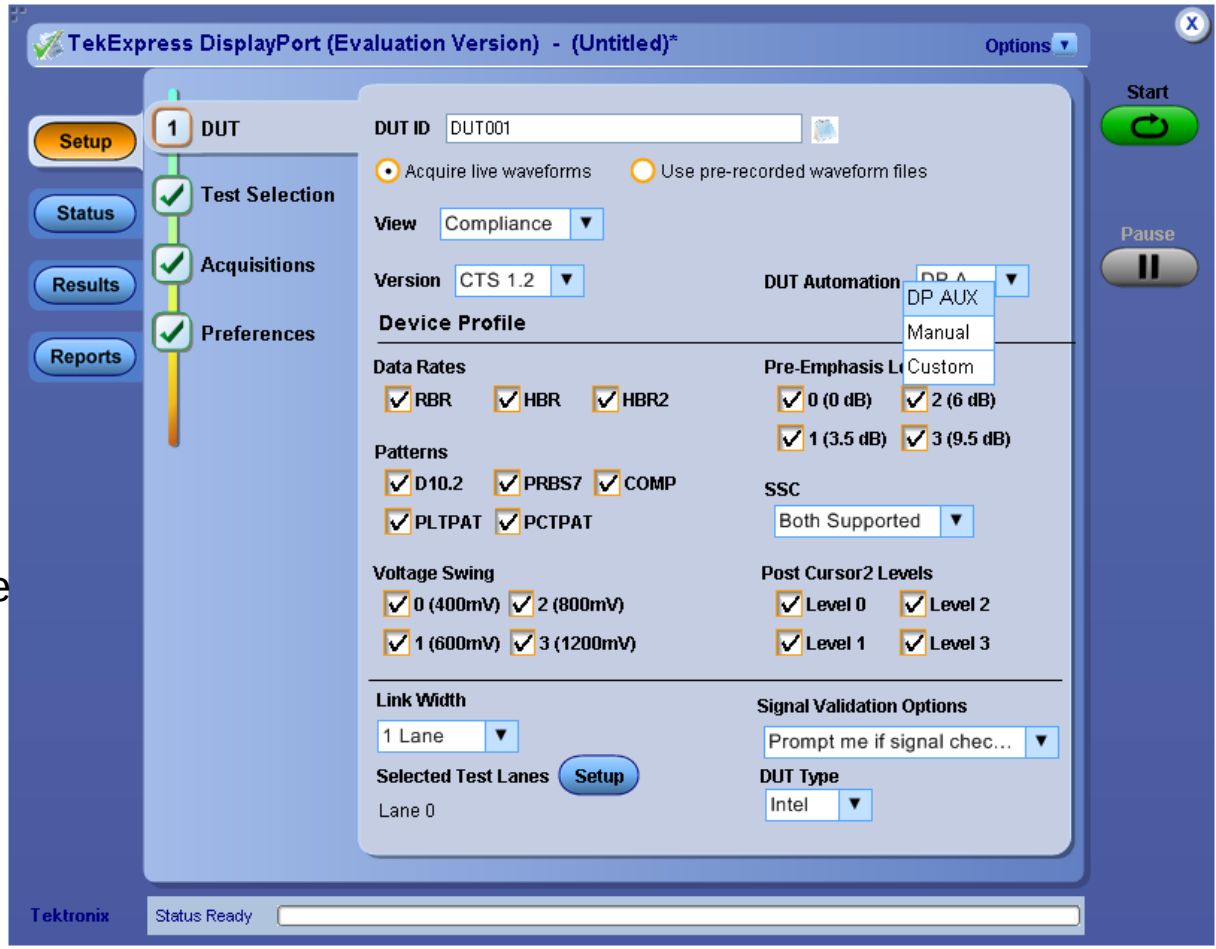
TekExpress DP1.2 Automation

- Comprehensive Display Port version 1.2 Physical Layer Conformance and Compliance verification tool.
  - All Core DP1.2 measurements
  - Keithley RF Switch and DP-AUX fully automated solution.
  - Selected measurements can be applied across all test permutations (SSC,CTLE's,swing,rates,pre-emphasis,etc) translates to **1728 measurements**. DP12 will provide full user intervention free, automated testing. This is the killer value proposition.



- Factory Automation API for full product control in silicon automation systems.
- Complimentary Fixtures and Compliance Interconnect Channel HW defined by VESA make this package a full customer solution with no compromises.

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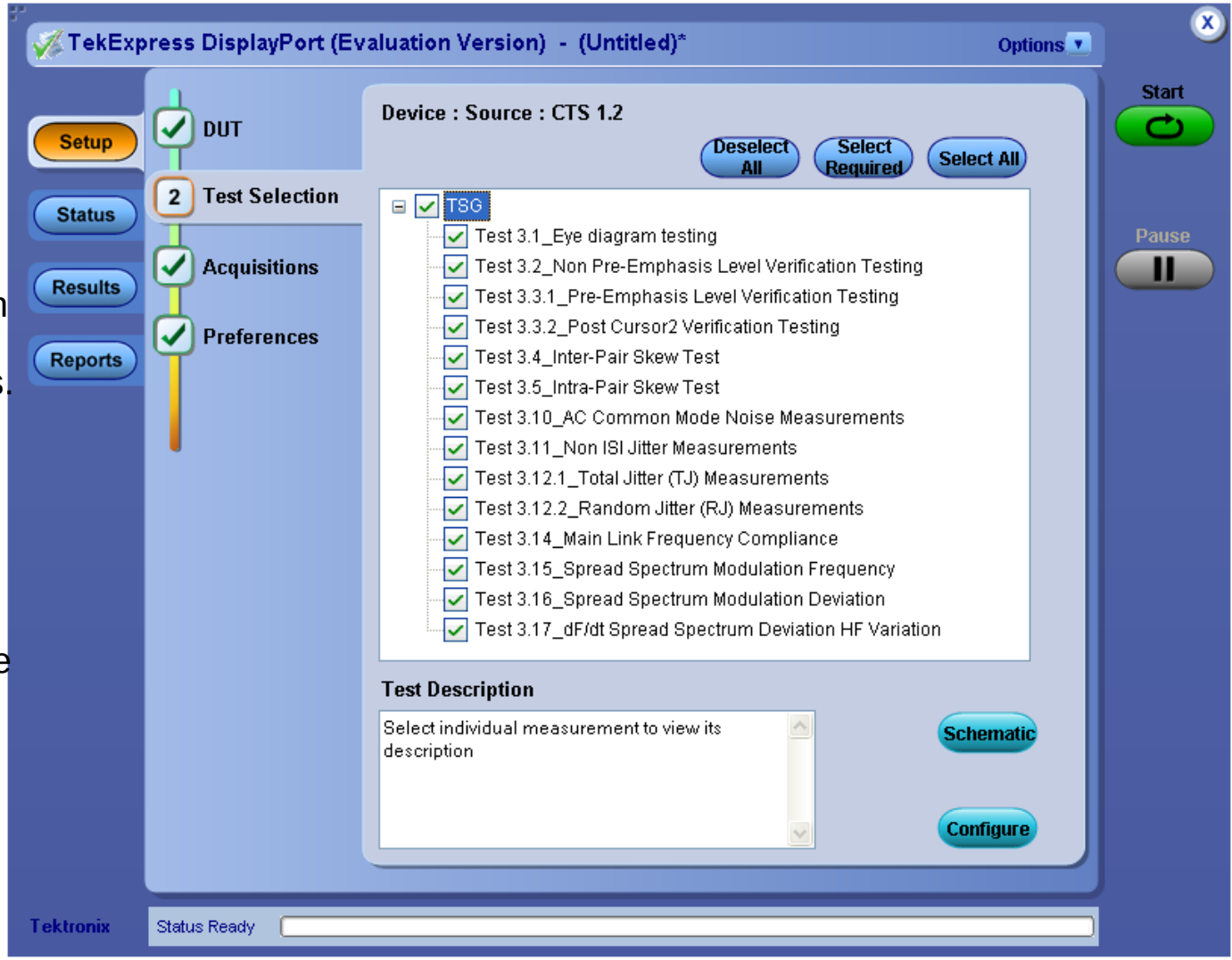
DP1.2 Test Selection

- **DP1.2**
  - Measurement selection is now provided as a function of the user specified test target capabilities.
  - If Post Curser 2 capabilities are not present in the DUT, the measurement list will not show them.
  - Configuration schematics and online help available for all measurements



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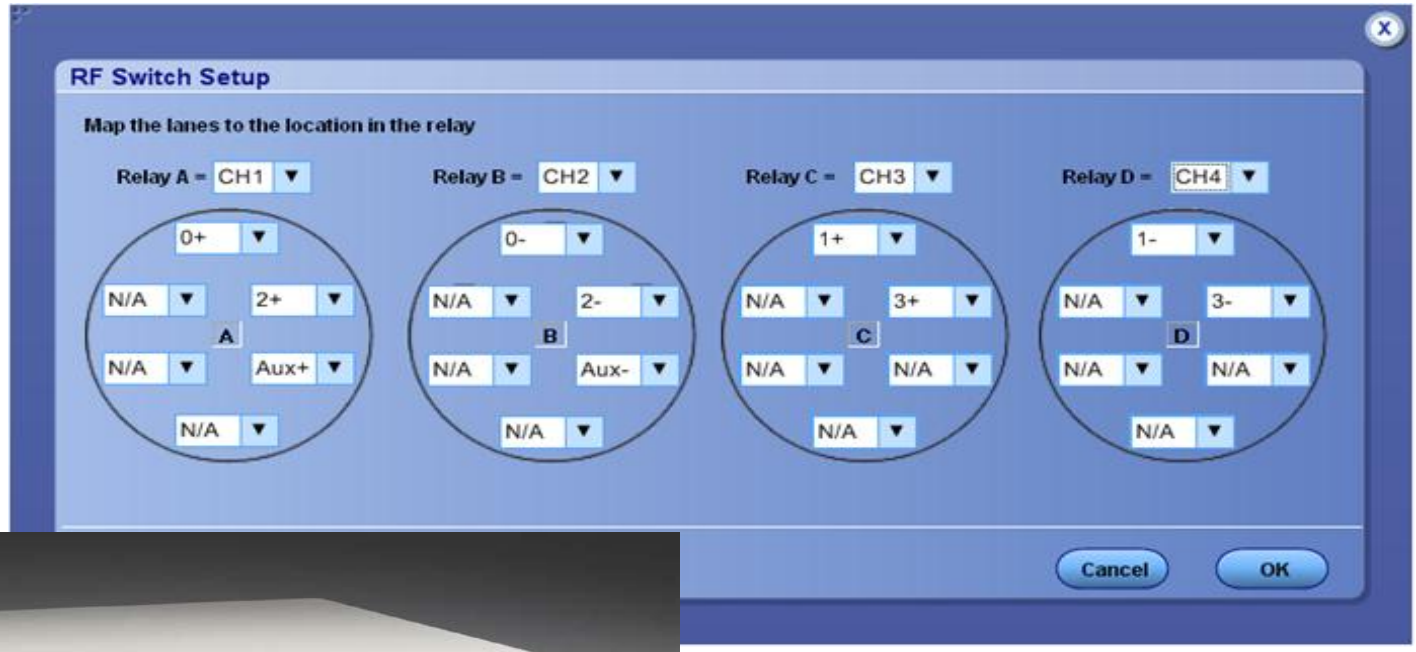
Keithley RF Switch Integration and Automation

- DisplayPort transmitter has both Differential tests and Single ended tests and with the integration of RF switch we have complete automated solution without any user intervention for switching between lanes with both single ended and differential tests in sequential automated passes.



- Keithley is now part of Tektronix.

DP1.2 Reporting

- **DP1.2**
  - Custom html reports which include user specified degrees of detail.
  - Reports and Session raw data are stored together allowing recalling a previous run and re-running the test (with different measurement configurations or limits) and re-generating a new report, **without the actual DUT present**.

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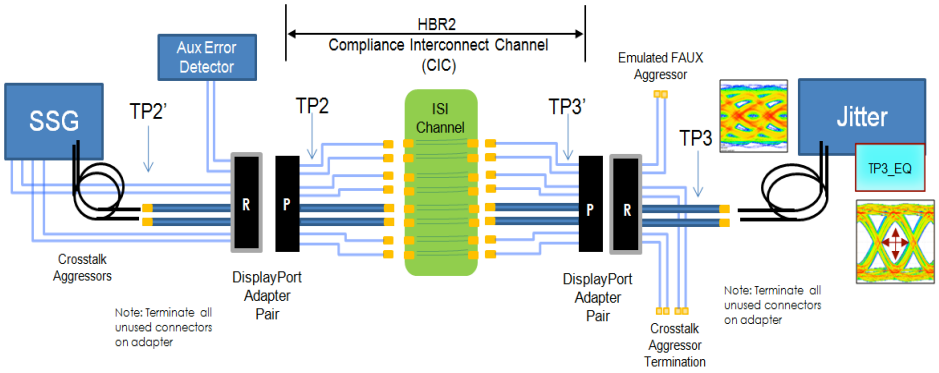
Challenges with Sink testing

- Transmitting pattern
  - Three different Complex patterns
- Stressor requirements
  - Rj, Sj, ISI Jitter stressors
  - Cross talk
  - Calibrated with CTLE equalizers
- Error detection
  - Need access to internal register



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Challenges to adding stressors

- Calibration process for all rates
  - Different test points for each type of calibration stress
  - Some stressor are calibrated with any other stressors

- What is different between calibrations for the different rates
  - HBR2 contain two SJ tones RBR/HBR single SJ tone.
  - HBR2/HBR Tj calibrated at TP3_EQ, RBR Tj calibrated at TP3
  - All three have different duration of testing

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR2 HBR RBR	2 MHz	10^{12}	1000	HBR2 =185s HBR=370s RBR=620s	0
HBR2 HBR RBR	10 MHz	10^{11}	100	HBR2=19s HBR=37s RBR=62s	+350ppm +350ppm +350ppm
HBR2 HBR RBR	20 MHz	10^{11}	100	HBR2=19s HBR=37s RBR=62s	0
HBR2 HBR	100 MHz	10^{11}	100	HBR2=19s HBR=37s	0

*To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds*

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What next for Tektronix Display Port tool sets

- Growing segment in Display Port is the Embedded Display Port(eDP)
  - Currently CTS specification is V1.3
  - Specification 1.4 is just release on Sep. 2012, but CTS spec is not ready yet
- Technology is used in Laptops and tables and more
  - eDP used to replace LVDS
  - Sources moving to eDP
  - Display moving at a slower pace
- Solution is a DPOJET plug in using the ADK tool set.
  - Available 4th Quarter
  - Support all eDP measurements
  - Printable report

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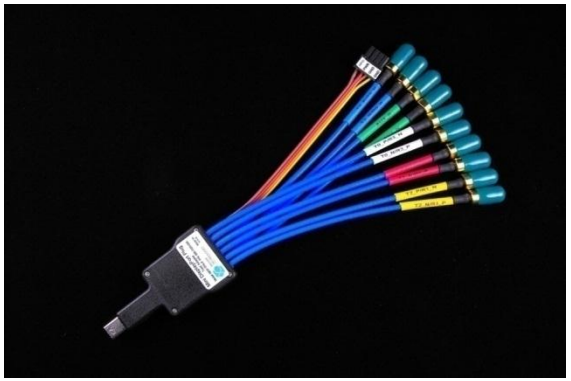
Complete Tektronix DisplayPort Instrument Portfolio for Source testing

- Equipment for Source testing
  - DSA71254C or higher for HBR2
  - DSA70804C or higher for HBR and RBR
  - P7313SMA for HBR2 (optional)
  - P7380SMA for HBR/RBR (optional)
  - VESA fixtures or Wilder technologies fixtures
  - DP Aux control (Required for Automated testing, optional for manual testing)
  - TekExpress DP12



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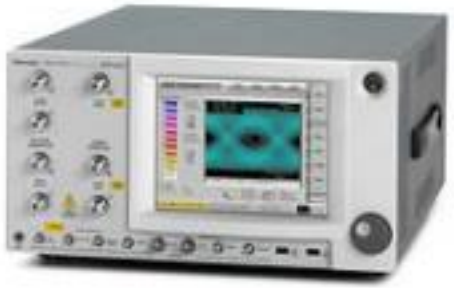
Complete Tektronix DisplayPort Instrument Portfolio for Reciever testing

- Equipment for Receiver testing
  - BSA85C
  - BSA12500ISI
  - 100ps TTC qty 2
  - 6 dB attenuators qty 2
  - DC block Qty 2
  - Assorted SMA Cables
  - One to Three way power splitters
  - VESA fixtures or Wilder technologies fixtures
  - DP Aux control (optional if the customer has a way to read the registers)
  - Tektronix Display Port 1.2 MOI



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