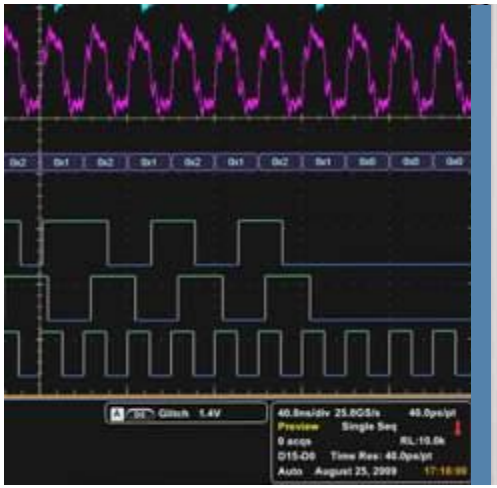
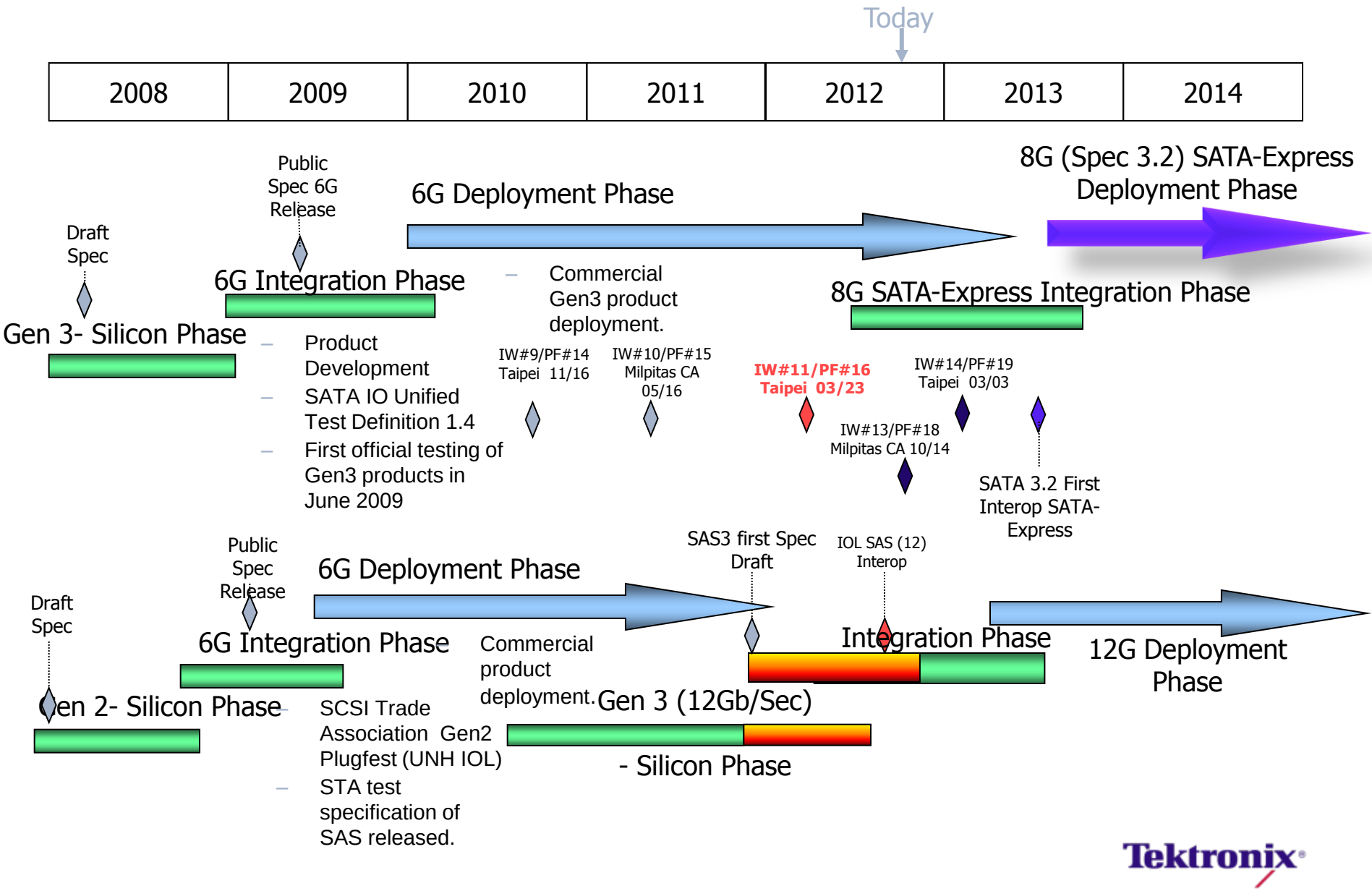
Storage PHY Test Solutions



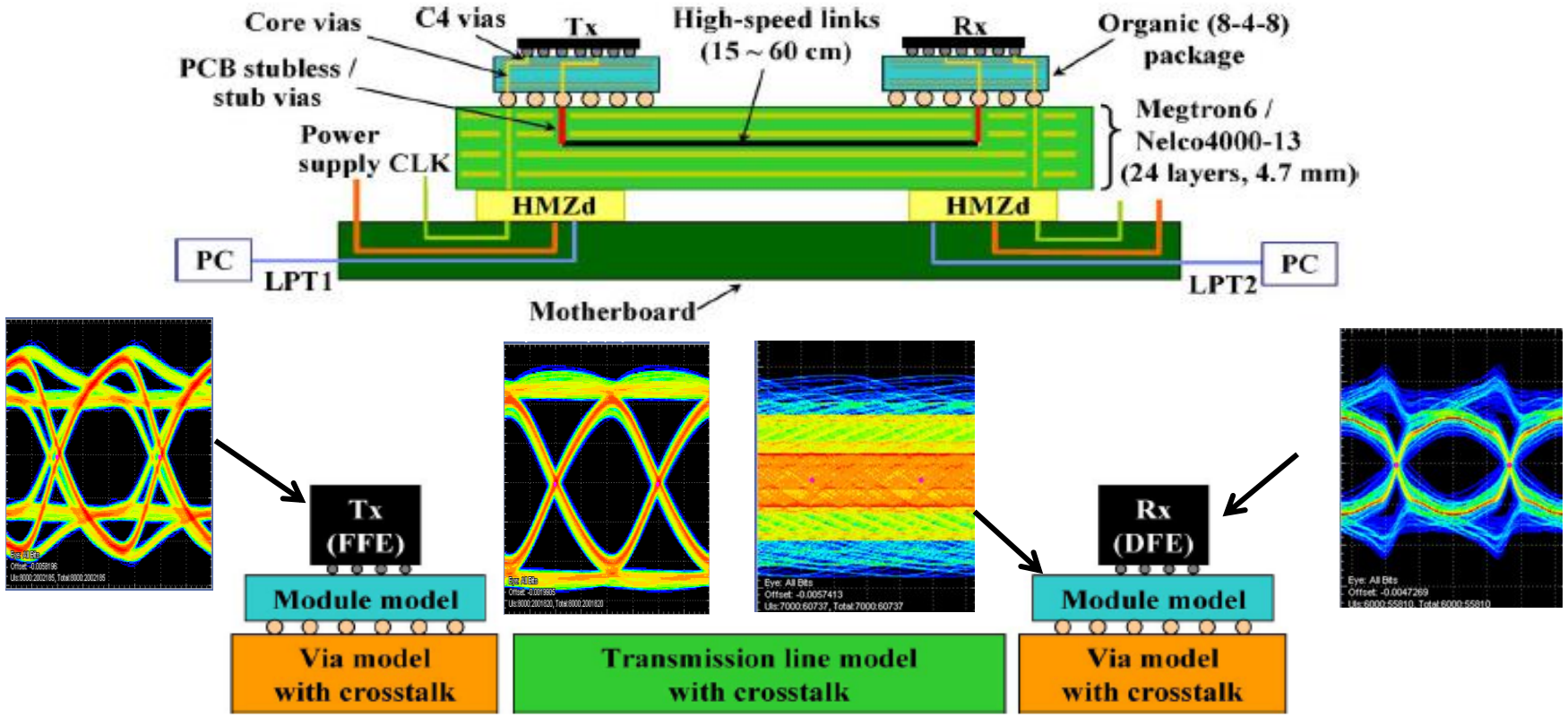
Tektronix®

Storage Timelines and Solutions Development



12G+ Design Problem:
1000mV, FFE, Crosstalk, DFE, 50mV

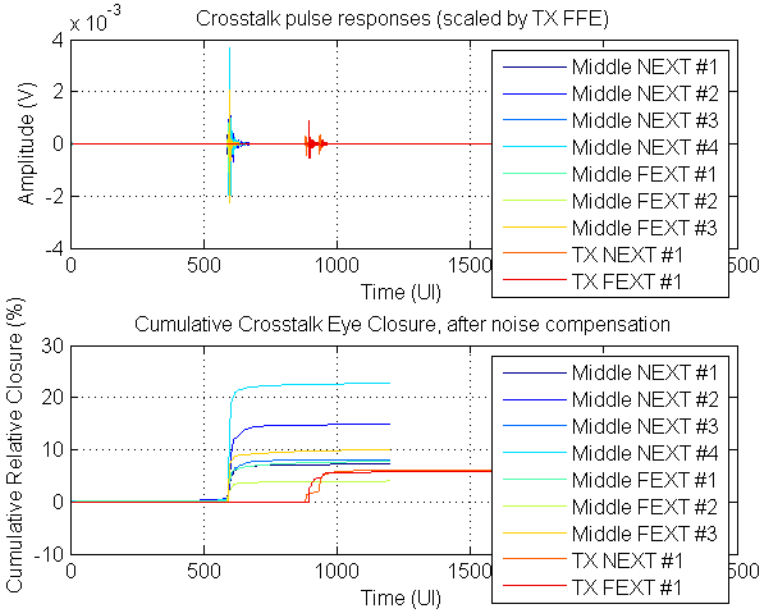
- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.



Tektronix

NEW Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization



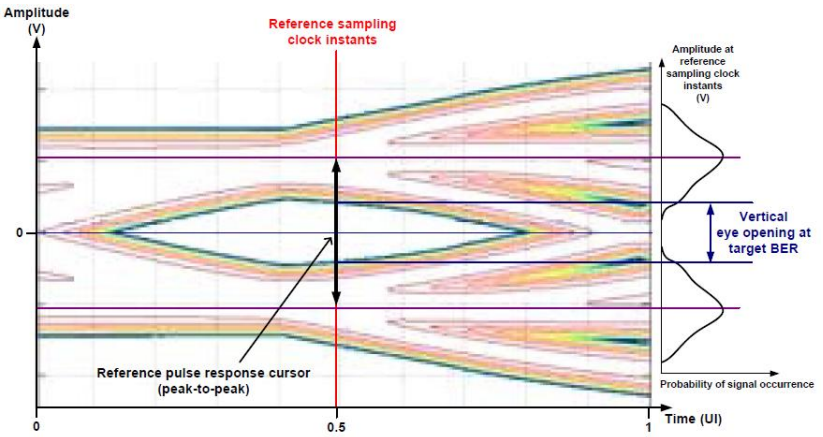


Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

Source: 12-244r3

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

Tektronix

SAS3_EYEOPENING provides 4 different metrics

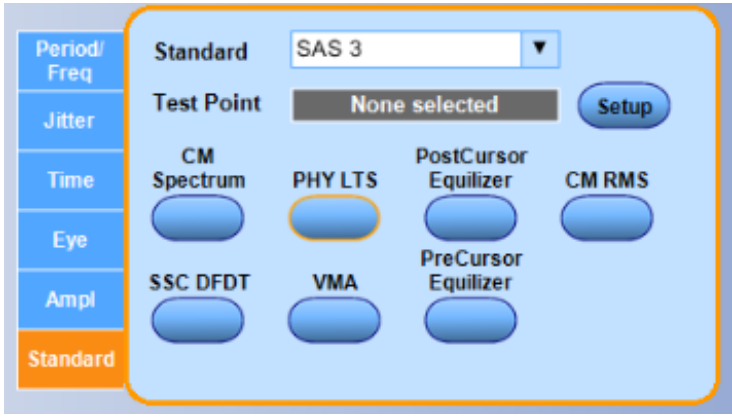
1. **Relative Vertical Eye Opening:** A direct indication of how much margin there is after equalization
   - Takes into account un-compensable ISI and crosstalk
   - ISI and crosstalk broken down in report
2. **Main Cursor Amplitude:** A direct indication of the amplitude after equalization
   - Assumes 800 mVppd max. TX launch amplitude, unless data is captured
3. **Maximal FFE correction**: A direct indication of how much FFE correction is required by the transmitter
   - Max(abs(Cpre/Ccntr,Cpost/Ccntr))
4. **Maximal DFE correction:** A direct indication of how much DFE correction is required by the receiver
   - Max(abs(DFE/Main))

Source: T10/11-234r1

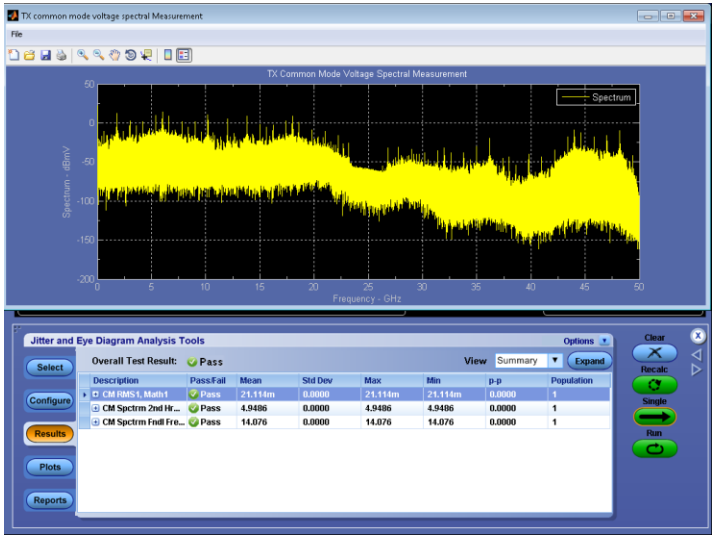
SAS-3 PHY Transmitter Solution – Option SAS3

Test0	Parameter	Conformance Min/Max
5.1.1	Maximum Noise During OOB IDLE	< 120 mV
5.1.2	OOB Burst Amplitude	> 240 mV
5.1.3	OOB Offset Delta	+/- 25 mV
5.1.4	OOB Common Mode Delta	+/- 50 mV
5.2.1	SSC Modulation Type	Center-, No- and Down-spreading
5.2.2	SSC Modulation Frequency	30 kHz < SSC_{freq} < 33 kHz
5.2.3	SSC Modulation Deviation	+/- 1000 ppm (center), 0 ppm (no spread) or +0/-1000 ppm (down)
5.2.4	SSC DFDT	850 ppm/µs
5.3.1	Physical Link Rate Long Term Stability	+/- 100 ppm
5.3.2	Common Mode RMS Voltage	< 30 mV
5.3.3	Common Mode Spectrum Mask Hits	Below Spectrum Limit Lines (0.1 to 6 GHz)
5.3.4	Peak to Peak Voltage	850 mV < Vpk-pk < 1200 mV
5.3.5	VMA	> 80 mV
5.3.6	Rise Time	> 20.8 ps
5.3.7	Fall Time	> 20.8 ps
5.3.8	Random Jitter	0.15 UI (12.5 ps)
5.3.9	Total Jitter	0.25 UI (20.8 ps)
5.3.10	SAS3_EYEOPENING	> 55 %
5.3.11	Pre Cursor Equalization	1 V/V < R_{pre} < 1.67 V/V
5.3.12	Post Cursor Equalization	1 V/V < R_{post} < 3.33 V/V

SAS3 12 Gb/s Tx Test Software



Common Mode Spectrum Measurement



Tektronix

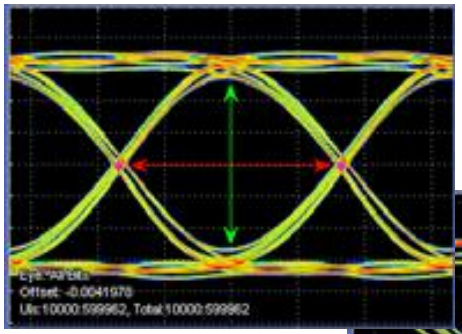
SAS-3 PHY Transmitter Solution – Option SAS3

- Automated transmitter validation for 12 Gb/s SAS physical layer specification
- Integrated SAS3_EYEOPENING measurement for accurate analysis of ISI and crosstalk effects and relative vertical eye opening after reference equalization
- Easily reconfigure existing measurements to create user-specified test parameters or test limits
- Multiple plots and measurement configurations provides a quick comparison of the same acquired data with different settings
- Simultaneous two lane testing of primary and secondary ports
- Detailed test reports with screenshots, setup details, and pass/fail limits

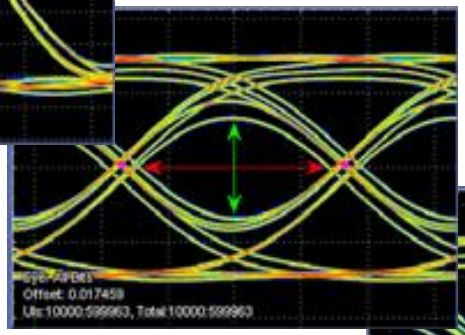
Beyond Compliance

- How much margin is there in my design?
- How many DFE/FFE taps are needed to meet the system budget?
- What is longest channel (cable/backplane) the system can tolerate?
- How does process/voltage/temperature affect device performance?

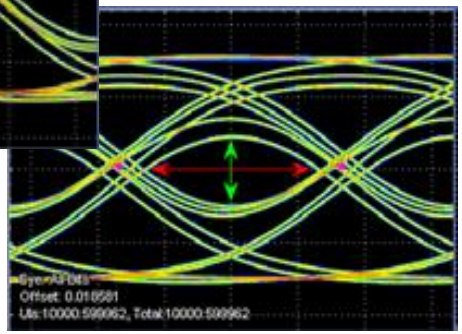
1m cable

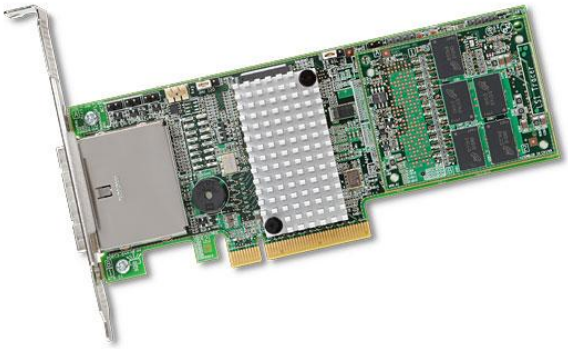


2m cable



3m cable

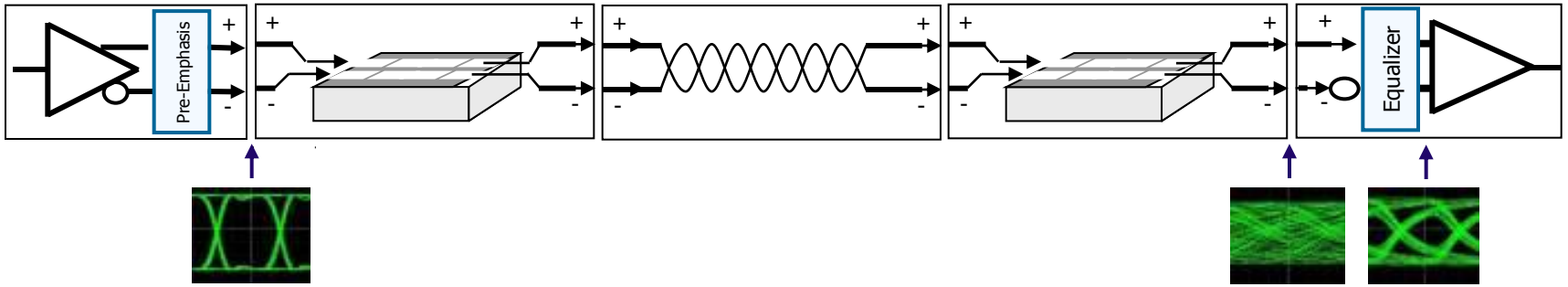




Tektronix®

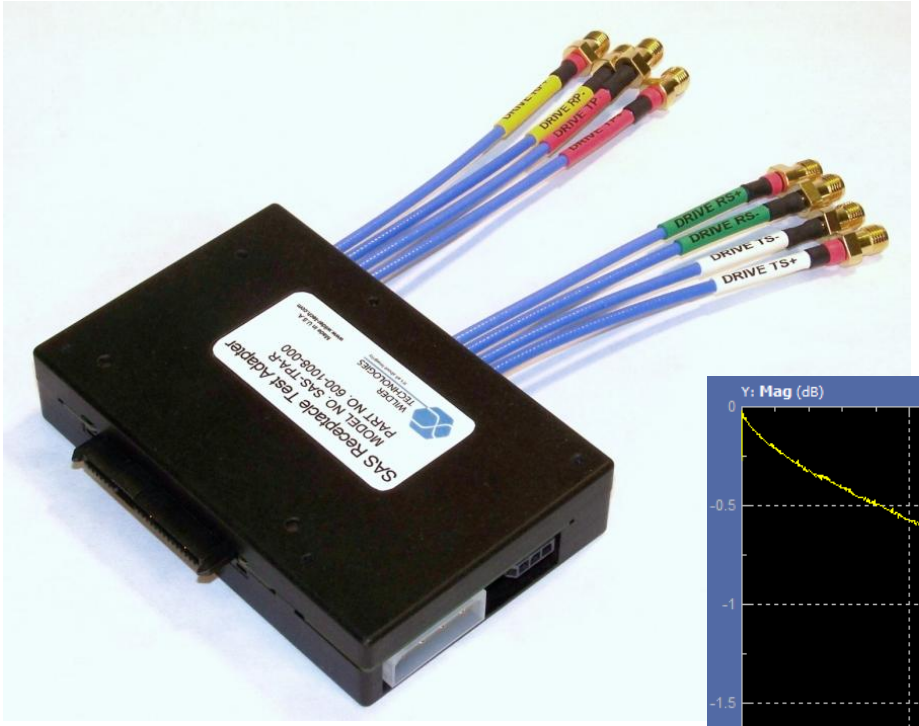
Flexible Link Analysis Tools – option SDLA

- DFE/FFE modeling
  - Reference equalizer vs. vendor-specific
  - Equalizer implementation for PHYs
- Enhanced de-embedding
  - Full four-port network characterization
- Channel emulation for margin analysis



Tektronix®

SAS Receptacle Test Adapter



Sdd21 (1x Thru) => -3dB@26 GHz

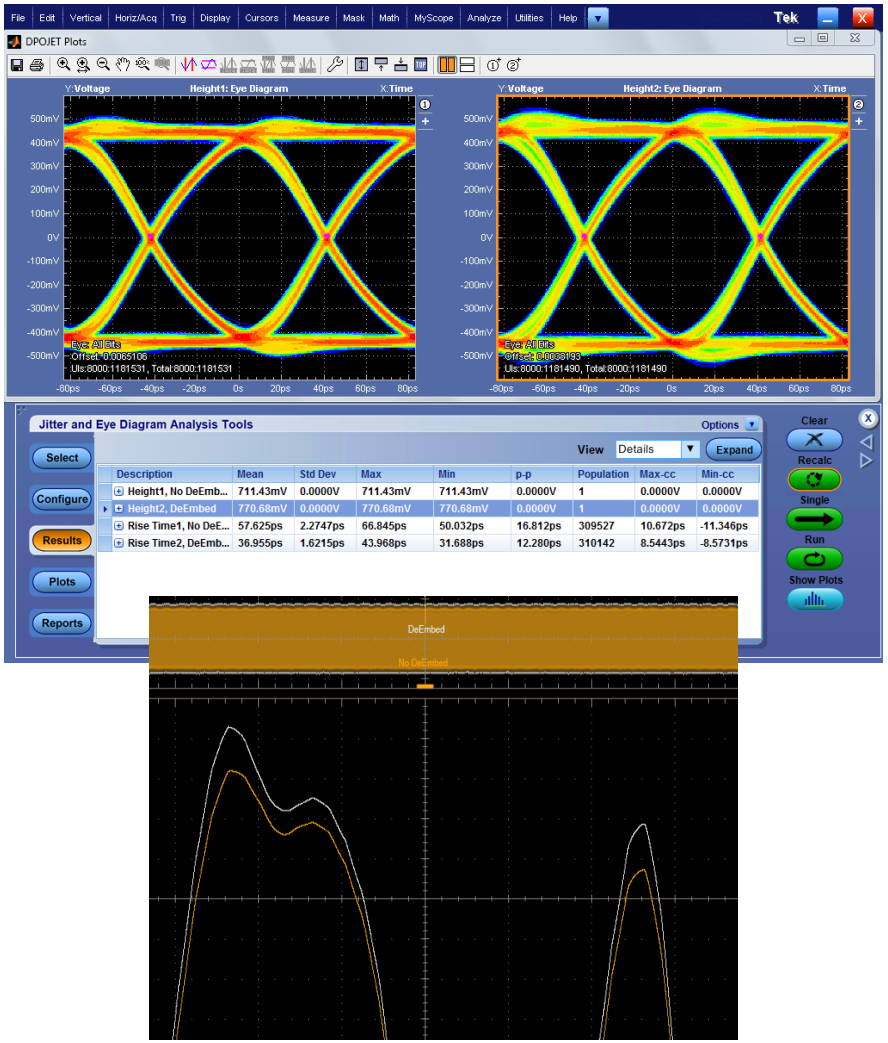
Tektronix®

Test Fixture De-embedding

- Why de-embed?
  - Tx measurements referenced to die (ET)
  - Improve margin with removal of fixture effects
- S-Parameters acquired from calibration fixture or model extraction
- Use inverse response to compensate for loss

	Before De-Embed	After De-Embed
Eye Height	711 mV	770 mV
Rise Time	57	37

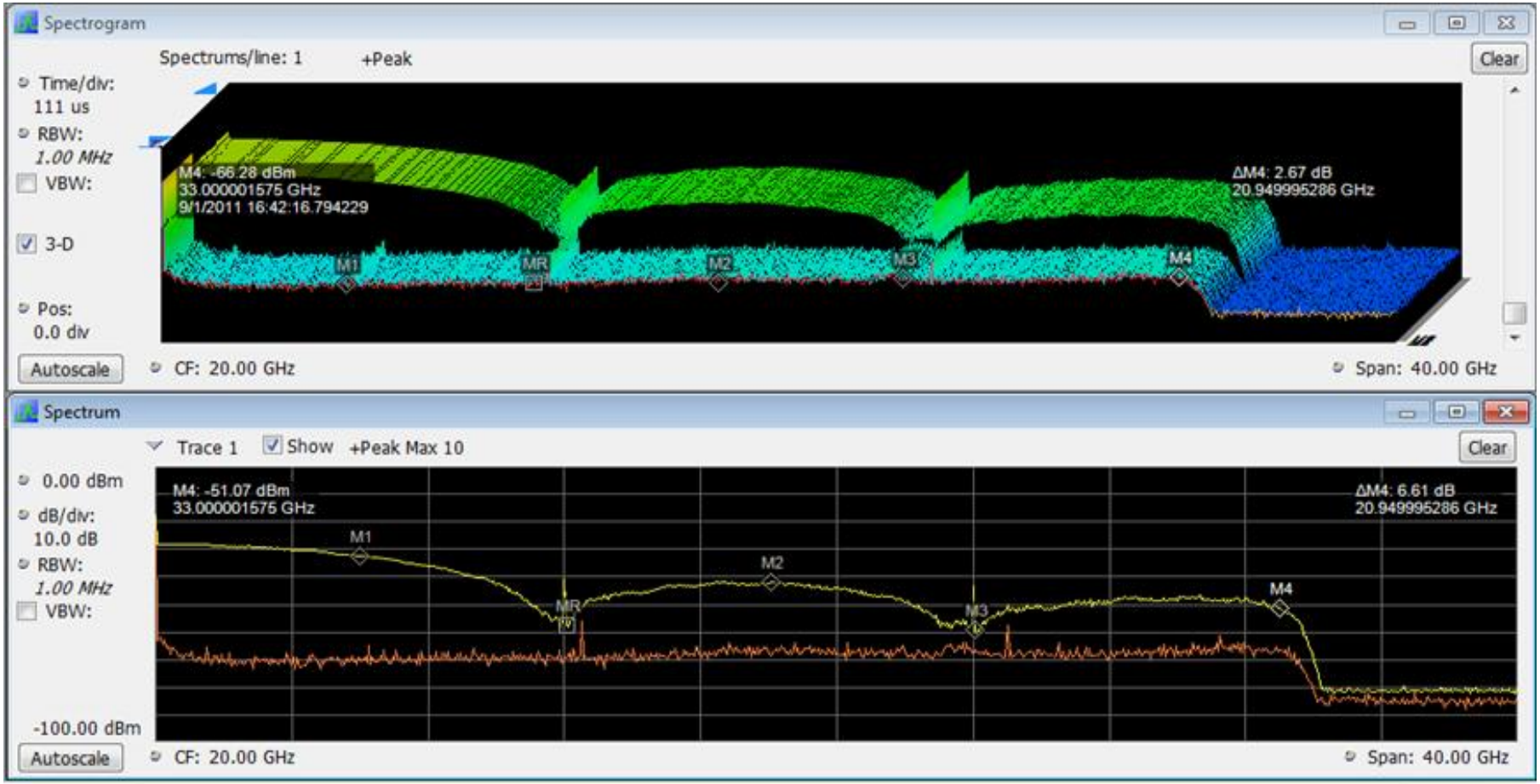
Before After



Tektronix

Bandwidth Considerations

SAS PRBS11 12G NRZ Power Spectrum



Marker Readout Table

Marker	Frequency	Δ Frequency	Δ Time	Spectrum	Δ Spectrum	Spectrogram	Δ Spectrogram
M2	18.050004939 GHz	5.99999865 GHz	---	-42.01 dBm	15.67 dB	-68.71 dBm	0.24 dB
M3	24.050003589 GHz	11.9999973 GHz	---	-59.20 dBm	-1.52 dB	-66.74 dBm	2.21 dB
M4	33.000001575 GHz	20.949995286 GHz	---	-51.07 dBm	6.61 dB	-66.28 dBm	2.67 dB

Tektronix

Recommended Equipment

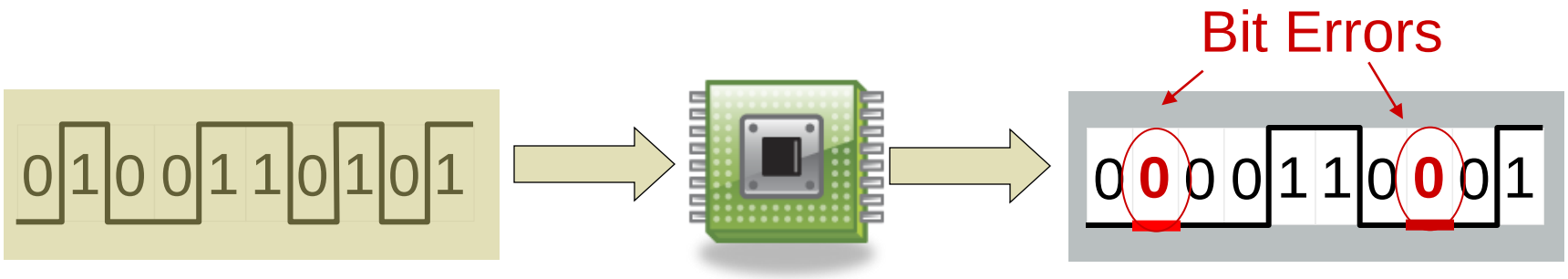
The following components are required for performing SAS12 Tx measurements

- DSA/DPO/MSO70K(C/D) Series Oscilloscope with Opt. 5XL or higher (Min. 20 GHz BW, ≥25 GHz recommended*)
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3
- Test Fixtures:
  - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
  - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
  - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase Matched Cable Set (qty: 2)

Tektronix®

SAS Implications for Receiver Testing

- System margins are decreasing, testing the transmitter only does not imply interoperability
- Receiver test requirements are expanding and will include testing with a crosstalk, ISI and Tx/Rx EQ
- Transmitter Equalization requires pre/post-cursor control
- Receiver Equalization is more sophisticated
  - Behavior equalizers (Continuous Time Linear and 5-tap Decision Feedback Equalization) must be used to compensate for channel loss
  - Transmitters must support back channel negotiation to auto-negotiate with Receivers to determine optimal equalization settings for testing



Tektronix

SAS 12 Gb/s Rx Test Setup

- Similar to SAS 6 Gb/s Rx configuration
- Rx calibration -> CJTPAT -> BER test
- Tektronix Method of Implementation (MOI) provides complete Rx Test procedure

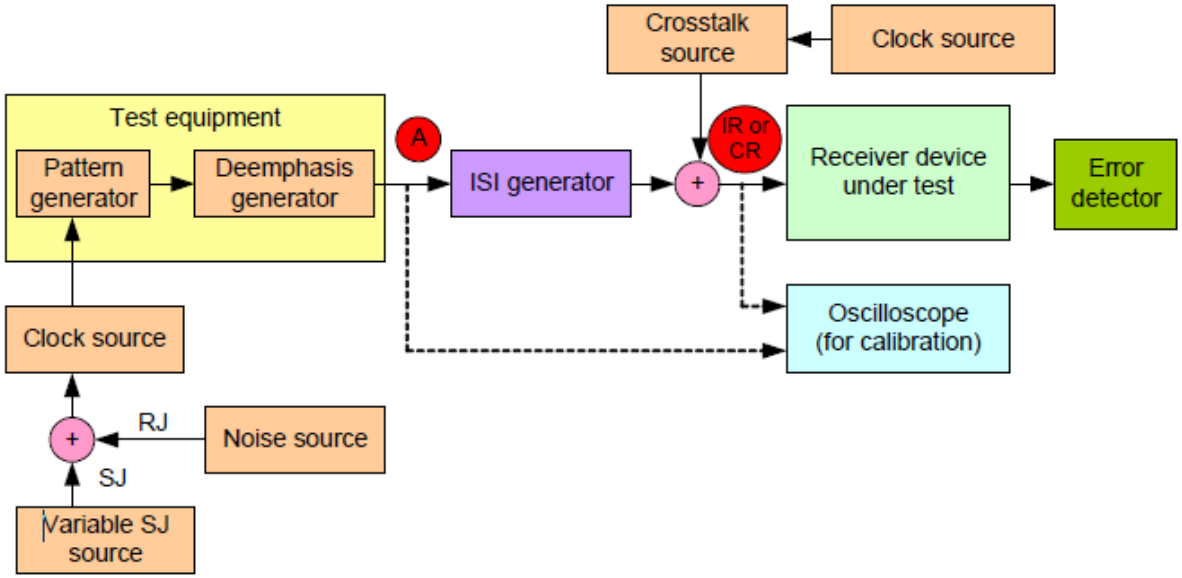
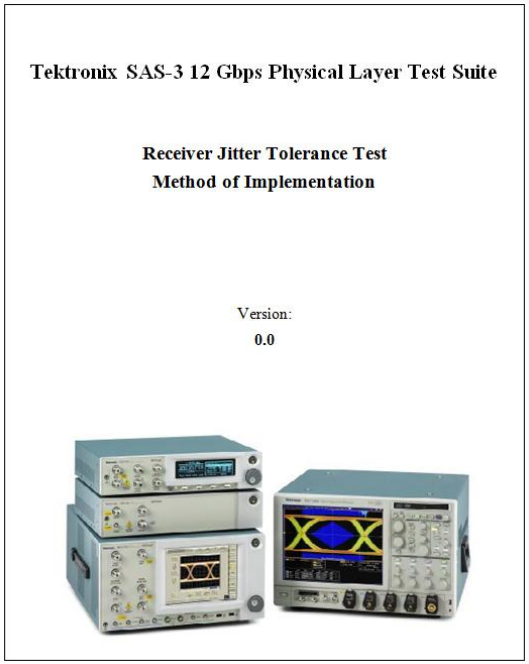


Figure 129 — Stressed receiver device jitter tolerance test block diagram

SAS 12 Gb/s Rx MOI



Source: sas3r03_18Oct2012

Tektronix

Receiver Test Made Easy with the BERTScope

Stressed Pattern Generator

1

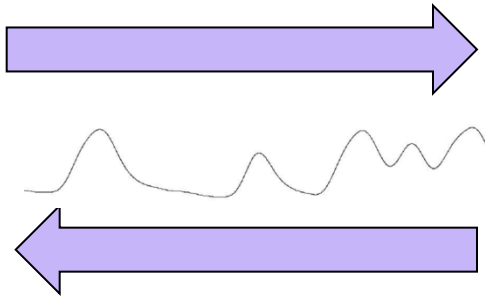
DPP provides pre-emphasis to emulate compliant transmitter

Error Detector

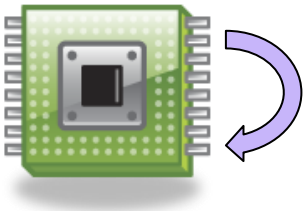
2

CR recovers a clock from the retransmitted data from the DUT

From Stressed Pattern Generator



loopback



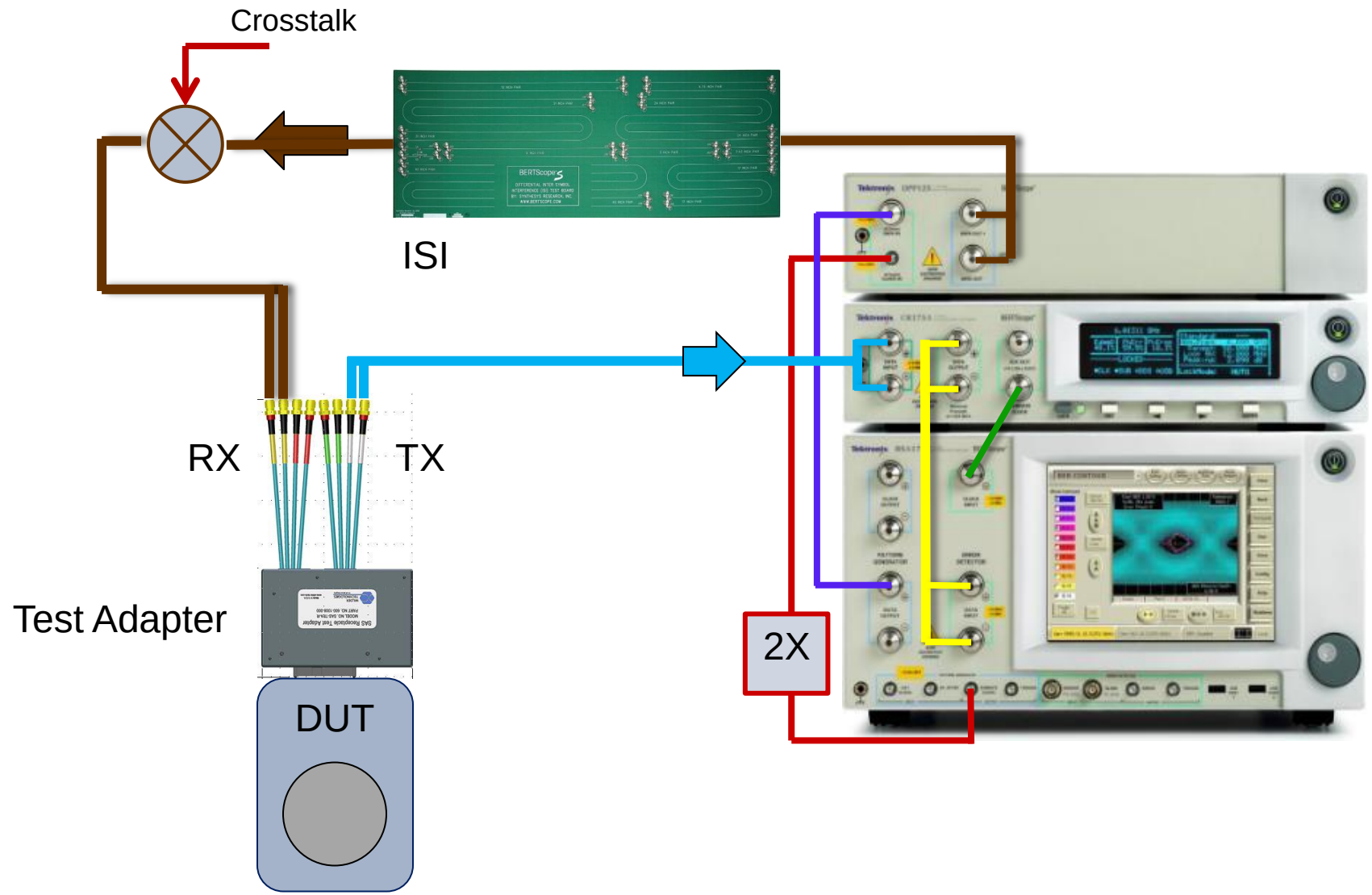
To Error Detector

Device Under Test (DUT)

Bits come back from DUT to **Error Detector** and compared to expected pattern for Bit Error Ratio (BER) measurement

Tektronix

SAS 12G Rx Equipment



Tektronix

Trained Link for Jitter Tolerance Test

- Complete Rx test exercises both CDR and Tx/Rx EQ capabilities
- Link optimization options
  - Iterate possible Tx/Rx EQ states and apply from 'best' optimized eye
  - Directly apply Preset based on typical configuration for worst case channel

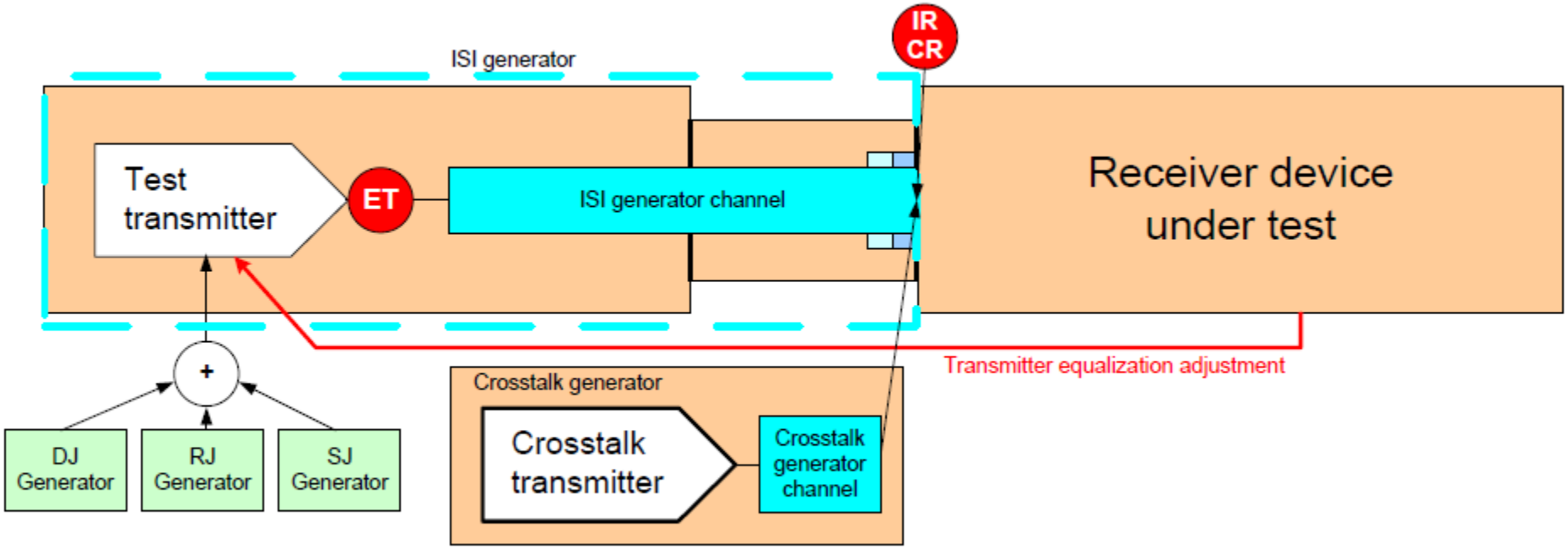


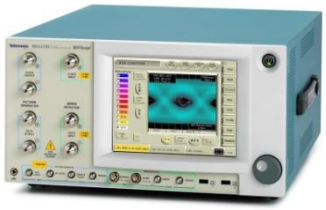
Figure Fh – Stressed receiver transmitter equalization adjustment

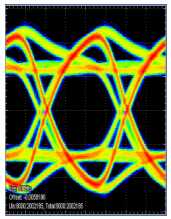
Tektronix

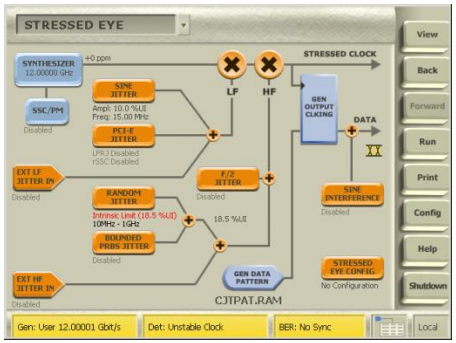
Stressed Pattern Calibration – Putting it Together

DPP125 Pre-Emphasis

1 Stressed Pattern Generator

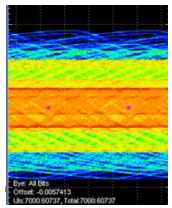




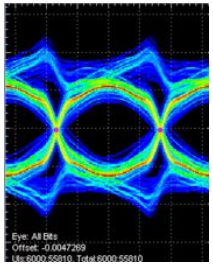


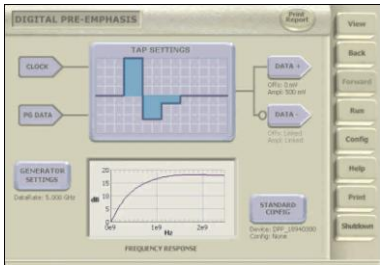
BERTScope

2 Channel (crosstalk/ISI)



DPO/DSA72504D





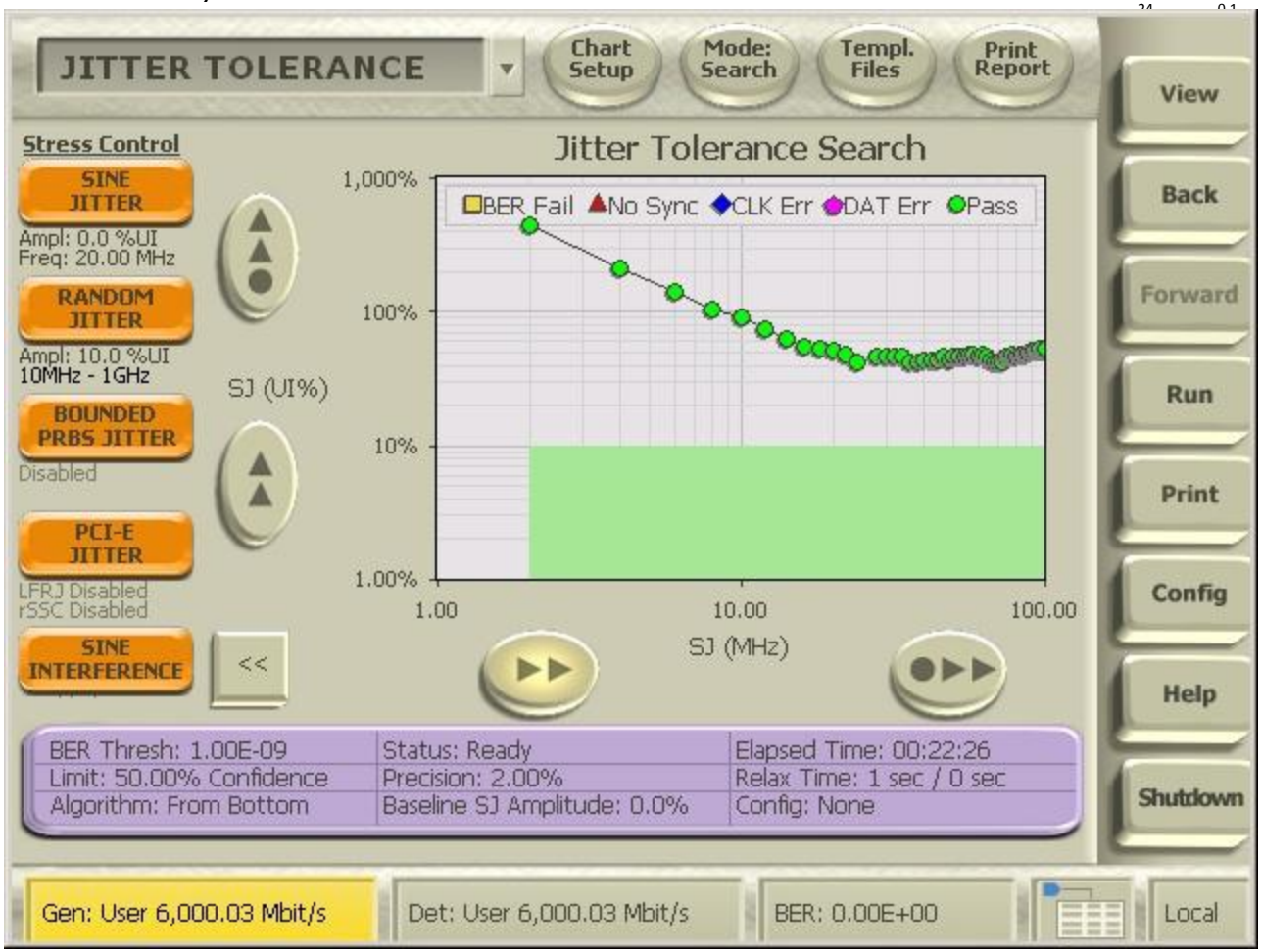
3 Link Training

Physical Setup → RJ/SJ Calibration → ISI Calibration → Crosstalk Calibration → Tx/Rx Training → RX Testing

Tektronix®

Rx Results (BERTScope)

- Automated Scan from 10 Hz to 100 MHz
- SAS-3 (6/12 Gb/s) spec requires 97, 240 kHz & 2.06, 3.6 and 15 MHz



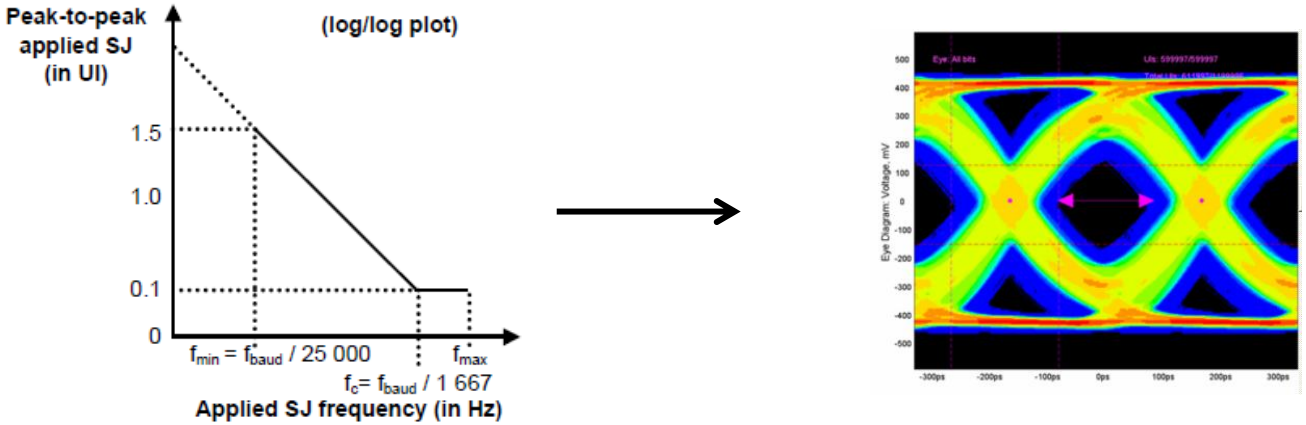
DATA

T-MHz	T-SJ	SJ	Bits	Errors	BER	Status	ThreshVX	DelayPS
	2	0.1	4.52	6E+08	0	0.00E+00 PASSED	0	267.531
	4	0.1	2.1	6E+08	0	0.00E+00 PASSED	0	266.451
	6	0.1	1.42	6E+08	0	0.00E+00 PASSED	0	266.451
	8	0.1	1.04	6E+08	0	0.00E+00 PASSED	-2	266.451
	10	0.1	0.9	6E+08	0	0.00E+00 PASSED	0	266.451
	12	0.1	0.74	6E+08	0	0.00E+00 PASSED	0	266.451
	14	0.1	0.64	6E+08	0	0.00E+00 PASSED	-2	266.451
	16	0.1	0.56	6E+08	0	0.00E+00 PASSED	0	266.451
	18	0.1	0.54	6E+08	0	0.00E+00 PASSED	1	266.451
	20	0.1	0.52	6E+08	0	0.00E+00 PASSED	0	266.451
	22	0.1	0.48	6E+08	0	0.00E+00 PASSED	0	266.451
		0.1	0.42	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	267.531
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	267.531
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
			0.48	6E+08	0	0.00E+00 PASSED	1	267.531
			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.44	6E+08	0	0.00E+00 PASSED	-1	267.531
			0.42	6E+08	0	0.00E+00 PASSED	-3	267.531
			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
			0.46	6E+08	0	0.00E+00 PASSED	-1	267.531
			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
			0.48	6E+08	0	0.00E+00 PASSED	-2	267.531
			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
			0.5	6E+08	0	0.00E+00 PASSED	0	266.451
			0.52	6E+08	0	0.00E+00 PASSED	-2	267.531
			0.52	6E+08	0	0.00E+00 PASSED	0	266.451
			0.52	6E+08	0	0.00E+00 PASSED	-1	267.531
			0.54	6E+08	0	0.00E+00 PASSED	0	267.531
			0.52	6E+08	0	0.00E+00 PASSED	0	266.451
			0.54	6E+08	0	0.00E+00 LIMIT REACHED	0	266.451

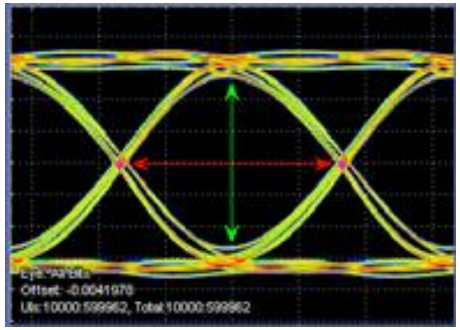
Tektronix

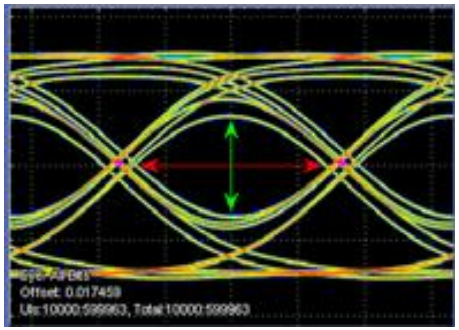
Need for Precise ISI generation

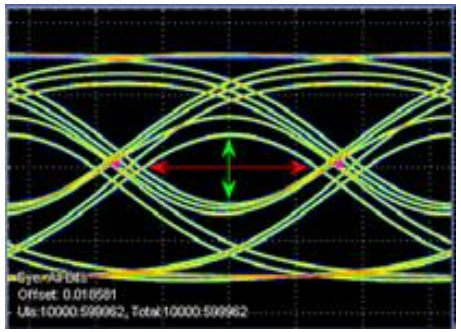
- Device margin testing against variable magnitude sinusoidal test vectors has been foundation of receiver characterization.



- Current PHY designs use sophisticated CTLE and/or DFE architectures, where tolerance and margining against DDJ is more important than SJ.





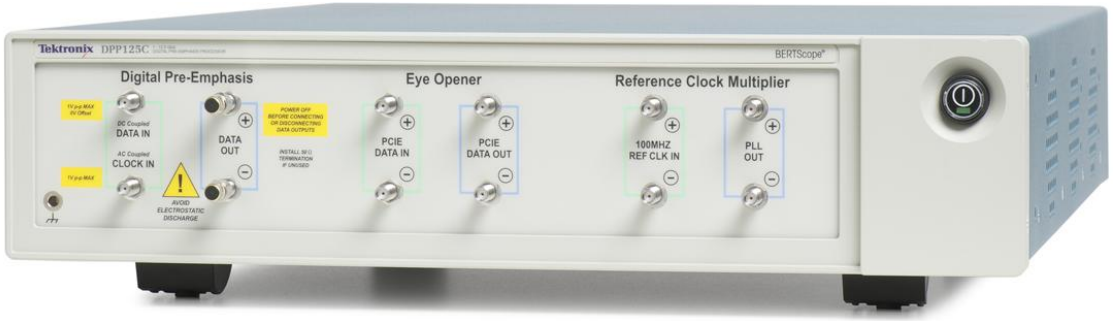


Tektronix®

NEW SAS 12 Gb/s Receiver Test Solutions

DPP125C Digital Pre-emphasis Processor

- Integrated eye opener functionality for testing DUTs with long channels
- Integrated clock doubler that enables full rate stress for 12 Gb/s

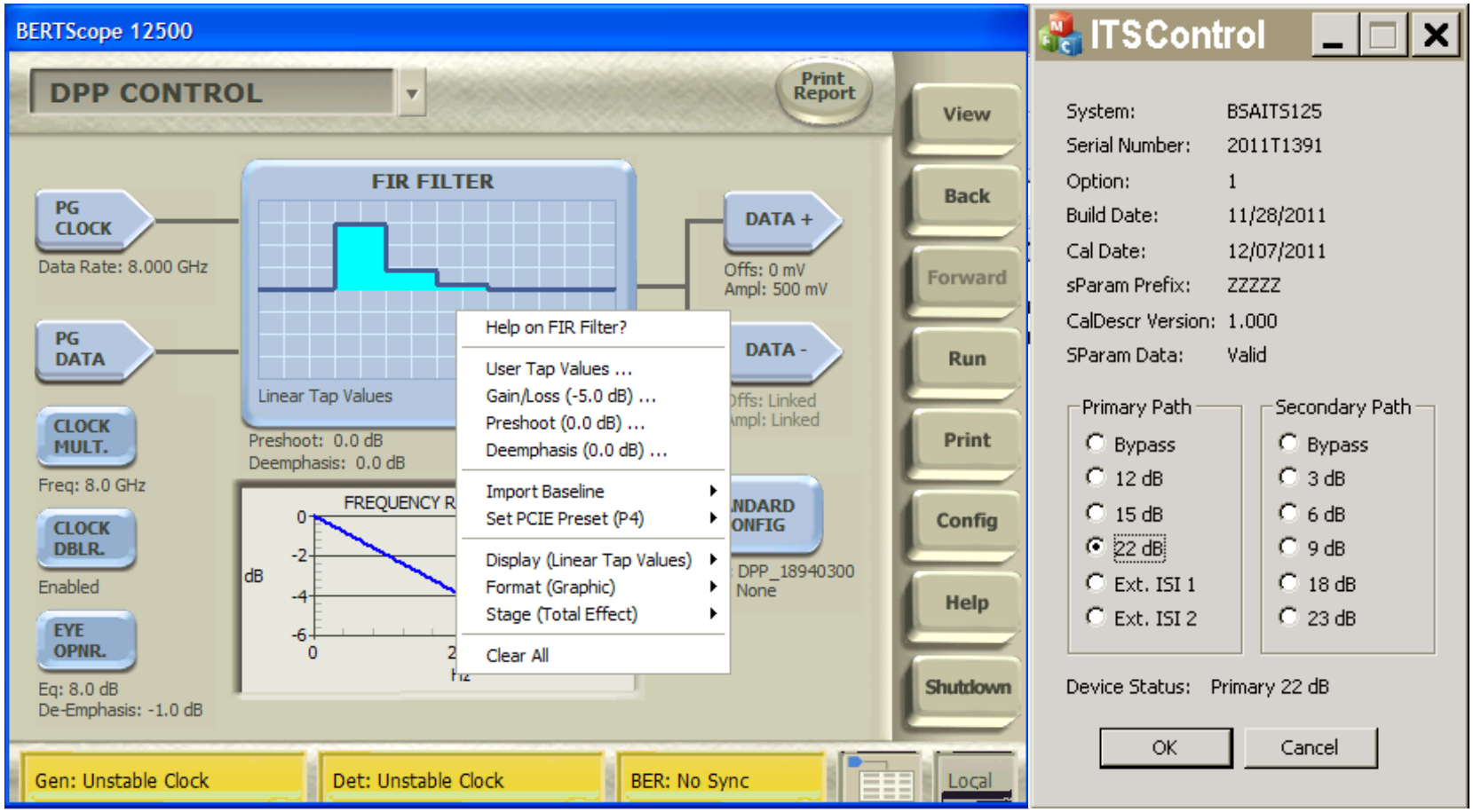


BSAITS125 Interference Test Set

- Programmable variable ISI for automated testing and precision setting
- Integrated CM and DM interference combiner

Tektronix

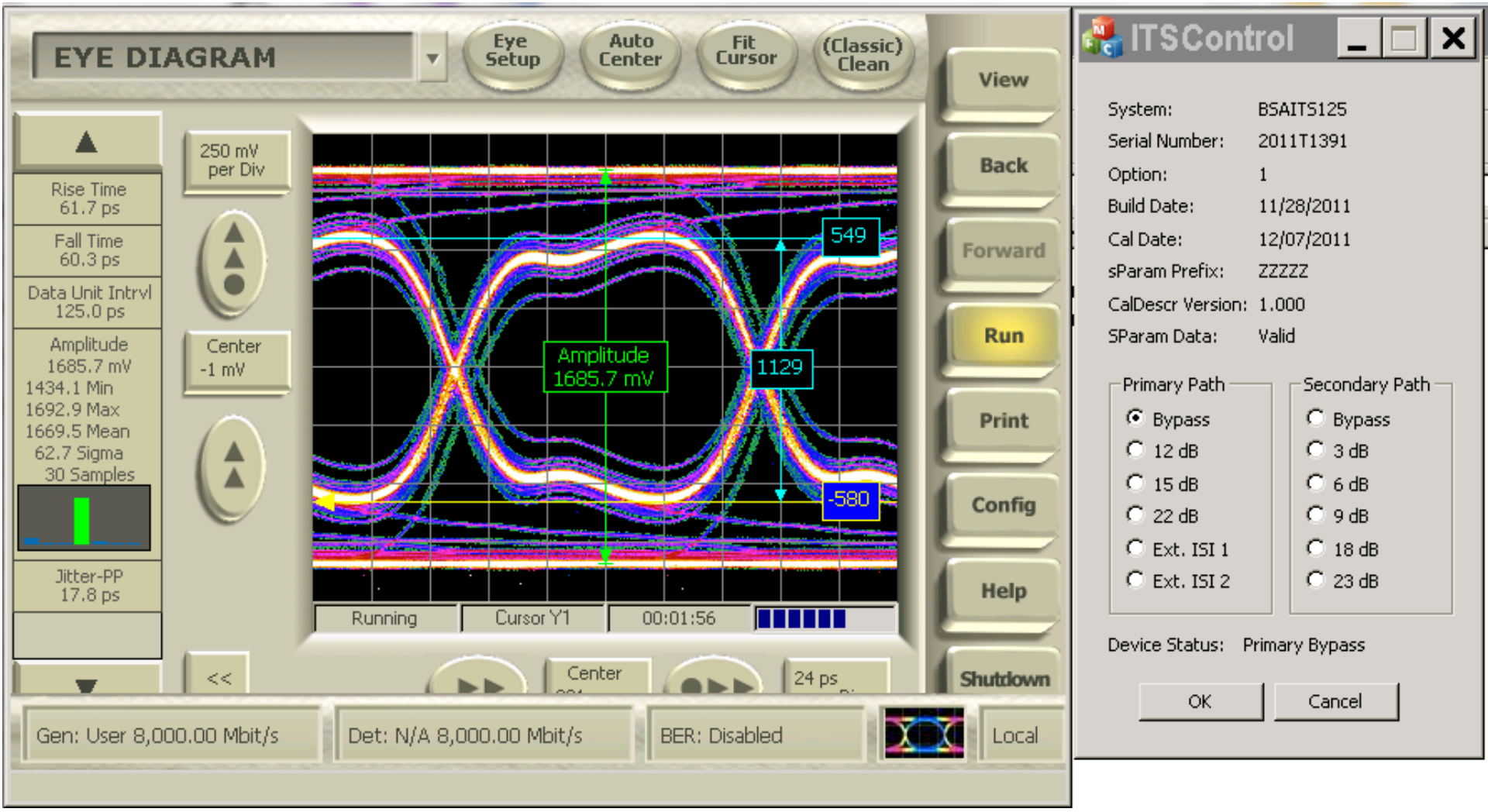
Data Dependent Jitter Variability with BSAITS



BSAITS automates selection of fixed ISI traces with fine (mdB) controls with the DPP FIR filter for a continuously variable high precision ISI source.

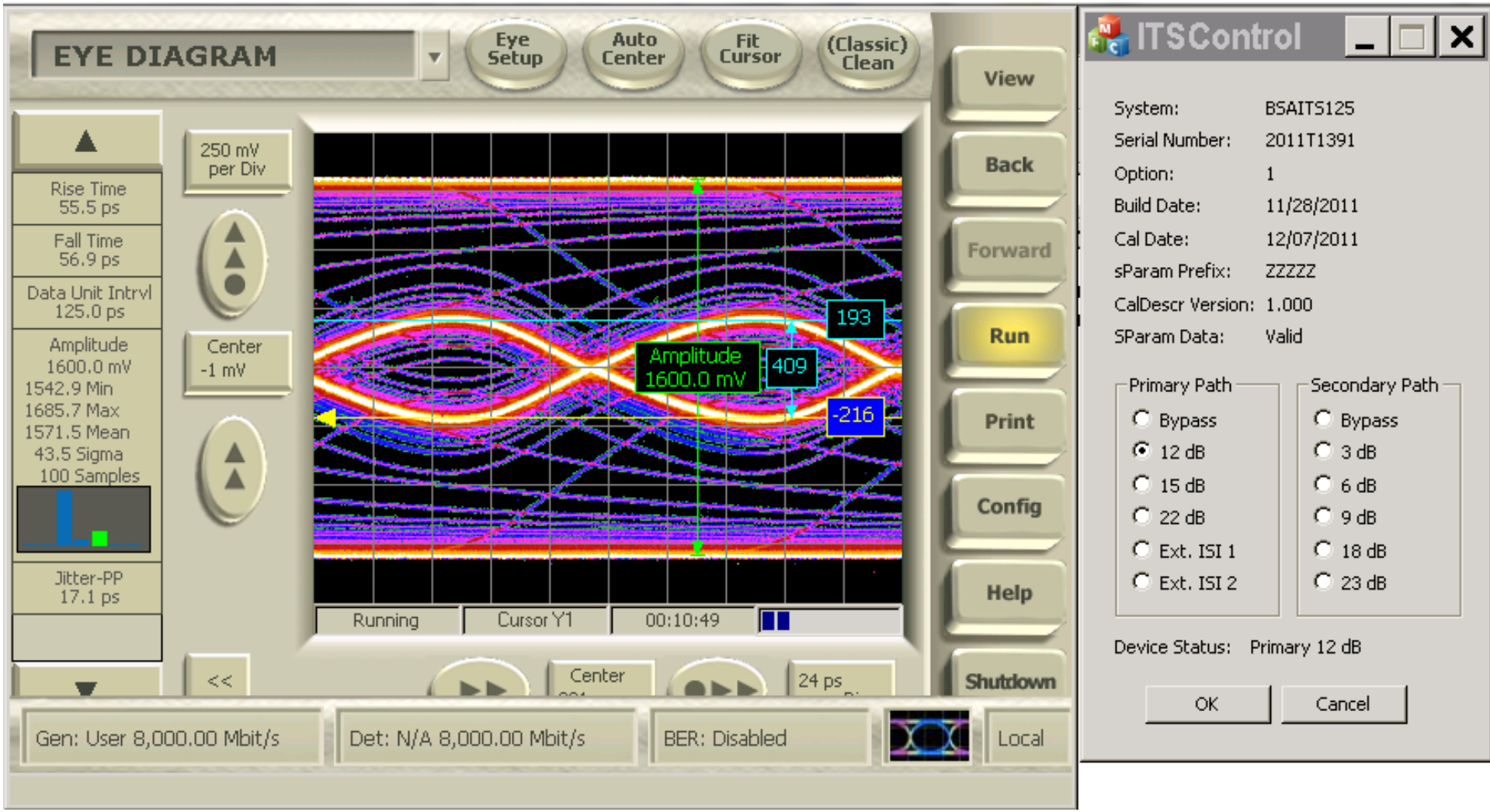
Tektronix

BSAITS Bypass mode



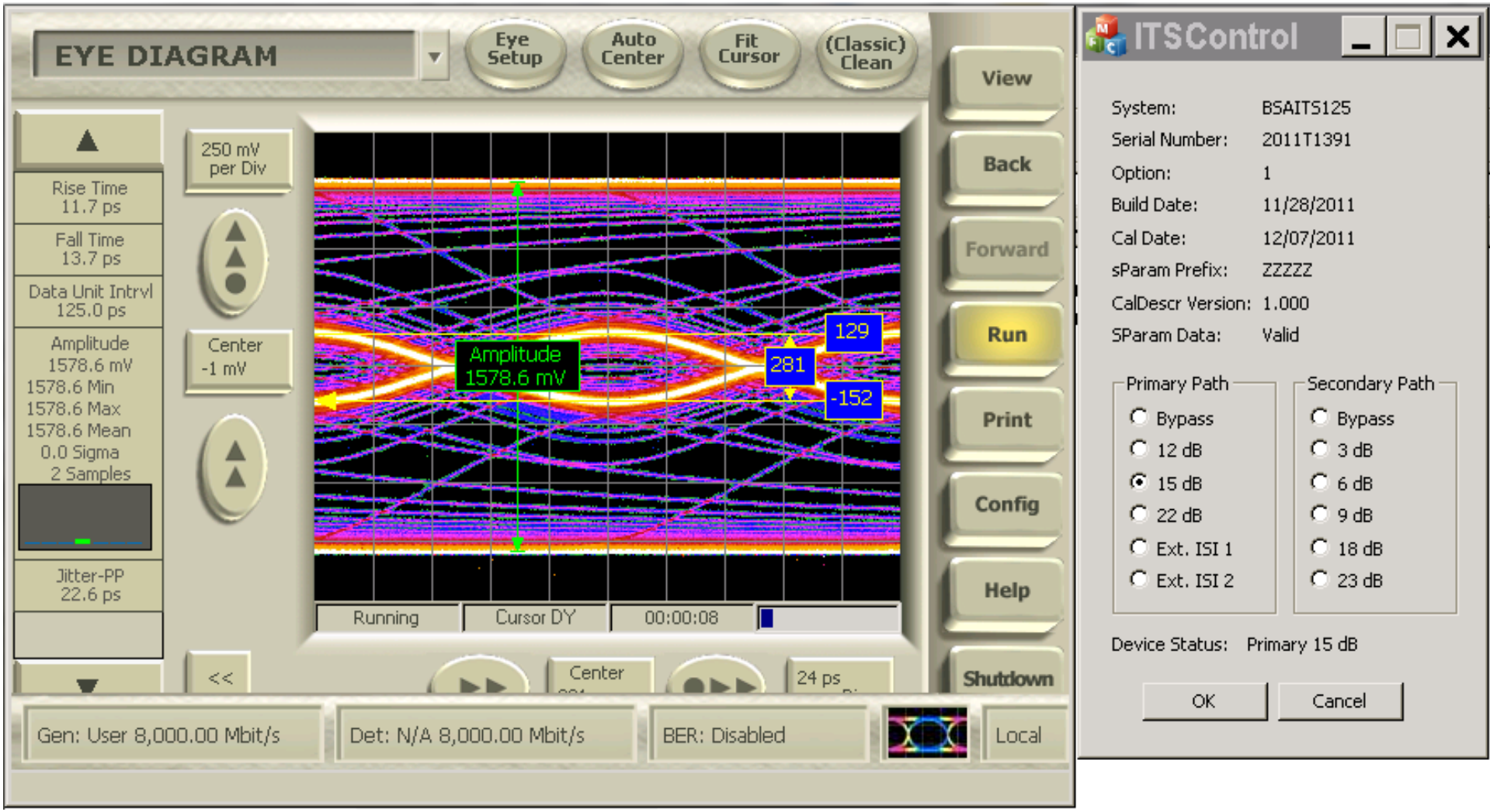
Tektronix®

BSAITS 12dB mode



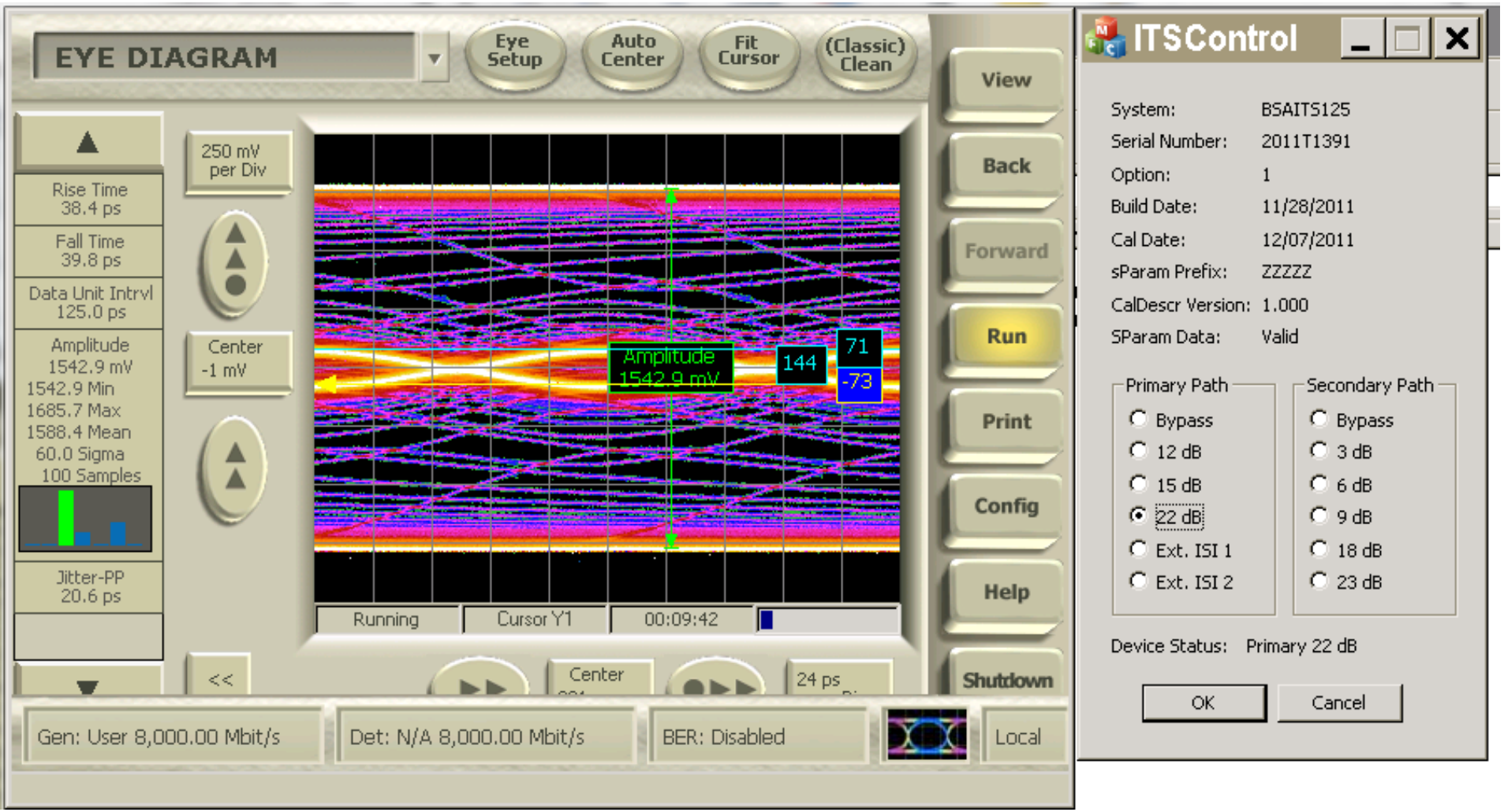
Tektronix

BSAITS 15dB mode



Tektronix

BSAITS 22dB mode



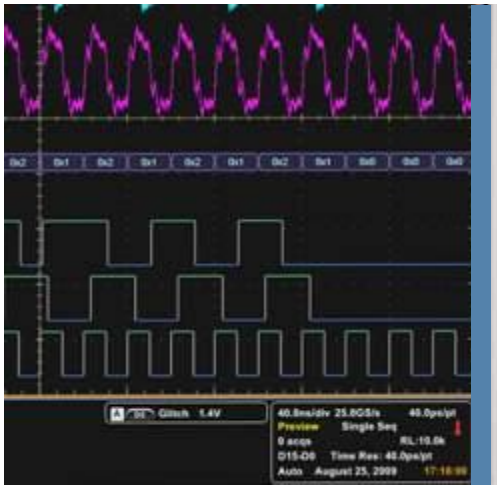
Tektronix

Complete Tektronix SAS Testing

Receiver Tests/Active Cable Tests **RSG/RMT**- Receiver Silicon, Active cable characterization and Compliance testing capability to 26 Gb/s	**BSA125C** with option **JMAP, STR** & **SF** **DPP125C**, **CR125A** and **BSAITS** for Digital Emphasis, Clock recovery and ISI generation	
Channel Tests **ICR**: Insertion Loss/Crosstalk analysis. **Rx/Tx** - Device and Host electrical channel performance, Crosstalk, Impedance and return loss **Passive Cable Tests** Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8300** Sampling Oscilloscope **80E10** TDR Sampling Module for DSA8300 Sampling Oscilloscope **80SICON** S-Parameter Analysis software	
PHY, TSG, and OOB Tests PHY – Signal timing stability and SSC analysis. TSG – Transmitter AC parametric, Jitter, Amplitude. OOB- Out Of Band signal validation	**DSA72504D** Real-Time Oscilloscope **Option SAS3** 12 Gbps Tx Test Software **TekExpress** SAS 6 Gbps Physical Layer Test software **DPOJET** Jitter/Eye Analysis software	

Tektronix®

Serial ATA PHY Validation

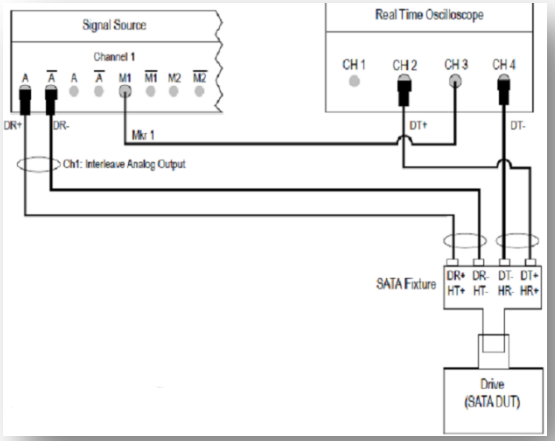


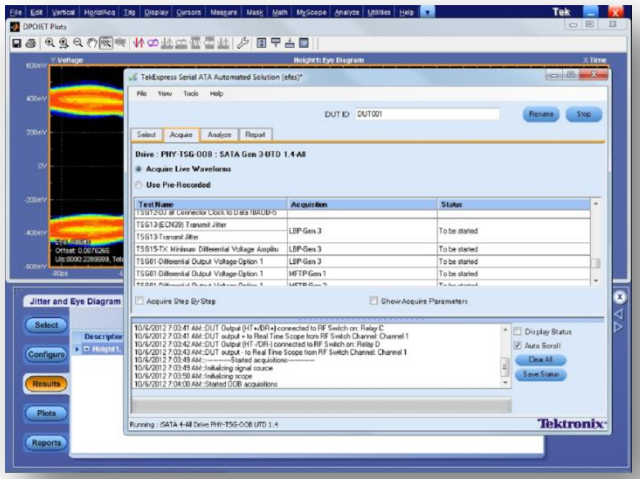
Basics of Serial ATA PHY Testing

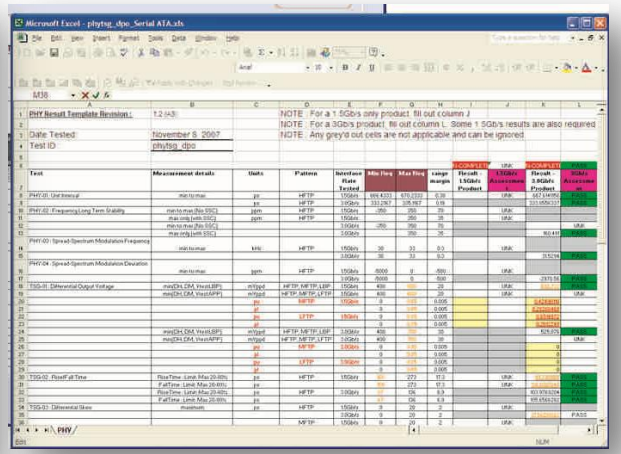
Startup
- Configure
- Calibrate

Validate
- Acquire
- Analyze

Report
- Save data
- Scorecard





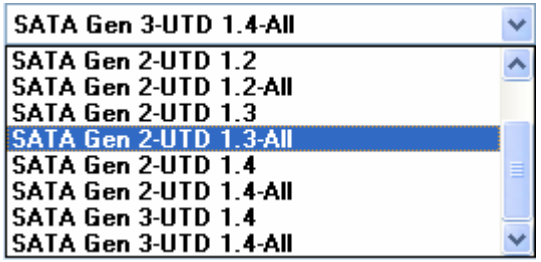


Tektronix®

SATA UTD 1.4 TSG/PHY/OOB Measurements

Drive : PHY-TSG-OOB SATA Gen 3-UTD 1.4-All

Select	Test Name
☑	Informative-df/dt Measurement
☑	Informative-Eye diagrams
☑	OOB01-OOB Signal Detection Threshold
☑	OOB02-UI During OOB Signaling
☑	OOB03-COMINIT_RESET and COMWAKE Transmit Burst Length
☑	OOB04-COMINIT_RESET Transmit Gap Length
☑	OOB05-COMWAKE Transmit Gap Length
☑	OOB06-COMWAKE Gap Detection Windows
☑	OOB07-COMINIT Gap Detection Windows
☑	PHY01-Unit Interval
☑	PHY02-Frequency Long Term Stability
☑	PHY03-Spread-Spectrum Modulation Frequency
☑	PHY04-Spread-Spectrum Modulation Deviation
☑	TSG01-Differential Output Voltage-Option 1
☑	TSG01-Differential Output Voltage-Option 2
☑	TSG02-Rise-Fall Time
☑	TSG03-Differential Skew
☑	TSG04-AC Common Mode Voltage
☑	TSG05-Rise-Fall Imbalance
☑	TSG06-Amplitude Imbalance
☑	TSG09-TJ at Connector, Clock to Data, fBAUD-500
☑	TSG10-DJ at Connector, Clock to Data, fBAUD-500
☑	TSG11-TJ at Connector, Clock to Data, fBAUD-500
☑	TSG12-DJ at Connector, Clock to Data, fBAUD-500
☑	TSG13-Transmit Jitter
☑	TSG14-TX Maximum Differential Voltage Amplitude
☑	TSG15-TX Minimum Differential Voltage Amplitude
☑	TSG16-Tx AC Common Mode Voltage



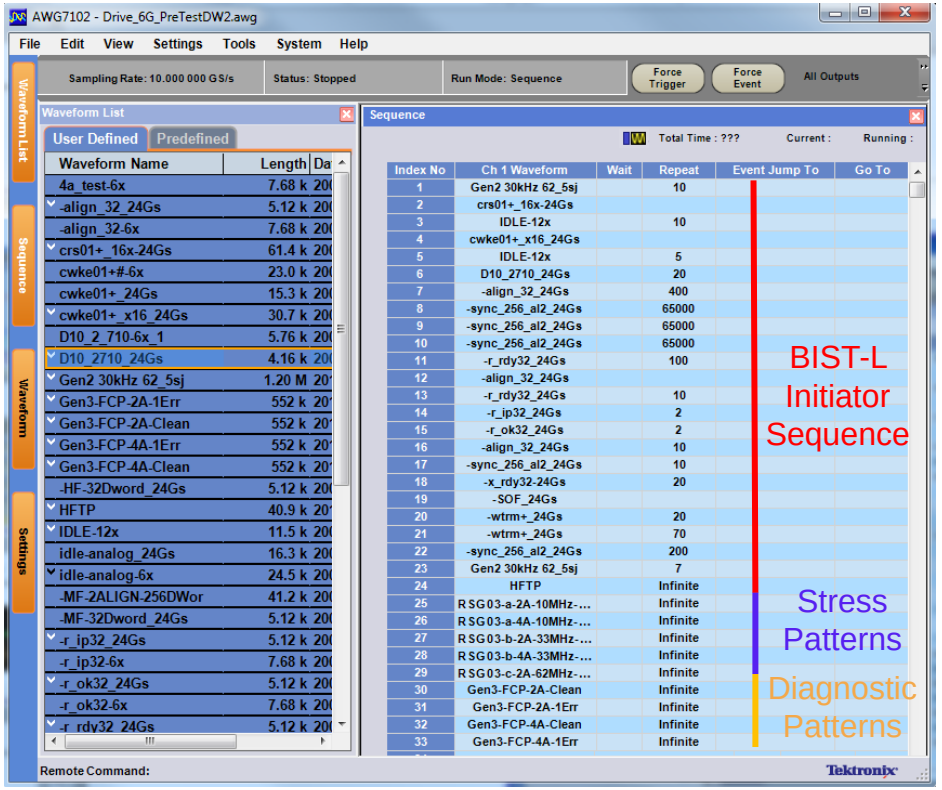
- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - New OOB patterns
  - TSG ECN additions

Tektronix

AWG Device State Control

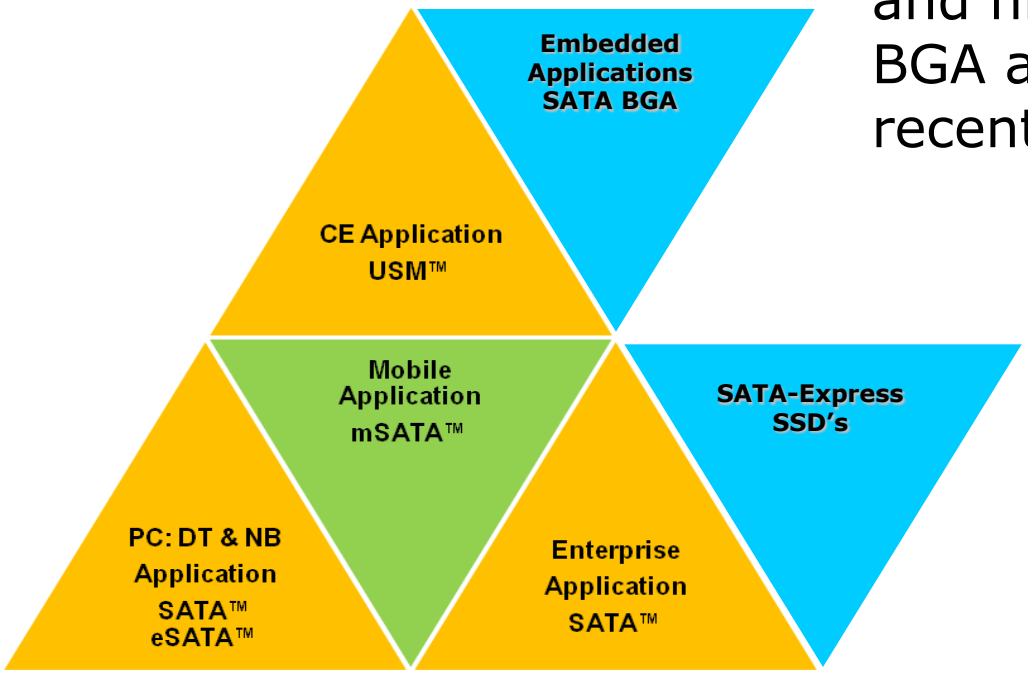
Real Time Scope	DPO72004B (GPIB8::1::INSTR)
BIST-L initialization by	**Auto**
Set scope scale, resolution and sampling rate	Custom Utility Operation without AWG User Defined Batch Script
Set vertical scales automatically	
BIST-L validation required	Always
Number of times AWG is turned ON/OFF for putting DUT in BISTL mode	2
Horizontal scale for PHY-TSG BIST-L acquisition (us/div)	4
Resolution for PHY-TSG BIST-L acquisition (ps/pt)	20
OOB validation required	First time only

- DUT control a significant challenge
  - BIST-L (loopback) required for compliance
- AWG has a successful track record of DUT control
  - Initiates loopback while seamlessly transitioning to Tx/Rx testing
- 3rd party tools available (Drivemaster, serial port control)



Tektronix

The SATA Ecosystem: Now

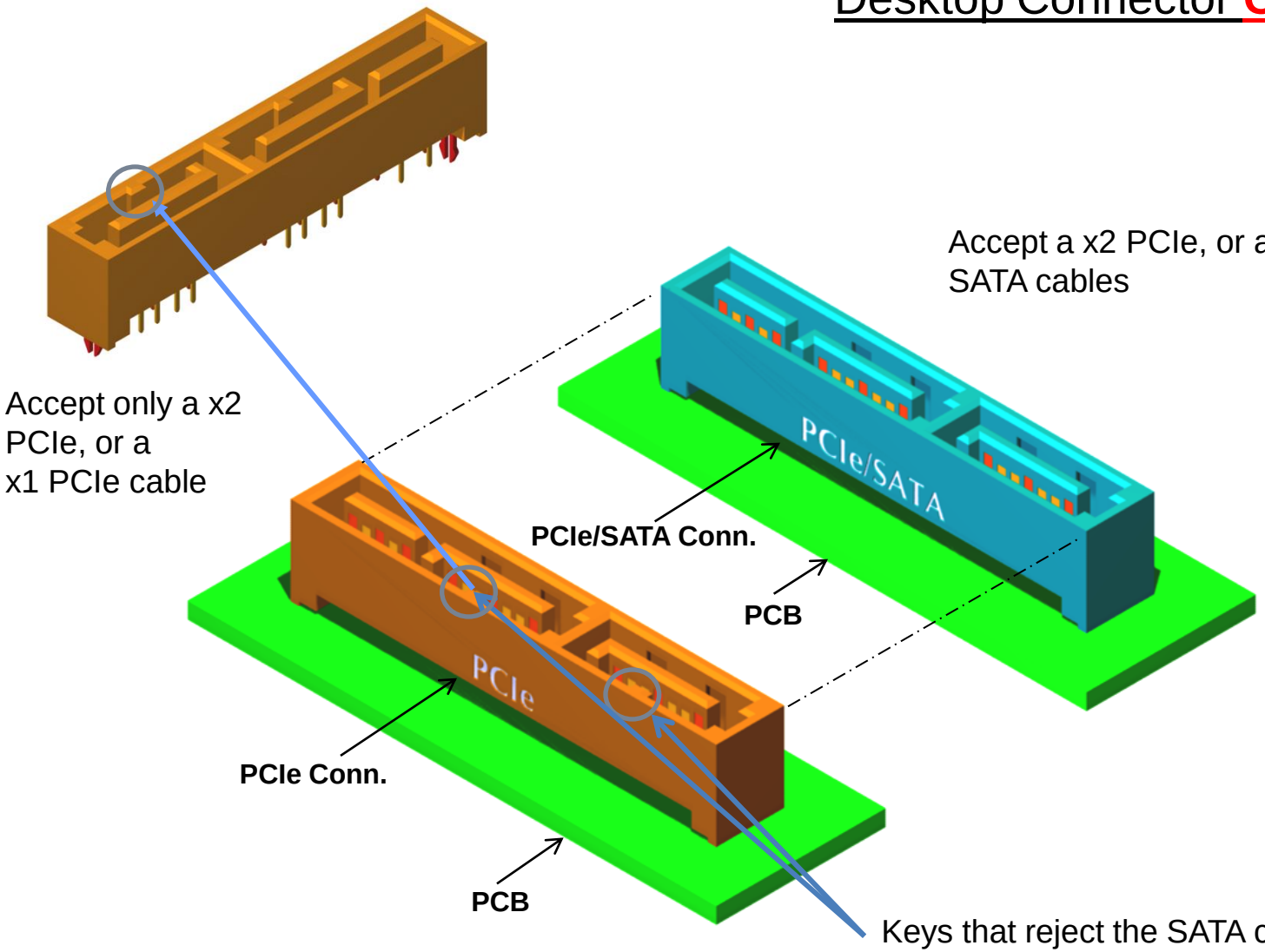


Today, SATA is expanding in specialized low power, compact and high performance areas with BGA and SATA-Express Solutions recently approved by SATA-IO.

Tektronix®

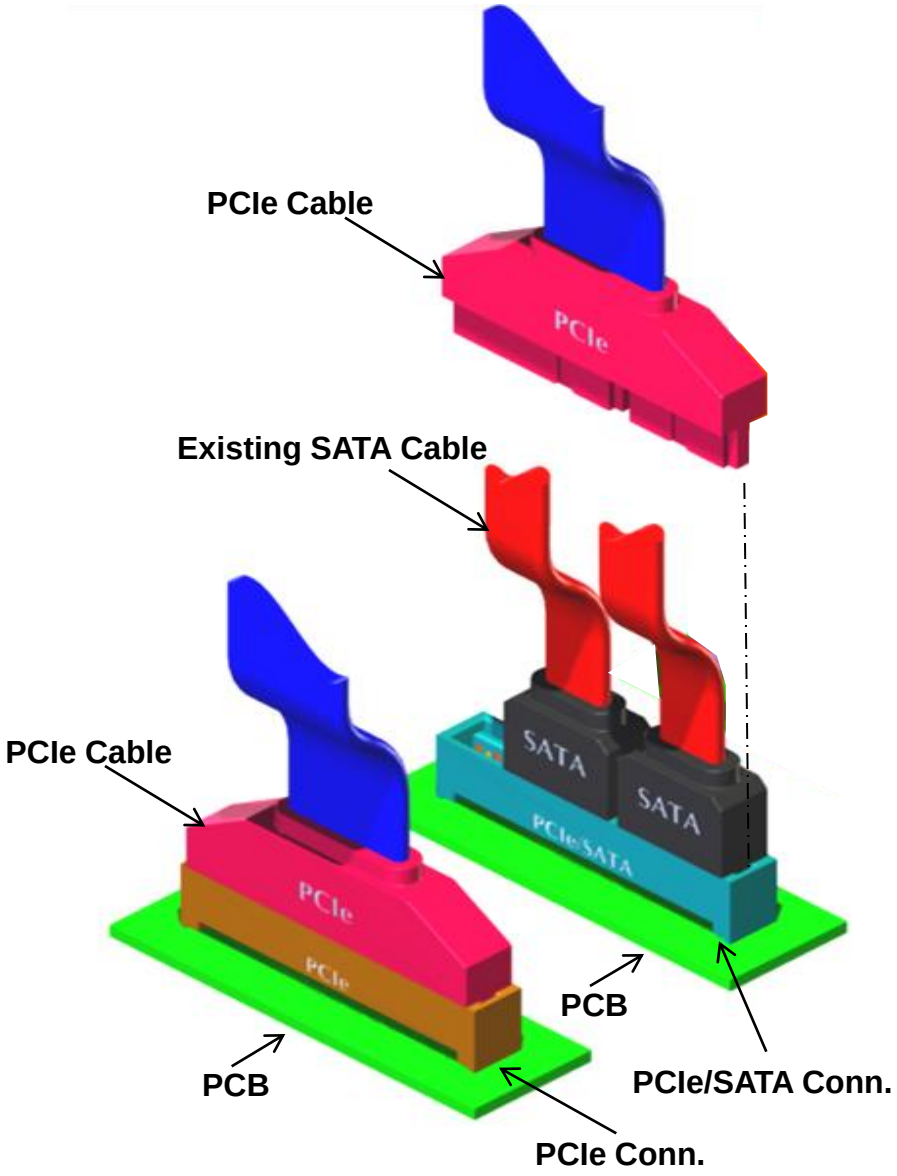
Enabling the New SATA Express Ecosystem

Desktop Connector **Concept**



Tektronix

Enabling the New SATA Express Ecosystem



Desktop Cables **Concept**

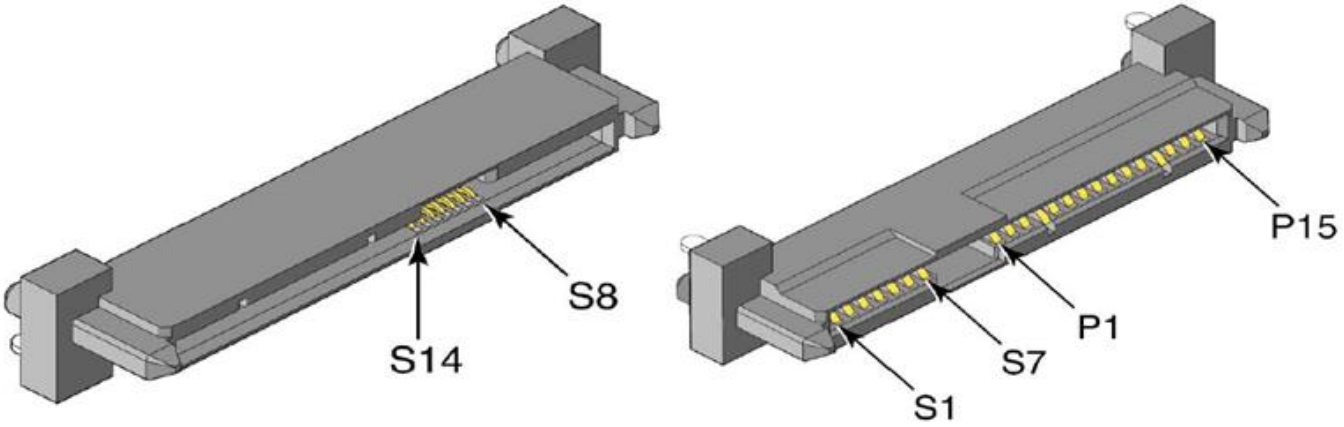
- SATA devices will coexist with next generation PCIe devices
- SATA cost/performance benefits
- Requires a connector that supports both PCIe and SATA
  - Allows a single motherboard (backplane) connector to support both interfaces
- HDD-compatible form factors to be defined for PCIe devices
  - Enables system-level mechanical compatibility
  - Preserves high-capacity storage

SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives

Tektronix®

Physical Connections

Pinout Table for Host Backplane Connector



Signal List Summary

Usage	Signals	Contacts
x2 PCIe muxed with SATA	2*(Tx and Rx pairs) + GND pins	14
Power	5V and 12V + GND pins	10
Device Activity Signal/Disable Staggered Spinup (optional)	DAS/DSS	1
SATA/PCIe DEVSLP	DEVSLP	1
PCIe sideband	PERST#	1
PCIe/SATA Interface Detect	IFDet	1
Reserved	RSVD	1

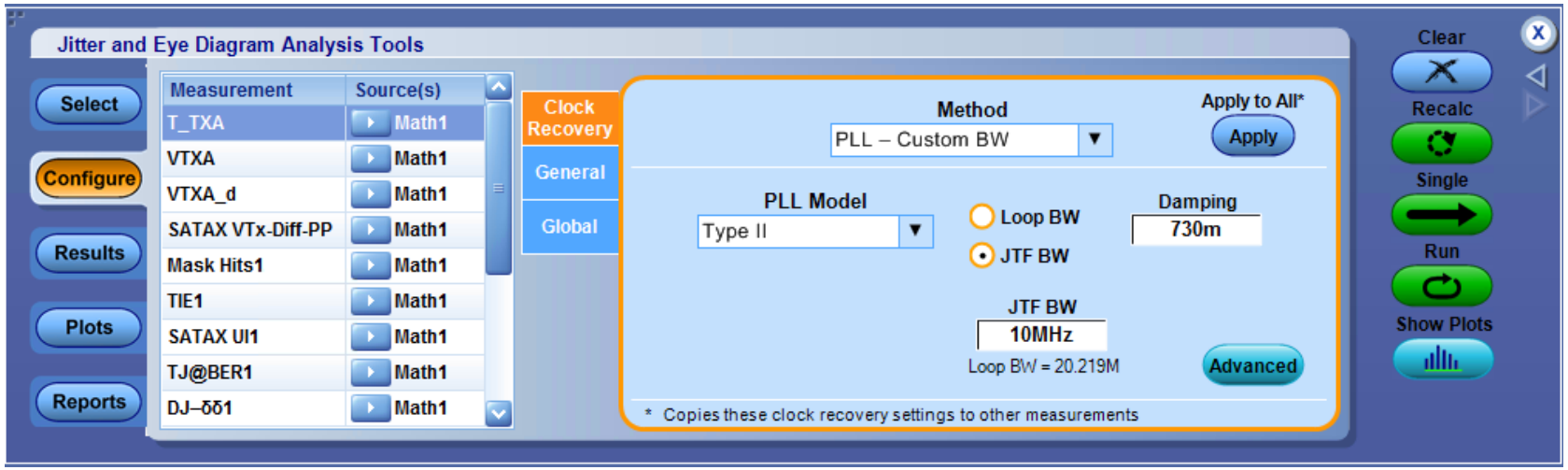
Source: SATA Express Specification (Technical Proposal)

Note, additional PCIe Ref Clk pins optional

Tektronix®

SATA Express = PCIe PHY Layer

- Tx Test parameters
  - Voltage
  - Package Loss
  - Transmitter Equalization
  - Jitter
- NEW Ref Clock Spec definition
  - Independent Ref Clock model
  - 2nd Order transfer function for SSC harmonics attenuation

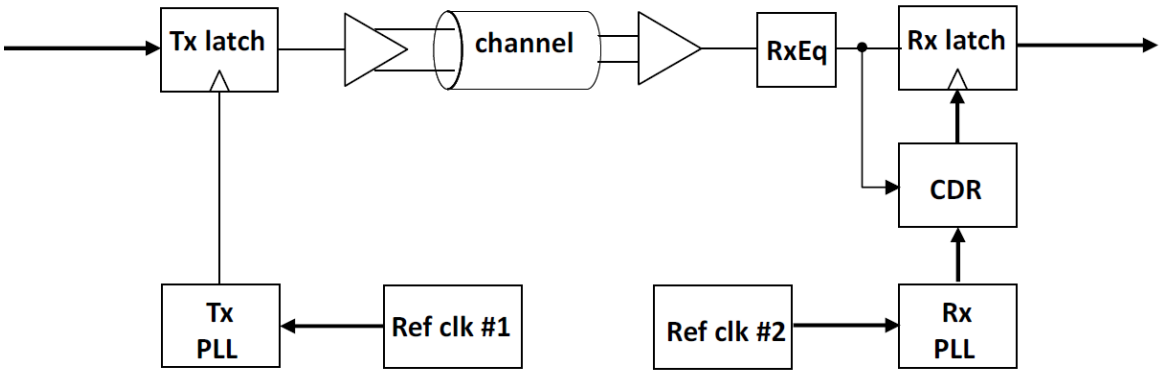


Tektronix

Clocking Architectures – PCIe vs. SATA

- SATA
  - Supports SSC
  - Embedded clock
- PCIe
  - Three different synchronization methods
    - Forwarded Ref clock
    - Data clocked Ref clock
    - Separate Ref clock
- Client PCIe application

  -> no need for "refclk“*



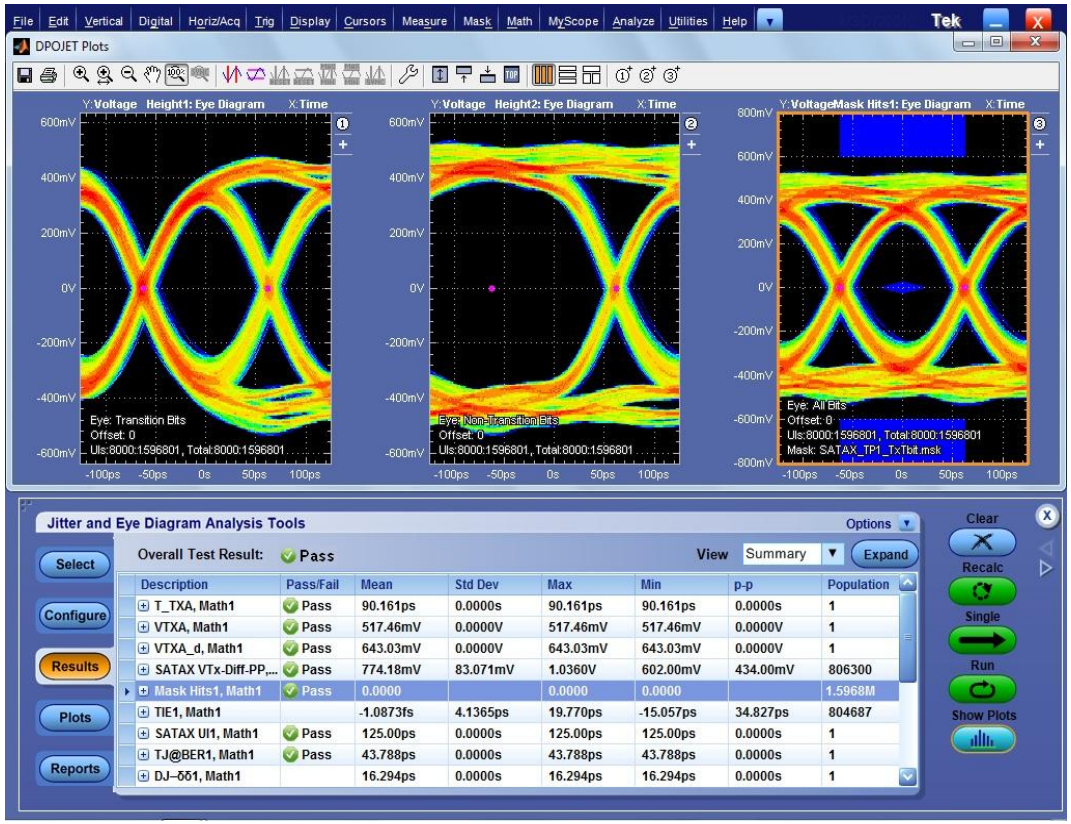
Independent Ref clock model for SATA Express

* PCI-SIG proposal under review

Tektronix

Tektronix Solutions for SATA Express Measurements

- DPOJET-based SATA Express setup (requires option PCE3)
- Support for Base/CEM spec measurements
- Supports all versions of PCI Express and includes SATA Express PLL configurations



Tektronix

SATA Express Signal Access

- Recommend Luxshare-ICT Dual Port SAS fixtures (SFF-8482)
- Similar dimensions but different pinout
- For device testing use plug fixture (TF-4R21) to mate with SATAe plug
  - Both ports accessible (29 pin)
- For cable testing use receptacle fixture (TF-4P22) to mate with SATAe receptacle
  - Only port A is accessible (22 pin)

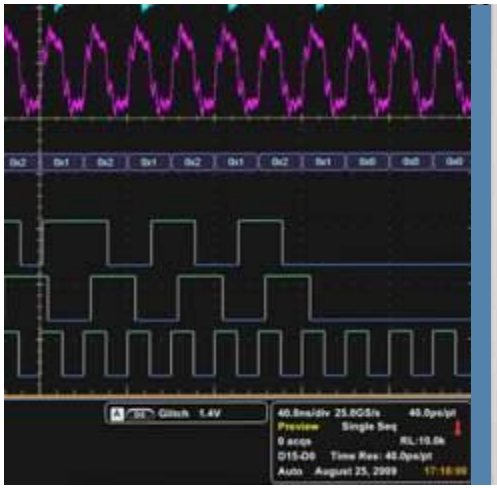
SAS Dual Port Plug Test Fixture

SAS Dual Port Receptacle Test Fixture

http://www.luxshare-ict.com/

Tektronix®

Thanks !



Tektronix®