Server class storage: Mainstream 6G testing needs and preparing for the 12G transition

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Agenda

- Introduction
- Storage Development Roadmap
  - Introduction
  - Industry Timeline
  - Design Considerations at ~12G
    - 12+ G Design Problem
    - Crosstalk
    - BUJ
    - WDP
    - Signal Amplitude
    - Instrumentation

REFERENCES:

[1] IEEE is 25Gb/s on-board signaling Viable?

KAM et al.: IEEE Transactions on advanced Packaging, Vol. 32, No. 2, May 2009.

[2] SAS 3.0 B-t-B Connector & Cable assembly Channel Performance @ 12Gbps "Modeling, Measurements & Simulations for BER compliance with multi Aggressor System Interconnect"

Doron Lapidot et al.:T10 Document # T10/10-219r0 (Tyco Electronics)

[3] IEEE CMOS SerDes core with feed-forward and decision-feedback equalization

T. Beukem et al.: *IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2633–2645*

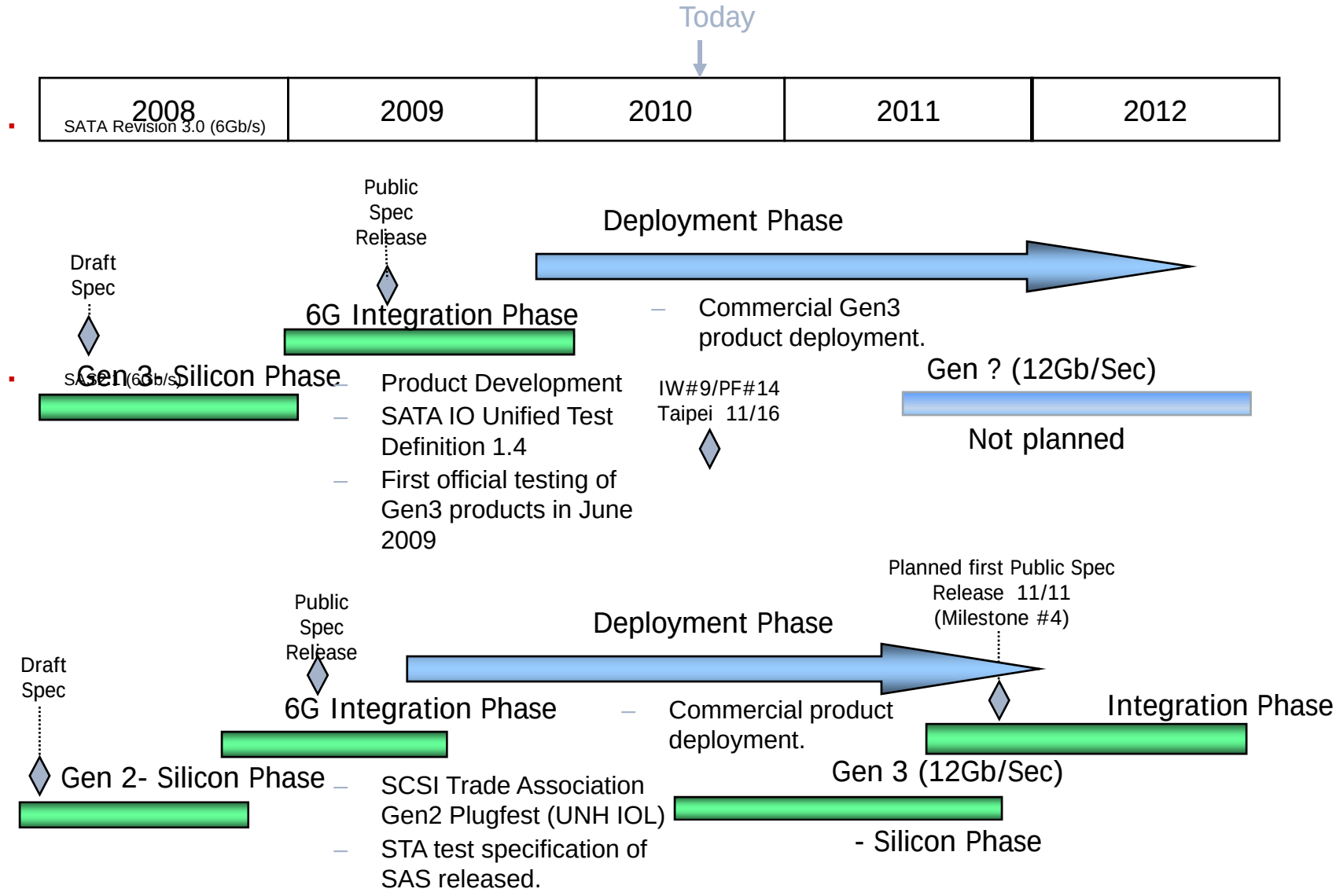
[4] Alcatel-Lucent: DSP & FEC: Towards the Shannon Limit

Timo Pfau ECOC'09 | WS1: DSP & FEC | Sept. 20, 2009

[5] Fujitsu: 56Gs/s ADC Enabling 100GbE

Ian Dedic, Fujitsu Microelectronics.: OFC2010 Invited Paper, Digital Transmission Systems

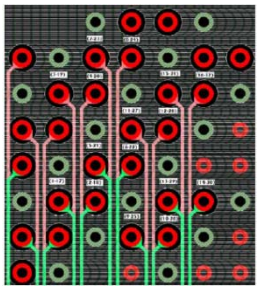
Storage Timelines and Solutions Development

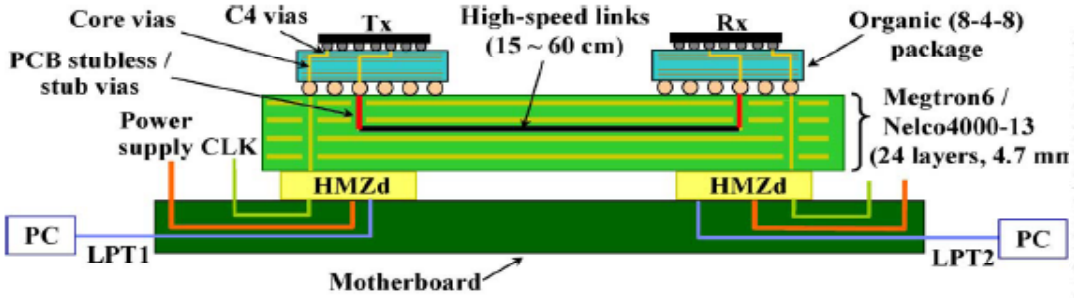


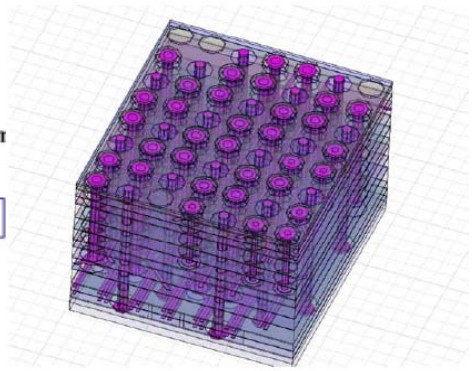
12+G Design Problem:
1000mV, FFE, Crosstalk, Crosstalk, Crosstalk, DFE, 50mV

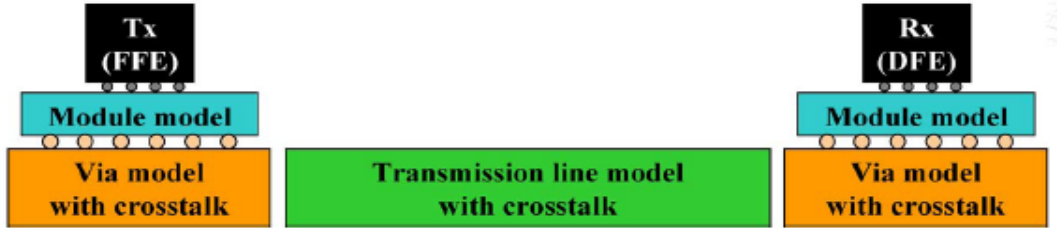
- Significant advances in Feed Forward Equalization and Decision Feedback Equalization are key to operating at 12+G.
- Mitigating the complex Channel Crosstalk and Signal loss problems which 12+G designs present, is the largest design challenge today.
- Crosstalk is often beyond the capability of current equalization architectures to combat, and needs to be quantified if accurate performance projections are to be made based on experimental measurements. For short channels, NEXT may be less of an issue since the insertion loss is not as severe; however, in longer links and at higher data rates it has the potential to become a dominant design consideration. Ref:[1]

KAM *et al.*: IS 25 Gb/s ON-BOARD SIGNALING VIABLE? 329









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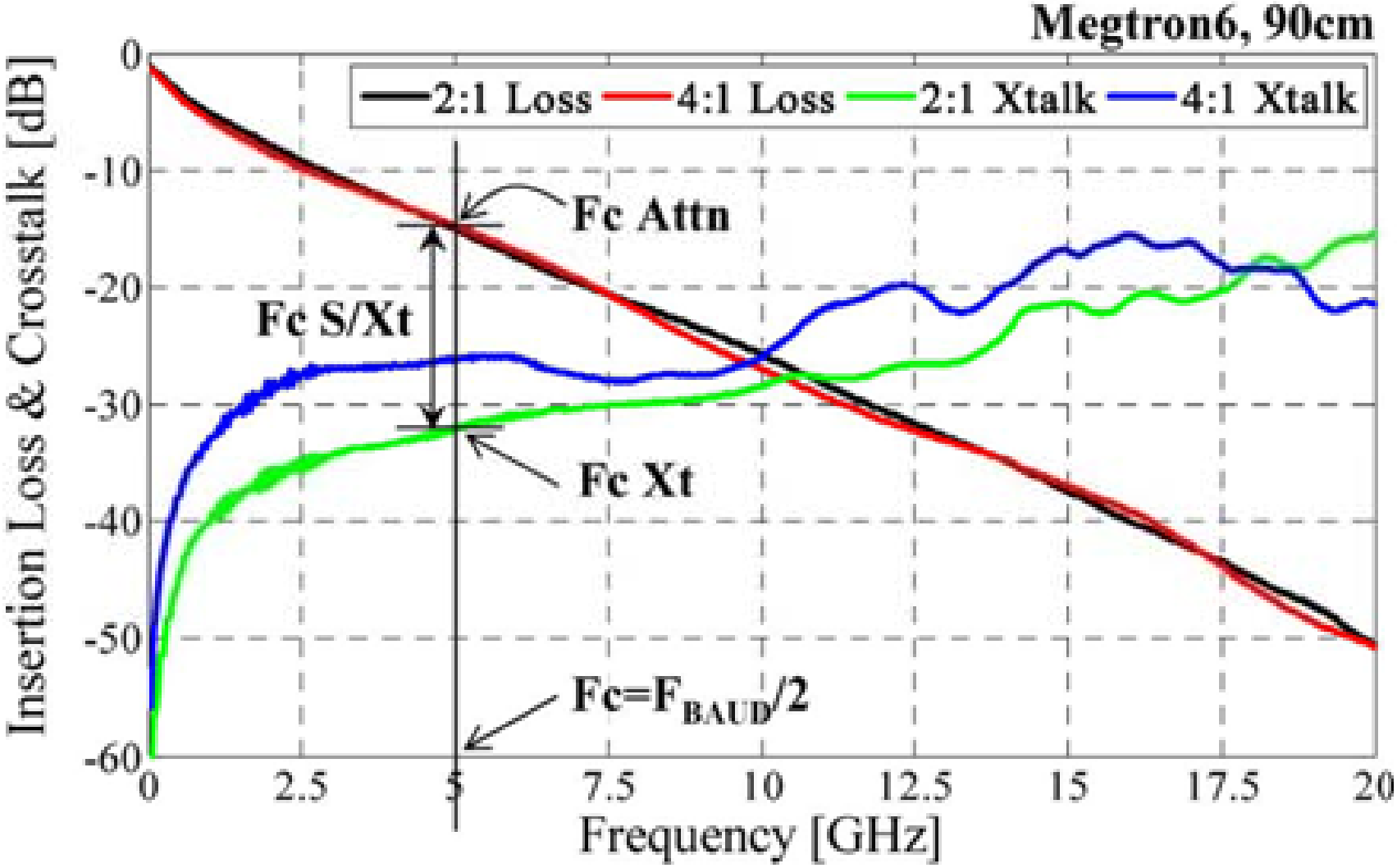
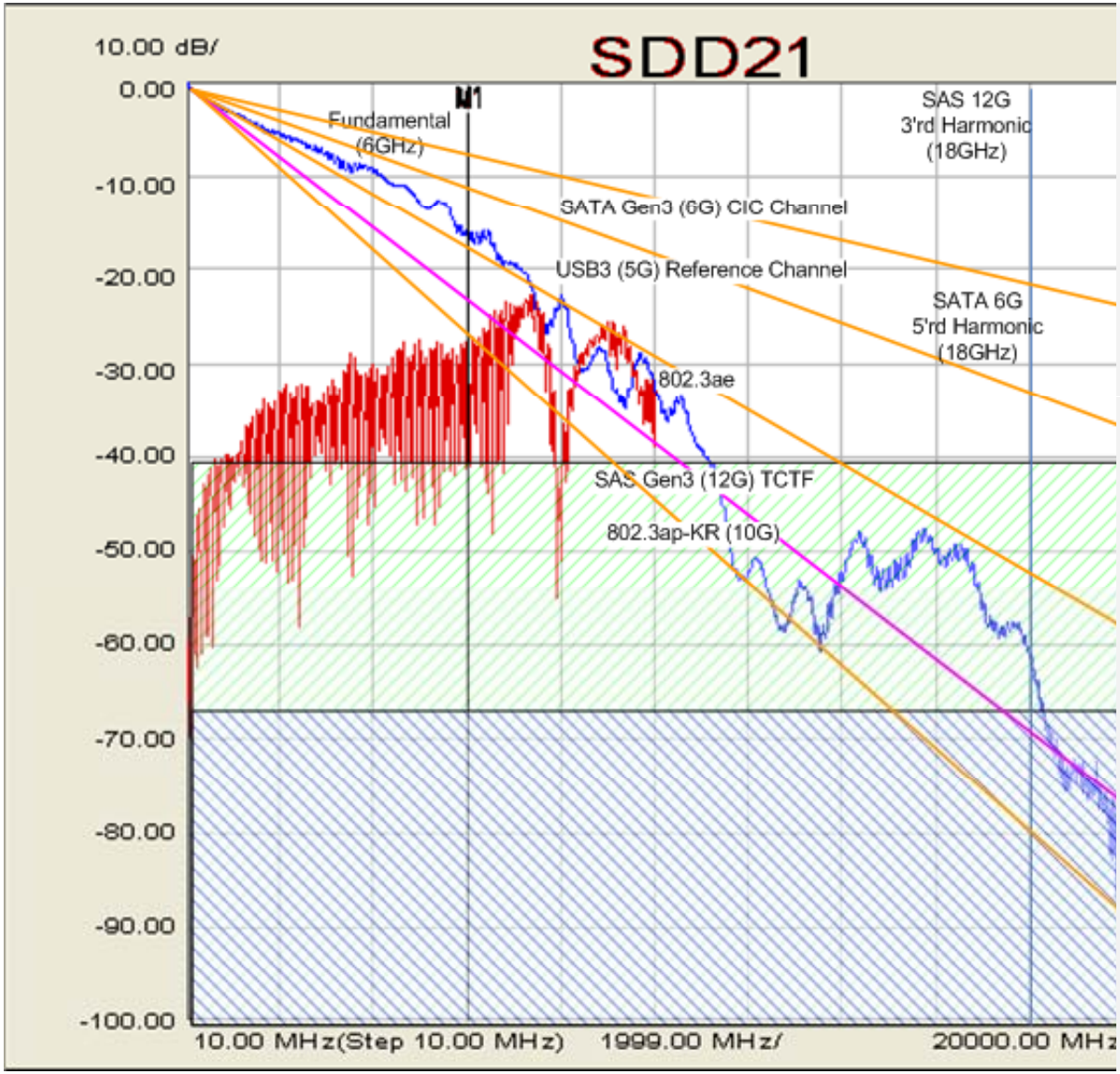
ICR or Fc S/Xt

Ref:[1] : IEEE

signal-to-crosstalk ratio, is defined as a ratio of signal attenuation to the power sum of all crosstalk aggressors at the frequency of half a given baud rate (5 GHz for 10 Gb/s signaling is given as an example here).



DFE/FFE Advances
-vs- Dynamic Range Range -vs Data Rates –vs- BW



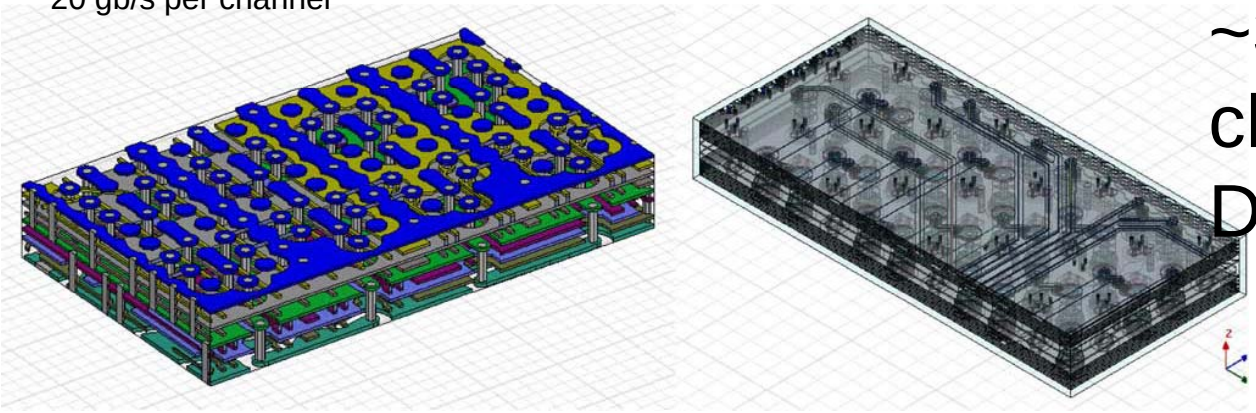
- 10+G datarates are being achieved by both advanced DFE, and FFE systems with link training and adaptive channel compensation.
- Channel bandwidth is largely being held constant from similar 6G solutions, with focus on ***extracting the un-tapped carrier capacity*** in the low dynamic range regions of the channel.
- 6-10 Meter solutions and associated reference channels are shown here.

Escape Bandwidth and Power

KAM *et al.*: IS 25 Gb/s ON-BOARD SIGNALING VIABLE?

METRIC	UNITS	Electrical		Optical	
		10 Gb/s	20 Gb/s	10 Gb/s	20 Gb/s
SYSTEM					
Overall Tech. Metric	[(Gb/s-m)*(Escape BW)] /[(mW/Gb/s)*(mm2/Gb/s)]	86	124	653	1762
Escape BW Limit	Tb/s for 50 mm module	6.3	12.6	23	46
LINK					
Distance * Baudrate	Gb/s - m	15	16	15	20
Maximum Distance	m	1.5	0.8	1.5	1.0
CHIP					
Power / Gb/s	mW/Gb/s	22.0	40.6	13.2	17.4
Silicon Area / Gb/s	mm2/Gb/s	0.05	0.04	0.04	0.03

Summary metrics comparing escape channel bandwidth and power dissipation for electrical and optical links at 10 and 20 gb/s per channel



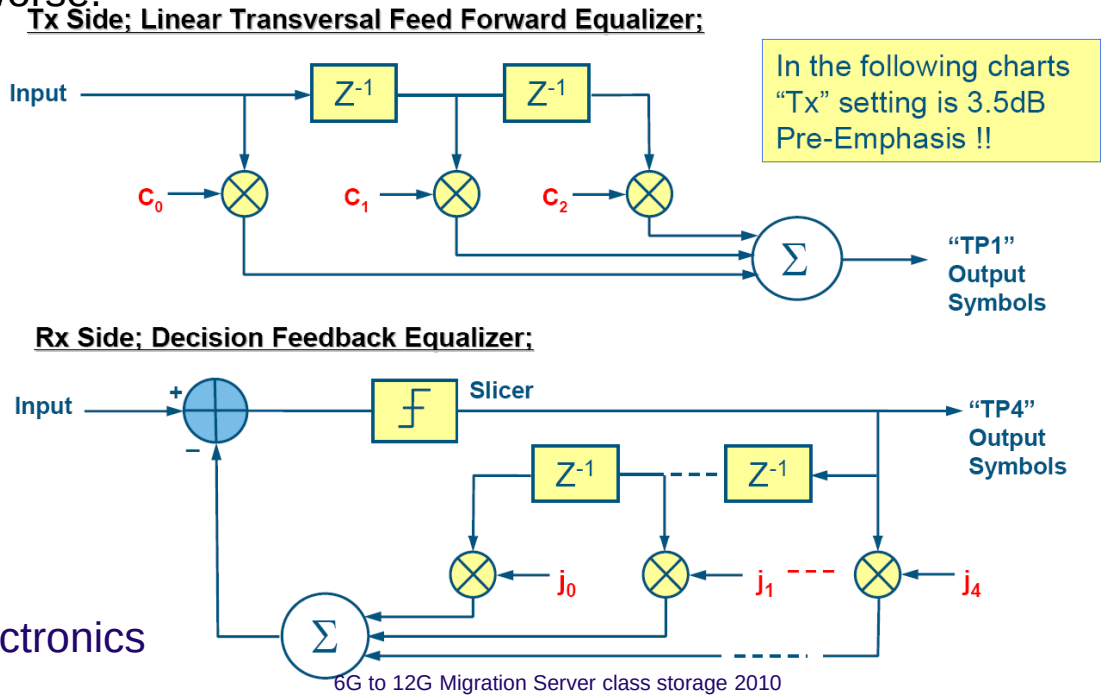
- 4-tap FFE/5-Tap DFE designed for even short reach configurations have significant power constraints. 12G links will need to consume/dissipate ~300mW per channel. 60mW per DFE tap.

Ref:[1,3]:

12G Design Problem: FFE, DFE

- A non-recursive DFE can only compensate a fixed time span of ISI. In very low-bandwidth channels, significant post-cursor ISI may fall outside the time span covered by the DFE taps.
- FFE can compensate ISI over a very wide time span since the FFE filter response is convolved with the impulse response of the channel.
- The utility of FFE alone drops off rapidly over complex channels which have spectral nulls (Via stubs, connectors, etc) which require many FFE taps to cancel reflections.
- Optimal solutions exist around 4-tap FFE with 20+ (20*60mW) tap DFE designs. More emphasis is required in the Receiver section of the topology as more aggressive FFE makes crosstalk worse.

Ref:[1], [2]



Ref:[2]: Tyco Electronics

Current 6GTx Requirements

5.7.4.6.1 Transmitter device signal output characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps overview

Table 59 specifies the signal output characteristics for the transmitter device for trained 1.5 Gbps, 3 Gbps, and 6 Gbps as measured with the zero-length test load (see 5.6.2), unless otherwise specified, attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements.

Table 59 — Transmitter device signal output characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps at IT and CT

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage [b]	mV(P-P)			50
Withstanding voltage (non-operational)	mV(P-P)	2 000		
Rise/fall time [c]	UI	0.25 [d]		
Reference differential impedance [e]	ohm		100	
Reference common mode impedance [e]	ohm		25	
Common mode voltage limit (rms) [f]	mV			30
RJ [g, i]	UI			0.15 [j]
TJ [h, i]	UI			0.25 [d]
WDP at 6 Gbps [k]	dB			13
WDP at 3 Gbps [k]	dB			7
WDP at 1.5 Gbps [k]	dB			4.5

18dB WDP at 12G?

[c] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5)(see table 241 in 10.2.9.2) on the physical link.

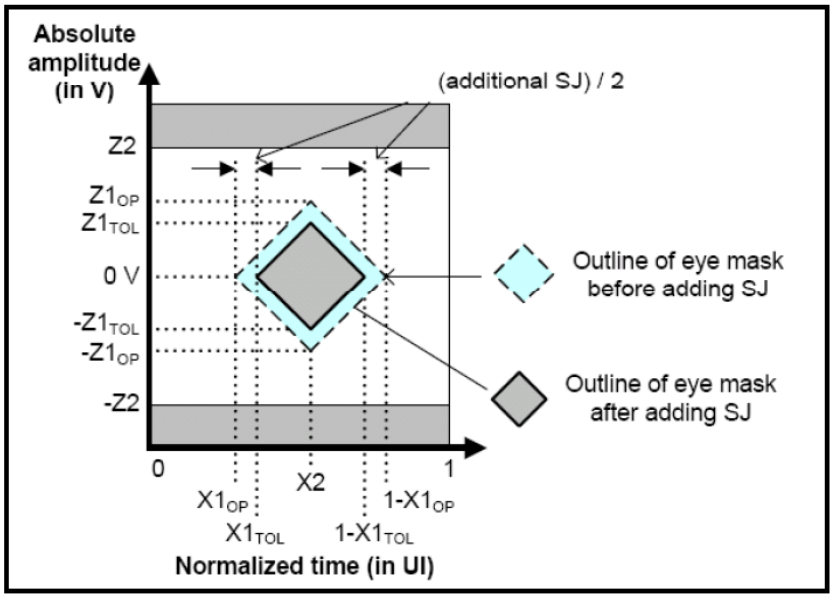
Preliminary 12G Tx Requirements

SAS 3.0 Channel Evaluation Baseline

1. In absence of SAS @ 12Gps, specifications were extrapolated based on SAS @ 6Gbps only for the following analysis.
2. Calculated based on SAS2 Spec rev 13, Sec 5.3.5.4 Receiver Device Jitter Eye Tolerance Mask. The following values were used:
   - $Z1_{OP}$=0.0875V (Gen2i minimum opening),
   - X2=0.5UI,
   - $X1_{TOL}$=0.325UI,
   - $X1_{OP}$=0.275UI,
   - Additional SJ=0.1UI,

Where UI = 83.33ps @ 12G

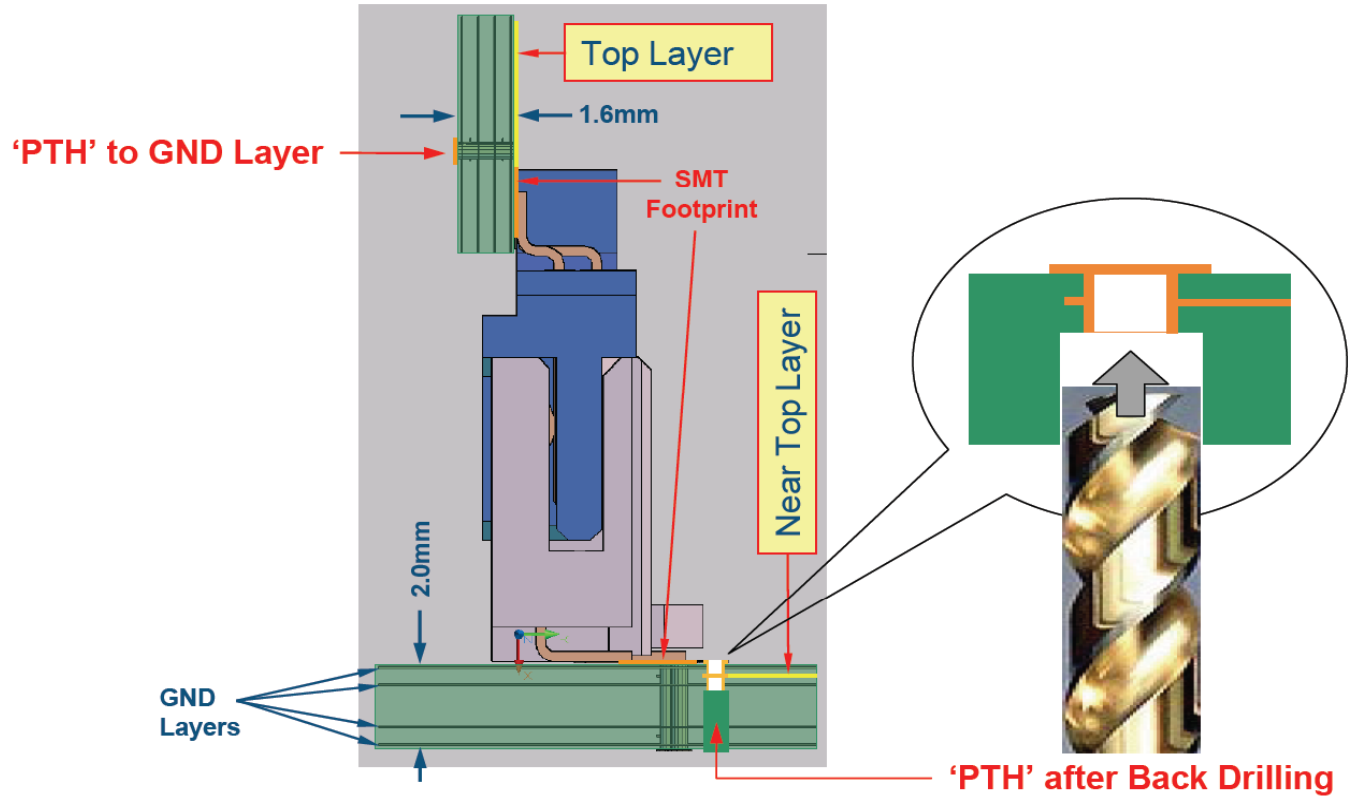
Risetime ≤ 27ps (20%-80%)
at the driver output



Ref:[2]: Tyco Electronics

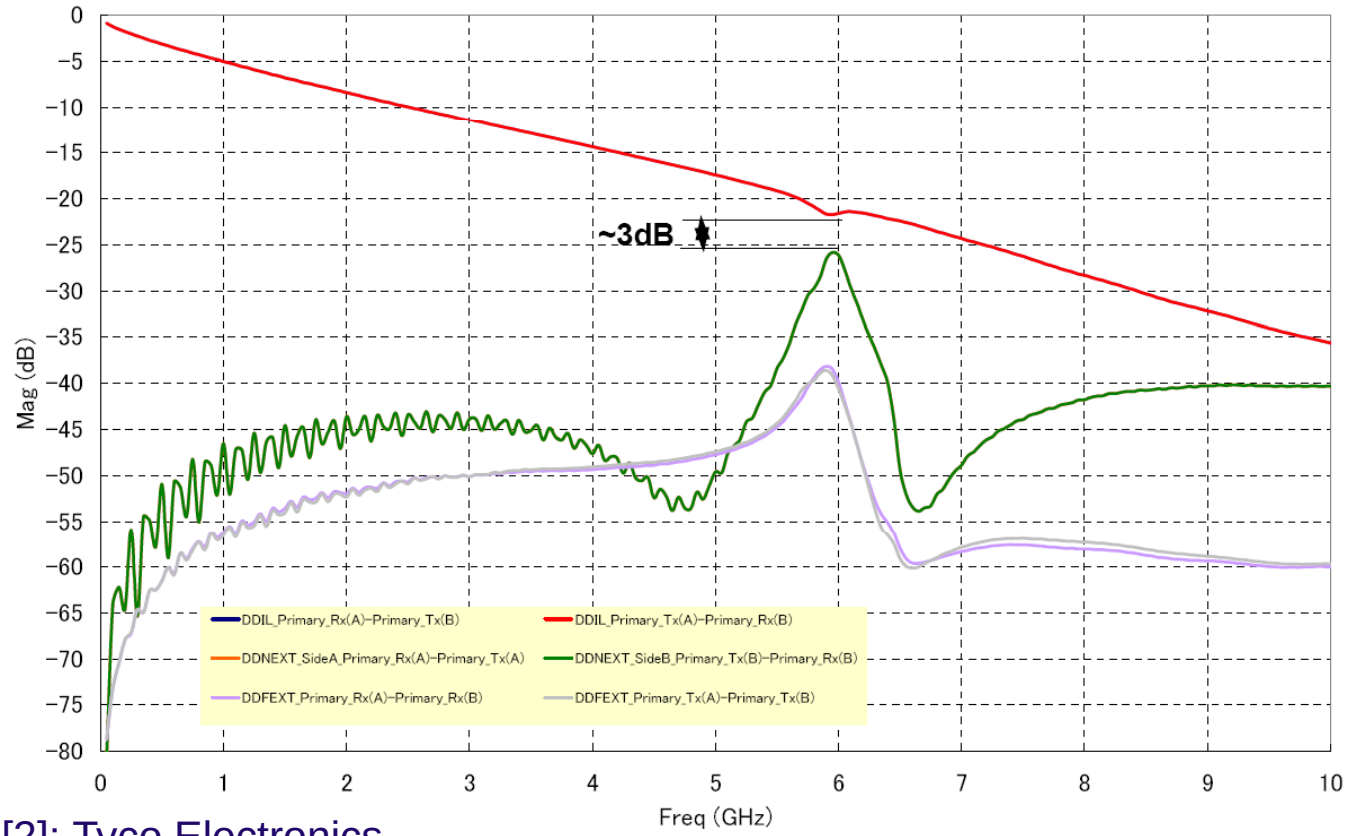
SAS 3.0 Channel Signal Integrity

SAS R/A SMT Plug to SMT Ver. Receptacle.
B/P - Near Top Layer Connection with Back Drilling



Conventional FR4 materials

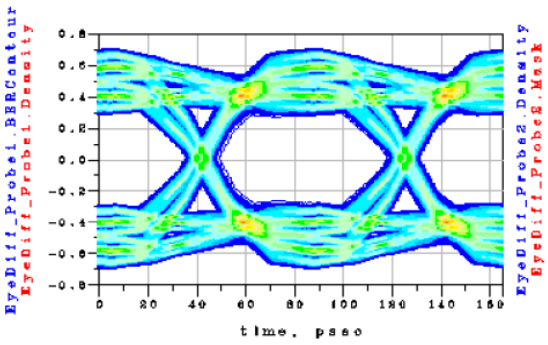
Channel Model 'ICR', Near Top Layer w/ Backdrilling, Primary Port (Device: FR4 Std. / Backplane: 22" FR4 Std.)



Ref:[2]: Tyco Electronics

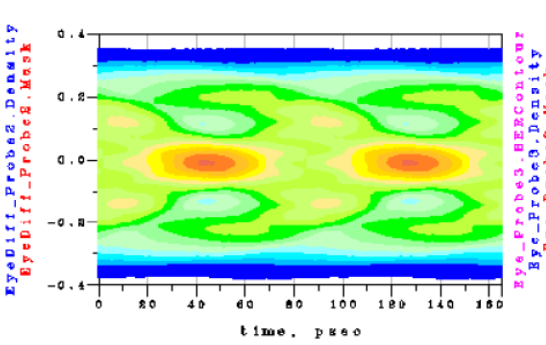
SAS, Primary Port Eye Pattern at TP4
Near Top Layer Backdrilled, 22” Std FR4 BP

Input



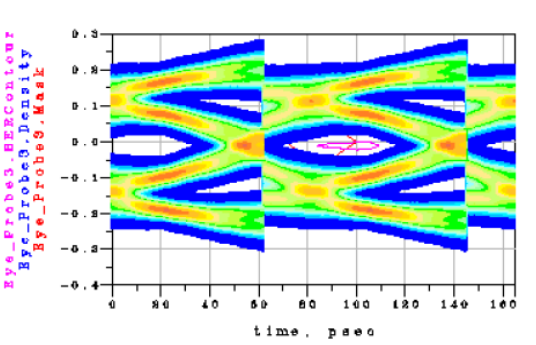
measurement	...obe1.Summary
Height	0.556
Width	7.083E-11
RiseTime	2.757E-11
JitterPP	1.144E-11
JitterRMS	2.288E-12
MaskViolated	0.000

Output with PE Only



measurement	...obe2.Summary
Height	0.000
Width	0.000
RiseTime	4.345E-11
JitterPP	8.333E-11
JitterRMS	2.220E-11
MaskViolated	1.000

Output with PE and DFE



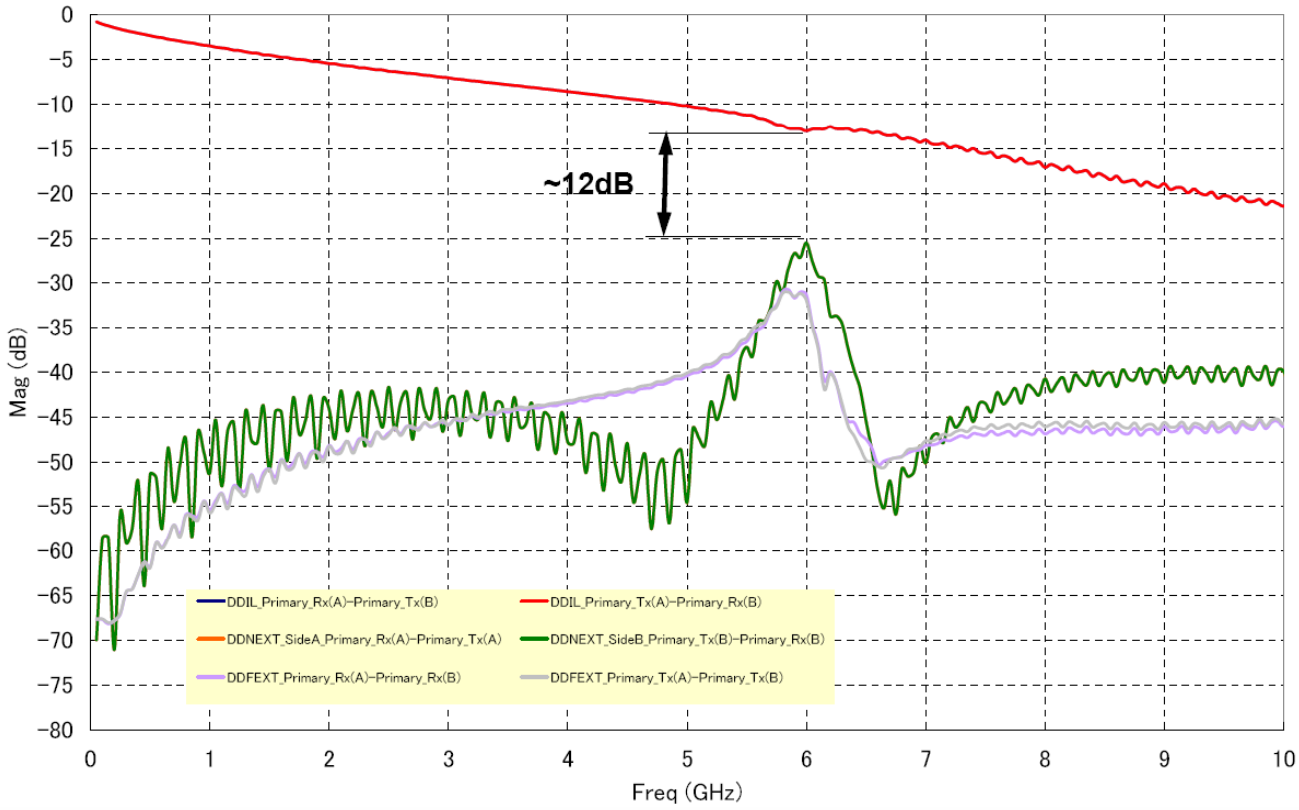
measurement	...obe3.Summary
Height	0.064
Width	4.208E-11
RiseTime	4.972E-11
JitterPP	3.426E-11
JitterRMS	6.851E-12
MaskViolated	1.000

- DFE taps: -0.063044, -0.031113, -0.020923, -0.012749, -0.010123

Ref:[2]: Tyco Electronics

High Speed FR4 FR4 materials

Channel Model 'ICR', Near Top Layer w/ Backdrilling, Primary Port (Device: FR4 Std. / Backplane: 22" FR4 High Speed)



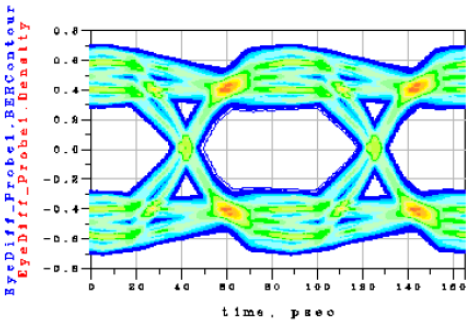
Ref:[2]: Tyco Electronics

High Speed FR4 FR4 materials

SAS, Primary Port Eye Pattern at TP4

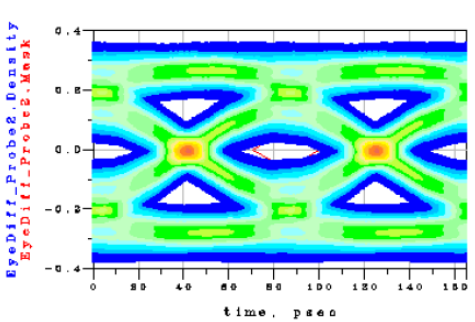
Near Top Layer Backdrilled, 22” Hi-Speed FR4 BP

Input



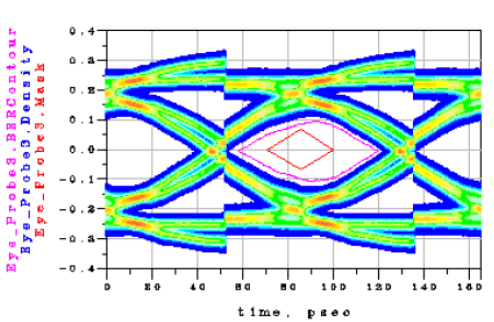
measurement	...obe1.Summary
Height	0.540
Width	7.083E-11
RiseTime	3.061E-11
JitterPP	1.161E-11
JitterRMS	2.321E-12
MaskViolated	0.000

Output with PE Only



measurement	...obe2.Summary
Height	0.044
Width	4.042E-11
RiseTime	5.352E-11
JitterPP	3.590E-11
JitterRMS	7.181E-12
MaskViolated	1.000

Output with PE and DFE



measurement	...obe3.Summary
Height	0.198
Width	7.083E-11
RiseTime	4.090E-11
JitterPP	1.069E-11
JitterRMS	2.137E-12
MaskViolated	0.000

- DFE taps: -0.052138, -0.012593, -0.017168, -0.006769, -0.008297

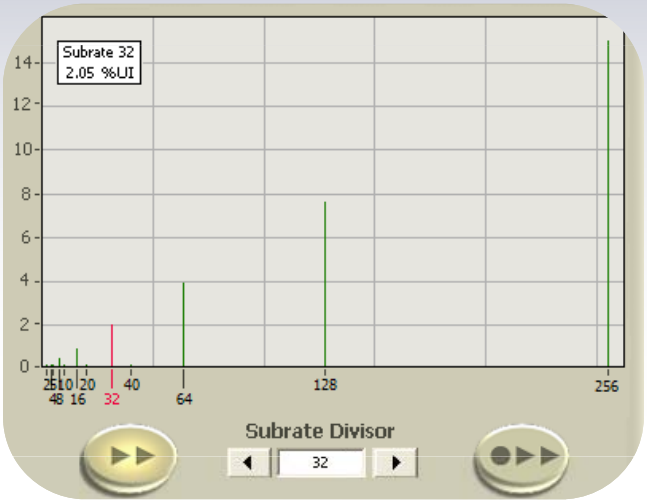
Ref:[2]: Tyco Electronics

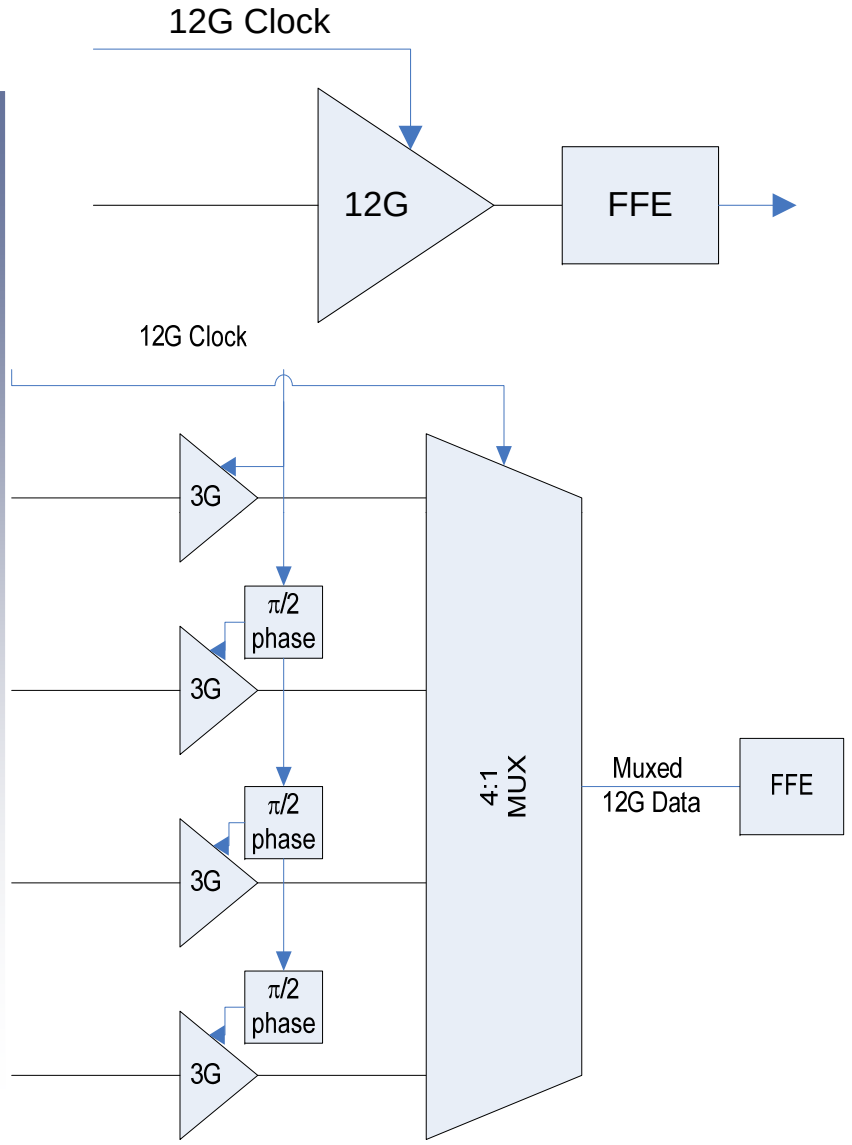
Transition into Jitter Analysis

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio. Packaging parasitics cannot be ignored here either and important from both a modeling and measurement needs.
- The channel performance has to be measured as a means of identifying layout errors or inadvertent coupling which reduces the Signal-to-Crosstalk ratio (ICR). Ref[1].
- The implications of complex channel interaction as well as SERDES multiplexing method, can be observed and identified in an output signal by examining the type and amount of Bounded Uncorrelated Jitter or BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk (NEXT) and BUJ which in most systems get's classified as Random if special steps are not observed.

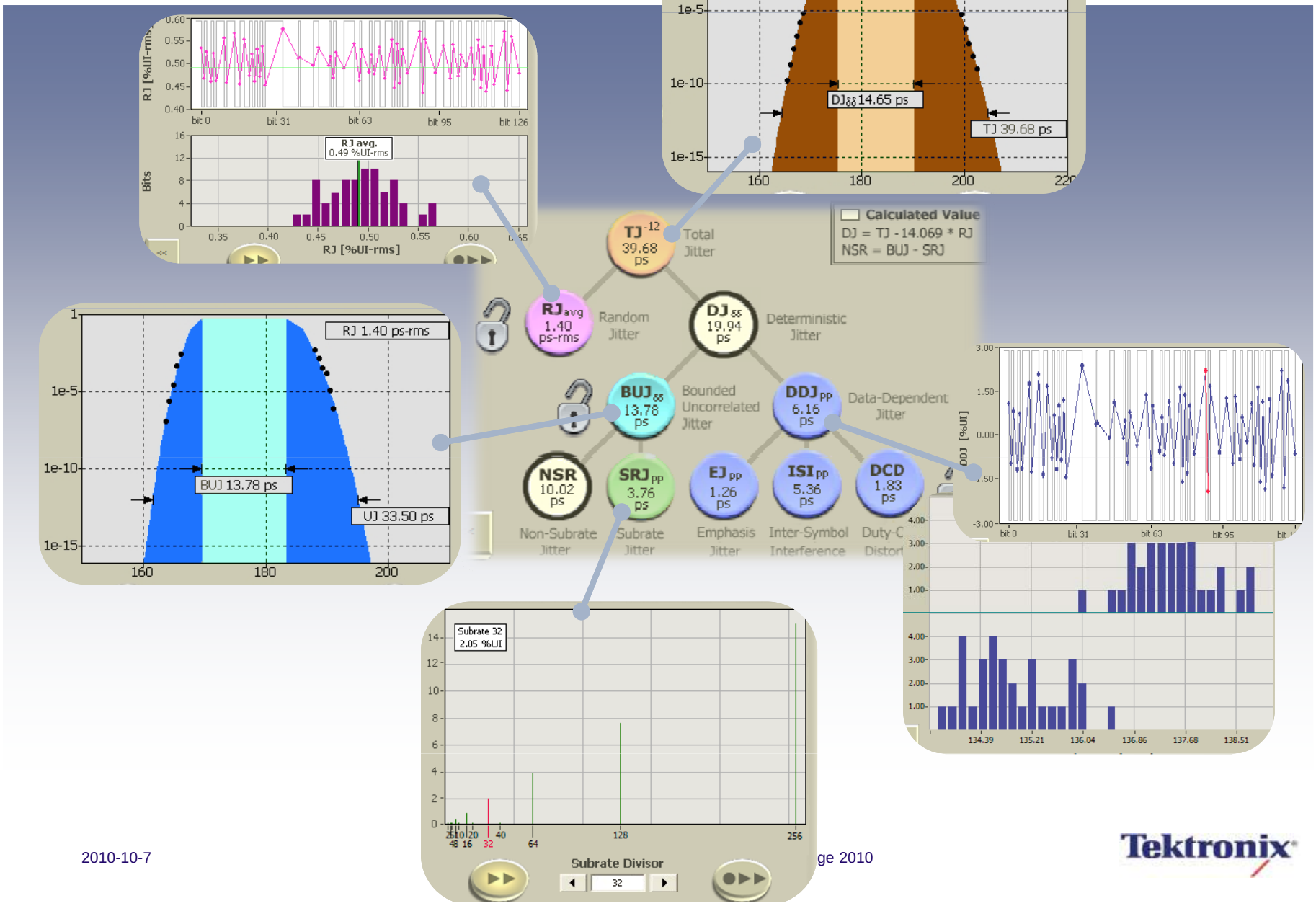
Preamble to 12 Migration

- Silicon providers are either working towards pushing native 10G phys to operate at 12G, while others will be adopting a muxing strategy which allows interleaved operation of multiple native lower speed phys to achieve 12, 14 and 17+G performance levels.
- Multiplexed phy designs can carry subrate harmonics onto the data.
  - F/2 Jitter





Comprehensive Jitter Mapping tools



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BERTScope for SAS

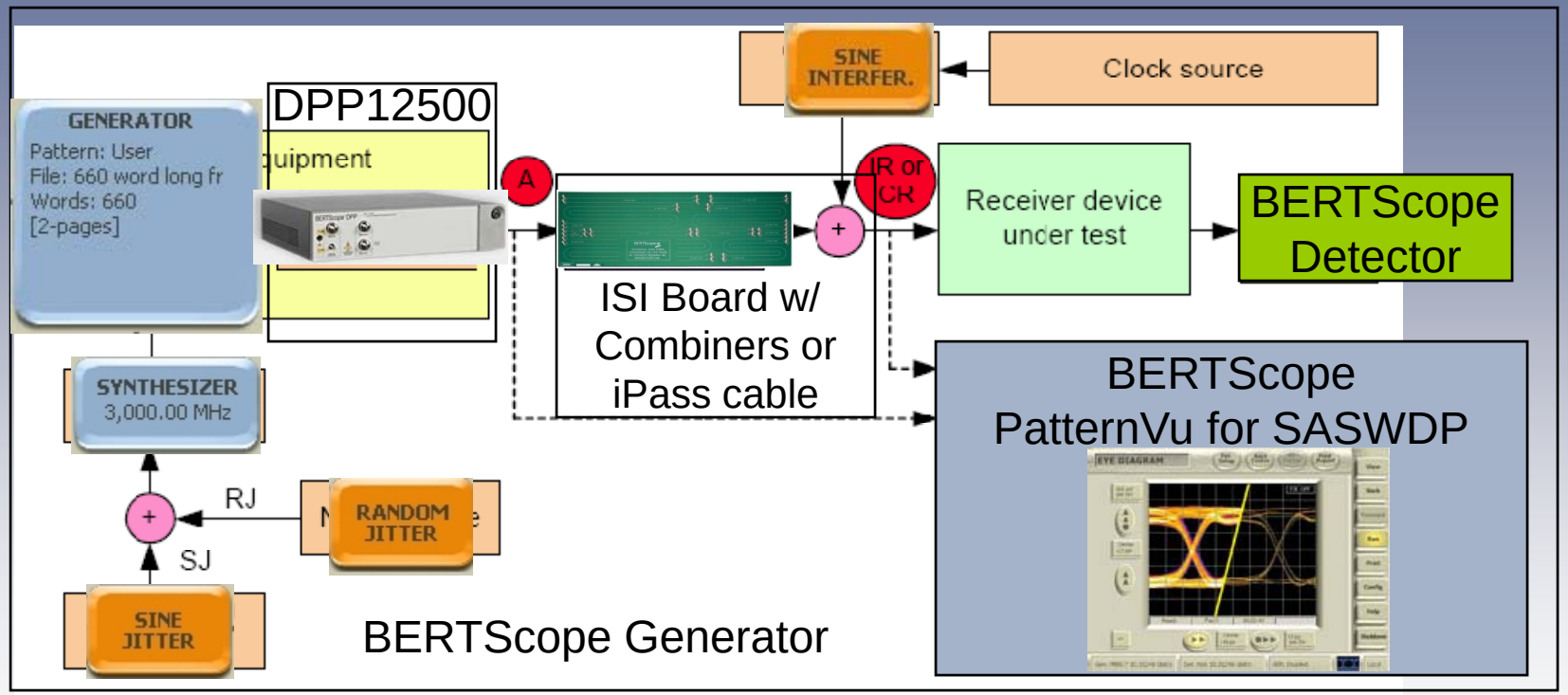
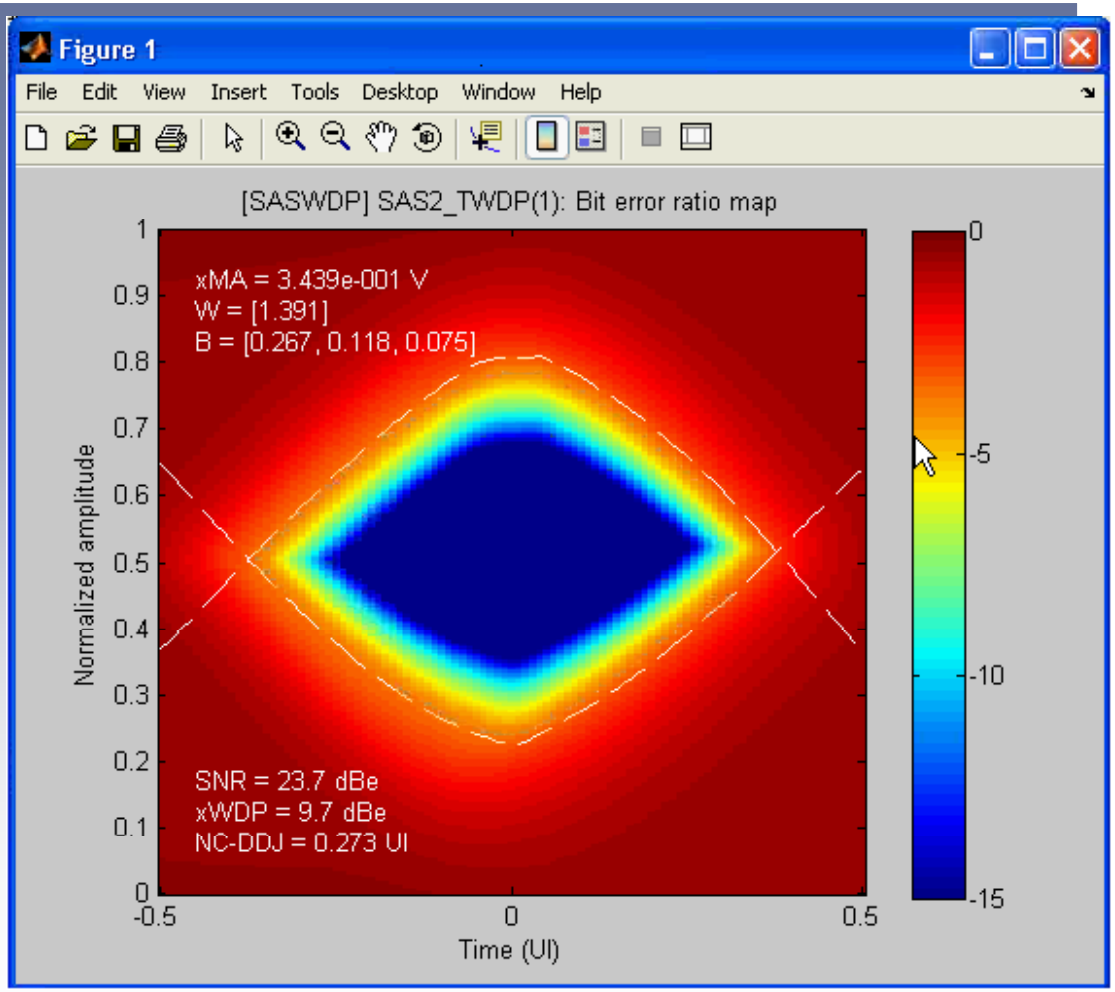


Figure 140 — Stressed receiver device jitter tolerance test block diagram

- **Tektronix BERTScope BSA 125C**, offers a degree of advanced impairment required to properly model SAS channel effects as well as the FFE components with the DPP125 Digital signal Pre-Processor module. This capability along with the BSA's Jitter MAP option allows comprehensive jitter breakdown and particularly unparalleled insights into bounded uncorrelated jitter components.

Waveform Distortion Penalty

- While the future outlook for a SAS 3.0 version of WDP is unclear at this point in time. This tool serves as valuable way to analyze the collective operation of FFE, Channel and DFE operating together.
- waveform distortion penalty (WDP): Is a simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device.

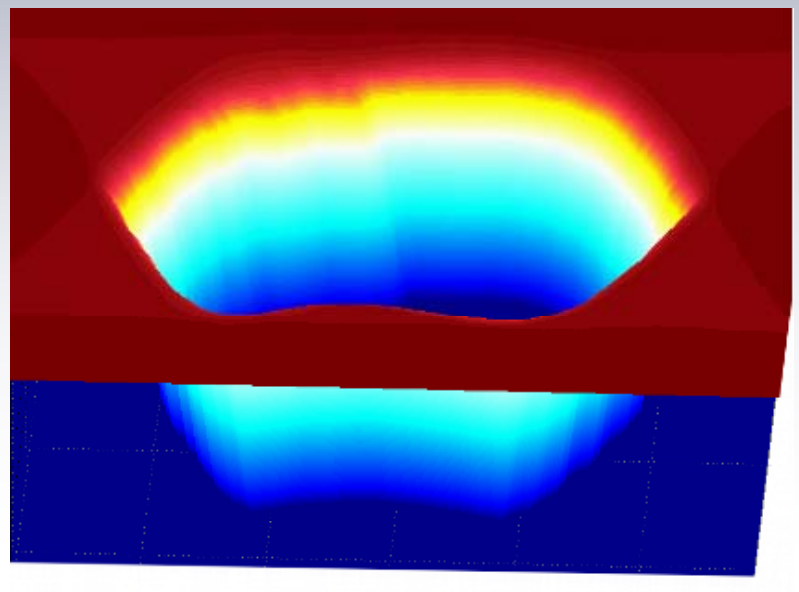


*SAS-WDP and related methodologies contains intellectual property of one or more third parties. Tektronix Inc, does not license, sell or distribute WDP. Any Intellectual property rights to run WDP with Tektronix instruments are not granted by Tektronix, and must be obtained by the instruments end users.

Jitter Methodology and BER contouring Oscilloscope Measurement Tools

- **80SJNB**, the premium jitter tool for sampling oscilloscopes, can measure and **decompose jitter** with great results thanks to the sampling oscilloscope's **low noise and jitter floor**. With signal levels at 12G regularly in the 45-60mV region, the Sampling Instruments high dynamic range make it well suited for vertical noise analysis and modeling of different DFE tap configurations.
- **All** of PJ, RJ, DDJ, DCD, Dual Dirac model, PWS, TJ, as well as a **breakdown for Noise** are available … but such complete analysis relies on relatively **short, repeatable** pattern of data being analyzed.

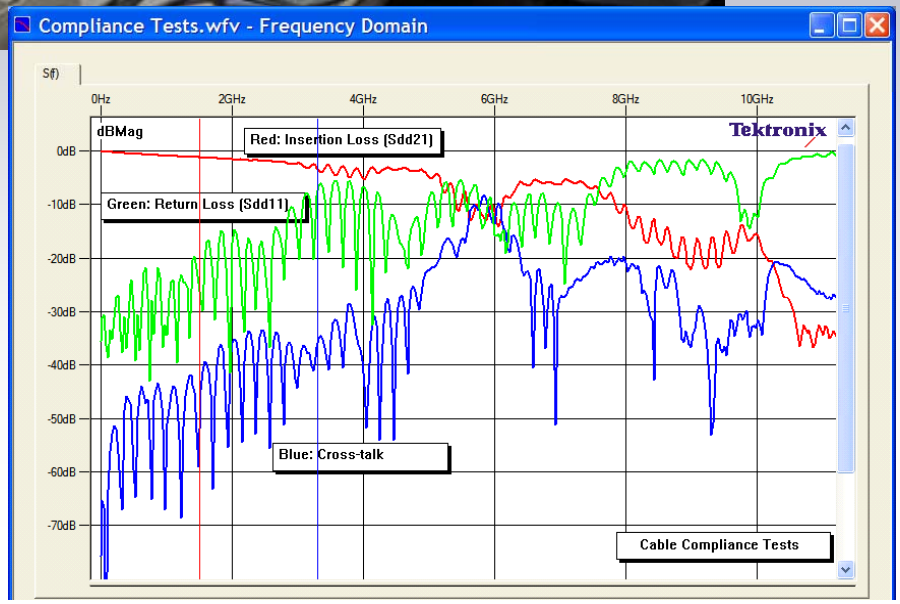
Analysis in 80SJNB: Premium jitter tool



12G Interconnect and Channel Measurements

- SAS 12Gbps
- SAS/SATA 6 Gbps
- SAS/SATA 3 Gbps
- SAS/SATA 1.5 Gbps

- Simple **time domain** tests
  - Impedance
  - Delay
  - Intra-pair, Inter-pair skew
- **Frequency domain** tests
  - Differential return loss
  - Differential insertion loss
  - Frequency domain crosstalk
- How much **performance** do you need?
  - 80E08 30GHz, or **80E10 50GHz TDR module** for -54dB dynamic range at required bandwidth



12G Instrument Solution Strategy

- Phase 0 (Silicon Designers): Transition into Phase 1 in November 2011
  - Equivalent Time Instrument: ICR, BER Contours, Far End Channel Amplitude measurements (30mV Eye), Near end Channel Transition Time measurements.
  - Real Time Instrumentation: Waveform Distortion Penalty, DFE modeling, System Debug.
  - BertScope: 12G stimulus and error detector for Receiver Testing.
- Phase 1-2 (ODM/OEM):
  - 20 GHz Real Time Instrumentation for Automated DFE, AC Parametric and Jitter measurements.
  - 12G BertScope for receiver testing.

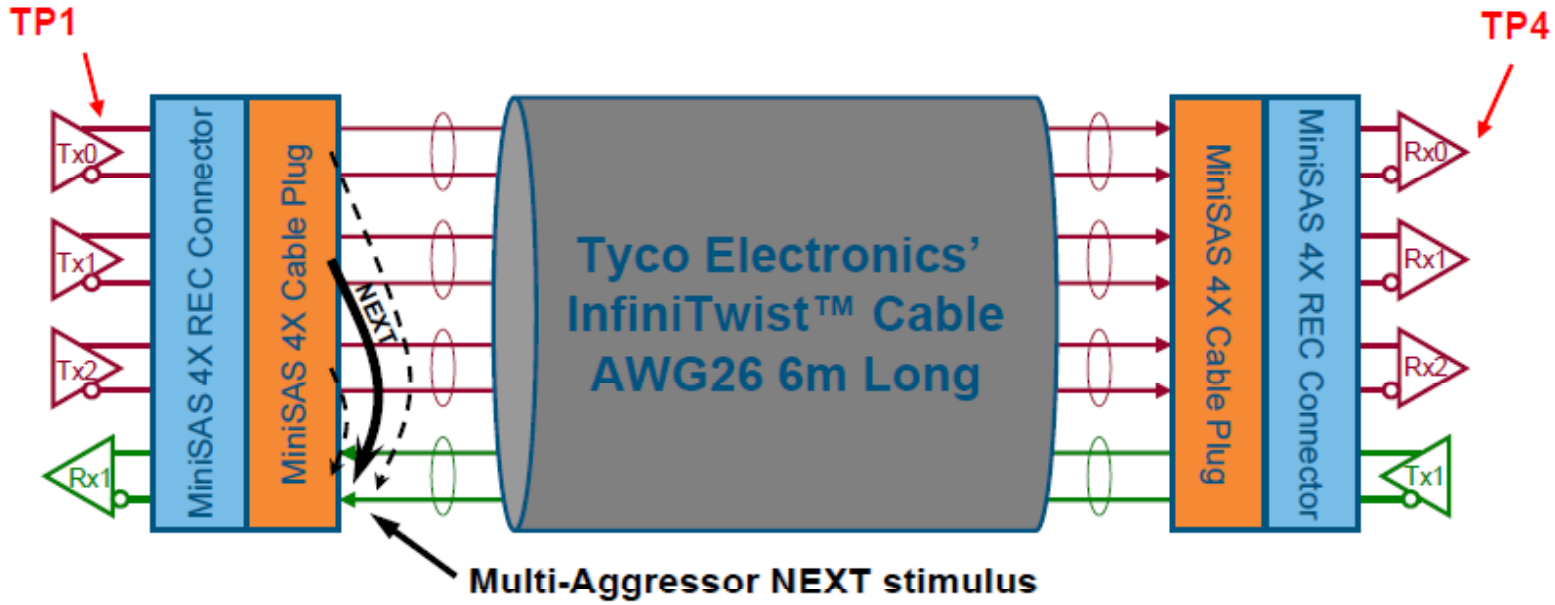
Complete Tektronix Storage Instrument Portfolio

RSG/RMT Tests **RSG/RMT**- Receiver jitter (synthesized ISI) and amplitude sensitivity compliance and margin test. To 6Gbps	**AWG7122B with Opt.1, 6 and 8** SerialXpress Digital Signal Generation
RSG/RMT Tests **RSG/RMT**- Receiver Silicon characterization and compliance testing capability to 26Gbps	**BSA125C** with **JMAP** and SSC and **HW Options DPP** 125A and **CR125A** provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features.
Rx/Tx Channel Tests **ICR**: Insertion Loss Cross Talk analysis. **Rx/Tx** - Device and Host electrical channel performance, Crosstalk, Impedance and return loss	**DSA8200** 80E10 TDR Sampling Module for DSA8200 Sampling Scope S-Parameter Analysis Software 80SICON Software for DSA8200
Cable Tests Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8200** 80E08 TDR Sampling Module for DSA8200 Sampling Scope
PHY, TSG, and OOB Tests PHY – Signal timing stability and SSC analysis. TSG – Transmitter AC parametric, Jitter, Amplitude. OOB- Out Of Band signal validation	**DSA72004B** DPOJET Jitter Analysis software SMA Adapters TCA-SMA 2 per scope Differential SMA Probe P7313SMA (optional)

Enabling Innovation in the Digital Age

Backup-Material

MiniSAS 4X External Cable Channel Model



Tx Side

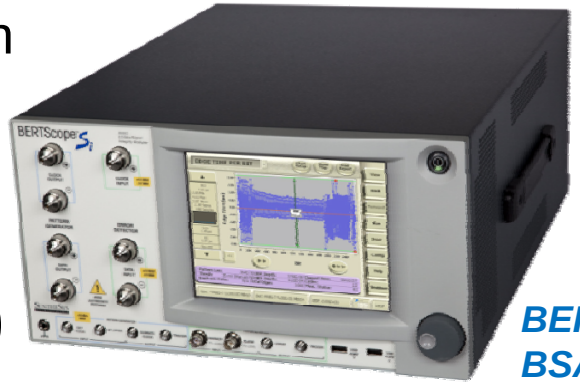
- PRBS 2^{12}-1 @ 12Gb/s Encoded 8B/10B
- 0.67V_{p-p}
- 20ps signal risetime (20% - 80%)
- 3.5dB Pre-emphasis (Max 1.0V_{p-p})
- RJ_{p-p}=0.1UI, DJ_{p-p}=0.15UI

Rx Side

- BER ≤ 10^{-12}
- Optimized DFE Equalization
- TP4 is after Equalization

Summary of BERTScope Rx Test Capabilities for SAS 12G

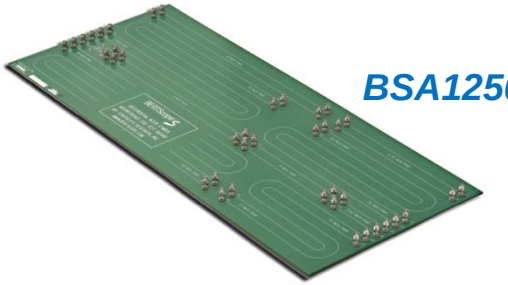
- BERTscope Stressed Pattern Generation
  - ✓Random Jitter
  - ✓Sinusoidal Jitter
  - ✓Pre-emphasis (DPP125A)
  - ✓Differential Mode Interference
  - ✓Common Mode Interference
  - ✓Calibration Channel (ISI Board)
- BERTScope Error Detection
  - ✓Clock Recovery (CR125A)
  - ✓Automated Jitter Tolerance Test



BERTScope BSA85C

DPP125A

CR125A

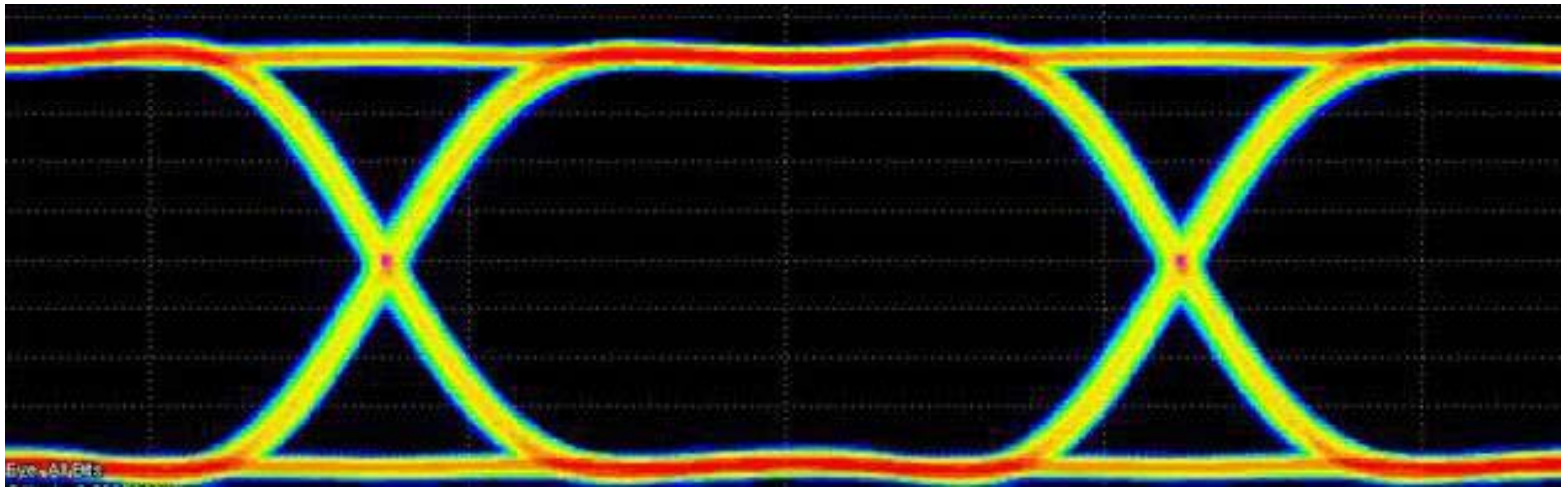


BSA12500ISI

Tektronix

8 Gb/s Eye Diagram

Tektronix 20 GHz Real Time, Rise Time 29ps



Tektronix 50 GHz Equiv. Time, Rise Time 29ps