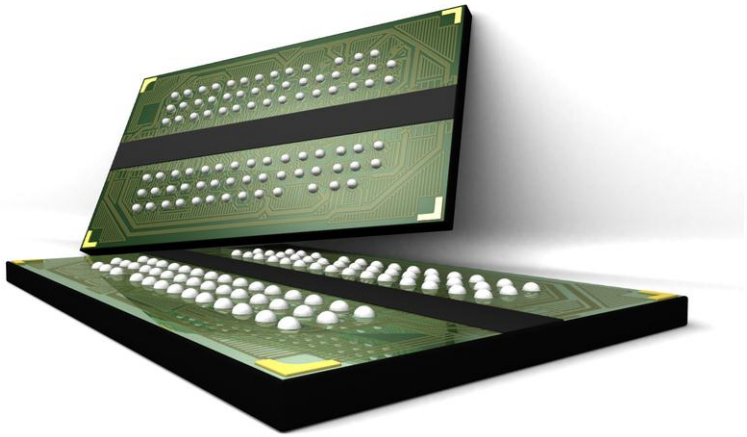
DDR PHY Test Solution



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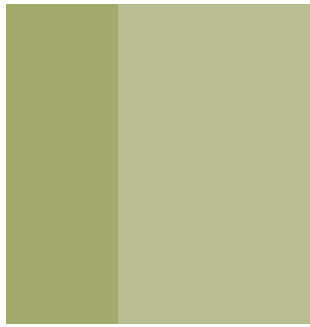
Agenda

- DDR Technology Overview and Roadmap
- DDR4
  - Specification Changes
- LPDDR3
  - Specification Changes
- Visual Triggering – VET
- DDRA Software
  - DDR4 Measurement Details
- Tektronix Probing Solution for DDR
  - DDR4 Scope Interposers
- Tektronix DDR Solution – Features and benefits

DDR Technology Overview & Roadmap



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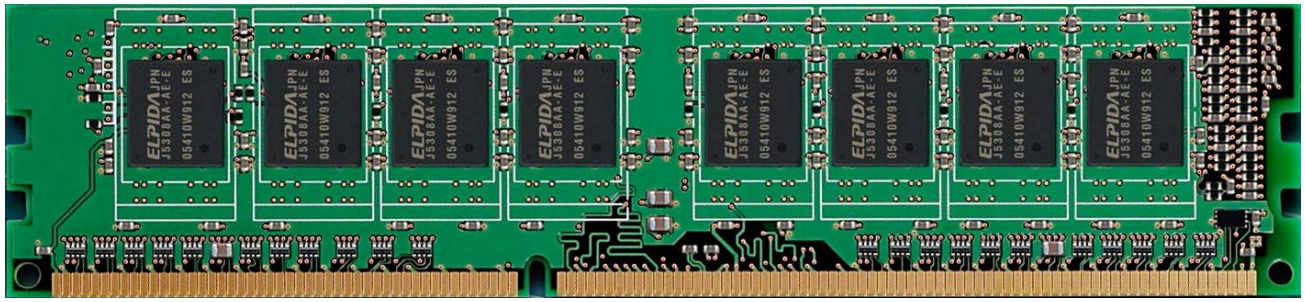
Memory Technology Overview

- DRAM - Dominant Memory Technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMM, SODIMM
  - Embedded systems
    - Cell phones, Ultra-Thin Notebooks, iPADs
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR4 release on 26th Sep 2012 Maximum 3200 MT/s data rates transfer
    - LPDDR3-E planned can go unto 2133MT/s
    - DDR3L operates at 1.35V
    - DDR3U operates at 1.25V
- DRAM variants
  - DIMM based - Speed and Performance
    - DDR, DDR2, DDR3 and DDR4
  - Low Power DDR
    - LPDDR, LPDDR2, LPDDR3, LPDDR3E, LPDDR4
  - Graphic DDR - Optimized for Speed - faster access
    - GDDR3, GDDR5 @ 5500 MT/s
  - Low Voltage DDR
    - DDR3L, DDR3U



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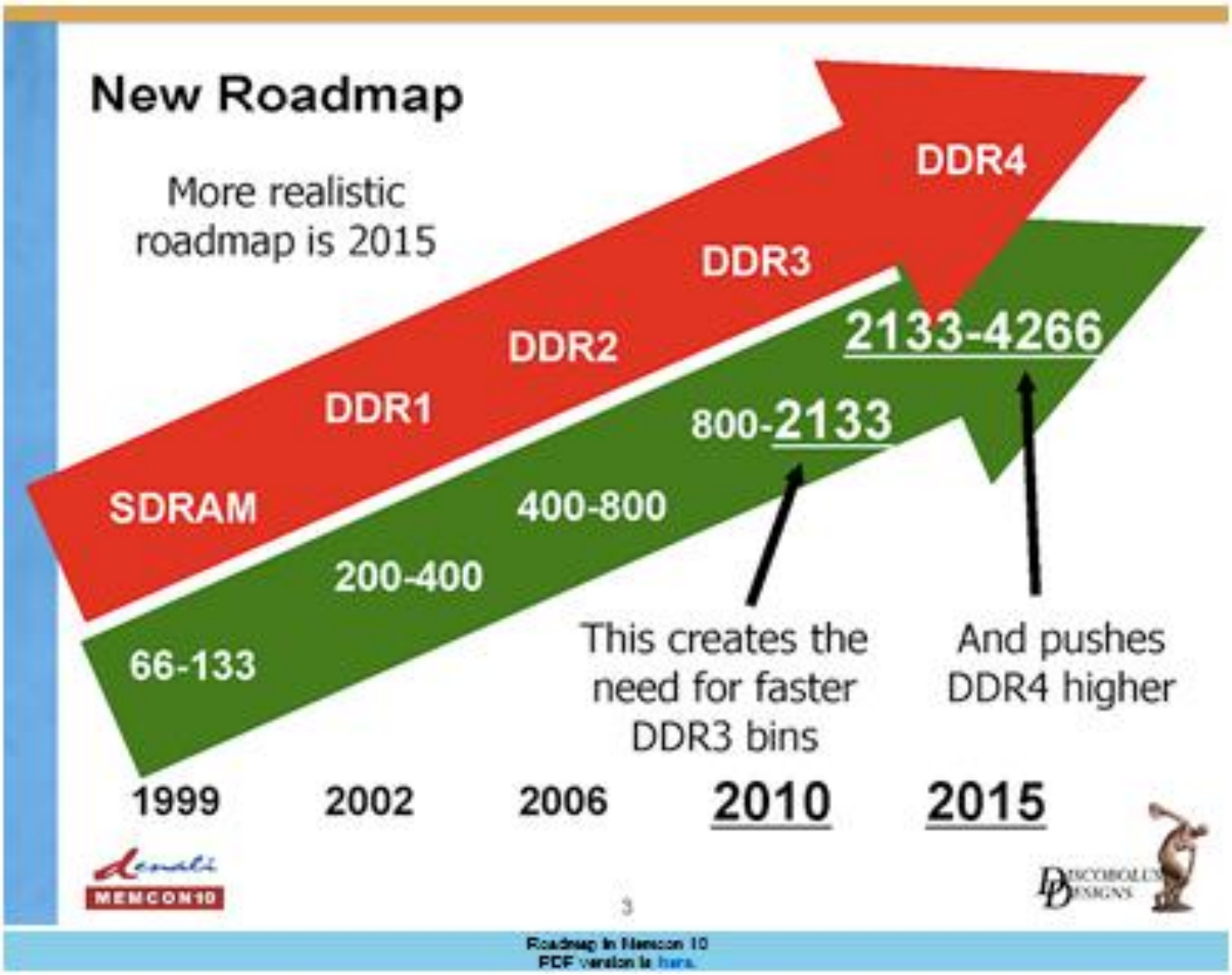
Memory Market Trends – Main Stream



Memory Market Trends - LPDDR

Mobile DRAM Technology Trend

- **Bring up right technology at right on time**
  - LP2-800 (‘10) → LP3-1600(‘12) → LP4-3200(‘14)

	’10	’11	’12	‘13	‘14	‘15
Interface VDD/VDDQ	LPDDR2 1.2V/1.2V		LPDDR3 1.2V/1.2V		LPDDR4	
				WIO and WIO2		
Speed	6.4GB/s	8.5GB/s	12.8GB/s		25.6GB/s+	
Density	2Gb	4Gb			8Gb	
PKG	Up to 4 die stacks : 1.0 mm → 0.9mm and below					

*Source : Samsung Presentation JEDEC Mobile Event Seoul

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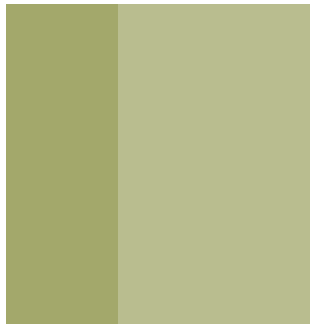
DDR4



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DDR4 DIMM

- SAMSUNG(三星), HYNIX(海力士), MICRON(美光) have DDR4 products
- ELPIDA(尔必达), NANYA(南亚) and other will have products by end of 2012
- DDR4 → 50% market share by 2015

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Specification Changes – DDR4

- Speeds 1600 – 3200 MT/s - JESD79-4 September 2012
- Voltage 1.2V or less
- V-center(avg) – New concept
- Derating measurements removed
- Mask-based versus setup/hold-based methodology
  - Removed tIH/tIS and tDS/tDH values
  - Added mask keep-outs
- Densely packed DIMM's with narrow spacing between components
- Statistical jitter approach planned for speeds >2133
  - Jitter 1600-2133 assumed to be all DJ
  - Jitter >2133 both DJ and RJ
- Electrical signaling
  - Pull-ups to 1.2V changes tri-state voltage
  - Read and Write use positive strobe pre-amble – Phase Alignment challenges

DDR4 Specification - The DQ input receiver compliance mask for voltage and timing

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	-	tbd	-	tbd	-	mV	7

12.4 The DQ input receiver compliance mask for voltage and timing is shown in the figure below

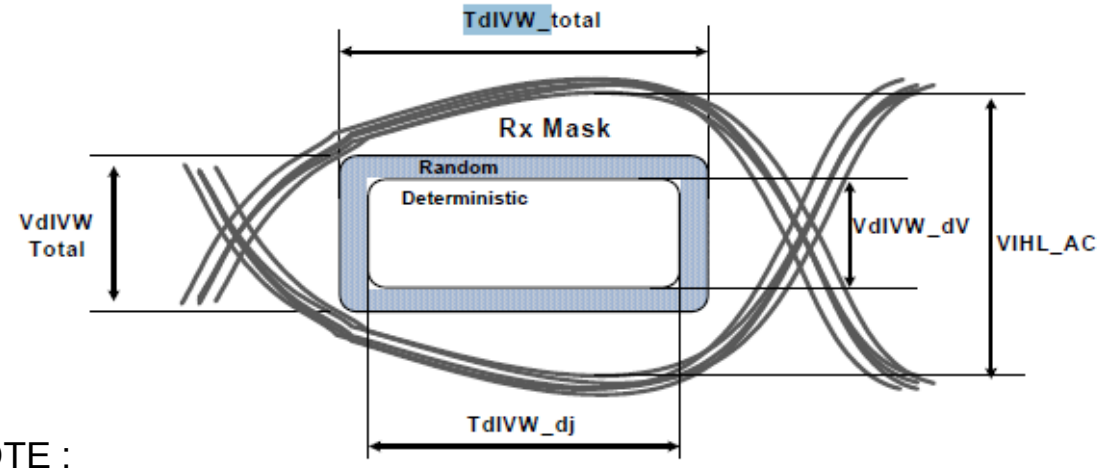

Figure 186 — DQ Receiver(Rx) compliance mask

JEDEC DDR4 draft v.99, AUG-2012, Page 224

NOTE :

- 1. For DQ in receive mode.
- 2. Data Rx mask voltage and timing total input valid window. Data Rx mask applied per bit post training and should include voltage and temperature drift terms. Design Target BER< tbd. Measurement method tbd.
- 6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd

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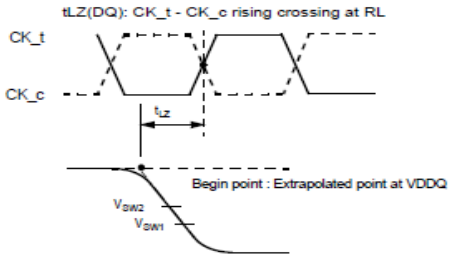
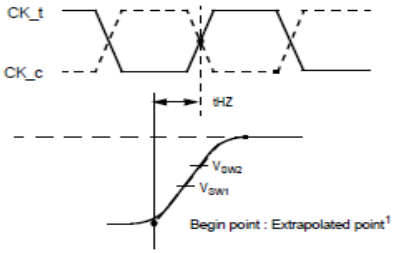
tLZ and tHZ Measurements



tLZ(DQ) begin point is above-mentioned extrapolated point.

tHZ(DQ) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK
tHZ(DQ) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK



tLZ(DQ) is begin point is above-mentioned extrapolated point.

NOTE : 1. Extrapolated point (Low Level) = VDDQ - ((VDDQ/(50+34)) X 34)
- Ron = 34ohm
- Reference Load= 50ohm

Figure 67 — tLZ and tHZ method for calculating transitions and begin points

[Table 41] Reference Voltage for tLZ, tHZ Timing Measurements

Measured Parameter	Vsw1	Vsw2	Figure	Note
tLZ	TBD	TBD	Figure 60	
tHZ	TBD	TBD		

tLZ is a two source timing measurement starting from the extrapolated point (at VDD = 1.2V) got by extending the slope between Vsw1 and Vsw2 to the nearest rising edge of clock.
tHZ is a two source timing measurement starting from the extrapolated point (at Vdd – Vdd(34/(50+34)) got by extending the slope between Vsw1 and Vsw2 to the nearest rising edge of clock.

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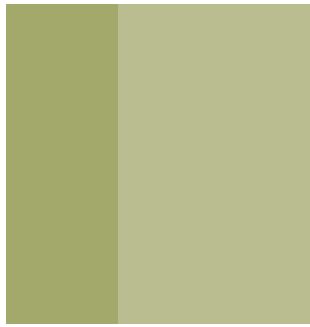
Derating

- Derating has been removed from the DDR4 spec. It will still apply to previous DDR specifications.
- Why?
  - Derating was not being used by many engineers due to dependence on DQS slew rate measurement
  - Not supported in simulation environment tool sets
  - Not supported in persistence test environment with RT scope
- DDR4 relies on DQ eye mask, similar to high speed serial
  - ≤ 2133, eye closure assumed to be DJ dominated
  - >2133, both RJ and DJ considered
- Practical vs. statistical approach
  - Practical approach ≤ 2133
  - Statistical approach will apply > 2133

LPDDR3



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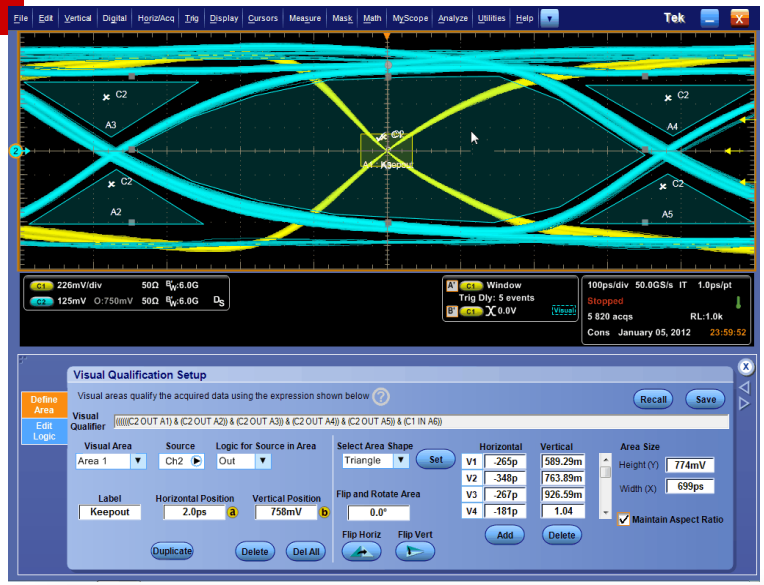
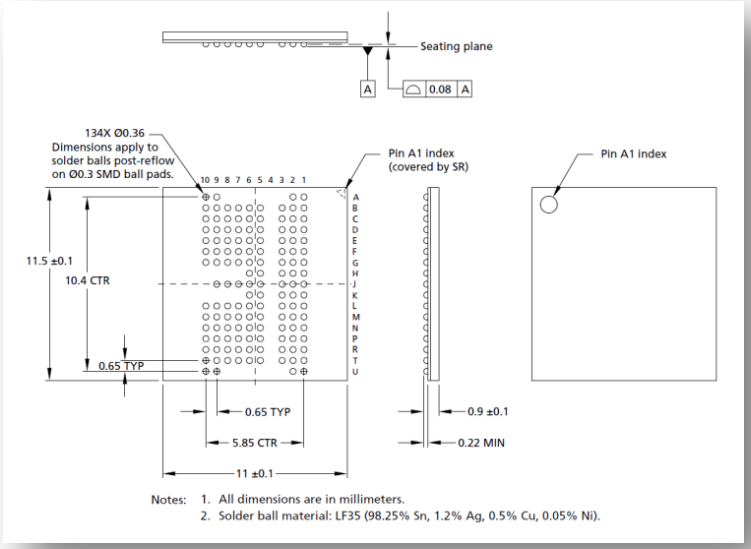
Mobile Memory = Faster, Smaller, Less Power





LPDDR3 Key Features

- Speed and Capacity
  - LPDDR3 achieves a data rate of 1600 Mbps (vs. 1066 Mbps for LPDDR2)
  - 4, 8, 16, 32Gb Package Options
- Battery Conservation
  - Low Voltage (300mV – 1.2V MAX)
  - Voltage Ramp and Device Initialization
    - Temperature-compensated(refresh less often at low temperatures) and partial array self refresh modes
    - Deep power down mode which sacrifices all memory contents
- Compact Packaging
  - PoP and Discrete Packages

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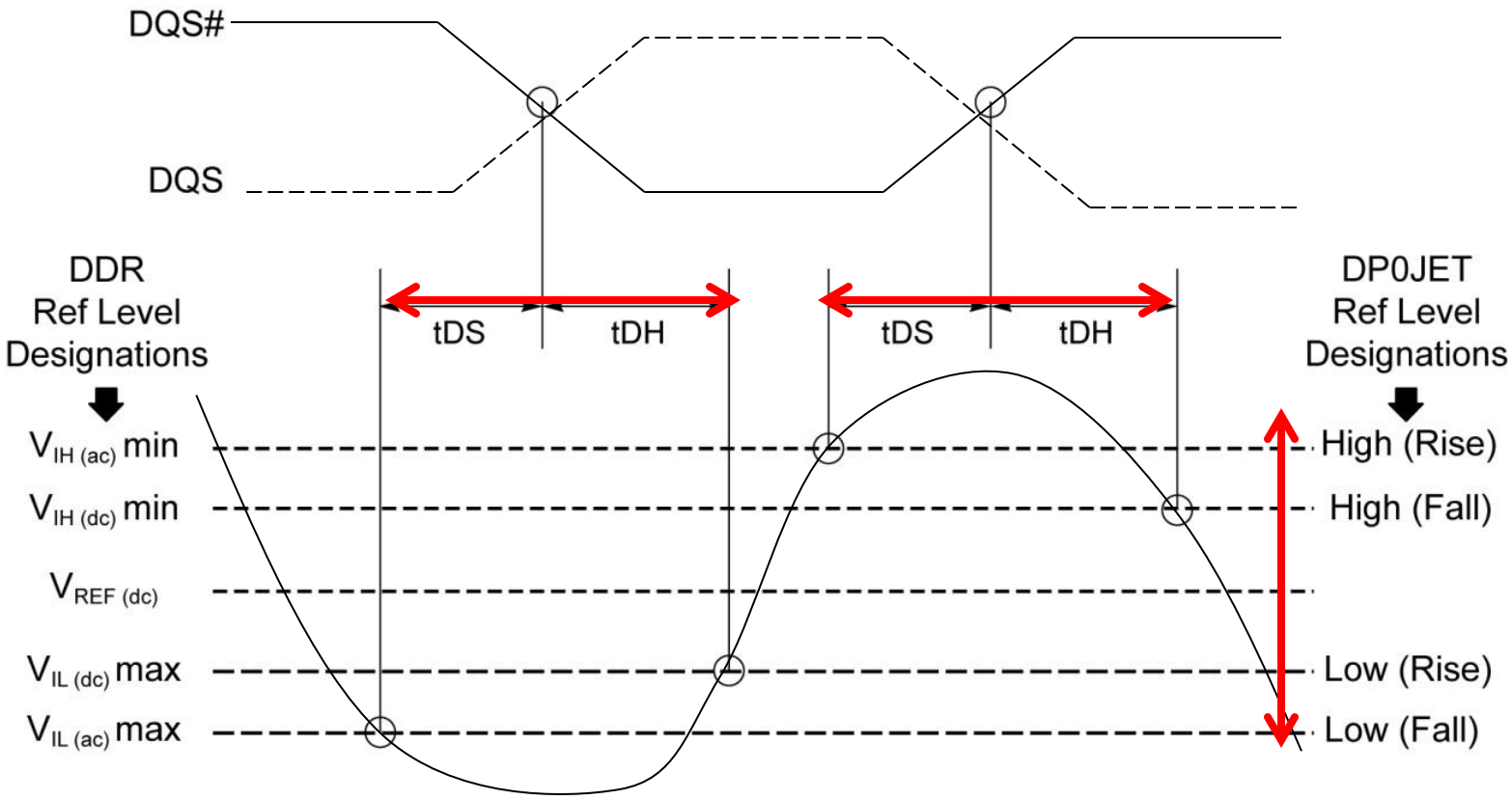
Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR:
- 1.8 V
- 200MHz



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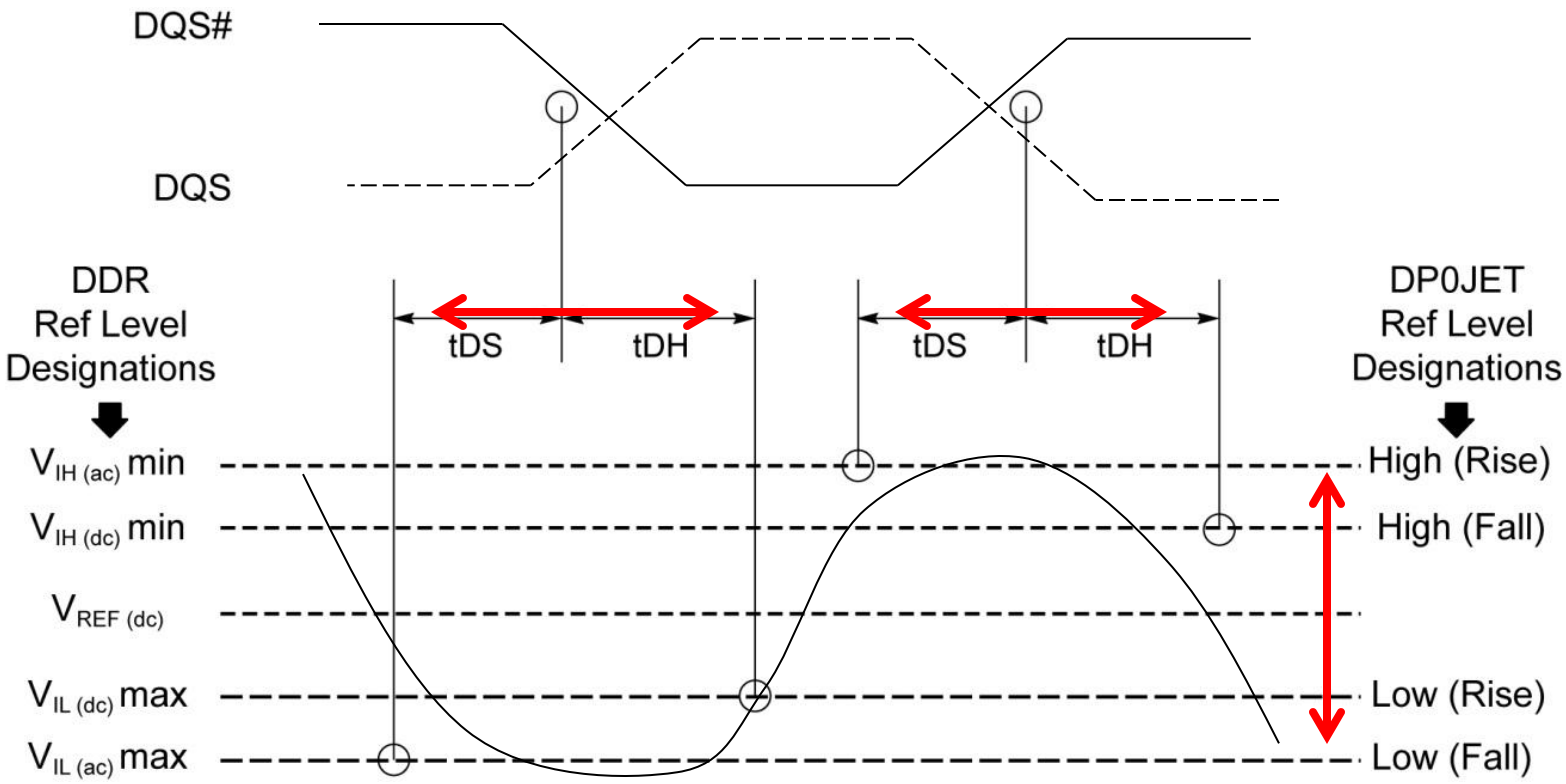
Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

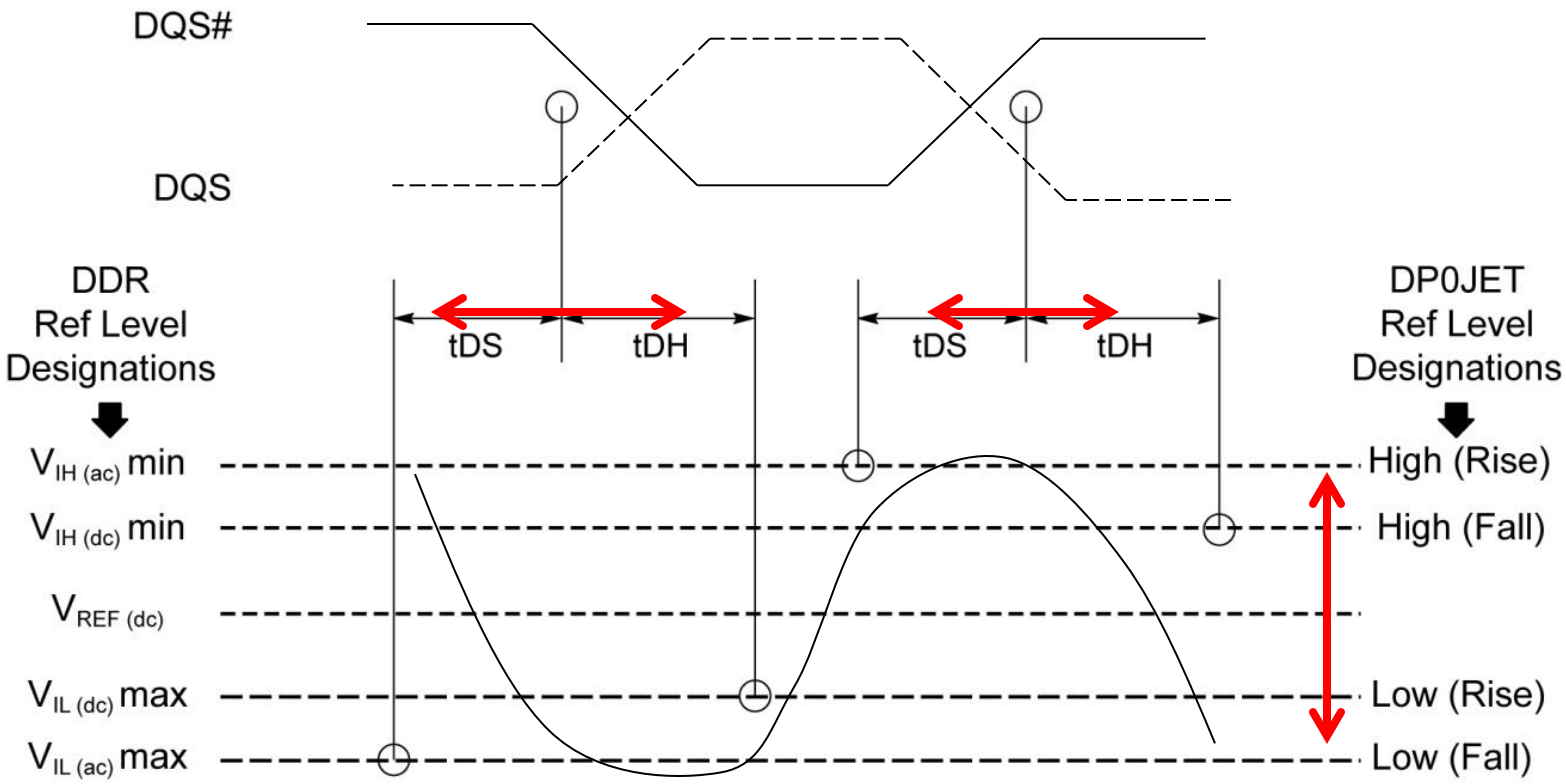
LPDDR2:
- 1.2 V
- 533MHz



Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR3:
- 1.2 V
- 800MHz



Faster Clock Frequencies

- Verifying Clock Cycles on shorter (1.25 ns) Clock Periods
  - Measurement Challenges: Do I have the right instrument settings to capture with proper margin?

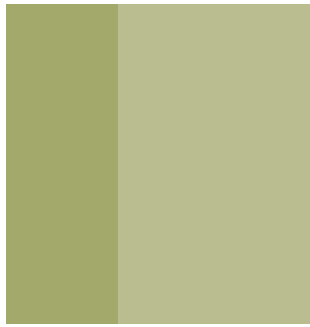
11.4 LPDDR3 Read and Write Latencies

Parameter	Value							Unit
Max. Clock Frequency	166	400	533	600	667	733	800	MHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	Mbps
Average Clock Period	6	2.5	1.875	1.67	1.5	1.36	1.25	ns
Read Latency	3[1]	6	8	9	10	11	12	t_{CK}(avg)
Write Latency	1[1]	3	4	5	6	6	6	t_{CK}(avg)

NOTE 1 RL=3/WL=1setting is an optional feature. Refer to supplier's Mode Register 2 settings.

	LPDDR2	LPDDR3
Max SE Slew Rate (V/ns)	3.5	4
Typical Clock Rate (MHz)	400	800
Period (ns)	2.5	1.25
Rise Time, 10% - 90% (ps)	738	369
Typ. Signal Swing (V)	0.8	0.8
Min. Rise Time (ps)	229	200

Visual Trigger & Masks



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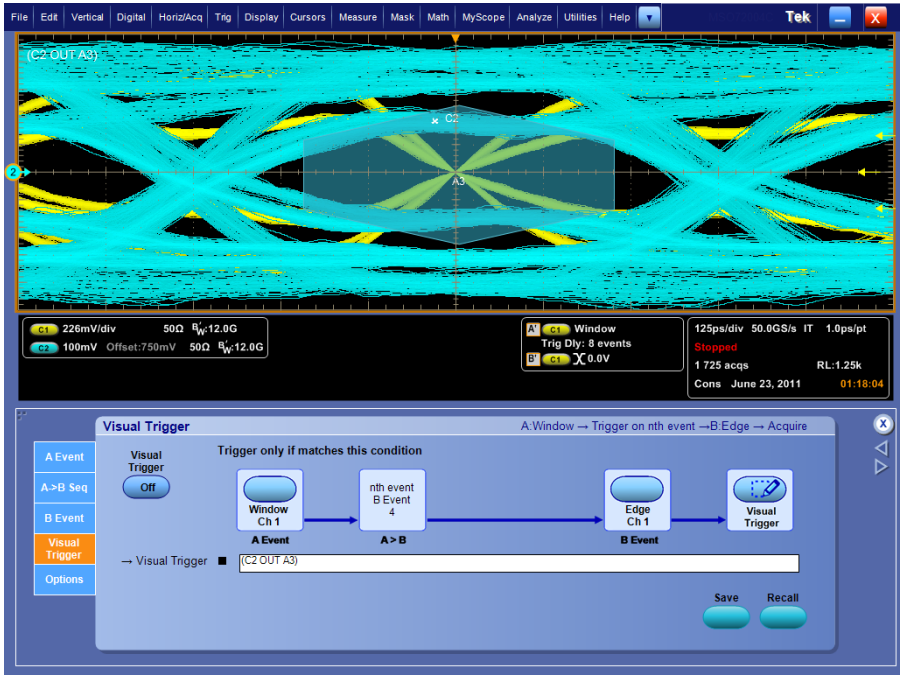
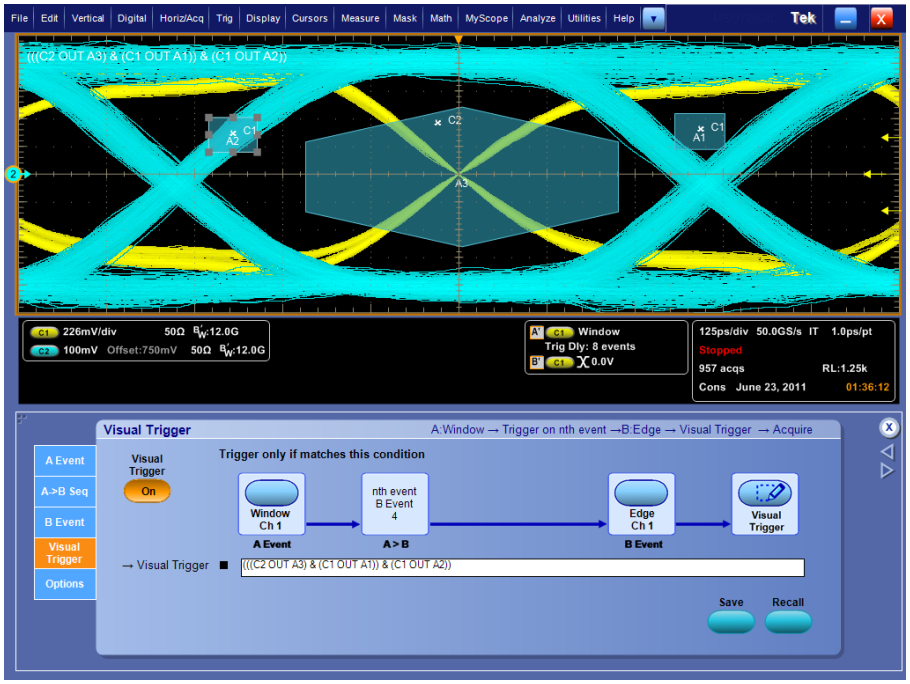
Visual Visual Tools – DDR Eye Diagram

- Hexagon shaped area applied to DQ used as a keep-out zone to isolate only target rank of interest.
- Use additional areas to target specific DQ patterns.

Before



After applying Visual Triggering Tool



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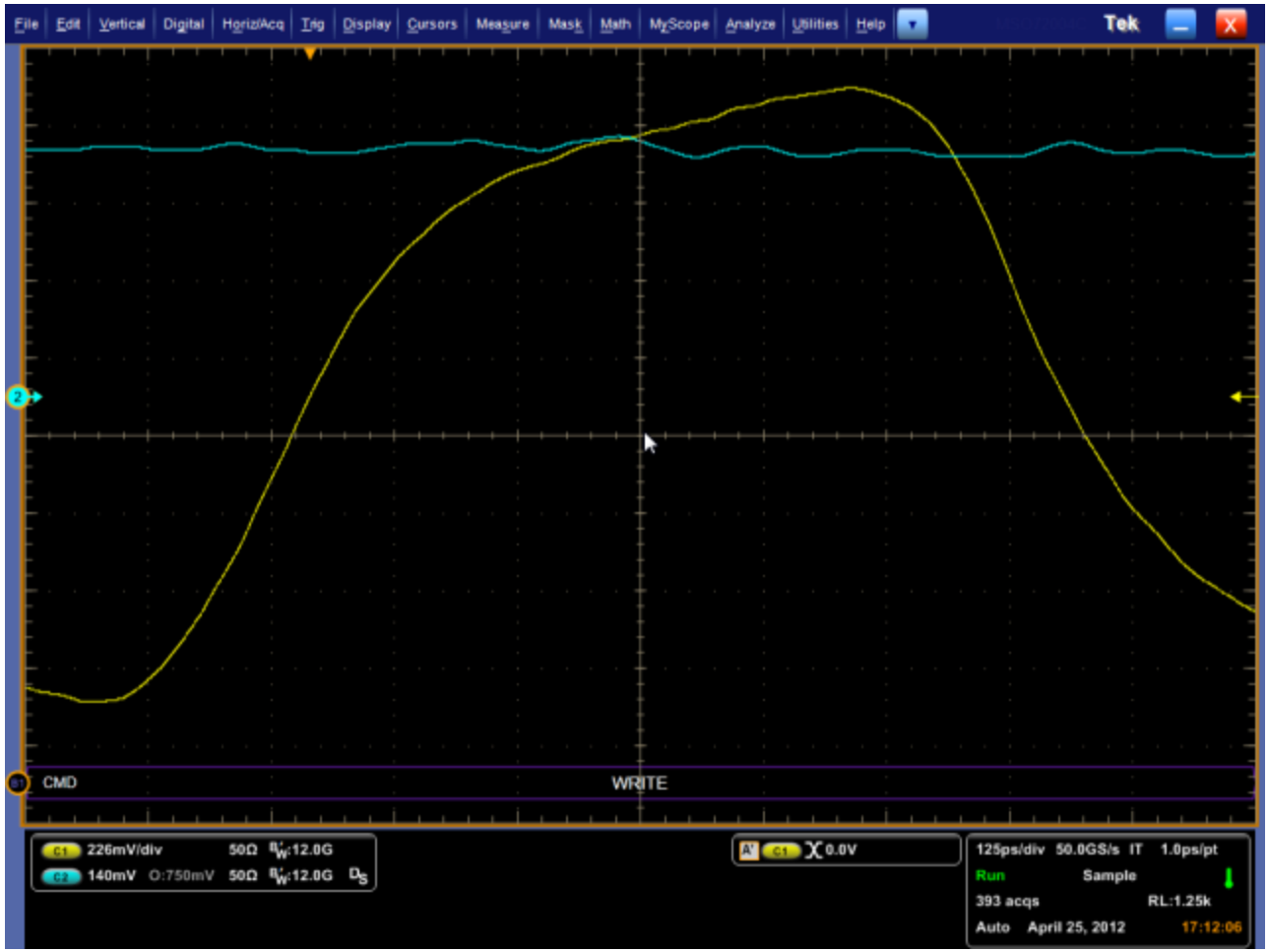
Visual Trigger

- Quick evaluation of DQ Signals



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Visual Trigger

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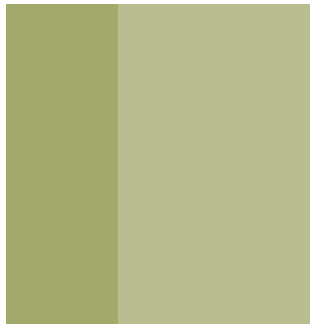
DDRA



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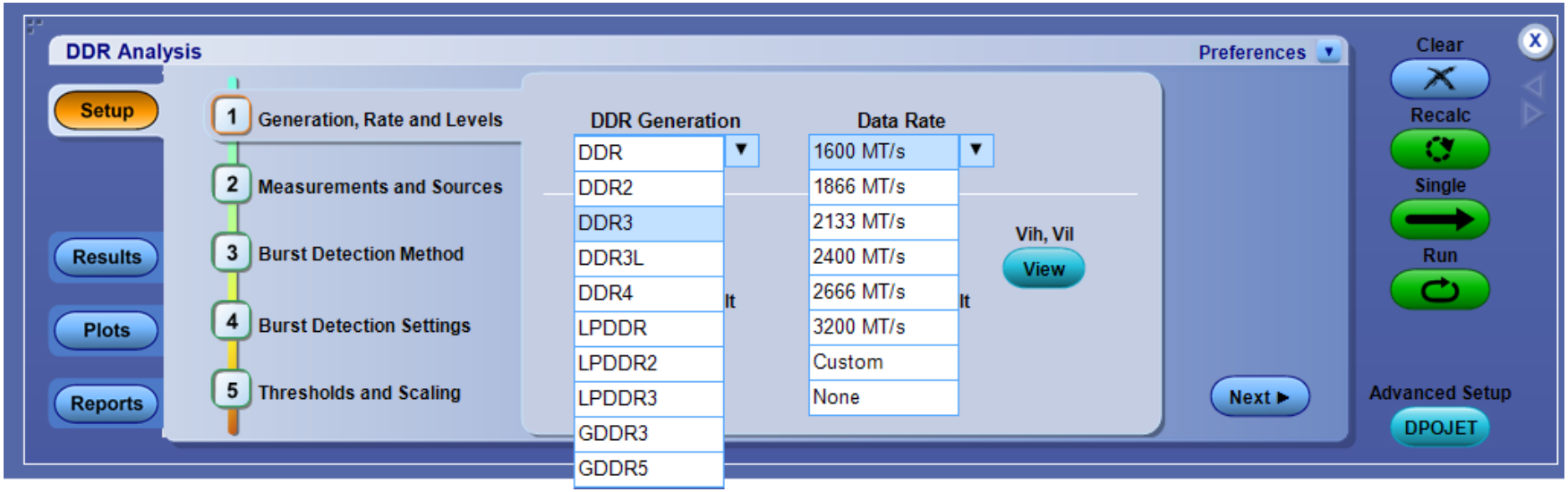
Support for Multiple DDR Generations

- **DDRA = One Application SW Package**
  - **DDR**
  - **DDR2**
  - **DDR3**
  - **DDR3L (Q4-12/Q1-13)**
  - **DDR4 (Q4-12/Q1-13)**
  - **LPDDR**
  - **LPDDR2**
  - **LPDDR3 (Q4-12/Q1-13)**
  - **GDDR3**
  - **GDDR5**



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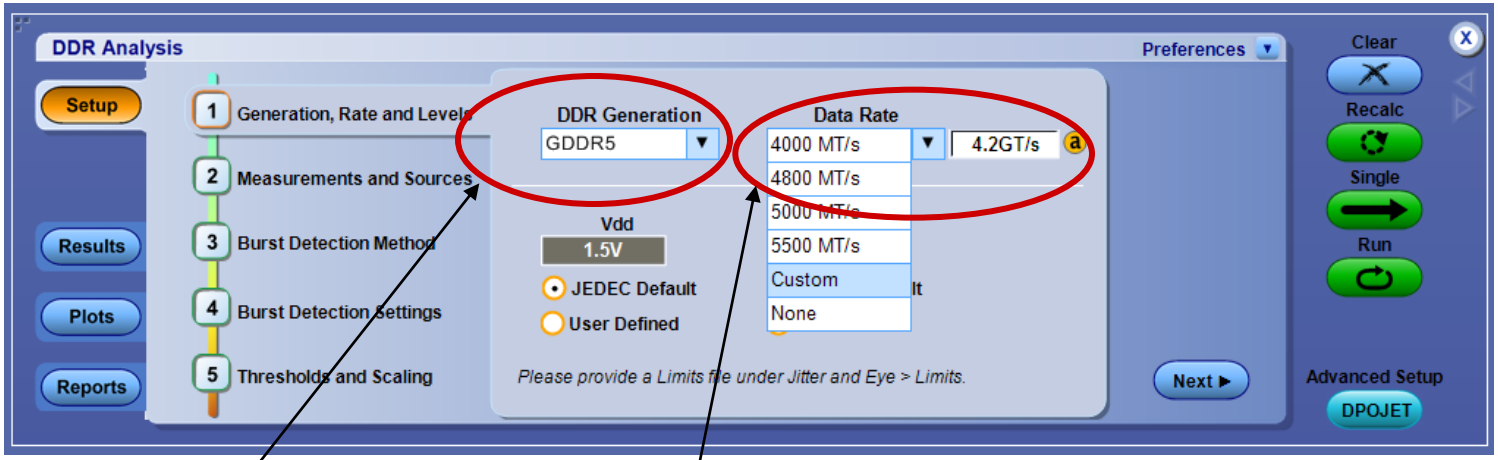
Ease of Use - DDRA Wizard

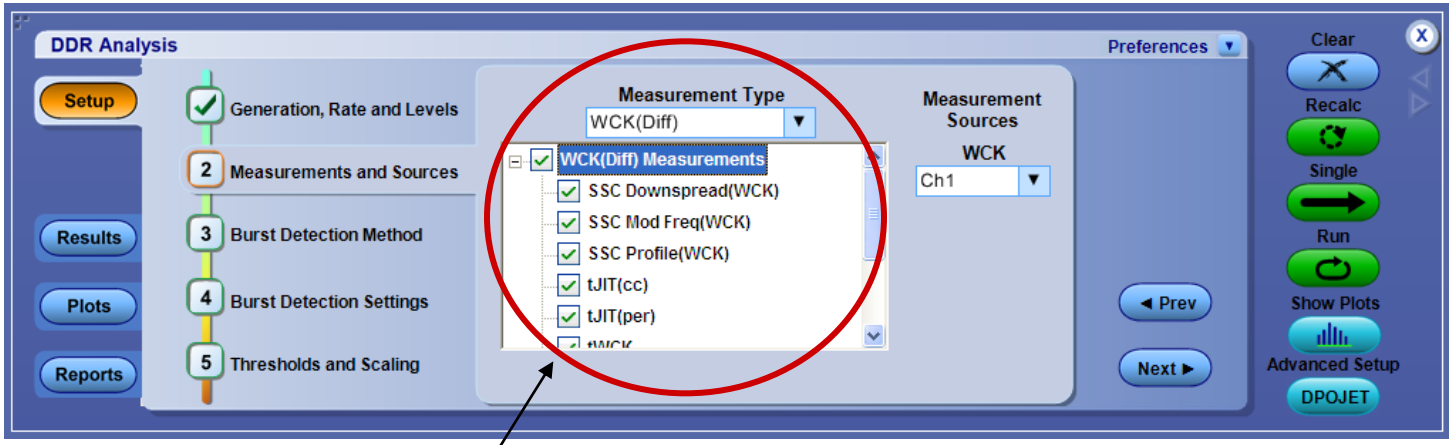
Step #1



Select DDR Generation

Select DDR Rate

Step #2



Choose measurements (Read / Write / CLK / Addr & Command)

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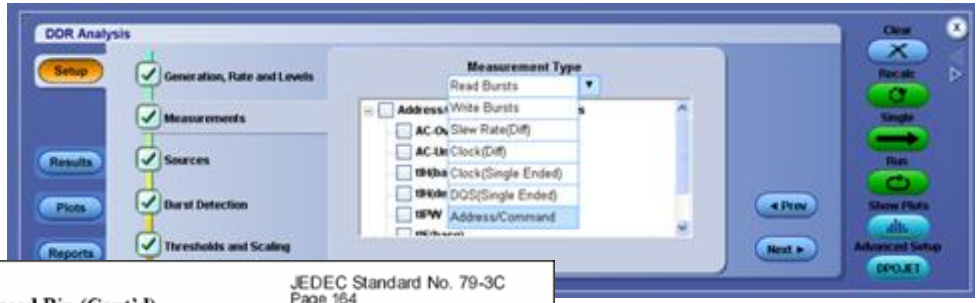
Challenge: Solving Measurement Complexity

- **JEDEC Standards specify unique measurements & methods**



JEDEC Standard No. 79-3C
Page 164

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	- 169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	- 175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	- 180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	- 184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	- 188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$^{t}ERR(nper)min = (1 + 0.68ln(n)) * {}^{t}JIT(per)min$ $^{t}ERR(nper)max = (1 + 0.68ln(n)) * {}^{t}JIT(per)max$								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK#	tLZ(DQ)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75		25		30		10		ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150		100		65		45		ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	ps	28
Data Strobe Timing											
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK(avg)	13, 19, g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 13, g
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)	13, g
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)	13, g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	- 400	400	- 300	300	- 255	255	- 225	225	ps	13, f

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Specification Changes DDR4 Measurements

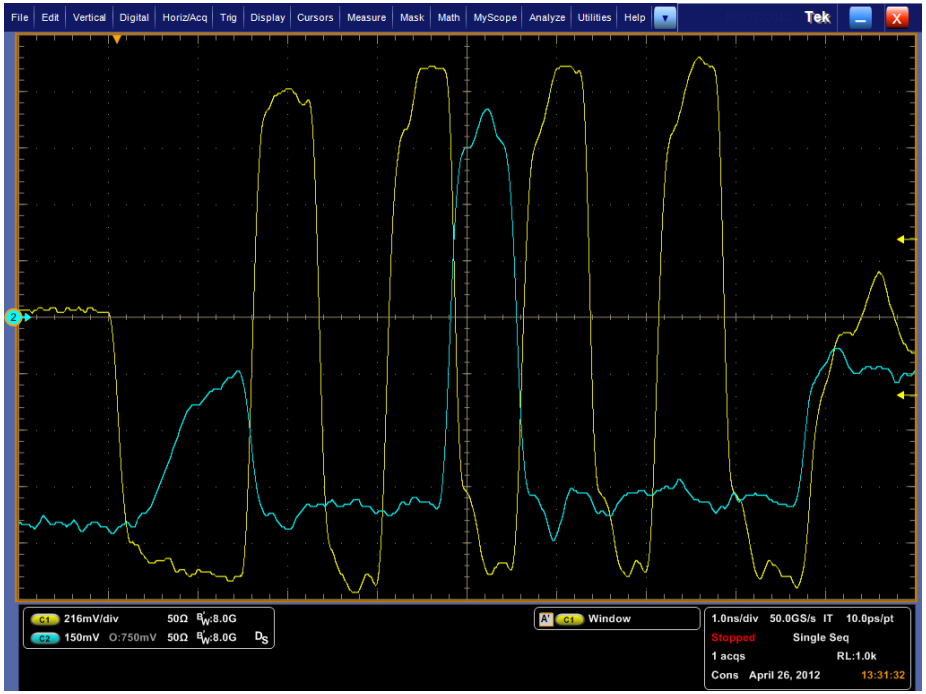
EXISTING MEASUREMENTS in DDRA			
VSEH	supported for DDR3	port to DDR4	Single-ended voltage swing - high
VSEL	supported for DDR3	port to DDR4	Single-ended voltage swing - low
AC - Overshoot Amplitude - SE	supported for DDR3	port to DDR4	DQS, DQS#, CK, CK#
AC - Undershoot Amplitude - SE	supported for DDR3	port to DDR4	DQS, DQS#, CK, CK#
Overshoot area	supported for DDR3	port to DDR4	Max overshoot area above VDD
Undershoot area	supported for DDR3	port to DDR4	Max undershoot area below VSS
tCK(avg)	supported for DDR3	port to DDR4	Clock period - average
tDQSH	supported for DDR3	port to DDR4	DQS Input high pulse width
tDQSL	supported for DDR3	port to DDR4	DQS input low pulse width
tDIPW	supported for DDR3	port to DDR4	DQ and DM Input Pulse Width
tIPW	supported for DDR3	port to DDR4	Address and Command Input Pulse Width
tIS (base)	supported for DDR3	port to DDR4	Address and Command - setup
tIH (base)	supported for DDR3	port to DDR4	Address and Command - hold
tDS - diff (base)	supported for DDR3	port to DDR4	DQ,DM Setup time to DQS(Diff/SE) - base - no derating
tDH - diff (base)	supported for DDR3	port to DDR4	DQ,DM Hold time to DQS(Diff/SE) - base - no derating
tQH	supported for DDR3	port to DDR4	DQ/DQS output hold time from DQS
tDSS	supported for DDR3	port to DDR4	DQS falling edge to CK setup time
tDSH	supported for DDR3	port to DDR4	DQS falling edge hold time from CK
tDQSQ - diff	supported for DDR3	port to DDR4	DQS - DQ Skew
tDQSCK - diff	supported for DDR3	port to DDR4	DQS output access time from CK/CK
tDQSS	supported for DDR3	port to DDR4	Write command to first DQS latching transition
tWPST	supported for DDR3	port to DDR4	DQS differential WRITE postamble
tRPRE	supported for DDR3	port to DDR4	DQS differential READ preamble
tRPST	supported for DDR3	port to DDR4	DQS differential READ postamble
tWPRE	supported for DDR3	port to DDR4	DQS differential WRITE preamble
Data Eye Width	supported for DDR3	port to DDR4	Eye Width
Data Eye Height	supported for DDR3	port to DDR4	Eye Height

Specification Changes DDR4 Measurements

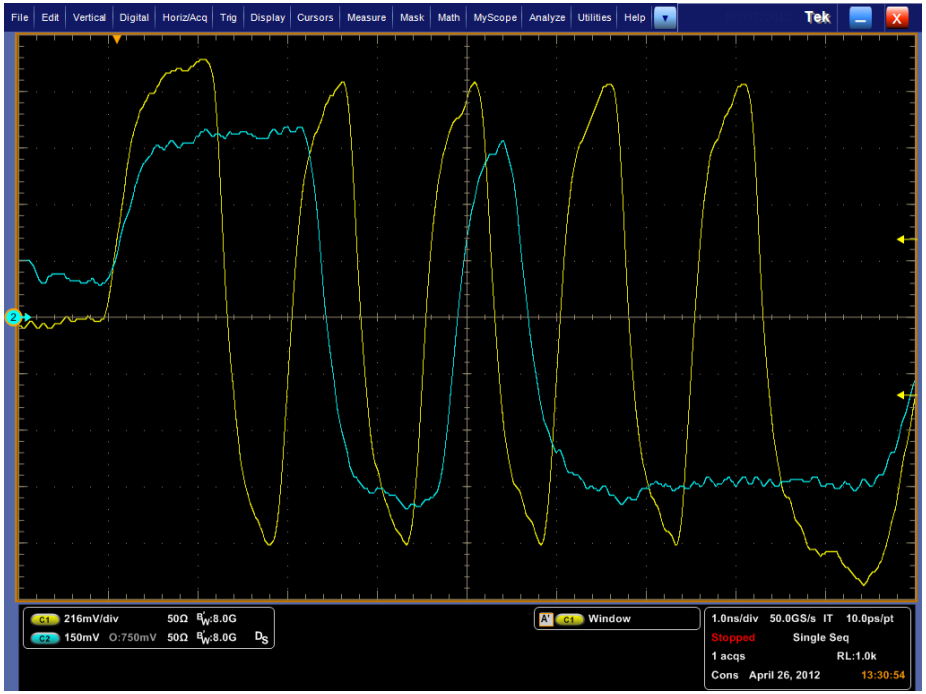
New Measurements for DDRA			Part Of New DDRA
tHZDQ		In DDR4 Spec	YES
tLZDQ		In DDR4 Spec	YES
tLZDQS		In DDR4 Spec	YES
tHZDQS		In DDR4 Spec	YES
tQSH		In DDR4 Spec	YES
tQSL		In DDR4 Spec	YES
DDR4 New Measurements			
VdIVW_total		NEW for DDR4	JEDEC TBD
VIN.RXMSK_dV		NEW for DDR4	JEDEC TBD
TdIVW_total		NEW for DDR4	JEDEC TBD
TdIVW_dj		NEW for DDR4	JEDEC TBD
VIHL_AC		NEW for DDR4	YES
TdIPW		NEW for DDR4	YES
Tdqs		NEW for DDR4	YES
Tdqh		NEW for DDR4	YES
Tdqs_dd		NEW for DDR4	JEDEC TBD
Tdqh_dd		NEW for DDR4	JEDEC TBD
SRIN_dIVW		NEW for DDR4	YES

Accurate Read/Write Burst Identification

- Locate the right kind of bursts (read vs. write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc.)



DDR3 Read Burst



DDR3 Write Burst

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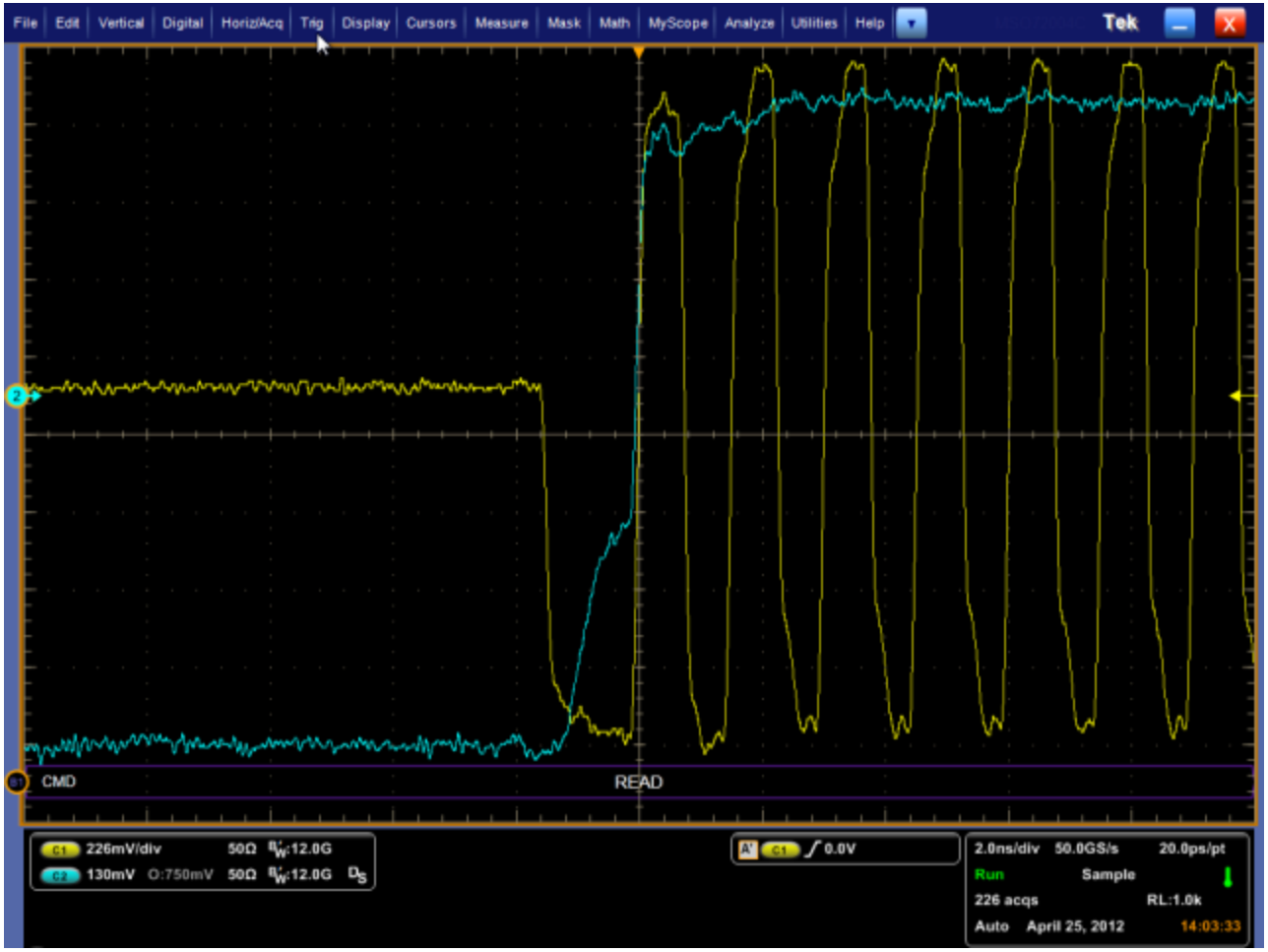
Triggering on DDR3 Signal



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Burst Detect on Command Bus using MSO Scope

- Using command bus state, specific transactions can be isolated
  - Analysis of analog signals is then used for fine burst positioning to gate measurements and this feature is available on a Mso scope

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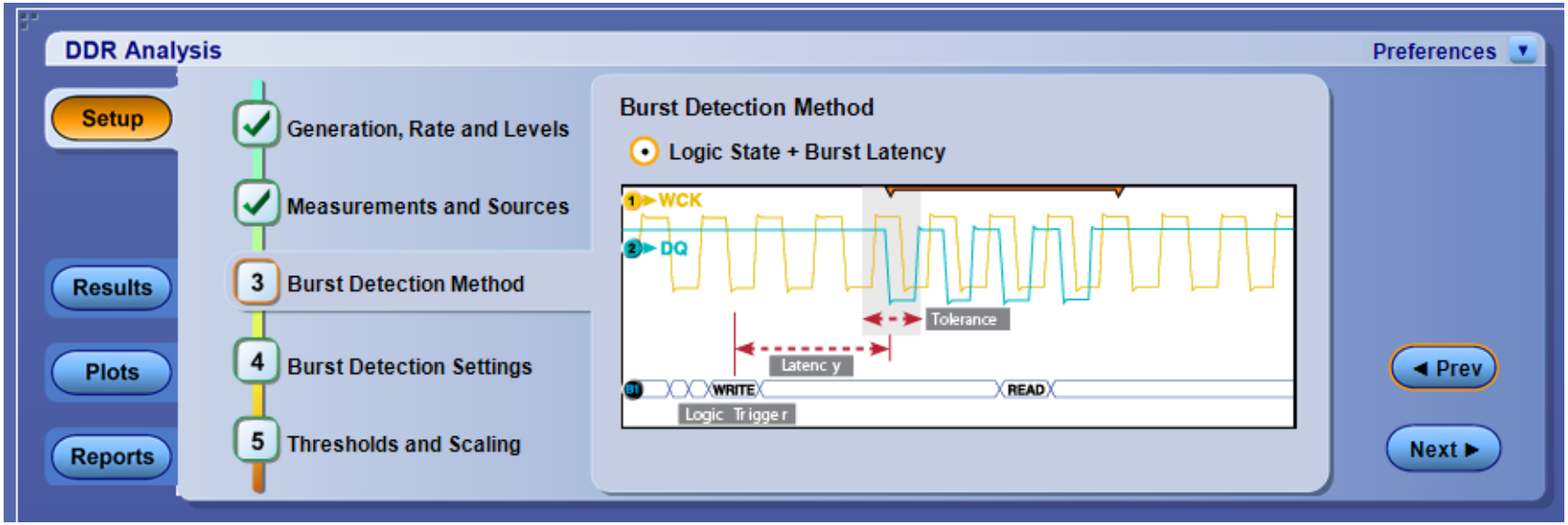
Burst Detection Method – Logic State

- Use MSO's Logic Pattern or Logic State search/mark on the DDR control bus signals (CS, RAS, CAS, WE, etc.) to capture the desired burst type
- Adjust Latency settings for particular DUT



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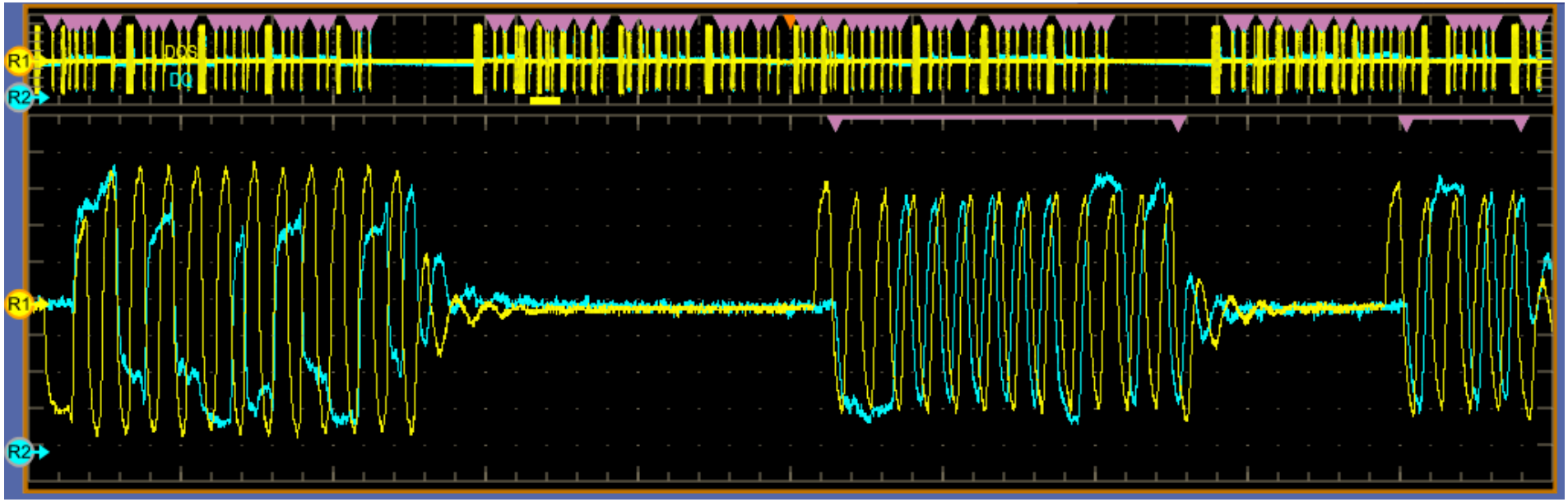
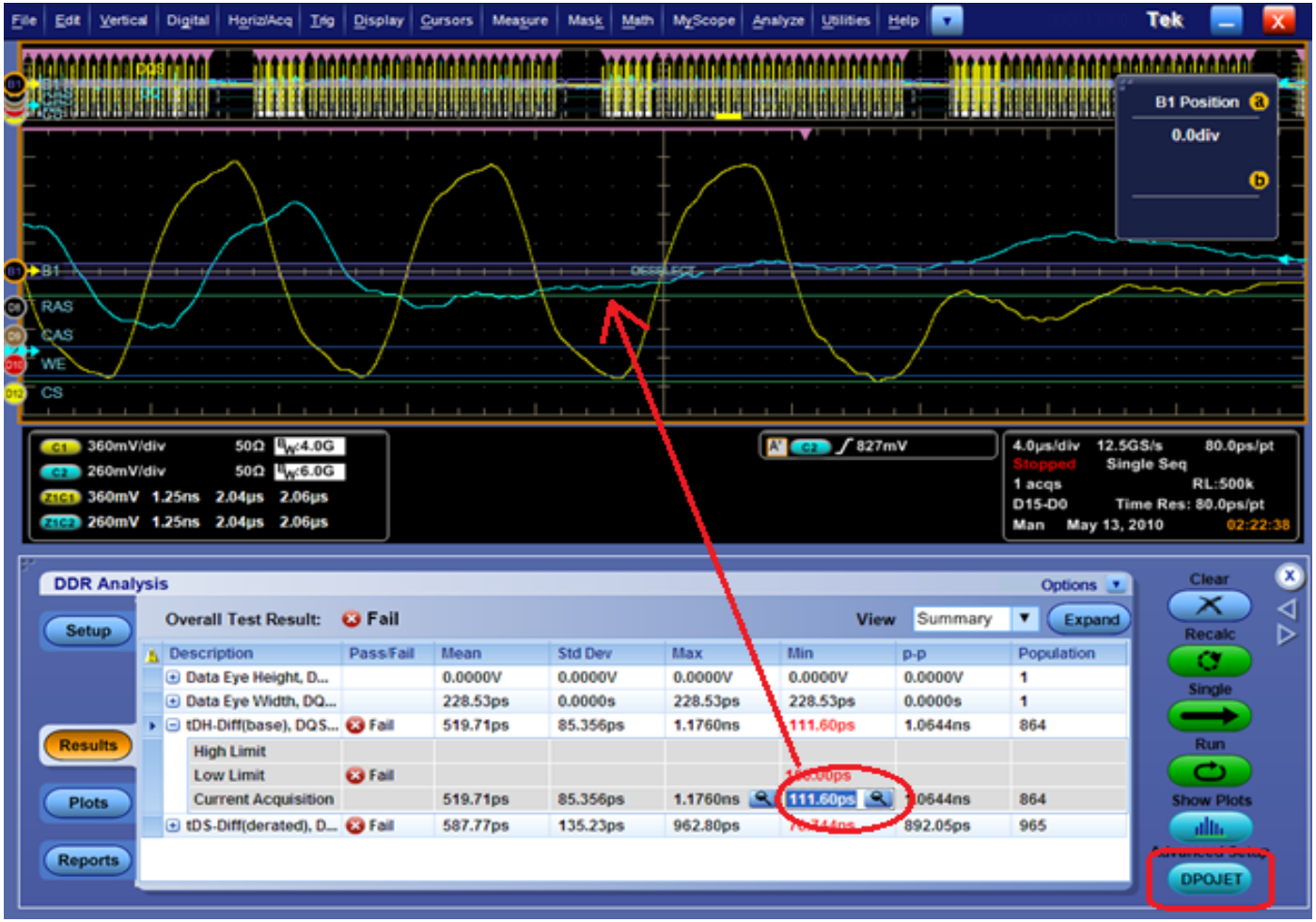
Read/Write Burst I.D. Using Search and Mark

- Advanced Search and Mark (ASM) dynamically applies a search algorithm to each acquired waveform, and marks specific features with visual delimiters
- ASM searches have been developed specifically for DDR Reads and Writes
- User controlled parameters to fine tune search algorithm
- DDRA application can read these marks and use them as measurement gates
- Single trigger post-process analysis of all parameters



What to do if compliance fails? - DPOJET

- "Find Worst Case Events" feature
  - Zoom to waveform from Min / Max for each measurement
  - Seamlessly move to DPOJET to analyze the problem and root cause



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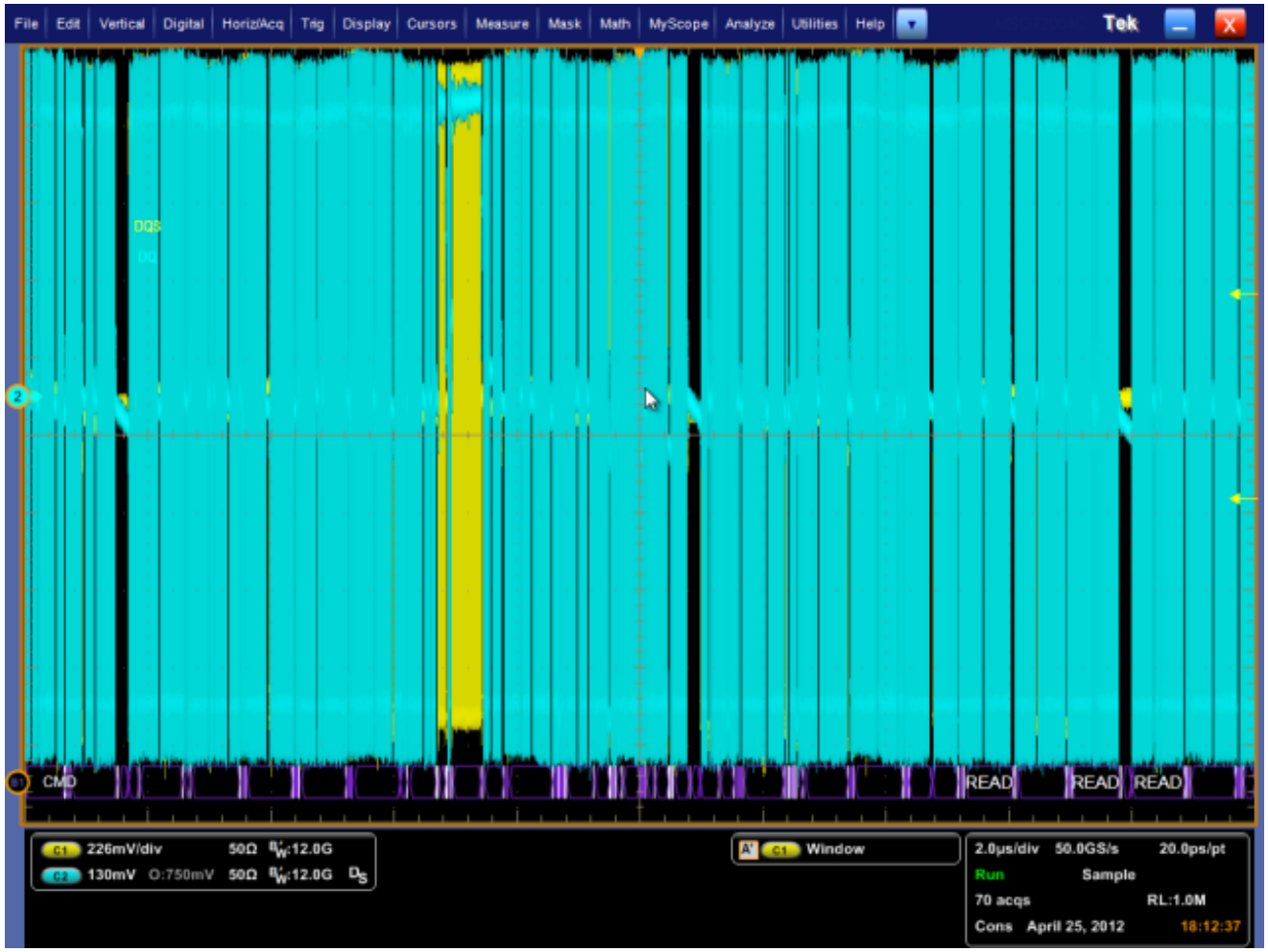
Post Processing – DDRA Software

- Simple and easy to us automations software makes life of design engineer much simple



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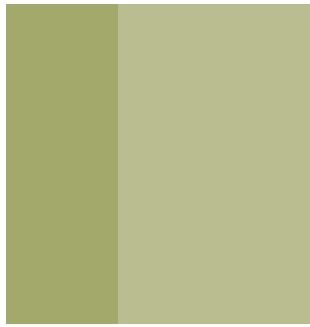
Probing Solution for DDR



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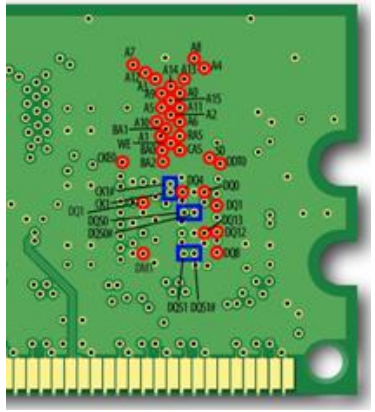
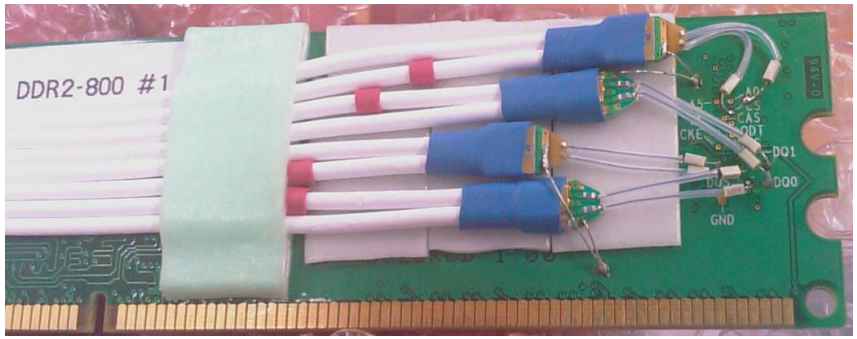
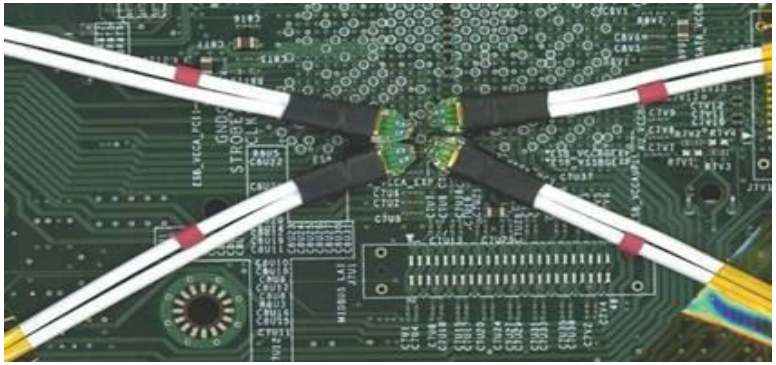
Signal Access & Probing



- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device
- Signal Access Methods
  - Direct Probing
  - Component Interposers
  - Socketed Interposers
- Probe Types
  - Analog Probing
    - DQ, DQS, Clock
  - Digital Probing
    - Address
    - Command
    - Power, Reset, and Reference





Densely packed high-speed circuits stress probe access

Analog Solder-In Probing Solutions for 70k Scopes

Socket Cable
020-2954-xx

TriMode Micro-Coax Tip
4GHz

P7500 Series
Tri-Mode Probes

P75TLRST Solder Tip
up to 20GHz

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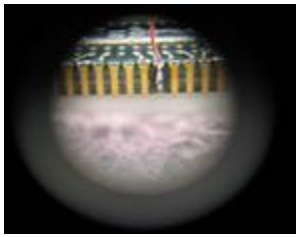
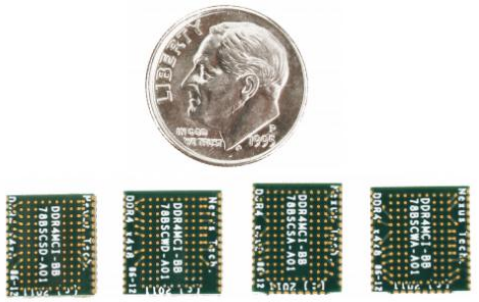
DDR4 Scope Interposers



- Form factors - x4/x8/x16 BGA versions available
- Design improvements will increase BW ~6GHz
- Built-in probe tap using 100ohm embedded resistor help place probe tip close to BGA
- De-embed filters to remove effects of interposer tap trace
- EdgeProbe Technology allows memory component size interposer
- Five versions avilable to give users maximum flexibility
  - Socketed: Full BGA visibility
    - Allows snap-in/snap-out of DDR4 components using micro socket
    - NEX-DDR4MP78BSCSK
  - Solder-down, Address/command version:
    - Narrow version, NEX-DDR4MCI78SCDSADD
    - Wide version, NEX-DDR4MCI78SCDWADD
  - Solder-down, Data version:
    - Narrow version, NEX-DDR4MCI78SCDSDAT*
    - Wide version, NEX-DDR4MCI78SCDWDAT



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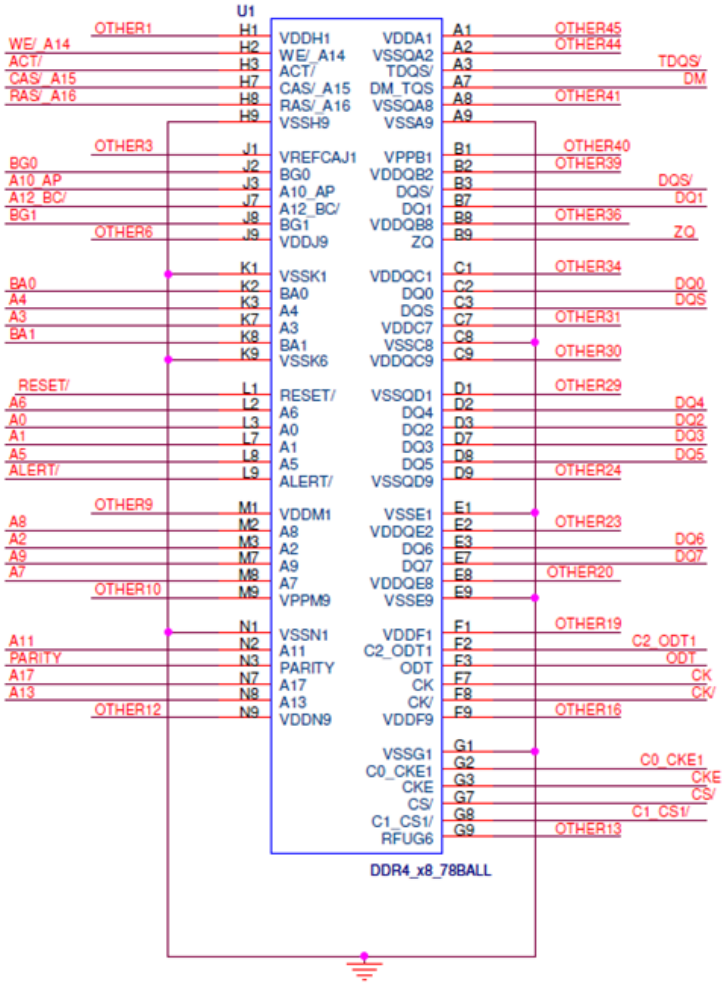
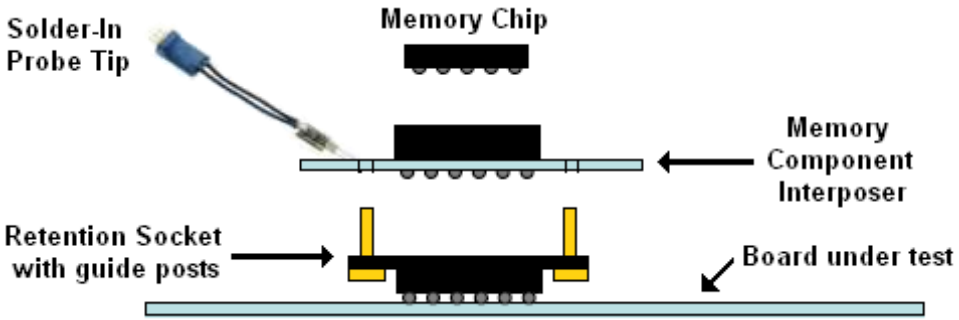
Socketed Version, All Signals
One Size, Larger Keep-out Region





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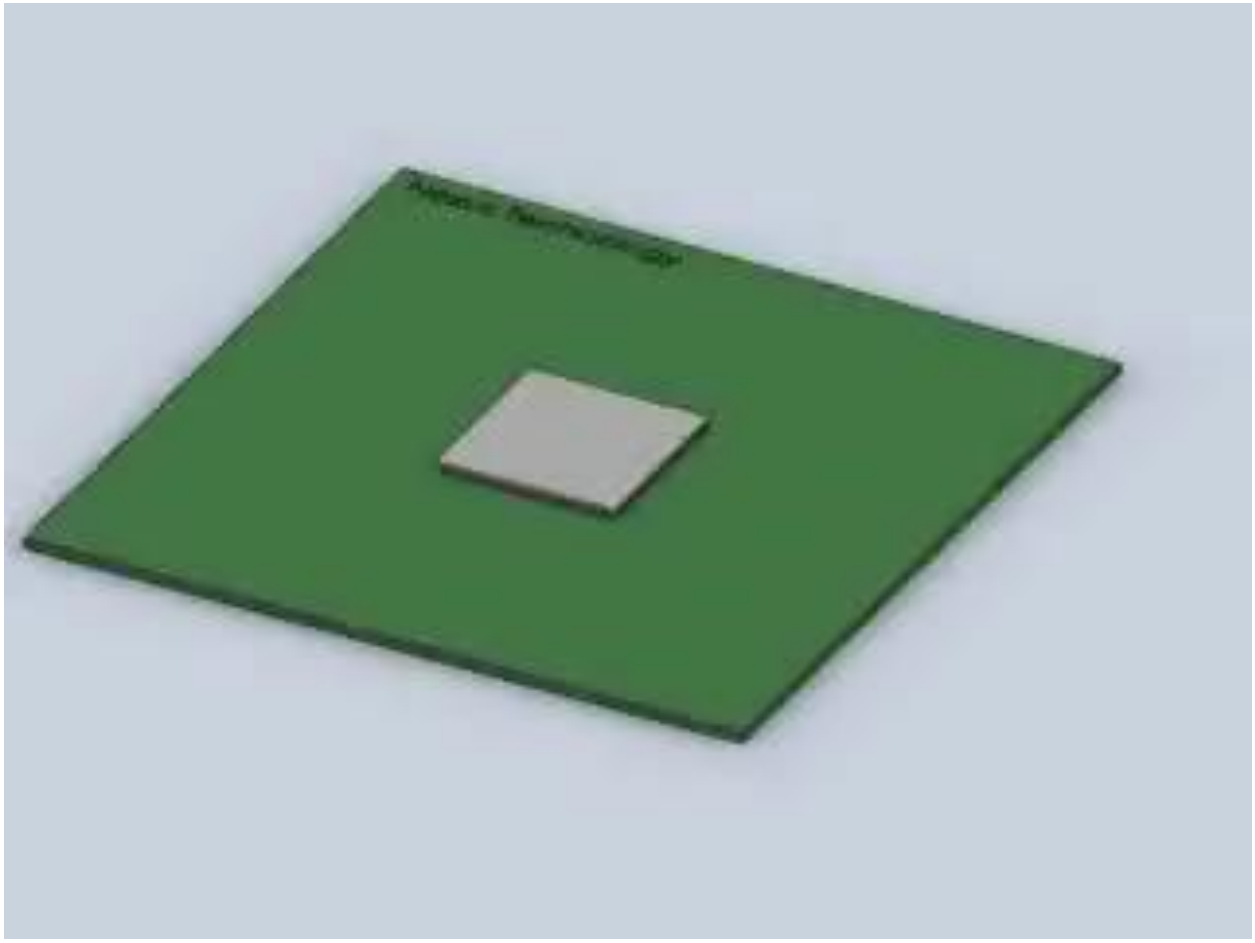
Socketed Interposer - Animation



Recommended Oscilloscopes for DDR4

- For DDR4 - Depending on Error Tolerance Levels
  - 12.5GHz/16GHz(MSO)

Specification Reference							
Generation	DDR	DDR2	DDR2	DDR3	DDR3	LPDDR3	DDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 3200MT/s
Max slew rate per JEDEC	5	5	5	10	12	8	18
Typical V swing	1.8	1.25	1.25	1	1	0.6	0.8
20-80 risetime (ps)	216	150	150	60	50	45	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	15.0
BW Recommendations (by end-user task, matched to scope BW availability)							
Chipset Development/ S.I.	2.5	3.5	4.0	12.5	12.5	12.5	16
System Level Test	2.5	2.5	3.5	8	12.5	12.5	12.5
Debug (low cost)	2.0	2.0	2.5	6	8	8	12.5

Definitions
Max Performance: highest accuracy, fastest slew rates
Typical: user anticipates slew rates of ~80% of spec or slower, accuracy important
Low Cost: user anticipates slew rates ~ 60% of spec, accuracy of 5-10% acceptable
Eventhough Specification suggests high slew rate however we don't expect devices to require more than 16GHz Scope BW to perform DDR4 measuremnts

Mapping Customer Challenge to Tektronix Solution

Customer Challenge	How does Tektronix help customer
Seamless movement from Compliance to Debug Environment	Tek customers have advantage of visibility and search on the DDR signal and provides much better debug tools. Customers can seamlessly move from compliance to debug environment and use world-class debug tool i.e. DPOJET.
Performing Bus/Digital measurements	Tektronix MSO70K up to 20GHz allows DDRA users to do two main things trigger on the DDR command bus, plus enables performing JEDEC bus-timing measurements.
Customer wants to Visually Trigger on Complex DDR signals.	Tektronix New Visual Trigger provides world-class features, flexibility & easy to use. Custom shapes and re-sizing of shapes are highly valued new features.
Customers working on memory design want one single application to support different DDR generations	DDRA supports all generations of DDR including DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3, GDDR3, GDDR5, DDR3L. Simplicity and lower cost-of-ownership. Tektronix Customers don't have to use multiple applications to work on different flavors of DDR. One single application meets the needs. DDRA reduces learning curve and is cost effective
Customers want to capturing Single Ended and Differential Signals without disturbing the setup	P75XX Series Probes include various Tri-Mode tips, including some designed for Nexus component interposers. "Micro-coax" tips are much more cost-effective. Tri-Mode is a big advantage for customers, allowing them to probe two data lines with a single tip, then use SW commands to switch test points.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Nexus EdgeProbe Technology

- Nexus Technology's Patent Pending EdgeProbe™ design is available with select DDR4 products. This technology allows for full analog acquisition of command, Address, Read and Write Data. Nexus Technology's Patent Pending EdgeProbe design removes mechanical clearance issues as the interposers are targeted to be the size of the memory components themselves. Embedded resistors within the interposers place the scope probe tip resistor extremely close to the BGA pad providing an integrated scope probe on all signals.