DDR PHY Test Solution
Agenda

- DDR Technology Overview and Roadmap
- DDR4
  - Specification Changes
- LPDDR3
  - Specification Changes
- Visual Triggering – VET
- DDRA Software
  - DDR4 Measurement Details
- Tektronix Probing Solution for DDR
  - DDR4 Scope Interposers
- Tektronix DDR Solution – Features and benefits
DDR Technology Overview & Roadmap
Memory Technology Overview

- **DRAM** - Dominant Memory Technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMM, SODIMM
  - Embedded systems
    - Cell phones, Ultra-Thin Notebooks, iPads
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR4 release on 26th Sep 2012 Maximum 3200 MT/s data rates transfer
    - LPDDR3-E planned can go unto 2133MT/s
    - DDR3L operates at 1.35V
    - DDR3U operates at 1.25V

- **DRAM variants**
  - DIMM based - Speed and Performance
    - DDR, DDR2, DDR3 and DDR4
  - Low Power DDR
    - LPDDR, LPDDR2, LPDDR3, LPDDR3E, LPDDR4
  - Graphic DDR - Optimized for Speed - faster access
    - GDDR3, GDDR5 @ 5500 MT/s
  - Low Voltage DDR
    - DDR3L, DDR3U
Memory Market Trends – Main Stream

New Roadmap

More realistic roadmap is 2015

SDRAM
66-133
1999

DDR1
2002
200-400

DDR2
400-800
2006

DDR3
800-2133
2010

DDR4
2133-4266
2015

This creates the need for faster DDR3 bins

And pushes DDR4 higher
Memory Market Trends - LPDDR

Mobile DRAM Technology Trend

- **Bring up right technology at right on time**
  - LP2-800 (‘10) → LP3-1600(‘12) → LP4-3200(‘14)

<table>
<thead>
<tr>
<th></th>
<th>’10</th>
<th>’11</th>
<th>’12</th>
<th>’13</th>
<th>’14</th>
<th>’15</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interface VDD/VDDQ</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LPDDR2 1.2V/1.2V</td>
<td>LPDDR3 1.2V/1.2V</td>
<td>LPDDR4</td>
<td>WIO and WIO2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>6.4GB/s</td>
<td>8.5GB/s</td>
<td>12.8GB/s</td>
<td>25.6GB/s+</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>2Gb</td>
<td>4Gb</td>
<td></td>
<td></td>
<td>8Gb</td>
<td></td>
</tr>
<tr>
<td><strong>PKG</strong></td>
<td></td>
<td></td>
<td>Up to 4 die stacks : 1.0 mm → 0.9mm and below</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Source: Samsung Presentation JEDEC Mobile Event Seoul*
DDR4
SAMSUNG(三星), HYNIX(海力士), MICRON(美光) have DDR4 products

ELPIDA(尔必达), NANYA(南亚) and other will have products by end of 2012

DDR4 → 50% market share by 2015
Specification Changes – DDR4

- Speeds 1600 – 3200 MT/s - JESD79-4 September 2012
- Voltage 1.2V or less
- V-center(avg) – New concept
- Derating measurements removed
- Mask-based versus setup/hold-based methodology
  - Removed tIH/tIS and tDS/tDH values
  - Added mask keep-outs
- Densely packed DIMM’s with narrow spacing between components
- Statistical jitter approach planned for speeds >2133
  - Jitter 1600-2133 assumed to be all DJ
  - Jitter >2133 both DJ and RJ
- Electrical signaling
  - Pull-ups to 1.2V changes tri-state voltage
  - Read and Write use positive strobe pre-amble – Phase Alignment challenges
NOTE:

1. For DQ in receive mode.

2. Data Rx mask voltage and timing total input valid window. Data Rx mask applied per bit post training and should include voltage and temperature drift terms. Design Target BER< tbd. Measurement method tbd.

6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd.
tLZ and tHZ Measurements

tLZ is a two source timing measurement starting from the extrapolated point (at VDD = 1.2V) got by extending the slope between Vsw1 and Vsw2 to the nearest rising edge of clock.

tHZ is a two source timing measurement starting from the extrapolated point (at Vdd – Vdd(34/(50+34))) got by extending the slope between Vsw1 and Vsw2 to the nearest rising edge of clock.
Derating

- Derating has been removed from the DDR4 spec. It will still apply to previous DDR specifications.

- Why?
  - Derating was not being used by many engineers due to dependence on DQS slew rate measurement
  - Not supported in simulation environment tool sets
  - Not supported in persistence test environment with RT scope

- DDR4 relies on DQ eye mask, similar to high speed serial
  - ≤ 2133, eye closure assumed to be DJ dominated
  - >2133, both RJ and DJ considered

- Practical vs. statistical approach
  - Practical approach ≤ 2133
  - Statistical approach will apply > 2133
LPDDR3
Mobile Memory = Faster, Smaller, Less Power

LPDDR3 Key Features

- **Speed and Capacity**
  - LPDDR3 achieves a data rate of 1600 Mbps (vs. 1066 Mbps for LPDDR2)
  - 4, 8, 16, 32Gb Package Options
- **Battery Conservation**
  - Low Voltage (300mV – 1.2V MAX)
  - Voltage Ramp and Device Initialization
    - Temperature-compensated (refresh less often at low temperatures) and partial array self refresh modes
    - Deep power down mode which sacrifices all memory contents
- **Compact Packaging**
  - PoP and Discrete Packages
Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR:
- 1.8 V
- 200MHz

Diagram showing DDR and DP0JET ref level designations with tDS and tDH measurements.
LPDDR3 Specification

Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR2:
- 1.2 V
- 533MHz

![Diagram showing voltage levels and timing parameters for DDR and LPDDR3 specifications.](image-url)
Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR3:
- 1.2 V
- 800MHz
Faster Clock Frequencies

- Verifying Clock Cycles on shorter (1.25 ns) Clock Periods
  - Measurement Challenges: Do I have the right instrument settings to capture with proper margin?

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Signal Swing (V)</td>
<td>3.5</td>
<td>4</td>
</tr>
<tr>
<td>Max. Data Rate (Mbps)</td>
<td>400</td>
<td>800</td>
</tr>
<tr>
<td>Period (ns)</td>
<td>2.5</td>
<td>1.25</td>
</tr>
<tr>
<td>Rise Time, 10% - 90% (ps)</td>
<td>738</td>
<td>369</td>
</tr>
<tr>
<td>Typical Clock Rate (MHz)</td>
<td>333</td>
<td>1600</td>
</tr>
<tr>
<td>Min. Rise Time (ps)</td>
<td>800</td>
<td>1.25</td>
</tr>
</tbody>
</table>

NOTE 1  RL=3/WL=1 setting is an optional feature. Refer to supplier’s Mode Register 2 settings.
Visual Trigger & Masks
Visual Visual Tools – DDR Eye Diagram

- Hexagon shaped area applied to DQ used as a keep-out zone to isolate only target rank of interest.
- Use additional areas to target specific DQ patterns.

Before applying Visual Triggering Tool

After applying Visual Triggering Tool
Visual Trigger

- Quick evaluation of DQ Signals
Visual Trigger
Support for Multiple DDR Generations

- DDRA = One Application SW Package
  - DDR
  - DDR2
  - DDR3
  - DDR3L (Q4-12/Q1-13)
  - DDR4 (Q4-12/Q1-13)
  - LPDDR
  - LPDDR2
  - LPDDR3 (Q4-12/Q1-13)
  - GDDR3
  - GDDR5
Ease of Use - DDRA Wizard

Step #1

- Select DDR Generation
- Select DDR Rate

Step #2

Choose measurements (Read / Write / CLK / Addr & Command)
Challenge: Solving Measurement Complexity

- JEDEC Standards specify unique measurements & methods
## Specification Changes DDR4 Measurements

<table>
<thead>
<tr>
<th>EXISTING MEASUREMENTS in DDRA</th>
<th>Supported for DDR3</th>
<th>Supported for DDR4</th>
<th>Supported for DDR3</th>
<th>Supported for DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VSEH</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>VSEL</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>AC - Overshoot Amplitude - SE</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>AC - Undershoot Amplitude - SE</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>Overshoot area</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>Undershoot area</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tCK(avg)</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDQSH</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDQSL</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDS</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDH</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDQSO</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDQSC</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tDQSS</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tRPRE</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tRPST</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>tWPRE</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>Data Eye Width</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
<tr>
<td><strong>Data Eye Height</strong></td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
<td>supported for DDR3</td>
</tr>
</tbody>
</table>

- **Single-ended voltage swing - high**
- **Single-ended voltage swing - low**
- **DQS, DQS#, CK, CK#**
- **Max overshoot area above VDD**
- **Max undershoot area below VSS**
- **Clock period - average**
- **DQS Input high pulse width**
- **DQS input low pulse width**
- **DQ and DM Input Pulse Width**
- **Address and Command Input Pulse Width**
- **Address and Command - setup**
- **Address and Command - hold**
- **DQ,DM Setup time to DQS(Diff/SE) - base - no derating**
- **DQ,DM Hold time to DQS(Diff/SE) - base - no derating**
- **DQ/DQS output hold time from DQS**
- **DQS falling edge to CK setup time**
- **DQS falling edge hold time from CK**
- **DQS - DQ Skew**
- **DQS output access time from CK/CK**
- **Write command to first DQS latching transition**
- **DQS differential WRITE postamble**
- **DQS differential READ preamble**
- **DQS differential READ postamble**
- **DQS differential WRITE preamble**
- **Eye Width**
- **Eye Height**
# Specification Changes DDR4 Measurements

<table>
<thead>
<tr>
<th>New Measurements for DDRA</th>
<th>Part Of New DDRA</th>
</tr>
</thead>
<tbody>
<tr>
<td>tHZDQ</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>tLZDQ</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>tLZDQS</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>tHZDQS</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>tQSH</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>tQSL</td>
<td>In DDR4 Spec</td>
</tr>
<tr>
<td>VdIVW_total</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>VIN.RXMSK_dV</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>TdIVW_total</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>TdIVW_dj</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>VIHL_AC</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>TdIPW</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>Tdqs</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>Tdqh</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>Tdqs_dd</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>Tdqh_dd</td>
<td>NEW for DDR4</td>
</tr>
<tr>
<td>SRIN_dIVW</td>
<td>NEW for DDR4</td>
</tr>
</tbody>
</table>
Accurate Read/Write Burst Identification

- Locate the right kind of bursts (read vs. write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc.)
Triggering on DDR3 Signal
Burst Detect on Command Bus using MSO Scope

- Using command bus state, specific transactions can be isolated
  - Analysis of analog signals is then used for fine burst positioning to gate measurements and this feature is available on a Mso scope
Burst Detection Method – Logic State

- Use MSO’s Logic Pattern or Logic State search/mark on the DDR control bus signals (CS, RAS, CAS, WE, etc.) to capture the desired burst type
- Adjust Latency settings for particular DUT
Read/Write Burst I.D. Using Search and Mark

- Advanced Search and Mark (ASM) dynamically applies a search algorithm to each acquired waveform, and marks specific features with visual delimiters.
- ASM searches have been developed specifically for DDR Reads and Writes.
- User controlled parameters to fine tune search algorithm.
- DDRA application can read these marks and use them as measurement gates.
- Single trigger post-process analysis of all parameters.
What to do if compliance fails? - DPOJET

- “Find Worst Case Events” feature
  - Zoom to waveform from Min / Max for each measurement
  - Seamlessly move to DPOJET to analyze the problem and root cause
Post Processing – DDRA Software

- Simple and easy to use automations software makes life of design engineer much simple
Probing Solution for DDR
Signal Access & Probing

- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device

- Signal Access Methods
  - Direct Probing
  - Component Interposers
  - Socketed Interposers

- Probe Types
  - Analog Probing
    - DQ, DQS, Clock
  - Digital Probing
    - Address
    - Command
    - Power, Reset, and Reference

Densely packed high-speed circuits stress probe access
Analog Solder-In Probing Solutions for 70k Scopes

P7500 Series Tri-Mode Probes

Socket Cable 020-2954-xx

TriMode Micro-Coax Tip 4GHz

P75TLRST Solder Tip up to 20GHz
DDR4 Scope Interposers

- Form factors - x4/x8/x16 BGA versions available
- Design improvements will increase BW ~6GHz
- Built-in probe tap using 100ohm embedded resistor help place probe tip close to BGA
- De-embed filters to remove effects of interposer tap trace
- EdgeProbe Technology allows memory component size interposer
- Five versions available to give users maximum flexibility
  - Socketed: Full BGA visibility
    - Allows snap-in/snap-out of DDR4 components using micro socket
    - NEX-DDR4MP78BSCSK
  - Solder-down, Address/command version:
    - Narrow version, NEX-DDR4MCI78SCDSADD
    - Wide version, NEX-DDR4MCI78SCDWADD
  - Solder-down, Data version:
    - Narrow version, NEX-DDR4MCI78SCDSDAT*
    - Wide version, NEX-DDR4MCI78SCDWDAT
Socketed Version, All Signals
One Size, Larger Keep-out Region
Socketed Interposer - Animation
Recommended Oscilloscopes for DDR4

- For DDR4 - Depending on Error Tolerance Levels
  - 12.5GHz/16GHz(MSO)

<table>
<thead>
<tr>
<th>Specification Reference</th>
<th>DDR2 to 400MT/s</th>
<th>DDR2 to 800MT/s</th>
<th>DDR3 to 1600MT/s</th>
<th>DDR3 to 2400MT/sto</th>
<th>LPDDR3 to 1600MT/s</th>
<th>DDR4 to 3200MT/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max slew rate per JEDEC</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>12</td>
<td>8</td>
<td>18</td>
</tr>
<tr>
<td>Typical V swing</td>
<td>1.8</td>
<td>1.25</td>
<td>1.25</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
</tr>
<tr>
<td>20-80 risetime (ps)</td>
<td>216</td>
<td>150</td>
<td>150</td>
<td>60</td>
<td>50</td>
<td>45</td>
</tr>
<tr>
<td>Equivalent Edge BW</td>
<td>1.9</td>
<td>2.7</td>
<td>2.7</td>
<td>6.7</td>
<td>8</td>
<td>8.9</td>
</tr>
</tbody>
</table>

**BW Recommendations (by end-user task, matched to scope BW availability)**

- **Chipset Development/ S.I.**: 2.5
- **System Level Test**: 2.5
- **Debug (low cost)**: 2.0

**Definitions**

- **Max Performance**: highest accuracy, fastest slew rates
- **Typical**: user anticipates slew rates of ~80% of spec or slower, accuracy important
- **Low Cost**: user anticipates slew rates ~60% of spec, accuracy of 5-10% acceptable

Even though Specification suggests high slew rate however we don’t expect devices to require more than 16GHz Scope BW to perform DDR4 measurements.
# Mapping Customer Challenge to Tektronix Solution

<table>
<thead>
<tr>
<th>Customer Challenge</th>
<th>How does Tektronix help customer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Seamless movement from Compliance to Debug Environment</strong></td>
<td>Tek customers have advantage of visibility and search on the DDR signal and provides much better debug tools. Customers can seamlessly move from compliance to debug environment and use world-class debug tool i.e. DPOJET.</td>
</tr>
<tr>
<td><strong>Performing Bus/Digital measurements</strong></td>
<td>Tektronix MSO70K up to 20GHz allows DDRA users to do two main things trigger on the DDR command bus, plus enables performing JEDEC bus-timing measurements.</td>
</tr>
<tr>
<td><strong>Customer wants to Visually Trigger on Complex DDR signals.</strong></td>
<td>Tektronix New Visual Trigger provides world-class features, flexibility &amp; easy to use. Custom shapes and re-sizing of shapes are highly valued new features.</td>
</tr>
<tr>
<td><strong>Customers working on memory design want one single application to support different DDR generations</strong></td>
<td>DDRA supports all generations of DDR including DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3, GDDR3, GDDR5, DDR3L. Simplicity and lower cost-of-ownership. Tektronix Customers don’t have to use multiple applications to work on different flavors of DDR. One single application meets the needs. DDRA reduces learning curve and is cost effective.</td>
</tr>
<tr>
<td><strong>Customers want to capturing Single Ended and Differential Signals without disturbing the setup</strong></td>
<td>P75XX Series Probes include various Tri-Mode tips, including some designed for Nexus component interposers. “Micro-coax” tips are much more cost-effective. Tri-Mode is a big advantage for customers, allowing them to probe two data lines with a single tip, then use SW commands to switch test points.</td>
</tr>
</tbody>
</table>
Nexus EdgeProbe Technology

- Nexus Technology's Patent Pending EdgeProbe™ design is available with select DDR4 products. This technology allows for full analog acquisition of command, Address, Read and Write Data. Nexus Technology's Patent Pending EdgeProbe design removes mechanical clearance issues as the interposers are targeted to be the size of the memory components themselves. Embedded resistors within the interposers place the scope probe tip resistor extremely close to the BGA pad providing an integrated scope probe on all signals.