Rx/Tx Testing for Industrial High Speed Serial Data Links at 28G

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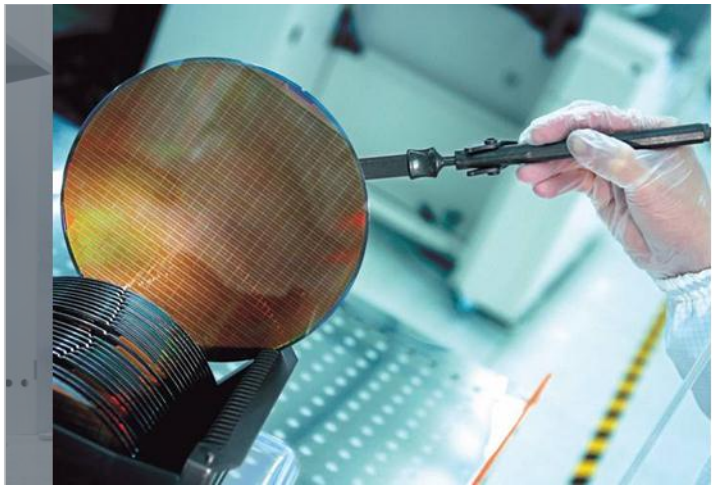

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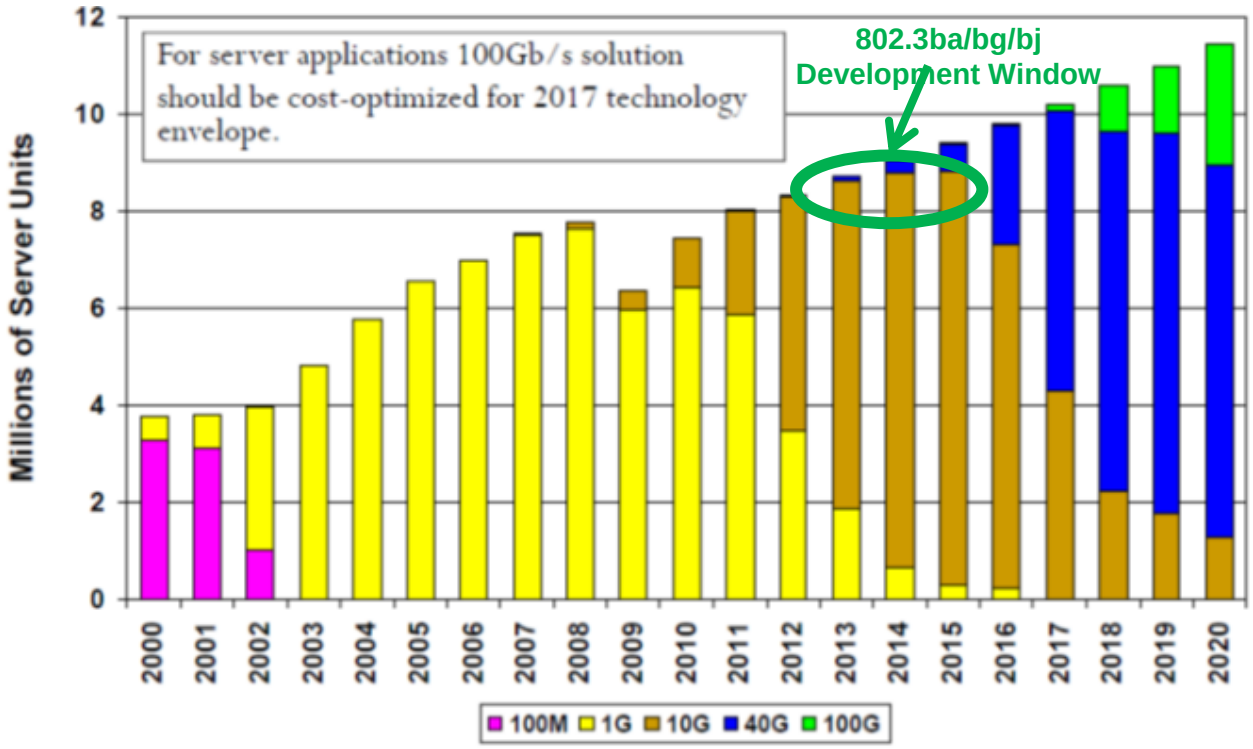
Economic Drivers: Commercial Deployment of 100G

- Design needs for 100G precede commercial deployment by 4 years
  - Early development in 2012 and steady provisioning through 2013/2014



Source: Ethernet Alliance, Feb 27, 2012

IEEE P802.3ba – Physical layer

Reach	40 GbE	100 GbE	Solution
1m Backplane	40GBASE-KR4	✘	4 x 10 Gb/s (reuse 10GBASE-KR)
10m Copper Cable	40GBASE-CR4	100GBASE-CR10	n x 10 Gb/s (reuse 10GBASE-KR)
100m OM3 MMF	40GBASE-SR4	100GBASE-SR10	n x 10 Gb/s
10km SMF	40GBASE-LR4	100GBASE-LR4	4 x 10 Gb/s and 4 x 25 Gb/s
40km SMF	✘	100GBASE-ER4	4 x 25 Gb/s

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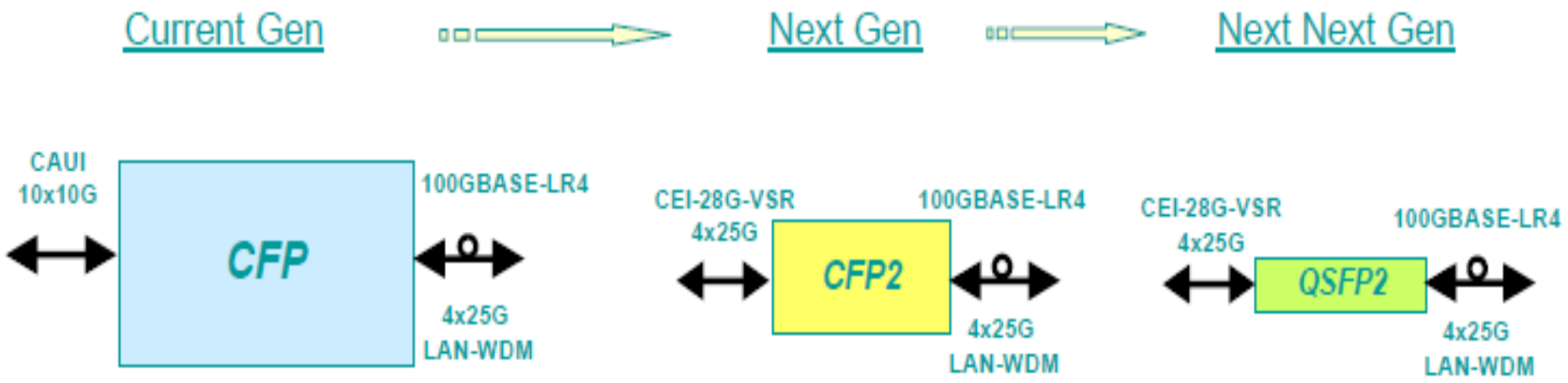
CEI-25G/28G-VSR: Common Electrical I/O



Module Characteristics	CFP	Next Gen CFP2	Next Gen QSFP2
Optics	**Discrete or Integrated**	**Integrated**	**Integrated**
Electrical I/O	**Re-timed**	**Re-timed or Asymmetric**	**Re-timed, Asymmetric or un-retimed**
Data Rates	. 10 x 10.3 (103.125 Gb/s) . 10 x 11.2 (111.81 Gb/s)	. 4 x 25.78 (103.125 Gb/s) . 4 x 27.95 (111.81 Gb/s)	. 4 x 25Gb/s (100Gb/s) . 4 x 25.78 (103.125 Gb/s . 4 x 27.95 (111.81 Gb/s) . 4 x 28Gb/s (112Gb/s)

CEI-25G/28G-VSR: Common Electrical I/O

- SFI: Serdes-Framer Interface, backplane, up to 25Gbps
- SPI: System Packet Interface, chip-chip/optics, up to 28Gbps

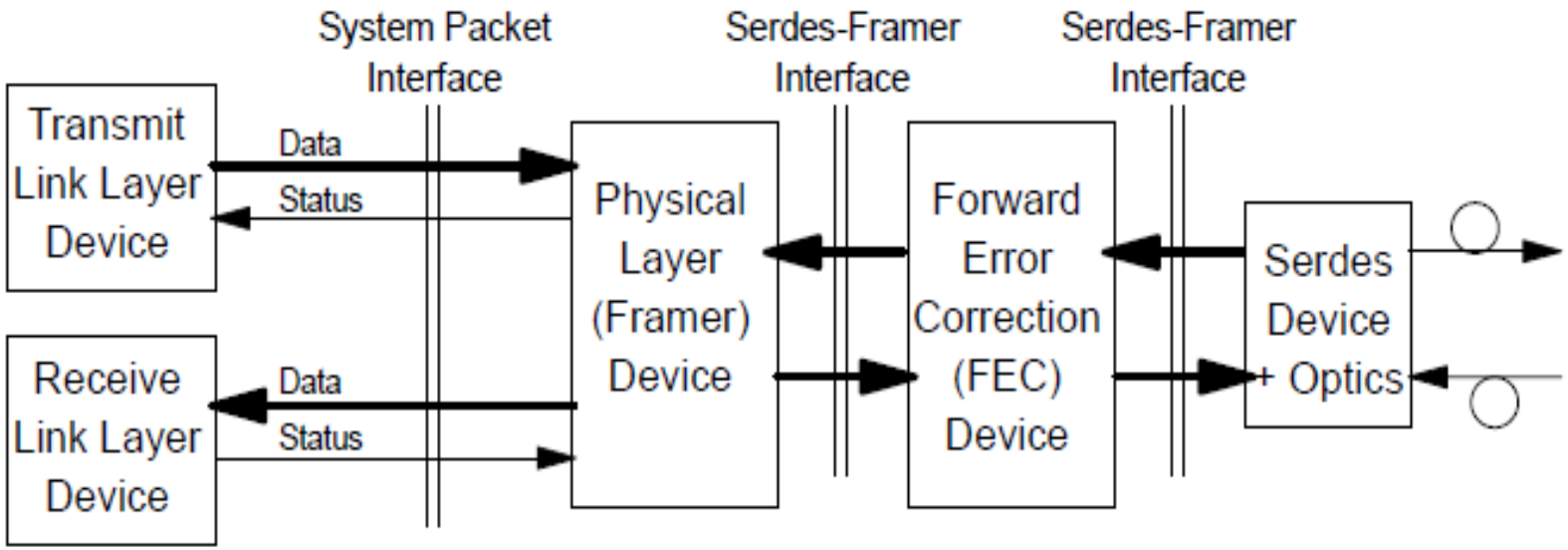
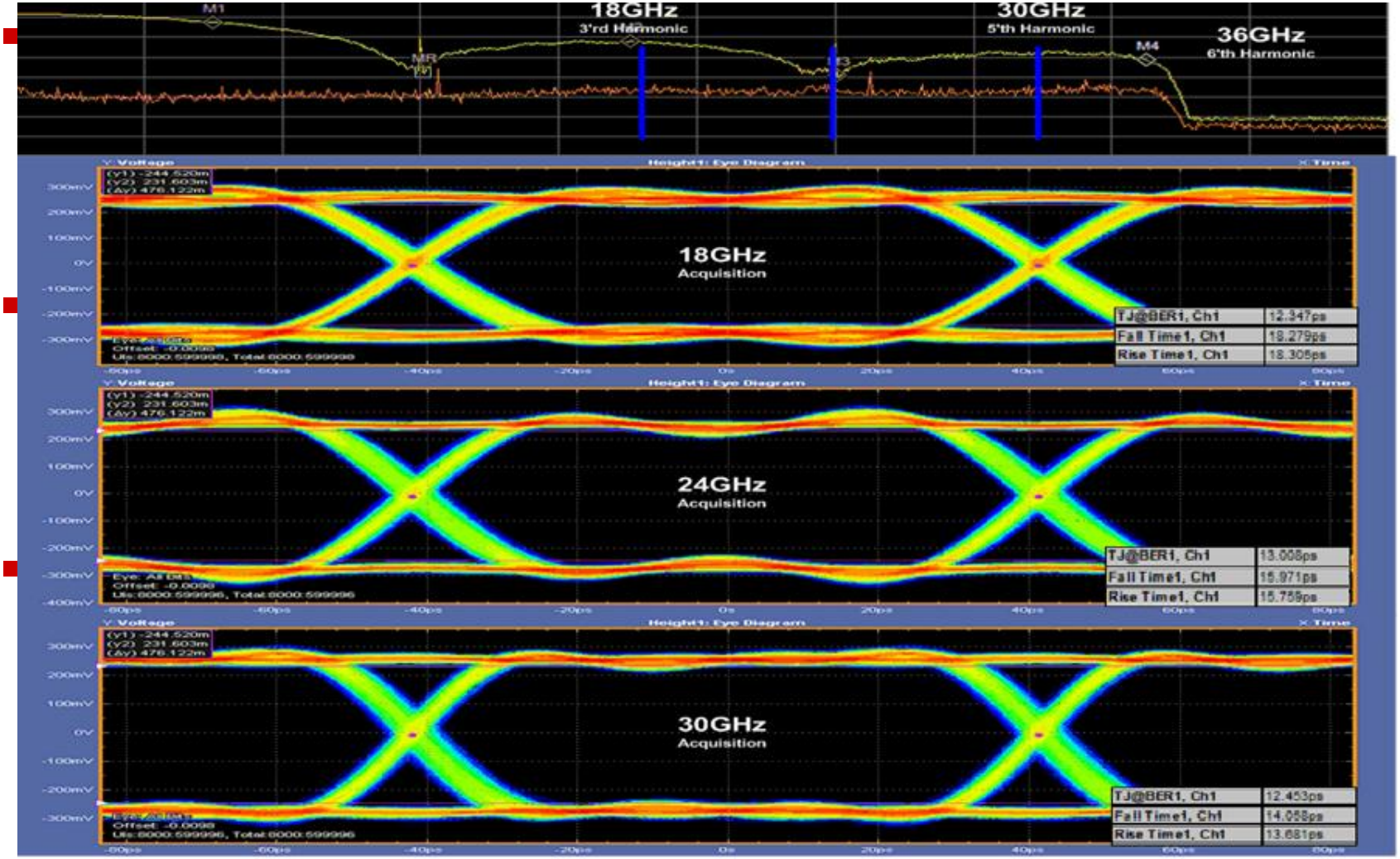


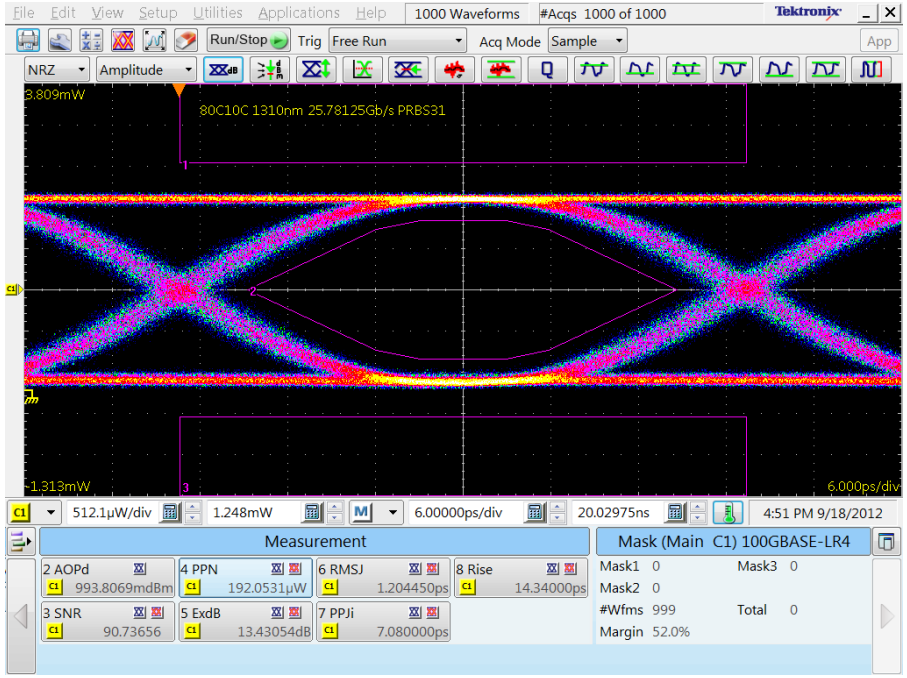
Figure 2 - OIF System Reference Model

100 Gb/s TX Physical Layer Test



Ethernet: Measurements for 40GBASE-LR4, 100GBASE-LR4/ER4

- Similar to **10GBASE-*R** single-mode optical
- Newly defined aspects are:
  - Optical **Reference Receiver** at **19.34 GHz**; Clock Recovery at **10 MHz PLL LBW**
  - **Masks** – scaled version of 802.3ae. **New masks for 25 and 28 Gb/s** available as files from Tektronix
  - Masks – **hit ratio** of 0.005%; **calculation in oscilloscope math** (contact Tektronix for details)
  - **TDP**, Transmitter Dispersion Penalty: **similar to 802.3ae**



100GBase-LR4 Mask Test
DSA8300 & 80C10C-F1
Reference Receiver

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Jitter Measurement use – J2, J9 and BER to 10^-15:

- The standard uses **J2** and **J9** jitter measurements
- The measurements are used for the definition of **Stressed Eyes**, and for measurement on **nPPI (Parallel Physical Interface)**
- BER depths of 2.5E-3, 2.5E-10, 10E-12 to 10E-15 are required

STANDARD		GEOMETRY	REACH	DATA RATE	BER
100 GbE	100GBASE-LR4 100GBASE-ER4	4 SM fibers	10 km 40 km	4×25.78125 Gb/s	≤ 10^{-12}
	100GBASE-SR4*	4 MM fibers	≤ 10 m	4×25.78125 Gb/s	≤ 10^{-12}
	100GBASE-CR4* 100GBASE-KR4*	4 cables, backplane	*	*	≤ 10^{-12}
OIF-CEI	OIF-28G-SR OIF-28G-VSR*	*N* traces on PCB	30 cm 15* cm	19.90-28.05 Gb/s	≤ 10^{-15}
Fibre Channel	32GFC	*N* channels optical and electrical	TBA*	28.05* Gb/s	≤ 10^{-12}*

Jitter Measurement Test Patterns

- The use of test patterns has key implications on the measurements tools.
- Pattern depth and algorithm requirements behind multiple pattern repeats can interfere in instrument choices. Particular attention needs to be paid here.

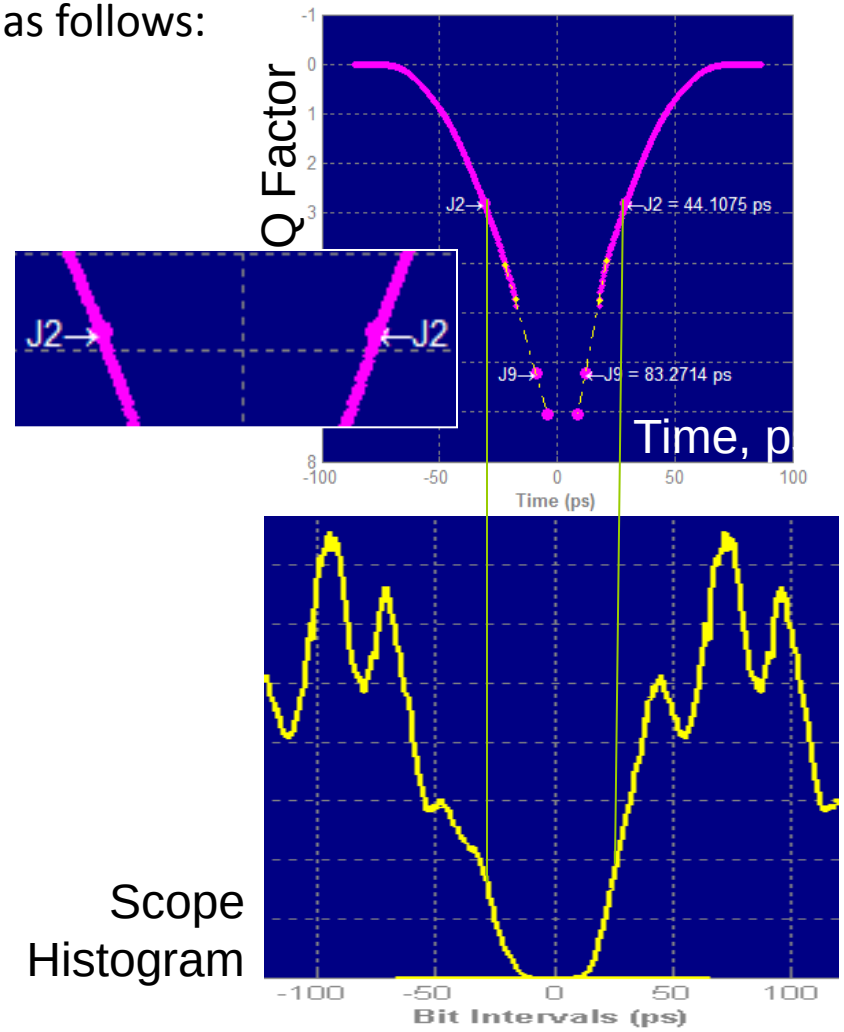
TEST PATTERNS	
0x00ff square wave	8 bits low, 8 bits high
PRBS9	511 bits
PRBS15	32,767 bits
PRBS31	2.1 Gbits
Scrambled idle	
OIF CID jitter tolerance pattern	(72 CID bits + ≥ 10328 from PRBS31 + seed) + complement

Jitter Methodology J2 and J9 Jitter – **J2**

- IEEE 802.3ba requires J2 and J9 jitter measurements, and defines J2 and J9 as follows:

- **IEEE 802.3ba 86.8.3.3.1 J2 Jitter**

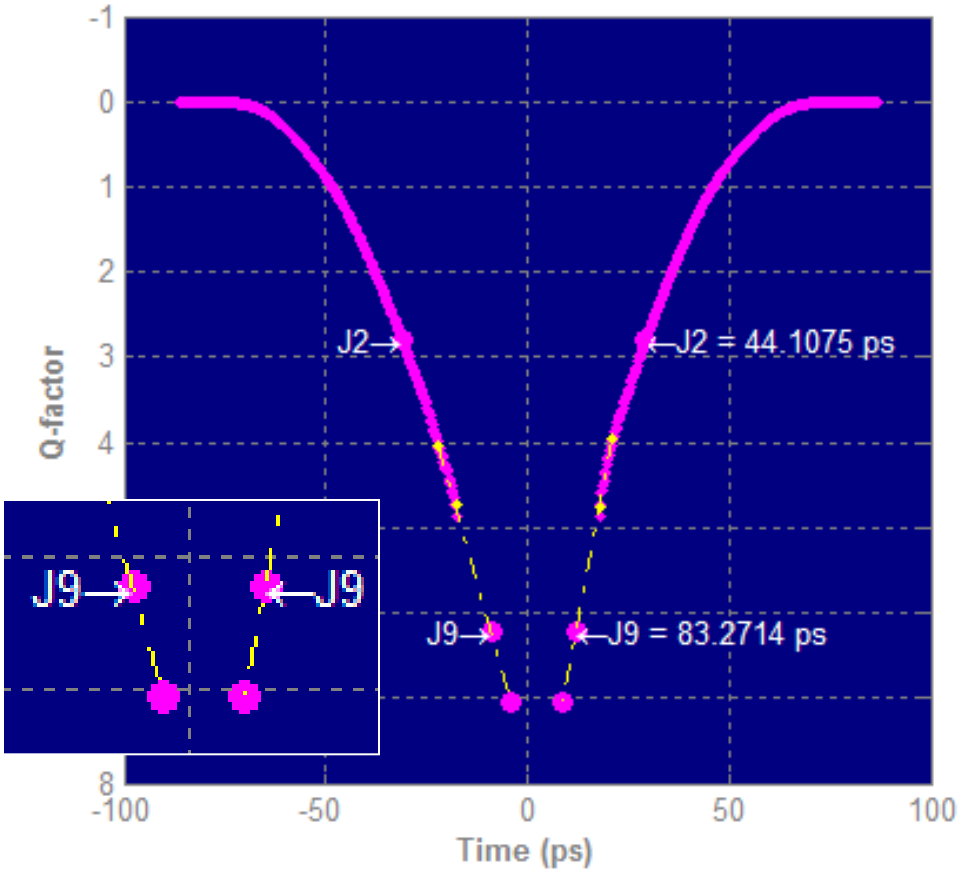
  J2 Jitter is defined as the time interval that includes all but **10^{-2}** of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. This may be measured using an oscilloscope, or if measured by plotting BER vs. decision time, J2 is the time interval between the two points with a **BER of 2.5×10^{-3}**. Oscilloscope histograms should include at least 10,000 hits, and should be taken over about 1% of the signal amplitude. Test Patterns are **PRBS31**, Scrambled Idle, or live traffic.



Jitter Methodology J2 and J9 Jitter – **J9**

- **IEEE 802.3ba 86.8.3.3.2 J9 Jitter**

  J9 Jitter is defined as the time interval that includes all but **10^{-9}** of the jitter distribution. If measured by plotting BER vs. decision time, it is the time interval between the two points with a BER of **2.5×10^{-10}**. Test Patterns are **PRBS31** or Scrambled Idle.



High Fidelity Connection to Device Under Test

- 80EXX sampling modules: 50G/60G/70G Bandwidth selectable

Optical modules: 150Mb ~ 100G

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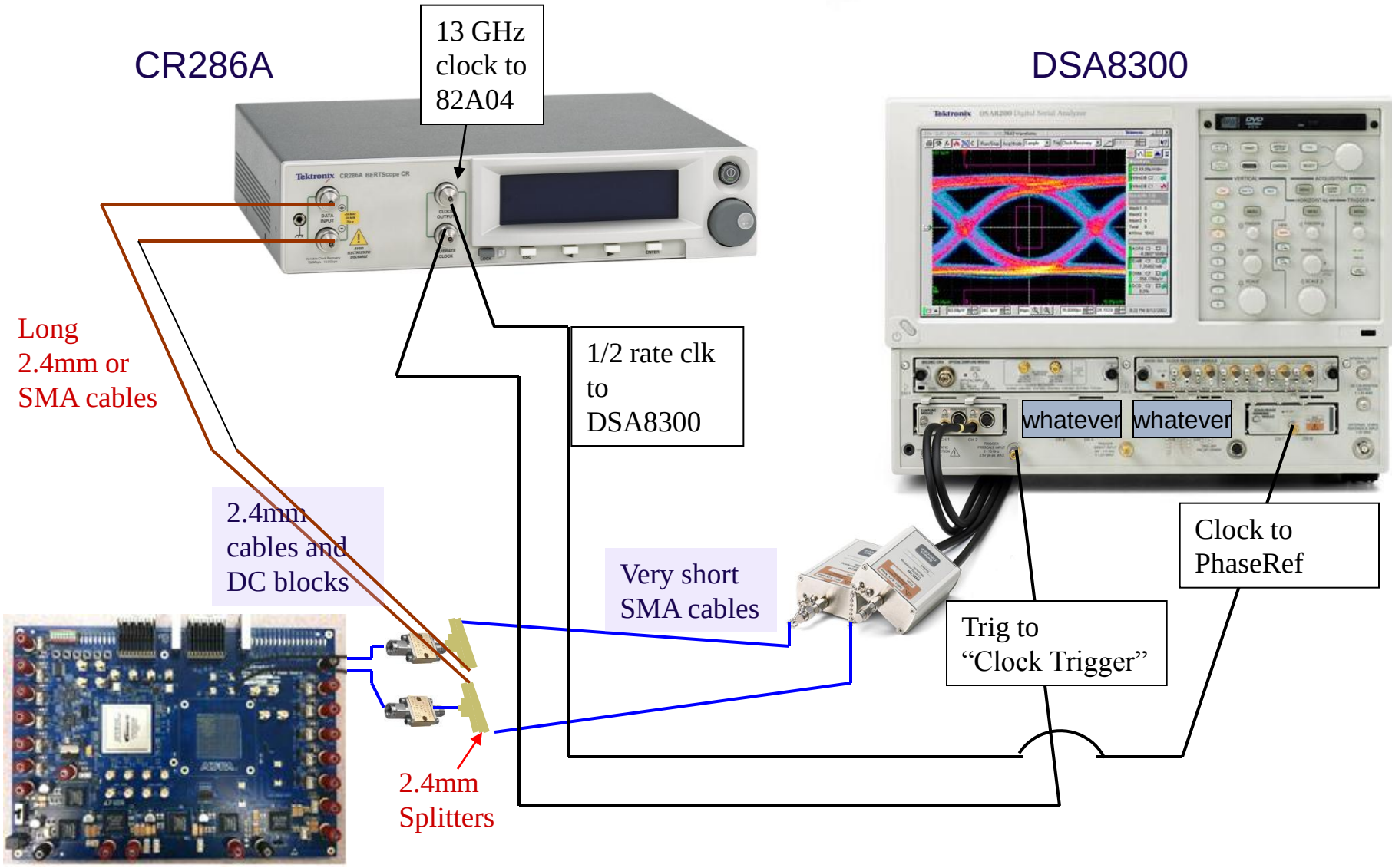
Practical Setup of 25/28 Gb/s Optical/Electrical test: Altera 25/28 G World Tour Sampling Setup



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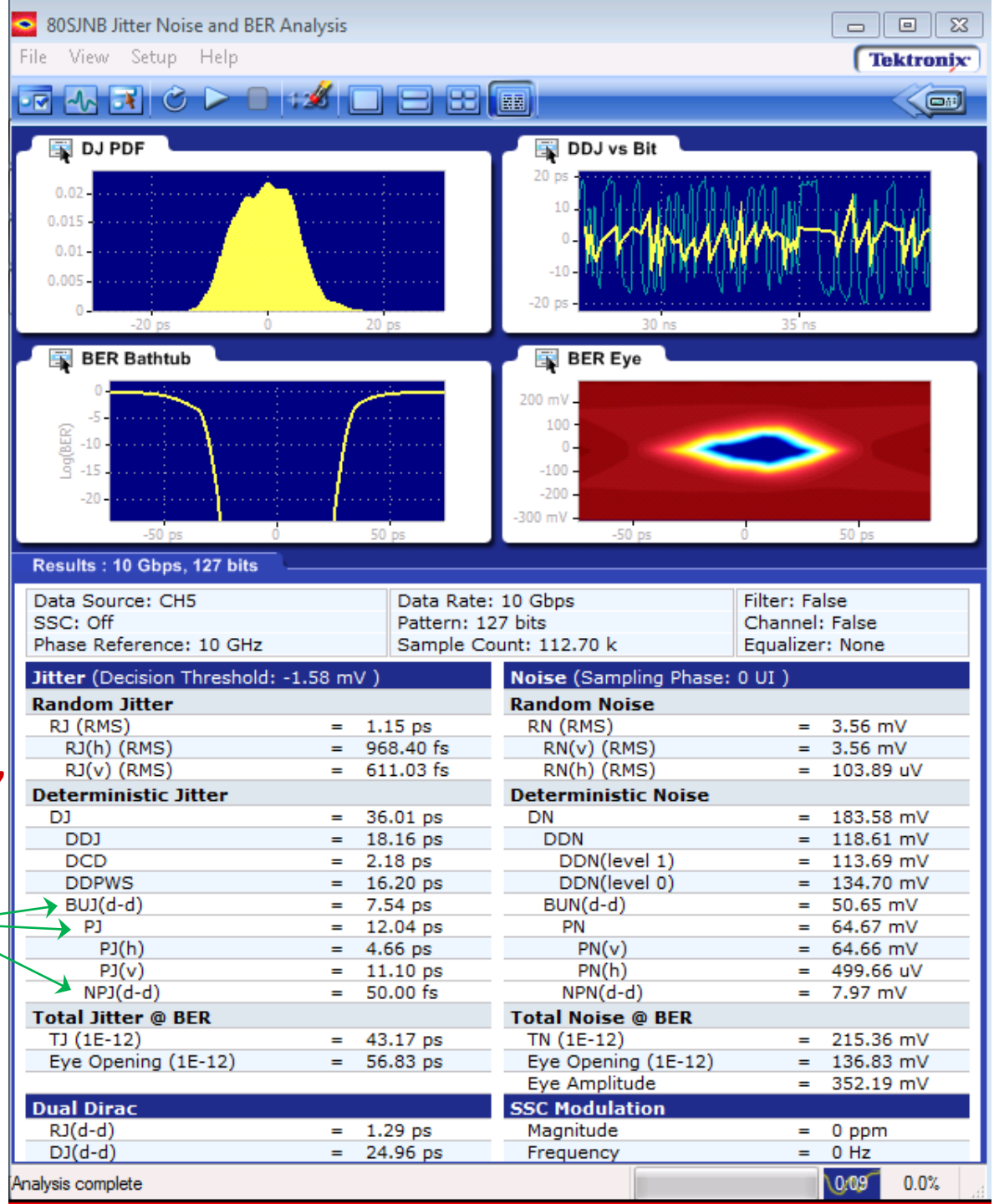
80SJNB: Jitter Analysis

- **80SJNB**, the premium jitter tool for sampling oscilloscopes, can measure and **decompose jitter** with great results thanks to the sampling oscilloscope's **low noise and jitter floor**.

- **All** of PJ, RJ, DDJ, DCD, Dual Dirac model, PWS, TJ, ***and* J2, J9**, as well as a **breakdown for Noise** are available

New breakdown



80SJNB: Jitter Analysis

- Key features:

- Characterize Jitter, Noise, and BER performance of HSS designs from 1 Gb/s to 60 Gb/s, such as Fiber Channel, IEEE 802.3 Ethernet, OIF CEI, SFP+, XFP, XAUI, XFI, InfiniBand, and other electrical or optical standards
- Separation of both jitter and noise provides highly accurate extrapolation of BER and eye contour
- J2 /J9 /Buj measurements, DDPWS measurement and plot in support of IEEE 802.3ba 100 GbE
- Transmitter measurement: Evaluate transmitter equalization(pre-emphasis/de-emphasis) from tap values of an FFE equalizer qualizing the transmitter-equalized waveform
- Test fixtures/cables de-embedding support

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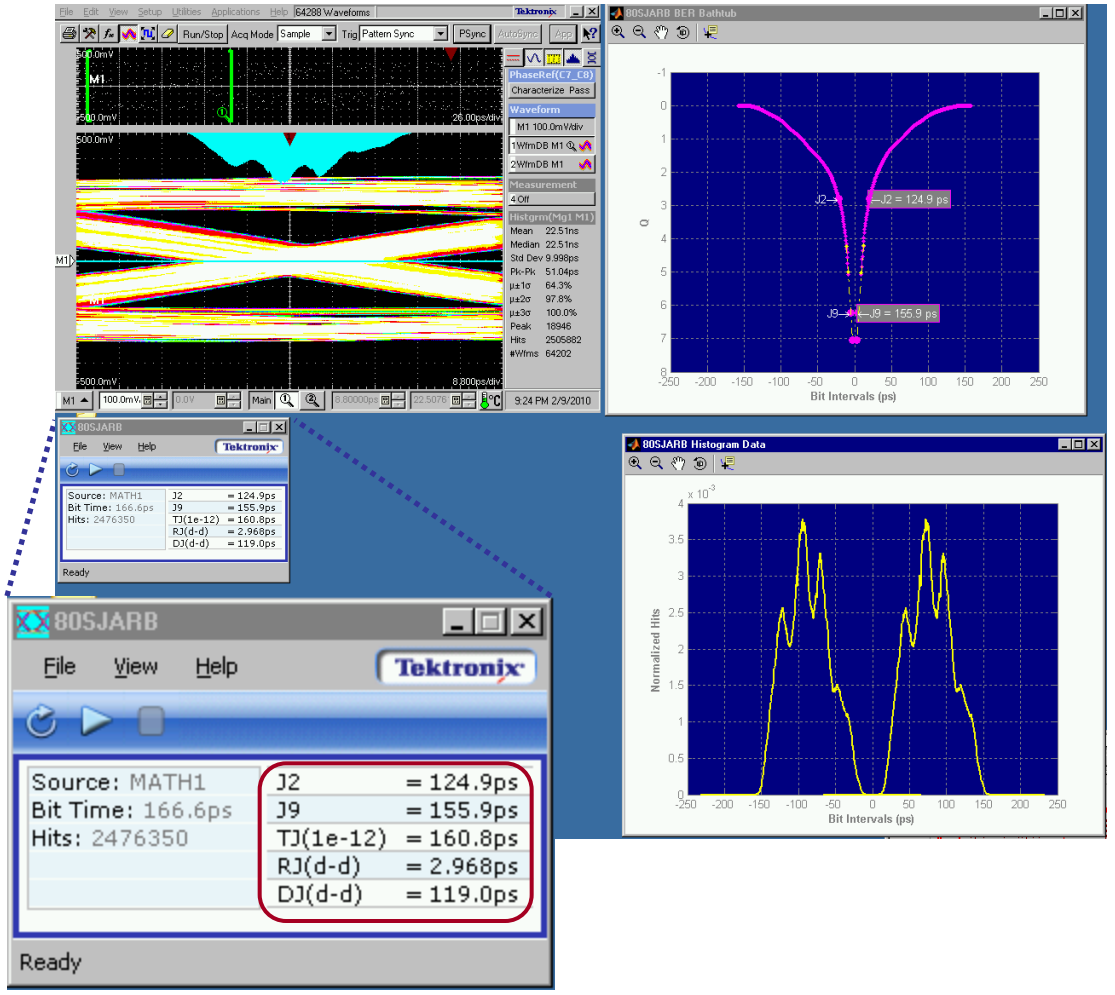
80SJARB: a companion tool to the 80SJNB: a Sampling Jitter Tool when the signal is PRBS31, Random Data

- **80SJARB Application**

80SJARB **measures jitter on random data** as well as long patterns (e.g. **PRBS31**), and reports:

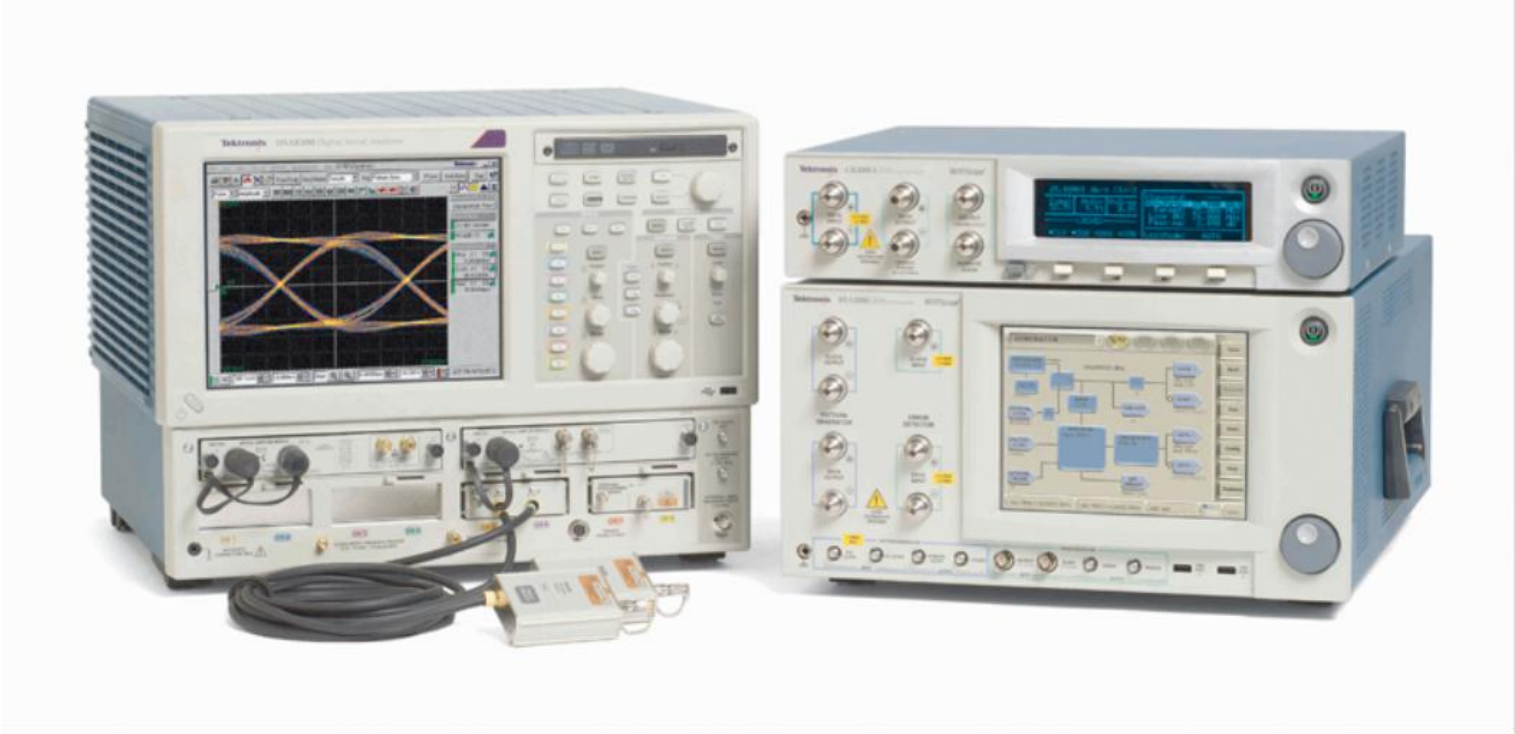
  - **J2**
  - **J9**
  - **$DJ_{\delta\delta}$, $RJ_{\delta\delta}$,** (Dual Dirac)
  - **TJ** at BER= 10^{-12} jitter.



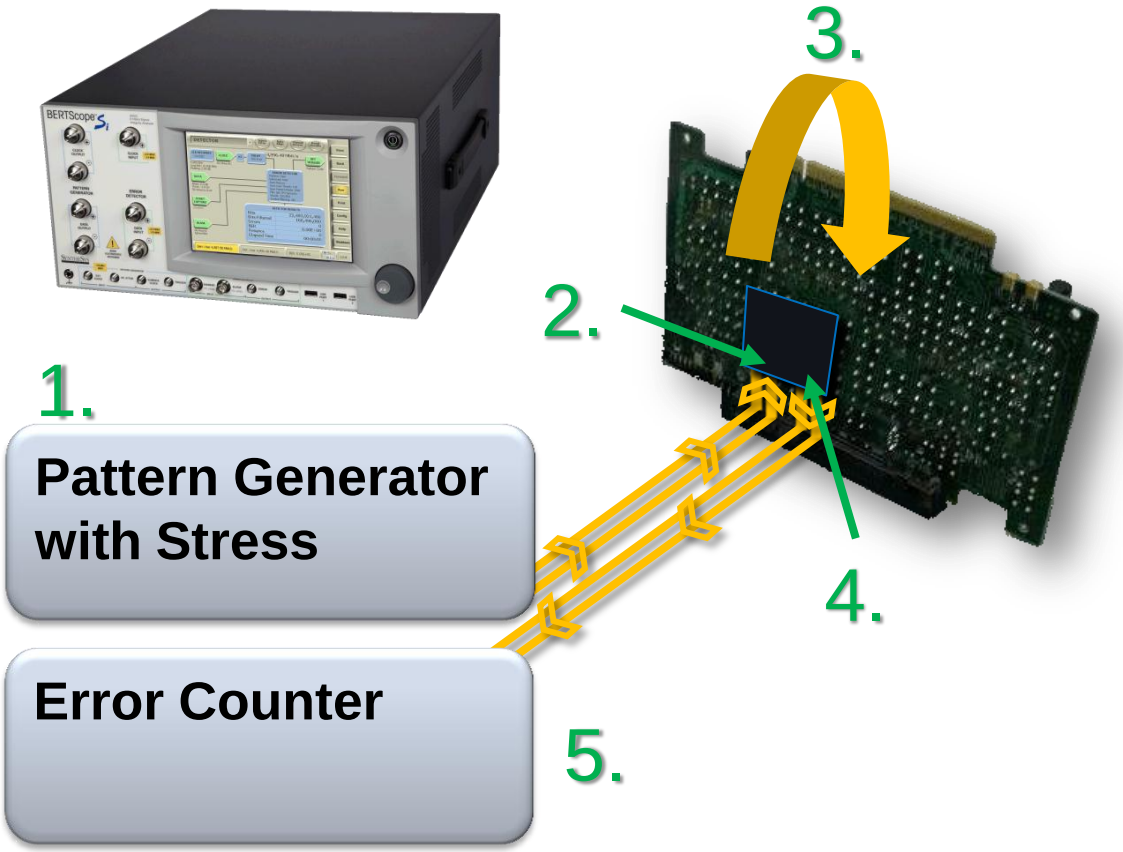
Receiver (RX) test at 100 Gb/s

Let’s look at the Receiver test

And do Receiver BERT Based Debug



Basic Receiver Testing



At the simplest level, receiver testing is composed of:

1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)

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Receiver testing

- BER: Bit Error Rate

Tx: 1011010001
Rx: 1011010011
} BER=10e-1

- Jitter Tolerance: evaluate performance of the Receiver to impaired signal

Rx/Tx testing for Industrial HSSD at 28G
Key Learning:

- BSA286C:
  - Support for rates through 29G offer 3% margin over standard base spec's.

Key Comms Rates	100GBase-*R4	100GBase-*R4 (FEC)	32G Fibre-Channel	CEI
Rate	25.7813	27.7390	28.0500	28.0500
I UI (period)	38.7879	36.0500	35.6500	35.6500
Allocated Rj (UI)	0.13	0.13	0.14	0.13
Rj in Psec RMS	0.3602	0.3348	0.3565	0.3310

  - <300pS Rj allows following the J2 and J9 jitter intercepts with margin.

- DSA8300/DSA8200 : <100 fs Jitter measurements.

Rx/Tx testing for Industrial HSSD at 28G Receiver Configuration and Calibration

- Using 802.3ba Rx case study
- Physical Medium Dependent (PMD) sub-layer and medium, type 40GBASE–SR4 and 100GBASE–SR10
- Rx and Tx testing
- Section 86 of the 802.3ba base spec (Page 271) is our target area.

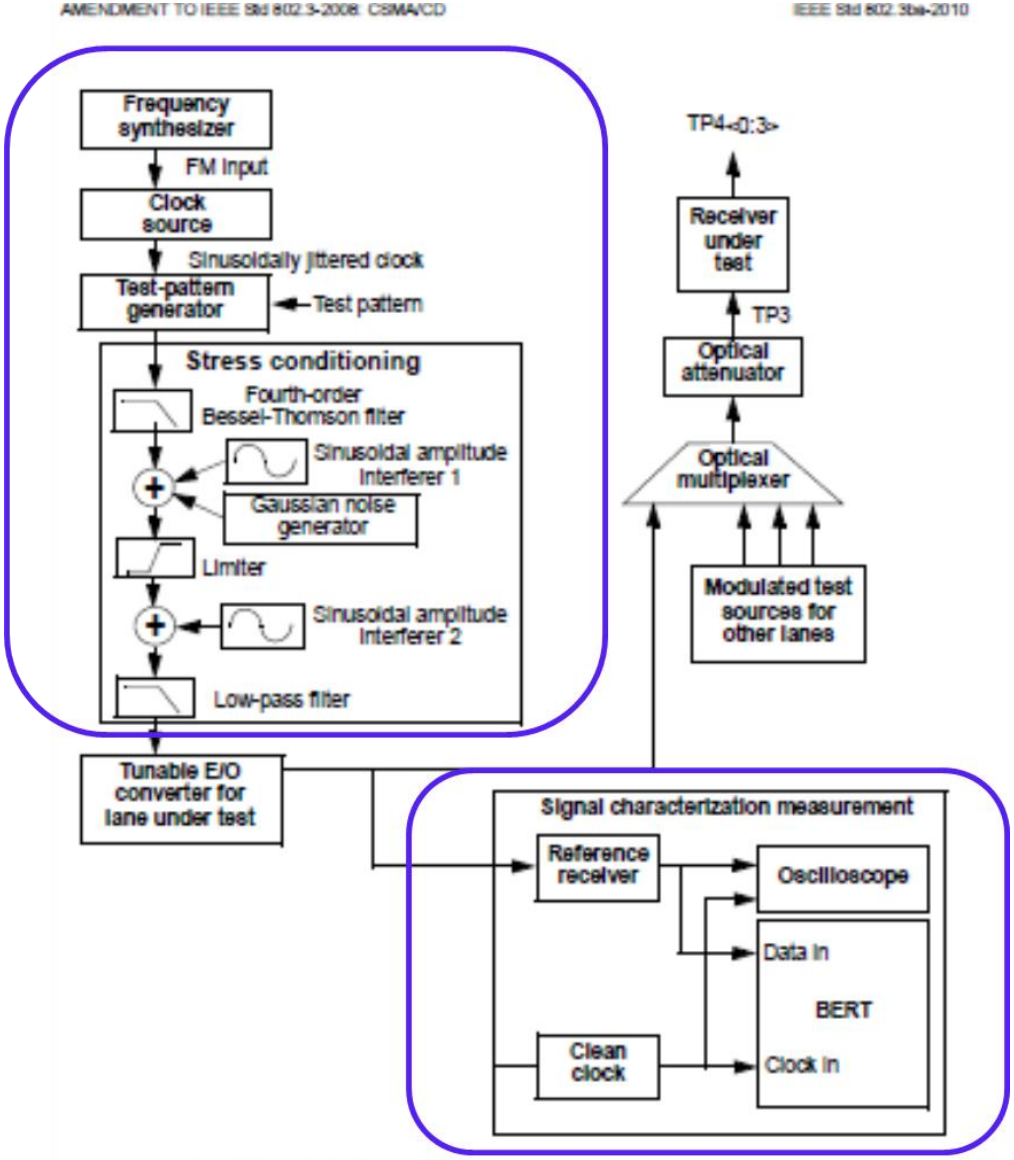
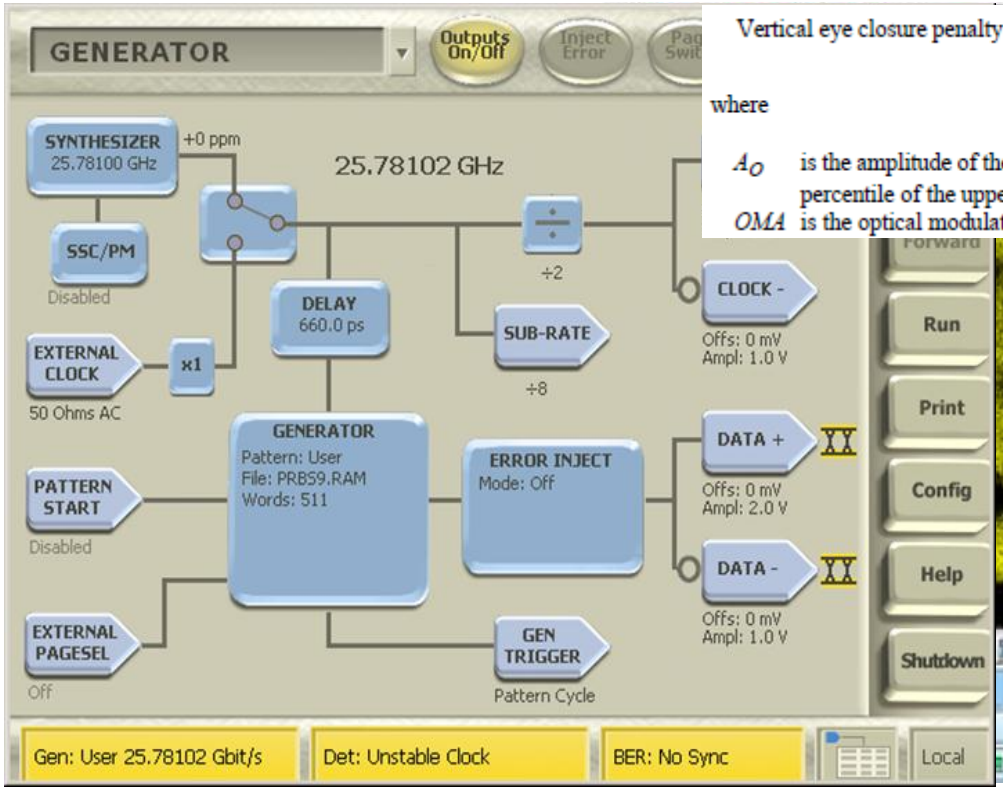


Figure 87–3—Stressed receiver conformance test block diagram

Rx/Tx testing for Industrial HSSD at 28G Receiver Configuration and Calibration

The target values from Table 88-8 of 802.3ba 2010 Spec.

Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty, each lane	1.8	3.5	dB
Stressed eye J2 Jitter,f each lane	0.3		UI
Stressed eye J9 Jitter,f each lane	0.47		UI

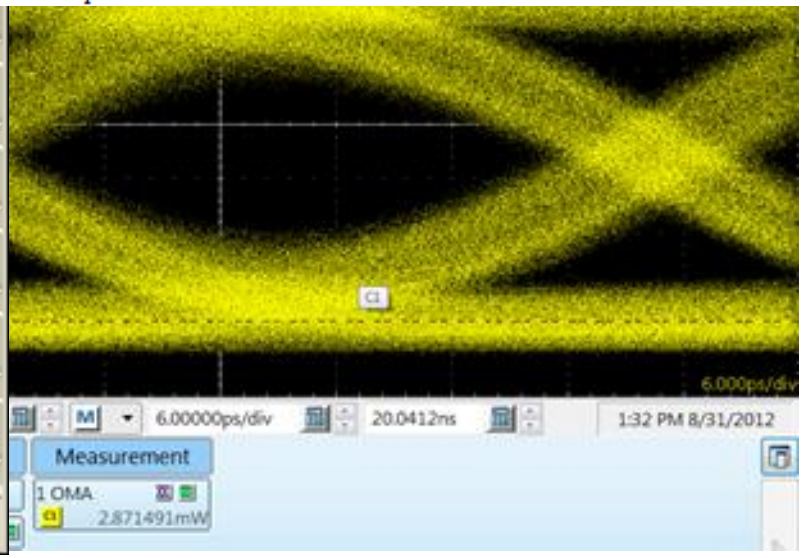


Vertical eye closure penalty $= 10\log_{10}\frac{OMA}{A_O}$ (dB) (87–1)

where

A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram

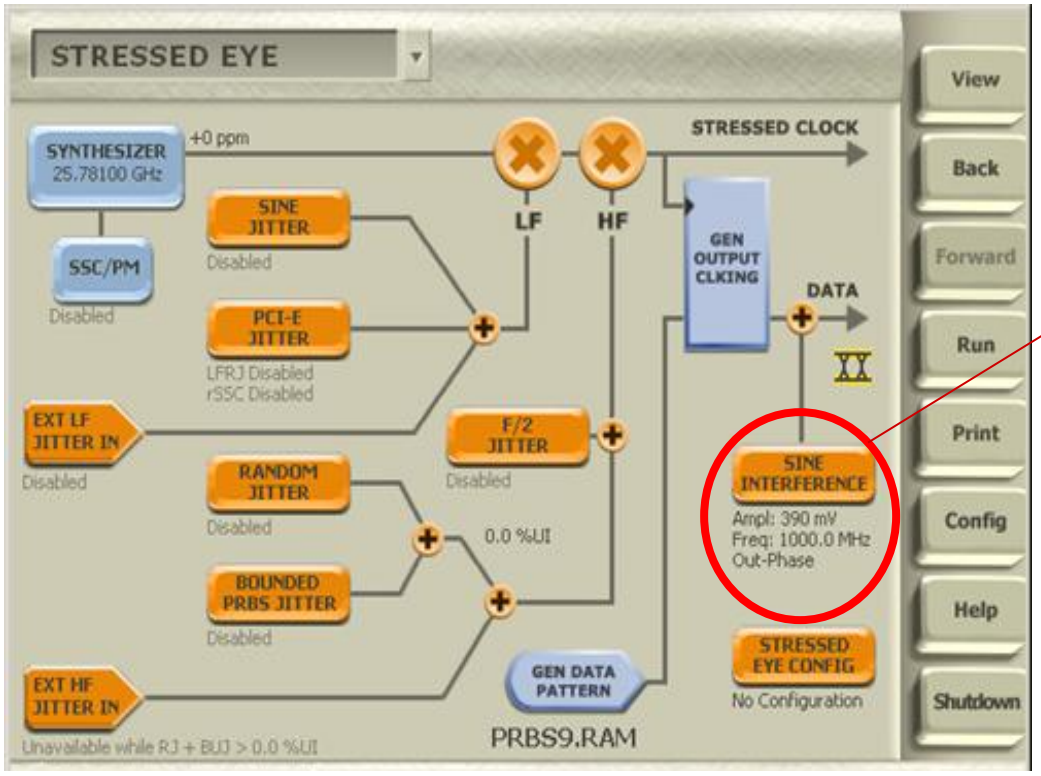
OMA is the optical modulation amplitude as defined in 87.8.5



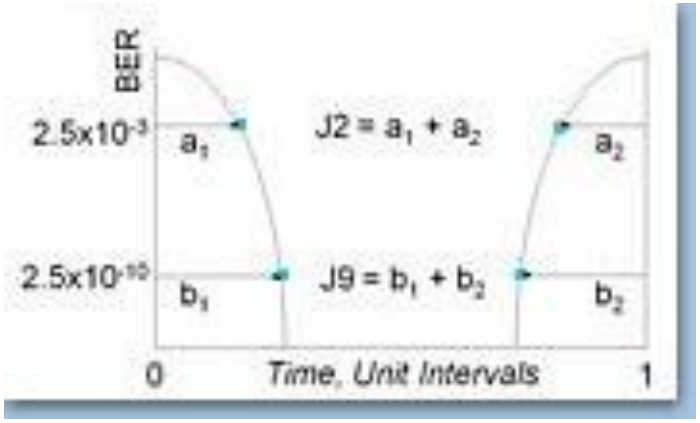
Rx/Tx testing for Industrial HSSD at 28G Receiver Configuration and Calibration

The target values from Table 88-8 of 802.3ba 2010 Spec.

Conditions of stressed receiver sensitivity test		
Vertical eye closure penalty, each lane	1.8	3.5
Stressed eye J2 Jitter, each lane	0.3	
Stressed eye J9 Jitter, each lane	0.47	



"The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may
be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the VECP, stressed eye J2 Jitter, and stressed eye J9 Jitter specifications are met simultaneously."



Rx/Tx testing for Industrial HSSD at 28G Receiver Configuration and Calibration

The target values from Table 88-8 of 802.3ba 2010 Spec.

Conditions of stressed receiver sensitivity test	
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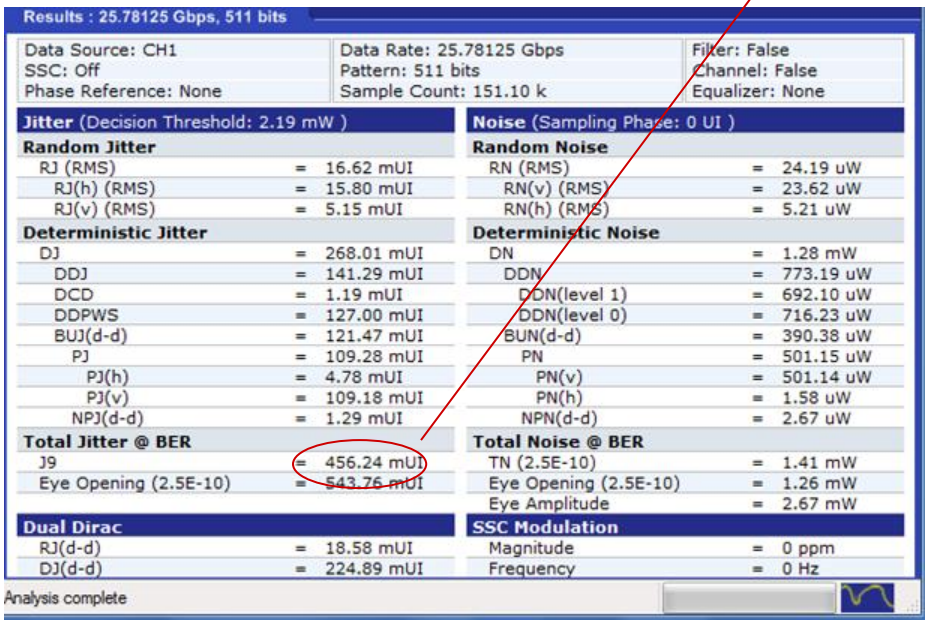
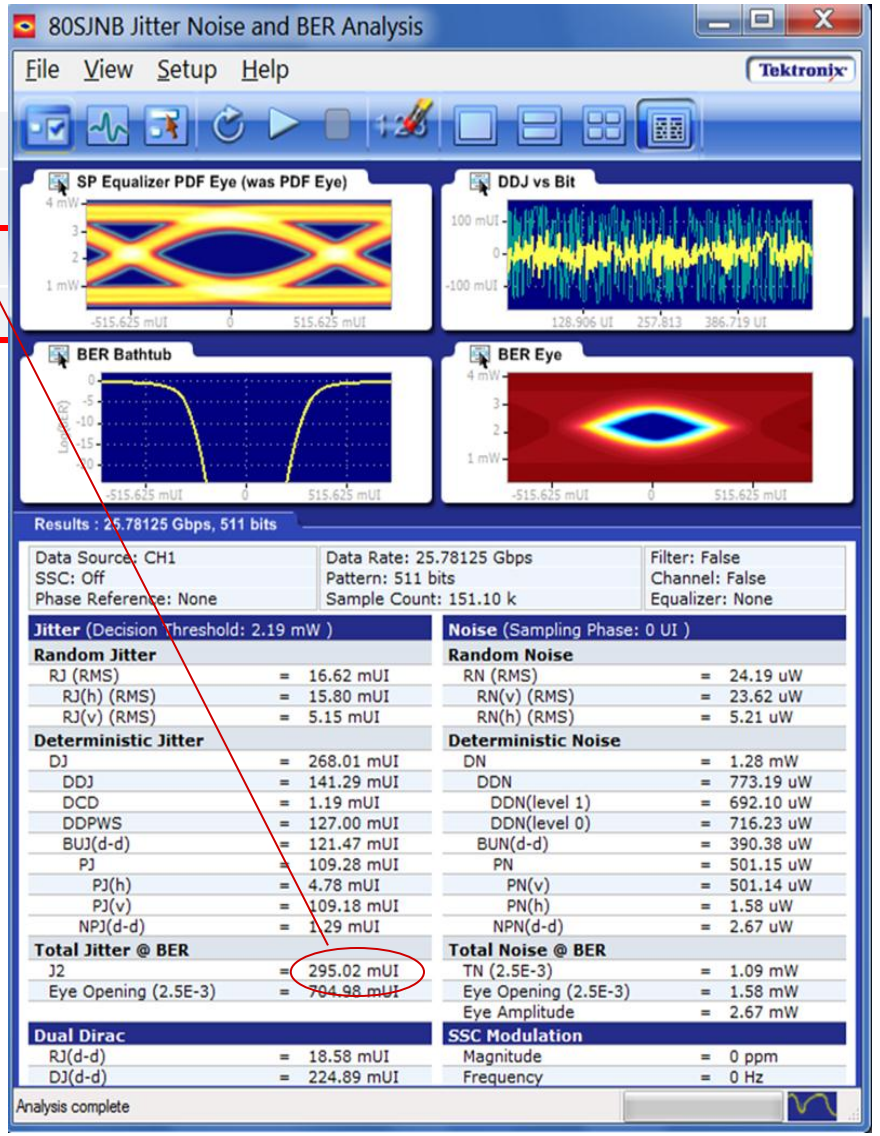
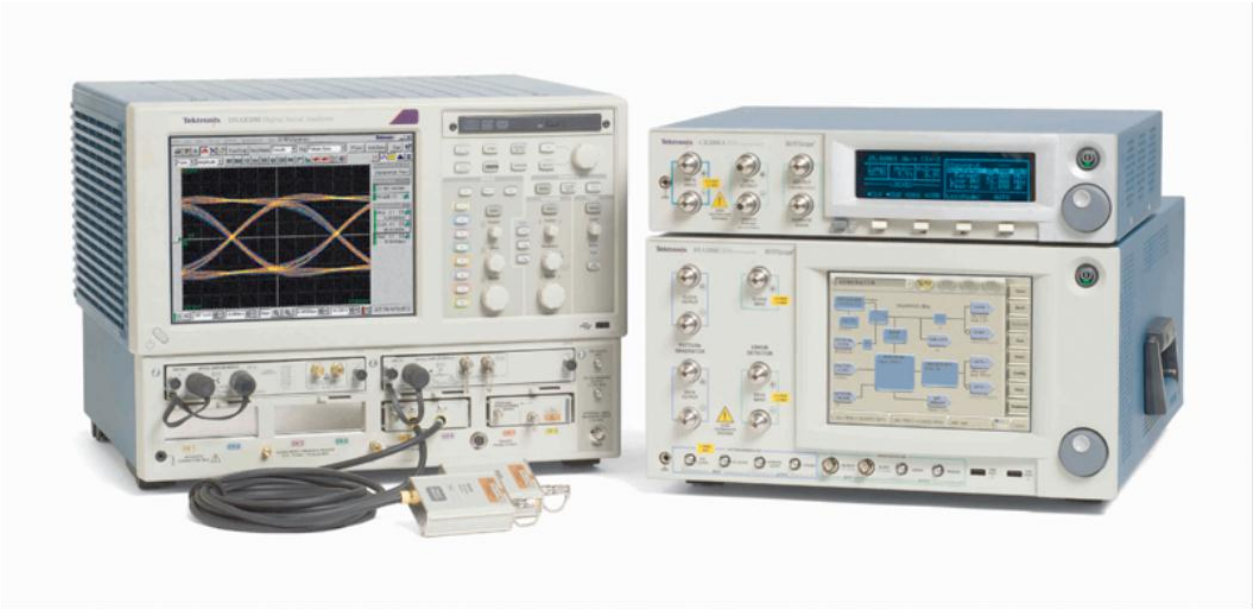


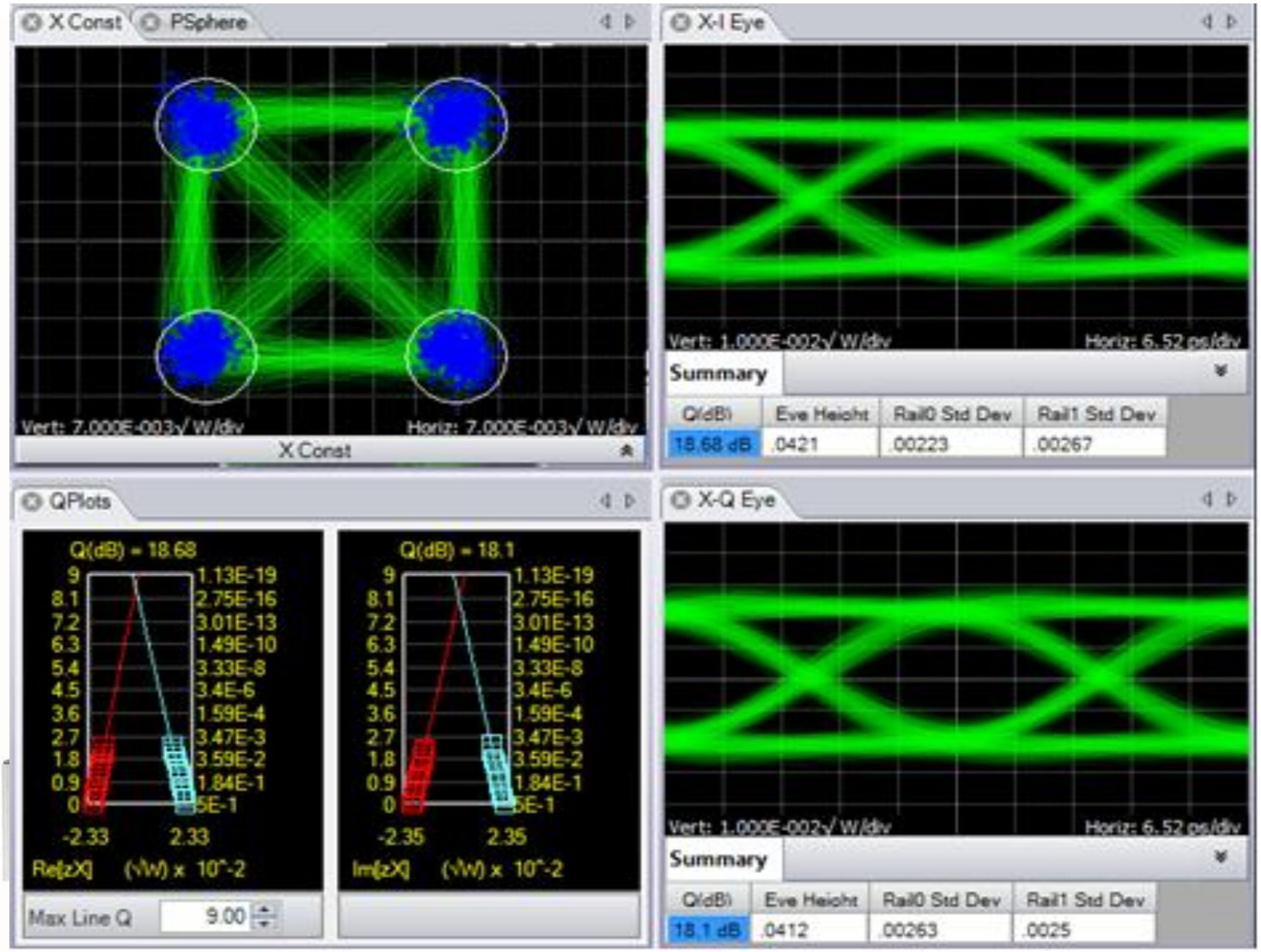


Rx/Tx testing for Industrial HSSD at 28G Summary

- BSA286: 28.6G pattern generator/Error detector, have low ~350fs intrinsic Rj to meet to the critical Rx requirements of 100GBE / CEI / 802.3 ba/bj and ect
- DSA8300: Over 70GHz Bandwidth, One Sampling Instrument can perform simultaneous optical, single and multi-channel electrical signal verification
- CR286A: 28.6G Clock Recovery, Established CRU technology and with proven performance and years of a deployed track-record.



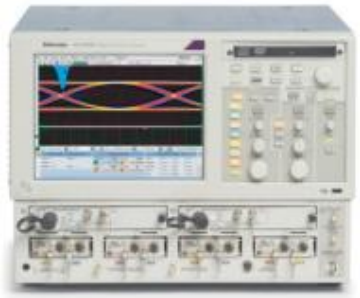
Coherent Optical Communication



What Tektronix offers ?

Tektronix has answers for 100G

- **DSA8300 Sampling Oscilloscope**
  - **>70GHz Bandwidth**
  - **<100 fsec jitter noise**
  - **Pass/Fail at high throughput**
  - **BUJ-Based Jitter Analysis**



- **BSA286C Bit Error Rate Tester**
  - **28.6 Gb/sec Data Rate**
  - **Low intrinsic jitter**
  - **Stressed, calibrated PRBS31 patterns**
  - **Error location & Jitter Analysis**

- **OM4000 Coherent Lightwave Analyzer**
  - **DP-QPSK Analysis**
  - **Constellation Mapping to BER**
  - **Works with RT or ET Scopes**

Thank you