Over 10Gbps transmission

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営業・技術本部 横浜営業所 アプリケーション技術グループ
主任技師
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**Session Agenda & Objectives**

- **Introduction to Signal Integrity Issues**
  - Where does loss come from
  - How materials effect transmission characteristics
  - Impedance discontinuities

- **Signal Conditioning Techniques**
  - EQ / Pre & De-Emphasis
  - Advanced SigCon techniques (DFE)
  - Retiming to remove random jitter

- **Tips**
  - Applications & Solutions

- **Summary**

- **Appendix**

**Session Objectives:**

- Become familiar with where loss comes from
- Understand various SigCon features
- Identify Solutions for common problems
Introduction to Signal Integrity Issues

Subhead text here
Progression towards 100Gbps….

<table>
<thead>
<tr>
<th>Year</th>
<th>Standardized</th>
<th>Data Rate</th>
<th>Unit Interval</th>
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<tbody>
<tr>
<td>1983</td>
<td>10 Mbps</td>
<td>100 ns</td>
<td></td>
</tr>
<tr>
<td>1995</td>
<td>100 Mbps</td>
<td>10 ns</td>
<td></td>
</tr>
<tr>
<td>1999</td>
<td>1 Gbps</td>
<td>1 ns</td>
<td></td>
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<tr>
<td>2006</td>
<td>10 Gbps</td>
<td>100 ps</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>100 Gbps</td>
<td>40 ps</td>
<td>(4 x 25 Gbps)</td>
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Interface Challenges

Doubling Data Rate, Reach Remains Same

Signal / Noise Problem

Shrinking CMOS Cells, PHY Integration, Jitter Problem

Higher Density, Chassis Life Extension

Cross Talk Problem

Plethora of Standards, Complex Designs

Power Density Problem

Time-to-Market Problem
Doubling Data Rate, Reach Remains Same

Signal Integrity Problem Growing

<table>
<thead>
<tr>
<th>Local Area Network (LAN)</th>
<th>&lt; 2009</th>
<th>2010</th>
<th>&gt; 2010</th>
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<tbody>
<tr>
<td></td>
<td>1 Gbps</td>
<td>10 Gbps</td>
<td>100 Gbps</td>
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<table>
<thead>
<tr>
<th>Server I/O</th>
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<tbody>
<tr>
<td>PCIe 2.5G</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCIe 5G</td>
<td></td>
<td></td>
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<tr>
<td>PCIe 8G</td>
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<table>
<thead>
<tr>
<th>Storage Area Network (SAN)</th>
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<tbody>
<tr>
<td>FC 4G</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FC 8G</td>
<td></td>
<td></td>
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<tr>
<td>FC 16G</td>
<td></td>
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<table>
<thead>
<tr>
<th>CPRI</th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>3 Gbps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 Gbps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9.8 Gbps</td>
<td></td>
<td></td>
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</table>

What happens to high speed signals after 26” of board trace?

- < 2006 (2.5 Gbps)
- 2006-2009 (5 Gbps)
- > 2009 (8 Gbps+)
Single Ended vs Differential

Inter Symbol Interference (ISI) and LOSS

Single Ended Signal

Differential Signal

Real World Differential Signal
Eye pattern is the collection of many overlaying patterns

Effects of ISI
Inter-Symbol Interference (ISI) Jitter

- ISI is data pattern dependant and is effected by the history of the stream
- Longer run lengths (i.e. PRBS-31) will tend to have more ISI if bandwidth is limited
- The “jitter trend” curve above shows how the pattern effects the jitter
- Reflections complicate the matter and add JITTER (not shown)
Transmission Loss Profile

Linear loss, Resonance, Reflections, X-talk

Ripples – Impedance discontinuities

Choppy – Crosstalk

Linear Loss
Where does LOSS come from?

*FR4 Loss vs. Length vs. Frequency*

- Loss proportional to \( \sqrt{f} \) (copper losses) and \( f \) (dielectric losses)
- Depends on transmission line geometries
- Depends on material properties

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**Cross Section**

- 5 8 5 8

**FR4 Test Traces**

- DS25BR100EVK
- FR4 Edge Coupled 100 Ohm Stripline

**Graph**

- Loss vs. Frequency
- Loss dB vs. Frequency
- 2.5Gbps

**Labels**

- 14 inches FR4
- 28 inches FR4
- 42 inches FR4
Common PCB Materials

- Better materials have low dielectric constants that are flat with frequency
- More exotic materials have lower loss, thus providing better signal quality over the same distance or longer reaches

<table>
<thead>
<tr>
<th>Name</th>
<th>Material</th>
<th>Dk (1MHz)</th>
<th>Dk (1GHz)</th>
<th>Dk (10GHz)</th>
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<tbody>
<tr>
<td>FR-4</td>
<td>GE</td>
<td>5.25</td>
<td>-</td>
<td>4.10</td>
</tr>
<tr>
<td>Nelco 4000-13</td>
<td>GE (Mod)</td>
<td>-</td>
<td>3.70</td>
<td>3.60</td>
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<tr>
<td>Hitachi FX-II</td>
<td>PTFE</td>
<td>-</td>
<td>3.60</td>
<td>3.40</td>
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<tr>
<td>Panasonic Megtron-6</td>
<td>PTFE</td>
<td>-</td>
<td>3.40</td>
<td>3.40</td>
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</tbody>
</table>

* PTFE: Polytetraflouroethylene (Teflon), GE: Glass Epoxy
Overcoming Impedance Discontinuities

- As signals propagate from board-to-board through traces, feed-thru’s and connectors, there are inevitable impedance discontinuities
- A TDR evaluation will highlight these discontinuities
- Careful layout, connector selection, and circuit board materials all factor into maintaining a relatively constant characteristic impedance
10G Design Considerations
Stubs matter

Molex iTrac Backplane
1m vs VIA stub length

SDD21 dB
0.38m_0.1stud
0.6m_0.1stud
1m_0.1stud
0.38m_2.4stud
0.6m_2.4stud
1m_0.6stud
1m_1.3stud
1m_5.5stud

Frequency MHz
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

Zo

1m BP & 0.1mm Stub

1m BP & 5.5mm Stub

Texas Instruments
Crosstalk – FEXT & NEXT

Crosstalk contributes to periodic jitter that can degrade system performance

- Crosstalk is interference caused by adjacent data channels and/or clocks

Far-End Crosstalk (FEXT)
- Crosstalk noise is injected into the victim channel at the far end of a channel and is measured at the receiver

Near-End Crosstalk (NEXT)
- Crosstalk noise usually from an adjacent transmitter is injected at the receive end and is measured at the receiver

*Far-End & Near-End Crosstalk Examples*
Signal Conditioning Techniques

Subhead text here
Right Tool for The Right Job
Redrivers, Retimers, and Advanced SigCon

Equalization & De-Emphasis Driver
Equalization & De-Emphasis Driver

Clock Data Recovery (CDR)
Clock Data Recovery (CDR)

Decision Feedback EQ (DFE)
Decision Feedback EQ (DFE)

Insertion Loss
Insertion Loss

Jitter
Jitter

X-Talk, Reflections
X-Talk, Reflections
Signal Conditioning: PE and DE

- Pre-Emphasis & De-Emphasis techniques address high frequency media loss by applying a frequency-selective boost or attenuation component to the data at the transmit end.

- **Pre-Emphasis (PE)**
  - Edge energy is boosted by creating an overshoot on every edge.
  - Typically used with LVDS.

- **De-Emphasis (DE)**
  - Edges are kept the same, but the settled amplitude is attenuated.
  - Typically used with CML.

\[
PE = 20 \times \log_{10}(A/B): \text{Transmit } V_{OD} = B \\
DE = 20 \times \log_{10}(B/A): \text{Transmit } V_{OD} = A
\]
Transmit Signal Conditioning Explained

*Pre-Emphasis (Pre-E) vs De-Emphasis (De-E) Waveforms*

**Output Pre-Emphasis**

- PE (dB) = 20\log_{10}(V_{high}/V_{low})
- DS25BR120 Simulation

**Output De-Emphasis**

- DE (dB) = 20\log_{10}(V_{ODPEn}/V_{ODDB})

<table>
<thead>
<tr>
<th>DATA_PATTERN</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
</tr>
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<tbody>
<tr>
<td>0 1 0 1 1 1 1 1 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</table>

**Pre-E Tends to be used with LVDS**
- Single direction – Longest links

**De-E Tends to be used with CML**
- Low EMI, Low Power, Bidirectional Shorter
Signal Conditioning: Receive Equalization

- Equalization is applied at the receive end
  - Selectively boosts high-frequency data
  - Compensates for the media’s high frequency roll-off
  - Includes a high-pass filter that ideally has a frequency response exactly opposite to the media loss that the equalizer is attempting to compensate
  - Equalizers may be active or passive; fixed, variable or adaptive

- Active Equalizers
  - Can add gain to high frequencies while attenuating low frequencies
  - Works best with low-level signals
  - Can often be “programmable” or “adaptive”
Advanced SigCon
Decision Feedback Equalizer (DFE)

- Helps to **open** the EYE in the amplitude domain to **reduce** BER
- Counters impact of **X-Talk** and **Reflections**
- Useful at the higher data rates where every ps matters most
- **Eye Openers**
  - **Equalizers** reduce Jitter in the X axis to open the EYE
  - **DFEs** reduces amplitude noise in the Y axis to open the EYE more
Eye-Opening Monitor (EOM)

- Many Uses: prototype, lab, factory test, remote diagnostics, Figure of merit (FOM) and more!
- Signal Fidelity measurement where it matters without probing effects, HEO, VEO (reg value)
- Featured on most high-speed RETIMER and DFE based Advanced SigCon solutions

10G, 100ps, 1.5ps & 6mV resolution
Random Noise and Jitter Revisited

- Random noise / jitter is not predictable
- Cannot be compensated with equalization

Results from the random nature of electrons and the random obstacles that the electrons overcome as they carry info down electrical channels

- Gaussian in nature
- 3 main system Components: driver jitter, channel jitter, and receiver jitter

Total Jitter

Random Jitter
unbounded, rms

Deterministic Jitter
pk-pk

Periodic Jitter
sinusoidal

Data-Dependent Jitter
data smearing

Bounded Uncorrelated
crosstalk

Duty Cycle Distortion
lead/trail edge

Inter-Symbol Interference
long/short bits
Jitter Limits Performance

**Bathtub Curve Performance**

Minimize Deterministic Jitter (DJ) via Equalization

Minimize Random Jitter (RJ) via retiming or clean clocks

Random jitter reduces the eye opening

**Scope Results**

Clock jitter is a critical requirement in high speed communications

Eye Open

Eye closing due to jitter

BER

$10^{-12}$

$10^{-15}$

0 0.2 0.5 0.8 1.0

1UI = 1/Data Rate

ISI, DDJ, VCC Noise

DJ

RJ

ISI, DDJ, VCC Noise

DJ

Clock jitter is a critical requirement in high speed communications
Using Retimers to Overcome RJ

Helps with minimizing Random Jitter (RJ), crosstalk, reflection, and residual Deterministic Jitter (DJ) in a channel.
Tips

Subhead text here
Today’s Tips

1 – How to extend a chassis’ life? – *Life Extender, Reach extender, Eye Opener*

2 – Active Cable – *Optimization!*

3 – 10G Backplane, PCIe-Gen3, SAS-3 – *Protocol Savvy*
1 How to extend a chassis’ life?

- Loss is a function of channel
  - Trace (e.g. FR4, 6mil, microstrip)
  - Via
  - Connectors
  - Data Rate

- Doubling of Data Rate – huge impact!

- Life Extension of H/W

- But Eye is closed!
  - Jitter 100%
  - Amplitude

- Open the EYE with a PowerSaver Equalizer Solution
1

PowerSaver Equalizers – EP Family

- DS38EP100 (2 to 5Gbps)
- DS80EP100 (5 to 12.5Gbps)
- EPs can be located at ANY point in the path
- Small Size (2.2mm x 2.5mm)
- No Power or GND connection required!
- Works with CML, LVPECL, or LVDS signaling
- Works with any codes: 8b10b, scrambled, DC….
- Bi-directional
- Economical boost solution that extends the life of a unit!
EP Design Considerations

- PowerSaver Equalizers **reduce jitter** and **open the eye** – provides a DE function
- **Will attenuate** the signal (8dB)
  - Must meet RX minimum sensitivity requirement
  - TX optimization – increase VOD (1Vpp) or use Pre-Emphasis – De-Emphasis not recommended
  - Can work with Active EQs Can stack but watch attenuation

- **DS38EP100** targeted at:
  - 2 to 5Gbps
  - 40” FR4 6mil microstrip or other
- **DS80EP100** targeted at:
  - 5 to 12Gbps
  - 20” FR4 6mil microstrip or other

*Extends the Data Rate or Extends the Reach*
Active Copper Cables

**Rack-to-Rack Reach**

How to extend the reach on lower gauge wires to replace fiber for lengths under 15 meters?

2.2m

10Gbps+

8m – 12m
Reach

`Permit Airflow`

`Installation Flexibility`
Data Center & HPC Cabling Solutions
Passive Copper, Active Copper, Active Optical

Passive Copper

QSFP: 5m, $X, 0W

Active Copper Cables

QSFP: 20m, $3X, 440mW

Active Optical Cables (AOC)

QSFP: 100m, $6X, 1000mW+
10G Base KR link training optimizes system level signal performance and power between TX and RX ASICS.

- **Passive (PowerSaver)**: Passes Link Training, Low Power, Attenuation impact
- **Limiting Stage**: Impacts Link Training
- **Linear Stage**: Passes Link Training, Preserves waveshape, Preserves Amplitude
Summary

Subhead text here
www.ti.com/sigcon

NEW SigCon Feature Site!

- Highlights
- Selection Tables
- Video Features / Demos
- System Block Diagrams
- Tools
- Applications Notes
- Design Guides
Thank You for attending!

APPENDIX
時間が余ったときに使用します。
What is the easiest way to reduce pins, cable bulk, interconnect cost, and GO FAR?

**USE TI’s Channel Link II Ser/Des**

**System Benefits**
- Reduces Wide Data bus and clock to one pair
- Extends interconnect length
  - Eliminates clock/data skew issues
- SigCon Features for Link extending
  - TX Equalization
  - RX Equalization

**Block Diagram**

*Data and Embedded Clock use a single pair of wires!*
Channel Link II Signal Conditioning

DS92LV2421/22 TX De-E and RX EQ

1.82 Gbps

Restores Amplitude

- **TP1**: No De-emphasis
  - $V_{Height} = 290mV$
  - Jitter = 403ps

- **TP2**: No EQ
  - $V_{Height} = 750mV$
  - Jitter = 228ps

- **TP3**: 3dB De-emphasis
  - No EQ
  - $V_{Height} = 825mV$
  - Jitter = 142ps

Open EYE Restores AMP

- **TP4**: EQ Boost = 1
  - $V_{Height} = 825mV$
  - Jitter = 142ps
How do I get a high speed signal to two places?

- Multi-drop, Multi-Point usually limited to <500 Mbps due to T-Line effects

- Point-to-Point Links are best for Signal Integrity when every ps matters!

- Desirable for many applications:
  - Redundancy
  - Fail Over
  - Front / Back Panel Options

- MUX Buffers provide a 1:2 FANOUT and 2:1 SELECT function
Storage: SAS / SATA

- **SAS 1.0 (3 Gbps), SAS 2.0 (6 Gbps)**
  - Primary target: Enterprise storage
  - Supports multiple initiators
  - Target length 8 meters of cable OR 30” FR4

- **SATA – 6 Gbps, 3 Gbps, 1.5 Gbps**
  - Primary target: Consumer storage
  - Target media length 1 meters of cable
  - eSATA (External SATA) supports 2 meter of cable

- **Both define OOB (Out-of-band) signaling**
  - OOB signal is a pattern of idle times and burst times
    - Idle time: Differential 0 V, No transitions (DC idle)
    - Burst time: Transmitted as a burst of ALIGN(0) primitives
  - Length of idle time distinguishes between OOB signal: COMINIT, COMWAKE, and COMSAS

- **Server storage applications:**
  - HBA (Host Bus Adapters), servers, storage racks, switches and routers
  - RAID (Redundant Array of Individual Disks) devices/JBODs (Just a Bunch of Disks)

**Protocol features!**
- Link Training
- OBB
- Idle
- LFPS

REDRIVERS cannot block
5 MUX Buffer Magic

- Signal conditioning on both input and output stages for maximum flexibility in physical placement

- Implement system redundancy with 2:1 Multiplex or 1:2 Fan-out option

- Extend reach on back-plane or cable for SATA/SAS/XAUI/RXAUI/Infiniband etc.

- DS64MB201 for SATA/SAS and 6Gbps applications

- DS100MB203 for KR and 10GE 10Gbps applications
Are 25/28 Gbps copper Interface even possible?

• **YES** – with TI’s BiCMOS 13 Process Technology

• **100GE Applications** –
  – Quad 25G Electrical
  – Quad 28G Electrical (adds overhead for FEC, etc.)

• **An alternative to Optical** (power, post, ease of connections)

• **Challenges:**
  – Edge rate required
  – Open EYE
  – Unit Interval of 40ps to 35.7ps!
  – Interconnect Losses
  – Signal to Noise
  – EMI
25 Gbps Retimers
5m Cable & 20” Backplane Performance

Recovered Eye – 25 Gbps

BER < 1e-15, PRBS-31
25G is real today with TI’s BiCMOS13 >100GHz process

- Un-equalized data after a 7.5inch stripline and 2 meters of cable at 25Gbps
- Equalized data after a 7.5inch stripline and 2 meters of cable at 25Gbps
- Re-timed data after a 7.5inch stripline and 2 meters of cable at 25Gbps

- 25/28 Gbps
- Advanced SigCon
- Low Power
- OPEN EYE
- Zero Error

Zero BER after 1day and 18Hrs 3.7 Peta-bits!